Green mode PFC/Forward PWM Controller **SG6931**

FEATURES OVERVIEW

- Interleaved PFC/PWM switching
- Green mode PFC and PWM operation
- Low-operating current
- Innovative *Switching-Charge*® multiplier-divider
- Multi-vector control for improved PFC output transient response
- Average-current-mode for input-current shaping
- PFC over-voltage and under-voltage protections
- PFC and PWM feedback open-loop protection
- Cycle-by-cycle current limiting for PFC/PWM
- Slope compensation for PWM
- Programmable PWM maximum duty cycle
- Power on sequence control and soft-start
- Brownout protection

APPLICATIONS

Switch mode Power Suppliers with Active PFC

Servo System Power Supplies

PC-ATX Power Supplies

DESCRIPTION

The highly integrated SG6931 is specially designed for power supplies consist of boost PFC and Forward PWM. It requires very few external components to achieve green-mode operation and versatile protections/compensation. It is available in 20-pin DIP and SOP packages.

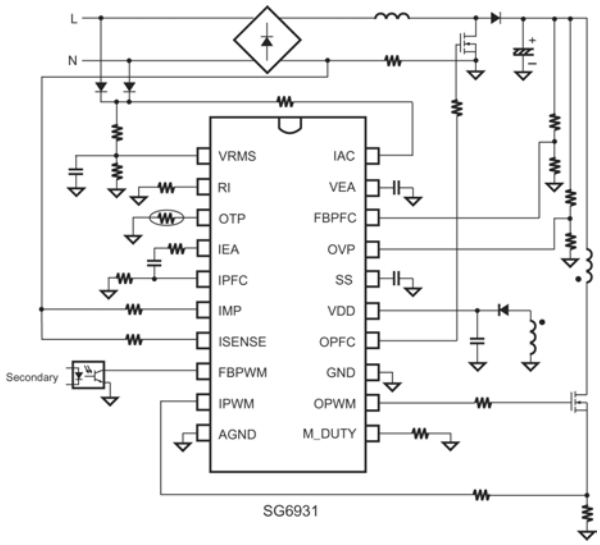
The patented interleave-switching feature synchronizes the PFC and PWM stages and reduces switching noise. At light load, the switching frequency is continuously decreased to reduce power consumption.

For PFC stage, the proprietary multi-vector control scheme provides a fast transient response in a low-bandwidth PFC loop, in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, SG6931 will shut off to prevent extra-high voltage on output.

For the Forward PWM stage, the synchronized slope compensation ensures the stability of the current loop under continuous-conduction-mode operation. Hiccup operation during output overloading is guaranteed. The soft start and programmable maximum duty cycle ensure safe operation.

In addition, SG6931 provides complete protection functions such as brownout protection and RI open/short protection.

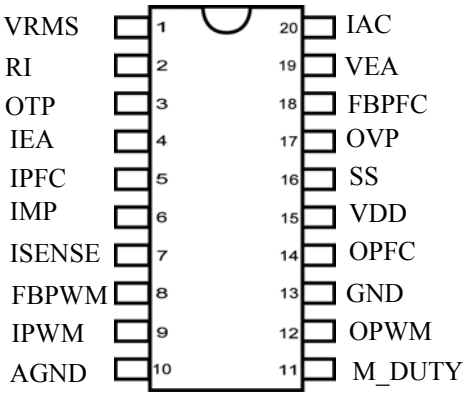
TYPICAL APPLICATION



MARKING DIAGRAMS

T: D = DIP, S = SOP
P : Z =Lead Free + ROHS Compatible
XXXXXXXX: Wafer Lot
Y: Year; WW: Week
V: Assembly Location

PIN CONFIGURATION



ORDERING INFORMATION

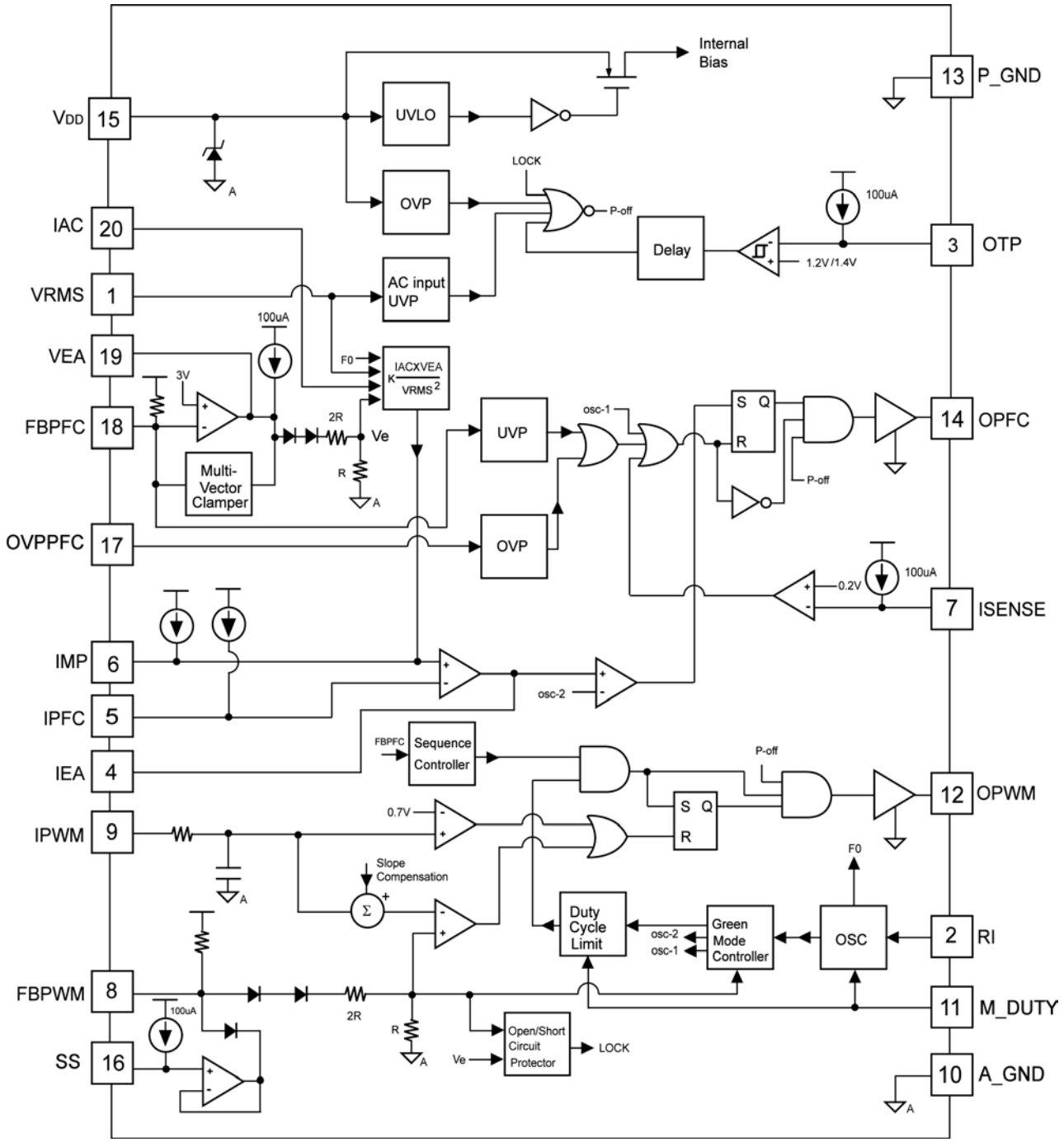
Part Number	Package
SG6931DZ	20-pin PDIP (Lead Free)
SG6931SZ	20-pin SOP (Lead Free)

PIN DESCRIPTIONS

Name	Pin No.	Type	Function
VRMS	1	Line-Voltage Detection	Line voltage detection. The pin is used for PFC multiplier and brownout protection.
RI	2	Oscillator Setting	Reference setting. One resistor connected between RI and ground determines the switching frequency. A resistor having a resistance between 12k ~ 47kΩ is recommended. The switching frequency is equal to [1560 / RI] kHz, where RI is in kΩ. For example, if RI is equal to 24kΩ, then the switching frequency will be 65 kHz.
OTP	3	Over Temperature Protection	This pin provides an over temperature protection. A constant current is output from this pin. If RI is equal to 24kΩ, then the magnitude of the constant current will be 100uA. An external NTC thermistor must be connected from this pin to ground. The impedance of the NTC thermistor decreases whenever the temperature increases. Once the voltage of the OTP pin drops below the OTP threshold, the SG6931 will be shutdown.
IEA	4	Output of PFC Current Amplifier	This is the output of the PFC current amplifier. The signal from this pin will be compared with an internal saw-tooth and hence determine the pulse width for PFC gate drive.
IPFC	5	Inverting Input of PFC Current Amplifier	The inverting input of the PFC current amplifier. Proper external compensation circuits will result in excellent input power factor via average-current-mode control.
IMP	6	Non-inverting Input of PFC Current Amplifier and Output of Multiplier	The non-inverting input of the PFC current amplifier and also the output of multiplier. Proper external compensation circuits will result in excellent input power factor via average current mode control.

ISENSE	7	Peak Current Limit Setting for PFC	The peak current limit setting for PFC.
FBPWM	8	PWM Feedback Input	The control input for voltage-loop feedback of PWM stage. It is internally pulled high through a 6.5 kΩ resistance. Usually an external opto-coupler from secondary feedback circuit is connected to this pin.
IPWM	9	PWM Current Sense	The current sense input for the PWM stage. Via a current sense resistor, this pin provides the control input for peak-current-mode control and cycle-by-cycle current limiting.
AGND	10	Ground	The signal ground.
M_DUTY	11	Maximum duty cycle of PWM stage	This input is used to determine the maximum duty cycle of the PWM stage. A constant current source 10uA (RI = 24kΩ) is output from this pin. Connecting a resistor from this pin to ground will generate a voltage V_{MD}. The maximum duty cycle will be: M_DUTY (%) =[(V_{MD} - 0.2V) ÷ 2.9V] x 100. The maximum duty cycle is clamped to 65%.
PGND	12	Ground	The power ground
OPWM	13	PWM Gate Drive	The totem pole output drive for PWM MOSFET. This pin is internally clamped under 18V to protect the MOSFET.
OPFC	14	PFC Gate Drive	The totem pole output drive for PFC MOSFET. This pin is internally clamped under 18V to protect the MOSFET.
VDD	15	Supply	The power supply pin. The threshold voltages for start-up and turn-off are 14V and 10V, respectively. The operating current is lower than 10mA.
SS	16	PWM Soft Start	During startup, the SS pin will charge an external capacitor with a 50uA constant current source. The voltage on FBPWM will be clamped by SS during startup. In the event of a protection condition occurring and/or PWM being disabled, the SS pin will be quickly discharged.
OVPPFC	17	PFC over-voltage input	The over-voltage input of the PFC stage. The comparator will disable the PFC output driver if this input exceeds 3.25V. This pin can be connected to the FBPFC pin or it can be connected to the PFC boost output through a divider network. This pin provides an extra input for PFC over-voltage protection.
FBPFC	18	Voltage Feedback Input for PFC	The feedback input for PFC voltage loop. The inverting input of PFC error amp. This pin is connected to the PFC output through a divider network.
VEA	19	Error-Amp Output for PFC voltage feedback loop	The error-amp output for PFC voltage feedback loop. A compensation network (usually a capacitor) is connected between this pin and ground. A large capacitor value will result in a narrow bandwidth and hence improve the power factor.
IAC	20	Input AC Current	For normal operation, this input is used to provide current reference for the multiplier. The suggested maximum IAC is 360 uA.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Value		Unit
V_{DD}	DC Supply Voltage*		25		V
I_{AC}	Input AC Current		2		mA
V_{High}	OPWM, OPFC, IAC		-0.5 to 25V		V
V_{Low}	Others		-0.5 to 7V		V
P_D	Power Dissipation	At T_A<50℃	0.8		W
T_J	Operating Junction Temperature		-40 to +125		℃
T_{stg}	Storage Temperature Range		-55 to +150		℃
$R_{\theta j\text{-}C}$	Thermal resistance (Junction to Case)		DIP	34.64	℃/W
			SOP	35.44	
T_L	Lead Temperature (soldering 10sec)		DIP	260	℃
			SOP	230	
ESD	ESD capability, HBM model		4.5		KV
	ESD capability, Machine model		250		V

*All voltage values, except differential voltages, are given with respect to the network ground terminal

RECOMMENDED OPERATING JUNCTOIN TEMPERATURE: -30°C~ 85°C*

* For proper operation

ELECTRICAL CHARACTERISTICS (V_{DD}=15V, T_A=25°C UNLESS NOTED)

VDD section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{DD\text{-}OP}$	Continuously Operating Voltage				20	V
$I_{DD\ ST}$	Start-Up Current	$V_{TH(ON)}$ – 0.16V		10	20	uA
$I_{DD\ OP}$	Operating Current	V_{DD} = 15V; OPFC, OPWM open		6	10	mA
$V_{TH\text{-}ON}$	Start Threshold Voltage		13	14	15	V
$V_{DD\text{-}min}$	Min. Operating Voltage		9	10	11	V
$V_{DD\text{-}OVP}$	VDD OVP1 (turn off PWM with delay)		23.5	24.5	25.5	V
$TV_{DD\text{-}OVP}$	Delay time of VDD OVP1	RI= 24kΩ	8		25	uS

Oscillator & Green-Mode Operation

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{RI}	RI Voltage		1.176	1.2	1.224	V
F_{OSC}	PWM frequency	RI= 24kΩ	62	65	68	KHz
$F_{OSC\text{-}MINFREQ}$	Minimum frequency in green mode	RI= 24kΩ	18	20	22	KHz
RI	RI range		12		47	kΩ
RI_{OPEN}	RI Pin Open Protection If RI> RI_{open} , PWM will be turned off			200		kΩ
RI_{SHORT}	RI Pin Short Protection If RI< RI_{short} , PWM will be turned off			2		kΩ

VRMS for UVP

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{RMS-UVP-1}$	RMS AC Voltage Under-Voltage Threshold to turn off PFC (with T_{UVP} delay) for UVP Mode1		0.75	0.8	0.85	V
$V_{RMS-UVP-2}$	Recovery level on VRMS for UVP mode1		$V_{RMS-UVP-1}$+0.17 V	$V_{RMS-UVP-1}$+0.19 V	$V_{RMS-UVP-1}$+0.21 V	V
T_{UVP}	Under Voltage Protection Propagation Delay Time (No delay for startup)	RI= 24kΩ	150	195	240	mS

PFC stage

Voltage Error Amplifier

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{REF}	Reference Voltage		2.95	3	3.05	V
Av_{-PFC}	Open-loop Gain			60		dB
Z_o	Output Impedance			110		kΩ
OVP_{FBPFC}	PFC Over-voltage-protection on OVP		3.2	3.25	3.3	V
$\triangle OVP_{FBPFC}$	PFC Feedback Voltage Protection Hysteresis		60	90	120	mV
$V_{FBPFC-H}$	Clamp-High Feedback Voltage		3.1	3.15	3.2	V
$G_{FBPFC-H}$	Clamp-High Gain			0.5		mA/ V
$V_{FBPFC-L}$	Clamp-Low Feedback Voltage		2.75	2.85	2.9	V
$G_{FBPFC-L}$	Clamp-Low Gain			6.5		uA/mV
$I_{FBPFC-L}$.	Maximum Source Current		1.5	2		mA
$I_{FBPFC-H}$.	Maximum Sink Current		70	110		uA
UVP_{VFB}	PFC Feedback Under Voltage Protection		0.35	0.4	0.45	V
V_{FBHIGH}	Output High Voltage on V_{EA}		6	7	8	V
$V_{RD-FBPFC}$	Voltage level on FBPFC to enable OPWM during startup		2.6	2.7	2.8	V
$T_{UVP-PFC}$	Debouce time of PFC UVP		40	70	120	uS

Current Error Amplifier

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OFFSET}	Input Offset Voltage ((-) > (+))			8		mV
A_I	Open-loop Gain			60		dB
BW	Unit Gain Bandwidth			1.5		MHz
CMRR	Common-mode Rejection Ratio	V_{CM} = 0 ~ 1.5V		70		dB
$V_{OUT-HIGH}$	Output High Voltage		3.2			V
$V_{OUT-LOW}$	Output Low Voltage				0.2	V
I_{MR1}, I_{MR2}	Reference Current source	RI=24 kΩ (I_{MR}=20+I_{RI}*0.8)	50		70	uA
I_L	Maximum Source Current			3		mA
I_H	Maximum Sink Current			0.25		mA

Peak Current Limit

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_P	Constant Current Output	RI = 24kΩ	90	100	110	uA
V_{pk}	Peak Current Limit Threshold Voltage Cycle-by-Cycle Limit (V_{sense} < V_{pk})	VRMS=1.05V	0.15	0.2	0.25	V
		VRMS=3V	0.35	0.4	0.45	V

T_{PD-PFC}	Propagation Delay				200	nS
$T_{BNK-PFC}$	Leading-Edge Blanking Time		270	350	450	nS

Multiplier

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{AC}	Input AC Current	Multiplier linear range	0		360	uA
I_{MO-max}	Maximum Multiplier Current Output;	RI=24 kΩ		230		uA
I_{MO-1}	Multiplier Current Output (low-line, high-power)	V_{RMS}=1.05V; I_{AC}=90uA; VEA=7.5V;RI=24 kΩ	200	230	280	uA
I_{MO-2}	Multiplier Current Output (high-line, high-power)	V_{RMS}=3V; I_{AC}=264uA; V_{EA}=7.5V;RI=24 kΩ	65	85		UA
V_{IMP}	Voltage of IMP Open		3.4	3.9	4.4	V

PFC Output Driver

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{Z-PFC}	Output Voltage Maximum (clamp)	V_{DD}=20V		16	18	V
V_{OL-PFC}	Output Voltage Low	V_{DD}=15V; I_O = 100mA			1.5	V
V_{OH-PFC}	Output Voltage High	V_{DD}=13V; I_O = 100mA	8			V
T_{R-PFC}	Rising Time	V_{DD}=15V; C_L=5nF O/P= 2V to 9V	40	70	120	nS
T_{f-PFC}	Falling Time	V_{DD}=15V; C_L=5nF O/P= 9V to 2V	40	60	110	nS
$DC_{(MAX)}$	Maximum Duty Cycle		93		97	%

PWM Stage

FBPWM

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$A_{v\text{-}PWM}$	FB to Current Comparator Attenuation		2.2	2.7	3.2	V/V
Z_{FB}	Input Impedance		4	5	7	kΩ
$FB_{OPEN\text{-}LOOP}$	PWM Open Loop Protection voltage		4.2	4.5	4.8	V
$T_{OPEN\text{-}PWM\text{-}Hiccup}$	The interval of PWM Open Loop Protection Reset	RI = 24kΩ	500	600	700	mS
$T_{OPEN\text{-}PWM}$	PWM Open Loop Protection Delay Time	RI = 24kΩ	80	95	120	mS
V_N	Frequency Reduction Threshold on FBPWM		1.9	2.1	2.3	V
S_G	Green-Mode Modulation Slope		60	75	90	Hz/mV
V_G	Voltage on FBPWM for minimum Green-mode frequency		1.35	1.6	1.75	V

PWM-Current Sense

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$T_{PD\text{-}PWM}$	Propagation Delay to Output – V_{LIMIT} Loop	VDD=15V, OPWM drops to 9V	60		120	nS
V_{LIMIT}	Peak Current Limit Threshold Voltage		0.65	0.7	0.75	V
$T_{BNK\text{-}PWM}$	Leading-Edge Blanking Time		270	350	450	nS
$\triangle V_{SLOPE}$	Slope Compensation $\triangle V_s = \triangle V_{SLOPE} \times (T_{on}/T)$ $\triangle V_s$: Compensation Voltage Added to Current Sense		0.4	0.45	0.55	V

PWM Output Driver

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{Z\text{-}PWM}$	Output Voltage Maximum (clamp)	V_{DD}=20V		16	18	V
T_{PWM}	The interval of OPWM Lags behind OPFC at Startup	RI=24 kΩ	2	4	6	mS
$V_{OL\text{-}PWM}$	Output Voltage Low	V_{DD}=15V; I_O = 100mA			1.5	V
$V_{OH\text{-}PWM}$	Output Voltage High	V_{DD}=13V; I_O = 100mA	8			V
$T_{R\text{-}PWM}$	Rising Time	V_{DD}=15V; C_L=5nF; O/P= 2V to 9V	30	60	120	nS
$T_{F\text{-}PWM}$	Falling Time	V_{DD}=15V; C_L=5nF; O/P= 9V to 2V	30	50	110	nS

Maximum Duty-Cycle

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DC_{MAX}	Maximum Duty Cycle for M_Duty open		62		66	%
I_{MD}	Constant Current Output	RI= 24kΩ	45	50	55	uA
$DC_{RD=31.8k\Omega}$	Maximum Duty Cycle for M_Duty =31.8kΩ	M_Duty = 31.8kΩ, RI= 24kΩ	46		50	%

OTP section

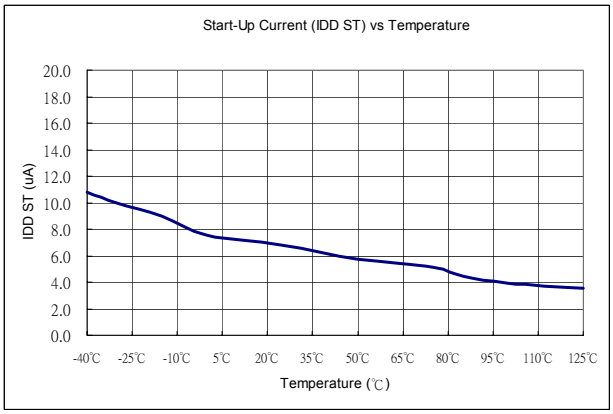
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{OTP}	OTP Pin Output Current	RI = 24kΩ	90	100	110	uA
$V_{OTP\text{-}OFF}$	OTP Threshold Voltage		1.15	1.2	1.25	V
$V_{OTP\text{-}ON}$	Recovery level on OTP		1.35	1.4	1.45	V

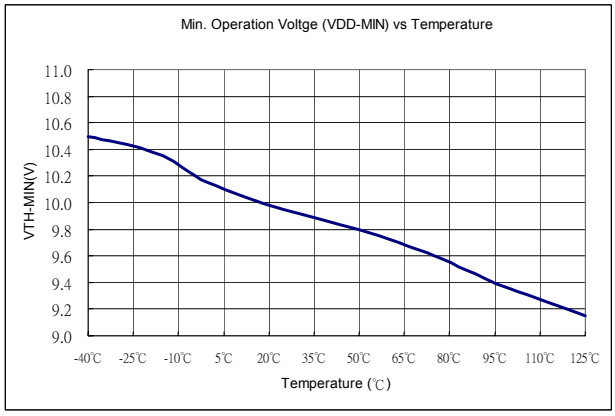
T_{OTP}	OTP Debounce Time	RI = 24kΩ	8		25	uS

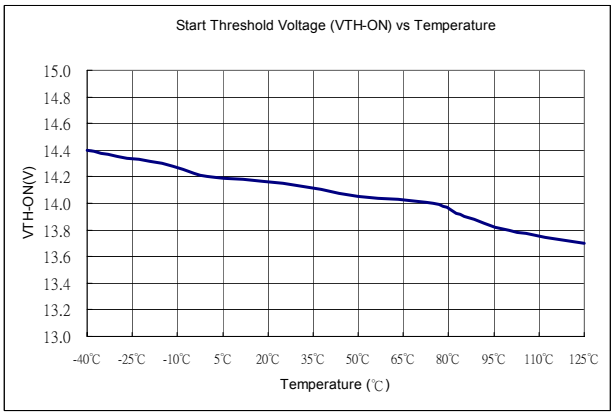
Soft Start

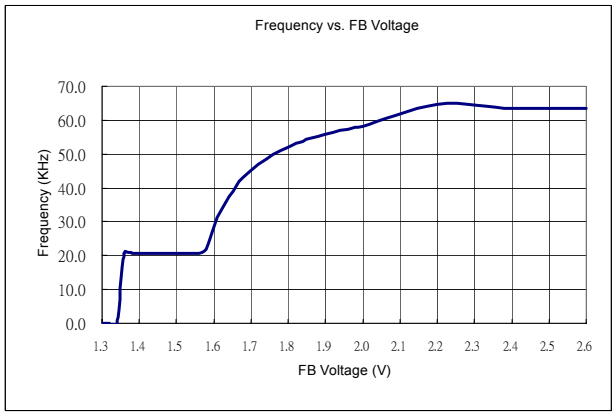
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SS}	Constant Current Output for Soft Start	RT= 24kΩ	44	50	56	uA
R_D	Discharge Resistance			470		Ω

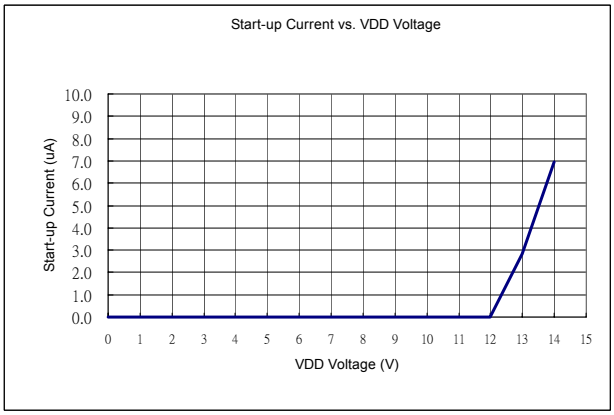
TYPICAL CHARACTERISTICS

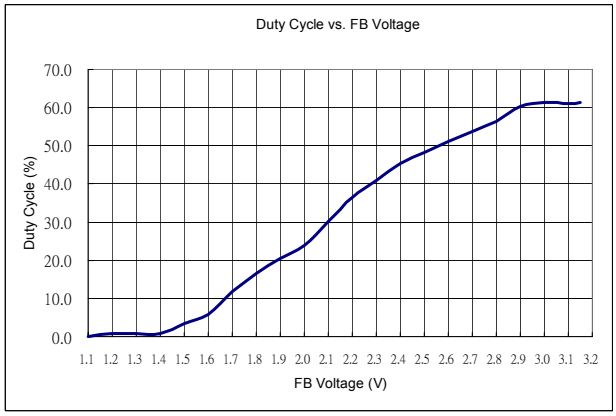












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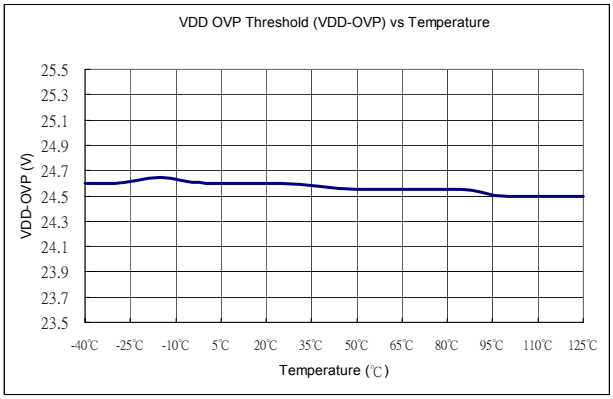

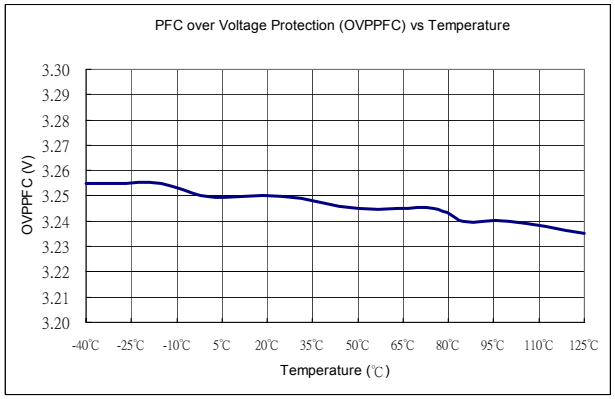

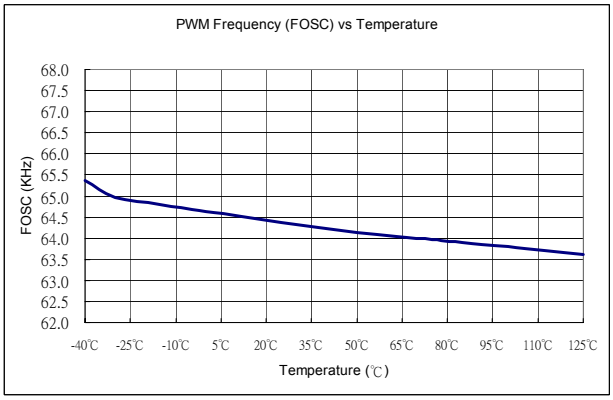

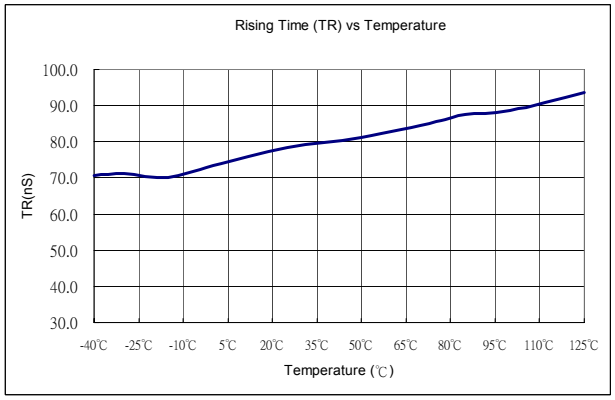

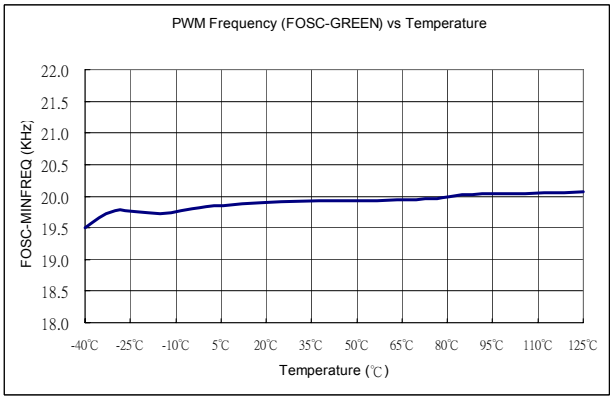

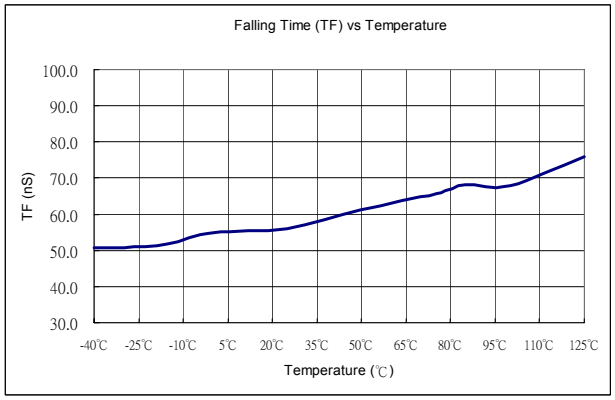

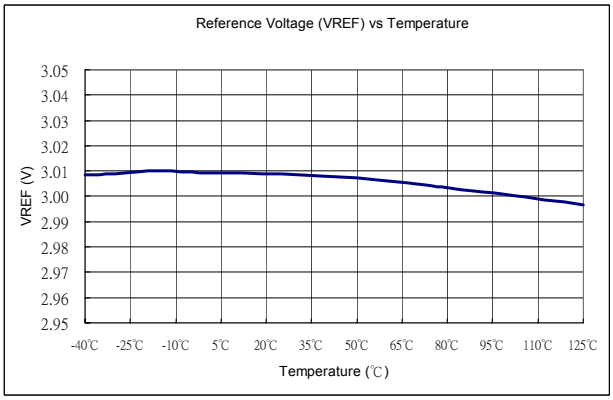

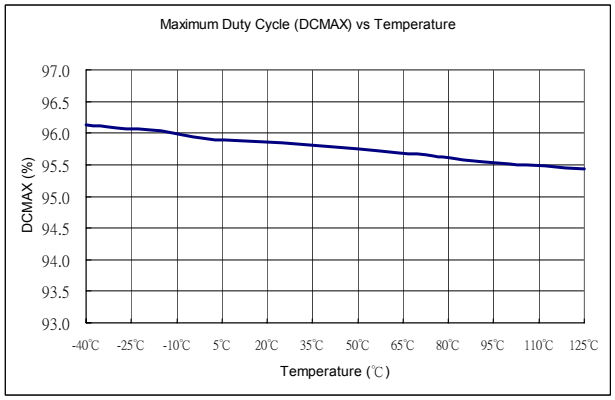

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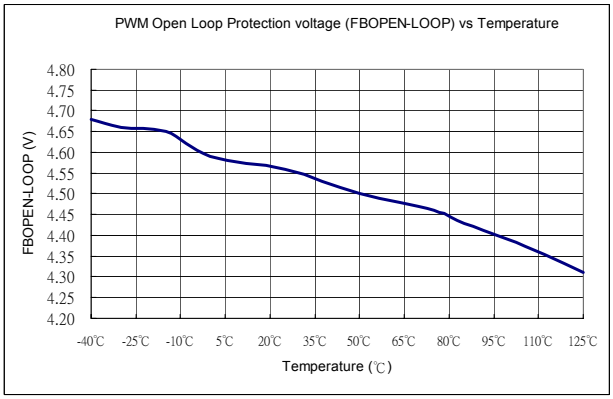
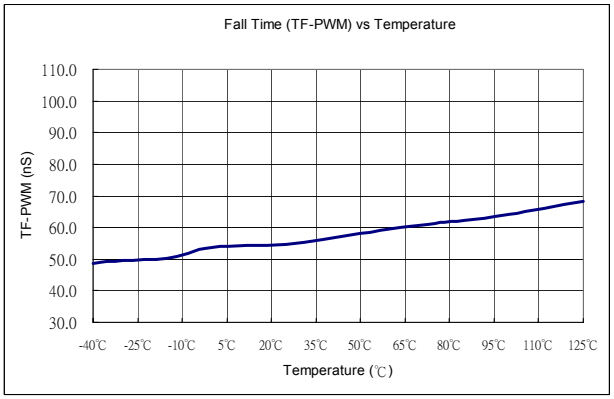
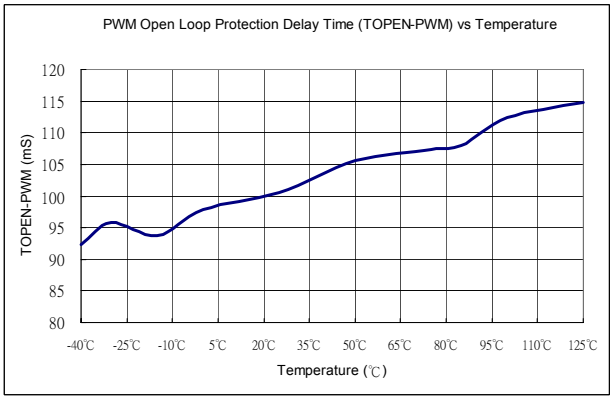
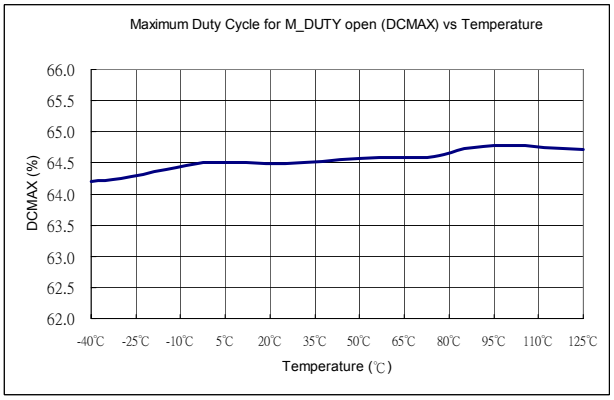
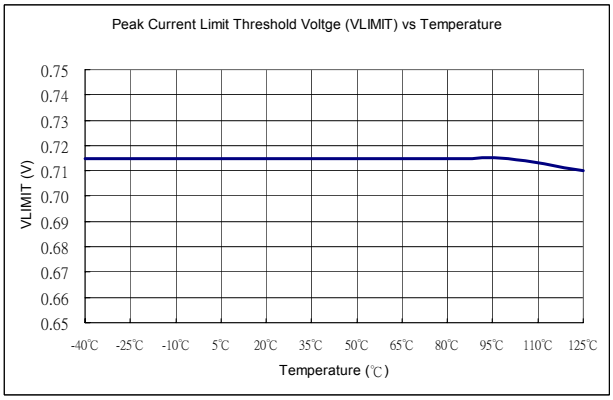
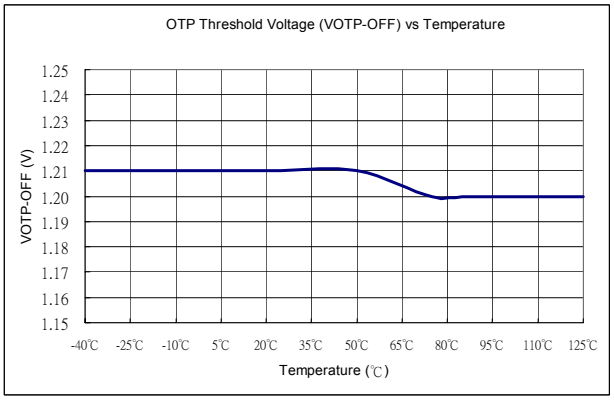


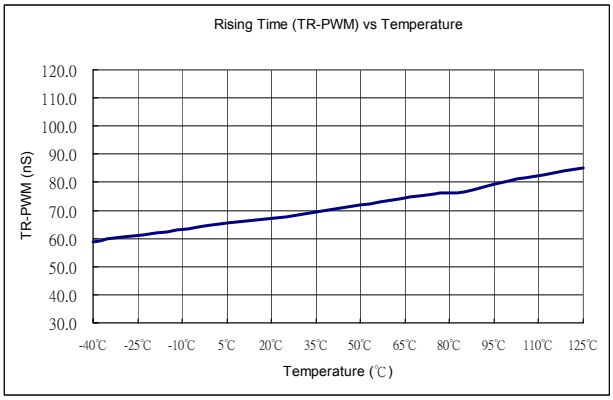


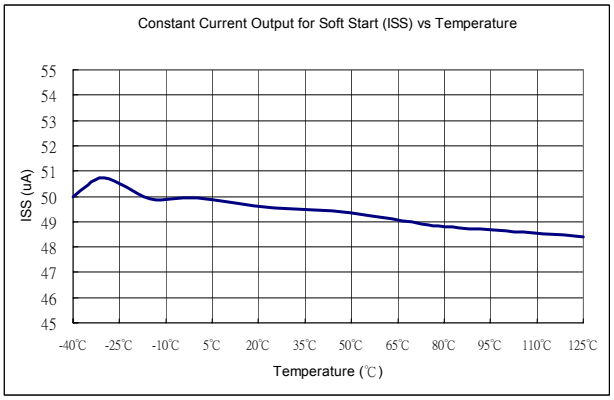


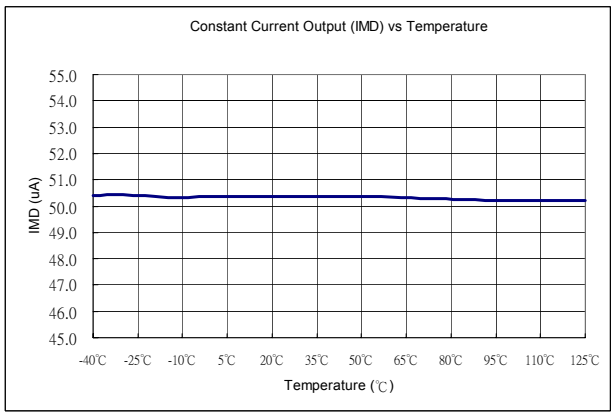











Constant Current Output (IMD) vs Temperature
55.0
54.0
53.0
52.0
51.0
50.0
49.0
48.0
47.0
46.0
45.0
IMD (uA)
-40℃ -25℃ -10℃ 5℃ 20℃ 35℃ 50℃ 65℃ 80℃ 95℃ 110℃ 125℃
Temperature (℃)

OPERATION DESCRIPTION

The highly integrated SG6931 is specially designed for power supply with boost PFC and forward PWM. It requires very few external components to achieve green-mode operation and versatile protections/ compensation.

The patented interleave-switching feature synchronizes the PFC and PWM stages and reduces switching noise. At light load, the switching frequency is linearly decreased to reduce power consumption.

The PFC function is implemented by average-current-mode control. The patented *Switching-Charge®* multiplier-divider provides high-degree noise immunity for the PFC circuit. This also enables the PFC circuit to operate over a much wider region. The proprietary multi-vector output voltage control scheme provides a fast transient response in a low-bandwidth PFC loop, in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, the SG6931 will shut off PFC to prevent extra-high voltage on output.

For the forward PWM, the synchronized slope compensation ensures the stability of the current loop under continuous-mode operation. Hiccup operation during output overloading is also guaranteed. To prevent the power supply from drawing large current during start-up, the start-up for PWM stage will be delayed 4ms after the PFC output voltage reaches its setting value.

In addition, SG6931 provides complete protection functions such as brownout protection and over voltage and RI open/short protection.

I_{AC} signal

Figure 1 shows that the IAC pin is connected to input voltage by a resistance. And the current I_{AC} will be the input for PFC multiplier. For the linear range of I_{AC} is 0~360uA, the wide range input voltage should be connected a resistance over 1.2M.

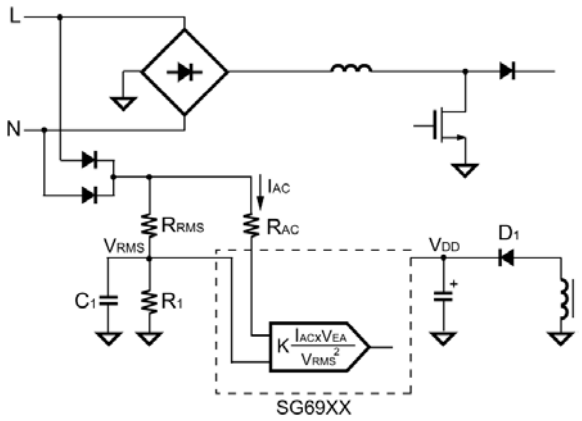


Figure 1 Input Voltage Detection

Switching Frequency and Current Sources

The switching frequency of SG6931 can be programmed by the resistor R_I connected between RI pin and GND. The relationship is:

$$f_{PWM} = \frac{1560}{R_I\ (k\Omega)}(kHz) \quad \text{----------(1)}$$

For example, a 24kΩ resistor R_I results in a 65 kHz switching frequency. Accordingly, constant Current I_T will flow through R_I.

$$I_T = \frac{1.2V}{R_I\ (k\Omega)}(mA) \quad \text{----------(2)}$$

I_T is used to generate internal current reference.

Line Voltage Detection (V_{RMS})

Figure 2 shows a resistive divider with low-pass filtering for line-voltage detection on VRMS pin. The V_{RMS} voltage is used for the PFC multiplier and brownout protection. For brownout protection, when the VRMS voltage drops below 0.8V, OPFC will be turn off.

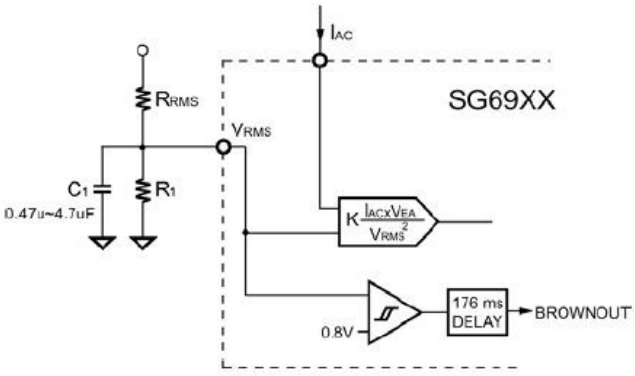


Figure 2 Line-voltage Detection on VRMS pin

Interleaved Switching and Green mode Operation

The SG6931 uses interleaved switching to synchronize the PFC and PWM stages. This reduces switching noise and spreads the EMI emissions. Figure 3 shows that an off-time T_{OFF} is inserted in between the turn-off of the PFC gate drives and the turn-on of the PWM.
The off-time T_{OFF} is increased in response to the decreasing of the voltage level of FBPWM. Therefore, the PWM switching frequency is linearly decreased to reduce switching losses.

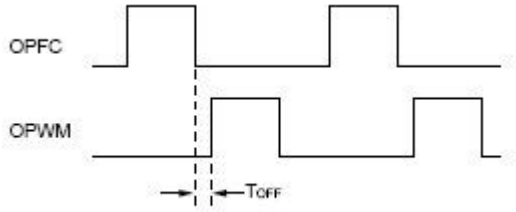


Figure 3 Interleaved Switching

PFC Operation

The purpose of a boost active power factor corrector (PFC) is to shape the input current of a power supply. The input current waveform and phase will follow that of the input voltage. Using SG6931, average-current-mode control is utilized for continuous-current-mode operation for the PFC booster. With the innovative multi-vector control for voltage loop and *Switching Charge* multiplier/divider for current reference, excellent input power factor is achieved with good noise immunity and transient response. Figure 4 shows the total control loop for the average-current-mode control circuit of SG6931.

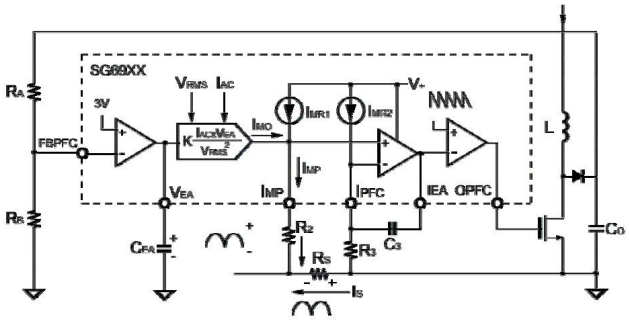


Figure 4 Control Loop of PFC Stage

The current source output from the *Switching Charge* multiplier/divider can be expressed as:

$$I_{MO} = K \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^2}(uA) \quad \text{---------- (4)}$$

I_{MP}, the current output from IMP pin, is the summation of I_{MO} and I_{MR1}. I_{MR1} and I_{MR2} are identical fixed current sources. R_2 and R_3 are also identical. They are used to pull high the operating point of the IMP and IPFC pins since the voltage across R_S goes negative with respect to ground.
Through the differential amplification of the signal across Rs, better noise immunity is achieved. The output of IEA will be compared with an internal sawtooth and hence the pulse width for PFC is determined. Through the average current-mode control loop, the input current Is will be proportional to I_{MO}.

$$I_{MO} \times R_2 = I_S \times R_S \text{ ----------(5)}$$

According to equation (5), the minimum value of R2 and maximum of Rs can be determined since I_{MO} should not exceed the specified maximum value.
There are different concerns in determining the value of the sense resistor Rs. The value of Rs should be small to reduce power consumption, but it should be large enough to maintain the resolution. A current transformer (CT) may be used to improve the efficiency of high power converters.

To achieve good power factor, the voltage for V_{RMS} and V_{EA} should be kept as DC as possible according to equation (4). In other words, good RC filtering for V_{RMS} and narrow bandwidth (lower than the line frequency) for voltage loop are suggested for better input current shaping. The trans-conductance error amplifier has output impedance R_O (>90kΩ) and a capacitor C_{EA} (1uF ~ 10uF) connected to ground (Figure. 5). This establishes a dominant pole *f1* for the voltage loop:

$$f_1 = \frac{1}{2\pi \times R_0 \times C_{EA}} \text{ ----------(6)}$$

The average total input power can be expressed as:

$$\begin{aligned} Pin &= Vin(rms) \times Iin(rms) \\ &\propto V_{RMS} \times I_{MO} \\ &\propto V_{RMS} \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^2} \quad \text{---------- (7)} \\ &\propto V_{RMS} \times \frac{\frac{Vin}{R_{AC}} \times V_{EA}}{V_{RMS}^2} \propto V_{EA} \end{aligned}$$

From equation (7), V_{EA}, the output of the voltage error amplifier, actually controls the total input power and hence the power delivered to the load.

Multi-vector Error Amplifier

The voltage-loop error amplifier of SG6931 is trans-conductance, which has high output impedance (> 90kΩ). A capacitor C_{EA} (1uF ~ 10uF) connected from VEA to ground provides a dominant pole for the voltage loop. Although the PFC stage has a low bandwidth voltage loop for better input power factor, the innovative *Multi-Vector Error Amplifier* provides a fast transient response to clamp the overshoot and undershoot of the PFC output voltage.

Figure 5 shows the block diagram of the multi-vector error amplifier. When the variation of the feedback voltage exceeds ± 5% of the reference voltage, the trans-conductance error amplifier will adjust its output impedance to increase the loop response. If R_A is opened, SG6931 will shut off immediately to prevent extra-high voltage on the output capacitor.

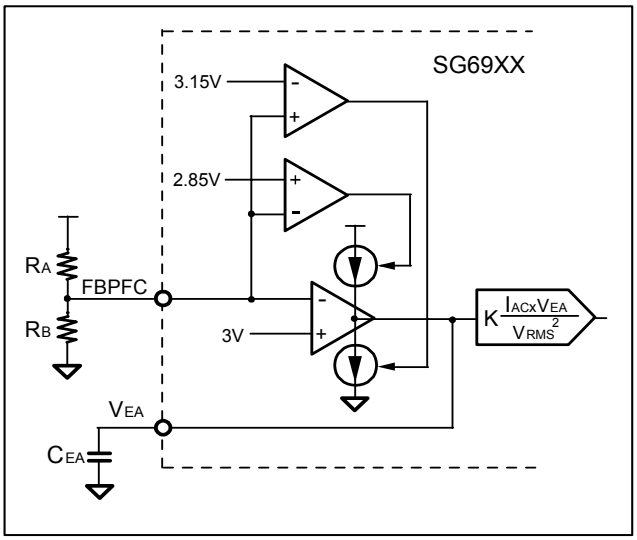


Figure 5 Multi-vector Error Amp.

Cycle-by-cycle Current Limiting

SG6931 provides cycle-by-cycle current limiting for both PFC and PWM stages. Figure 6 shows the peak current limit for the PFC stage. The PFC gate drive will be terminated once the voltage on ISENSE pin goes below V_{PK}.

The voltage of V_{RMS} determines the voltage of V_{PK}. The relationship between V_{PK} and VRMS is also shown in Figure 7.

The amplitude of the constant current I_P is determined by the internal current reference I_T, according to the following equation:

$$Ip = 2 \times I_T = 2 \times \frac{1.2V}{R_I} \text{ ---------- (8)}$$

Therefore the peak current of the I_S is given by (V_{RMS}<1.05V)

$$I_{S\_peak} = \frac{(Ip \times R_P) - 0.2V}{R_S} \text{ ---------- (9)}$$

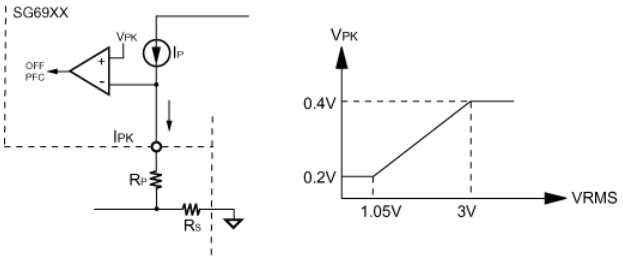


Figure 6 Current Limit

Power On Sequence & Soft Start

The SG6931 is enabled whenever the line voltage is higher than the brownout threshold. Once the SG6931 is active, the PFC stage is enabled first. The PWM stage is enabled following a 4mS delay time after FBPFC voltage exceeds 2.7V. During startup of PWM stage, the SS pin will charge an external capacitor with a constant current source. The voltage on FBPWM will be clamped by SS during startup. In the event of a protection condition occurring and/or PWM being disabled, the SS pin will be quickly discharged.

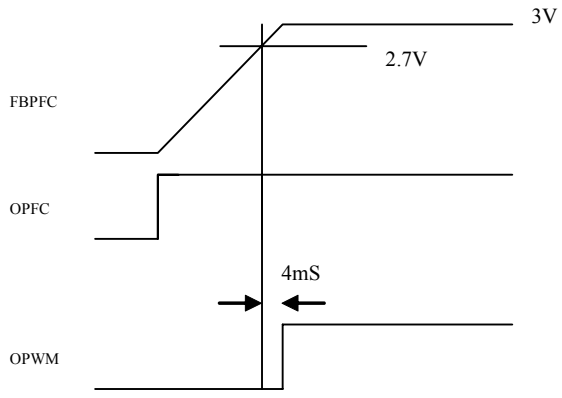


Figure 7 Power on Sequence

Forward PWM and Slope Compensation

The PWM stage is designed for forward power converters. Peak current mode control is used to optimize system performance. Slope compensation is added to stabilize the current loop. The SG6931 inserts a synchronized positively sloped ramp at each switching cycle. The positively sloped ramp is represented by the voltage signal $V_{s\text{-}comp}$. In this example, the voltage of the ramp signal is 0.55V.

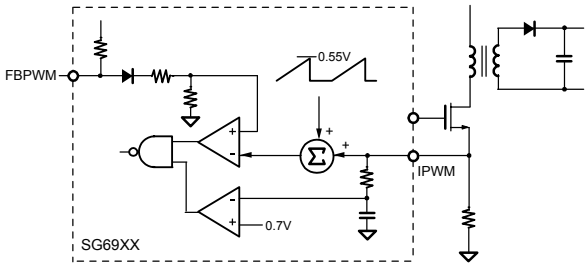


Figure 8 Slope Compensation

Maximum Duty Cycle of PWM stage

An internal constant current, I_{MD}, is sourced from this pin. Connecting a resistor from this pin to ground will generate a voltage V_{MD} and determine the maximum duty cycle. It is given by,

$$M_{\_DUTY}(\%) = \frac{V_{MD} - 0.2V}{2.9V} \times 100$$

In this example, a 31.8kΩ resistor is connected to the M_DUTY pin. I_{MD} =50uA when RI=24 kΩ. This will result in a 48% maximum duty cycle for the PWM stage. The maximum duty cycle of the SG6931 is 66%. A 1nF capacitor paralleled with the 31.8kΩ resistor to improve the stability is needed.

Limited Power Control

Every time when the output of power supply is shorted or over loaded, the FBPWM voltage will increase. If the FB voltage is higher than a designed threshold, 4.2V, for longer than 95msec, the PWM output will then be turned off.

Gate Drivers

SG6931 output stages are fast totem-pole gate drivers. The output driver is clamped by an internal 18V Zener diode in order to protect the power MOSFET.

Protections

The SG6931 provides full protection functions to prevent the power supply and the load from being damaged. The protection features include:

PFC Feedback Over-voltage Protection. When the PFC feedback voltage exceeds the over-voltage threshold, the SG6931 will inhibit the PFC switching signal. This protection also prevents the PFC power converter from operating abnormally while the FBPFC pin is open.

Second PFC Over Voltage Protection (OVP_PFC). The PFC stage over-voltage input. The comparator will disable the PFC output driver if this input exceeds 3.25V. This pin can be connected to the FBPFC pin, or it can be connected to the PFC boost output through a divider network. This pin provides an extra input for PFC over voltage protection.

PFC Feedback Under Voltage Protection. The SG6931 will stop the PFC switching signal whenever the PFC feedback voltage drops below the under-voltage threshold. This protection feature is designed to prevent the PFC power converter from experiencing abnormal conditions while the FBPFC pin is shorted to ground.

VDD Over-voltage Protection. The PFC and PWM stages will be disabled whenever the V_{DD} voltage exceeds the over-voltage threshold.

RI pin Open / Short Protection. The RI pin is used to set the switching frequency and internal current reference. The PFC and PWM stages of SG6931 will be disabled whenever the RI pin is short or open.

PCB Layout

Note that SG6931 has two ground pins. Good high-frequency or RF layout practices should be followed. Avoid long PCB traces and component leads. Locate decoupling capacitors near the SG6931. A resistor (5 ~ 20 Ω) is recommended connecting in series from the OPFC and OPWM to the gate of the MOSFET.

Isolating the interference between the PFC and PWM stages is also important. Figure 9 shows an example of the PCB layout. The *ground trace 1* is connected from the ground pin of SG6931 to the decoupling capacitor, which should be low impedance and as short as possible. The *ground trace 2* provides a signal ground. It should be connected directly to the decoupling capacitor C_{DD} and/or to the ground pin of the SG6931. The *ground trace 3* is independently tied from the decoupling capacitor to the PFC output capacitor C_O. The ground in the output capacitor C_O is the major ground reference for power switching. In order to provide a good ground reference and reduce the switching noise of both the PFC and PWM stages, the *ground traces 6 and 7* should be located very near and be low impedance.

The IPFC pin is connected directly to R_S through R_3 to improve noise immunity (Beware that it may incorrectly be connected to the ground trace 2). The IMP and ISENSE pins should also be connected directly via the resistors R_2 and R_P to another terminal of R_S.

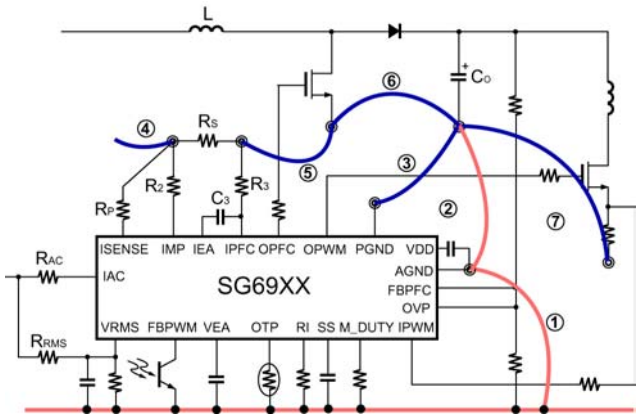
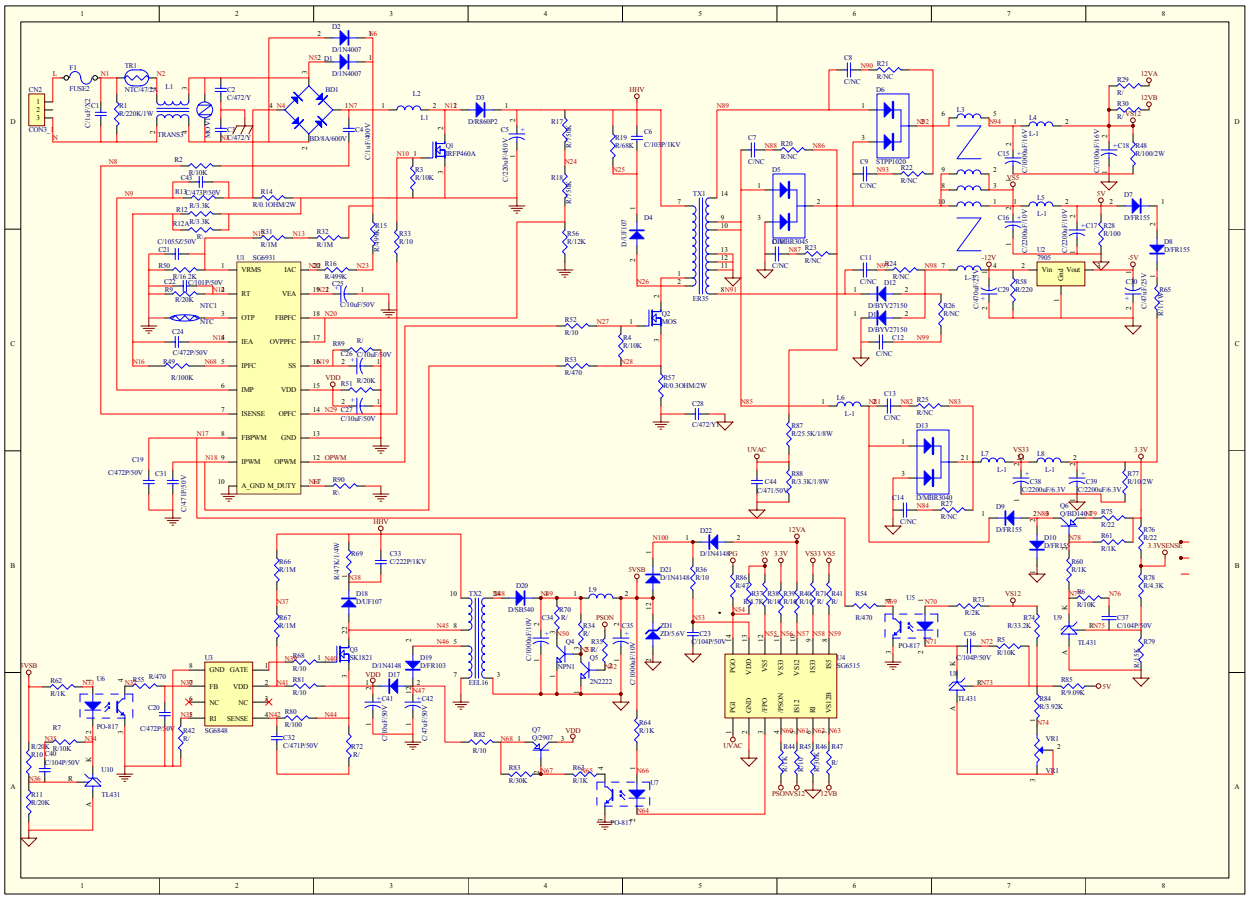


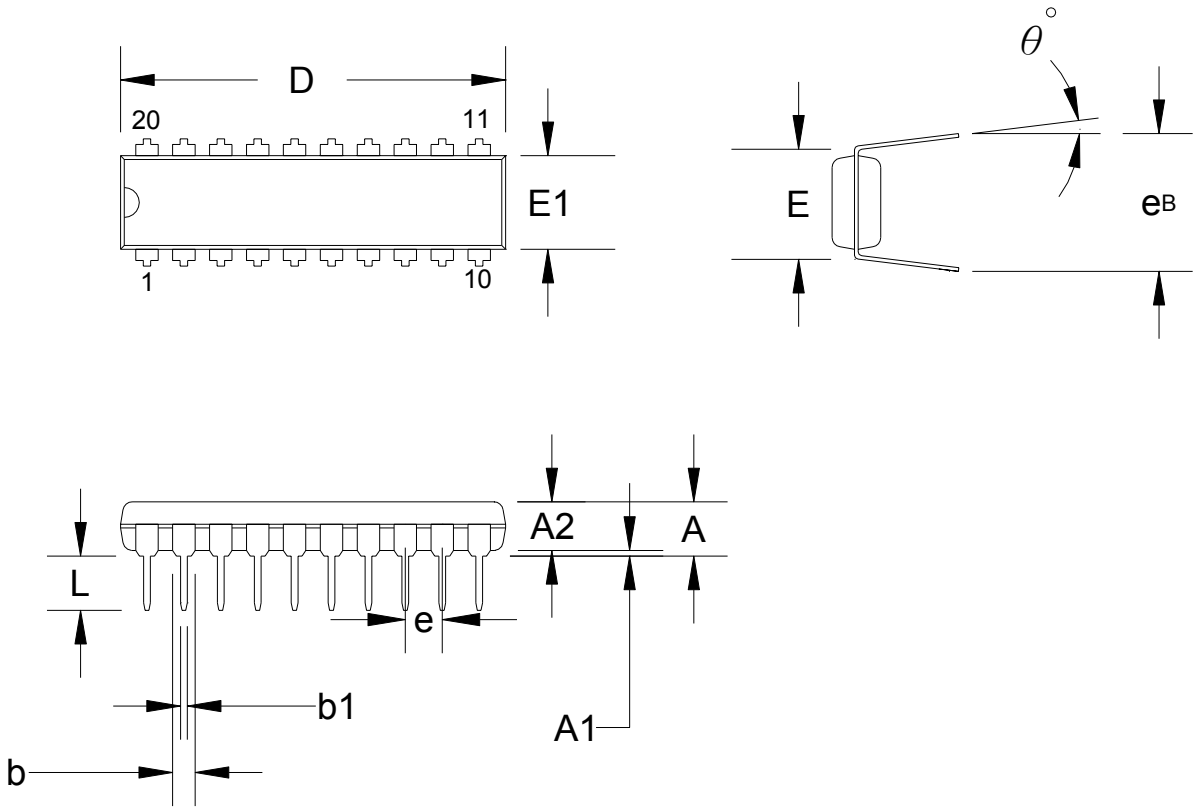
Figure 9 PCB Layout

Reference Circuit



PACKAGE INFORMATION

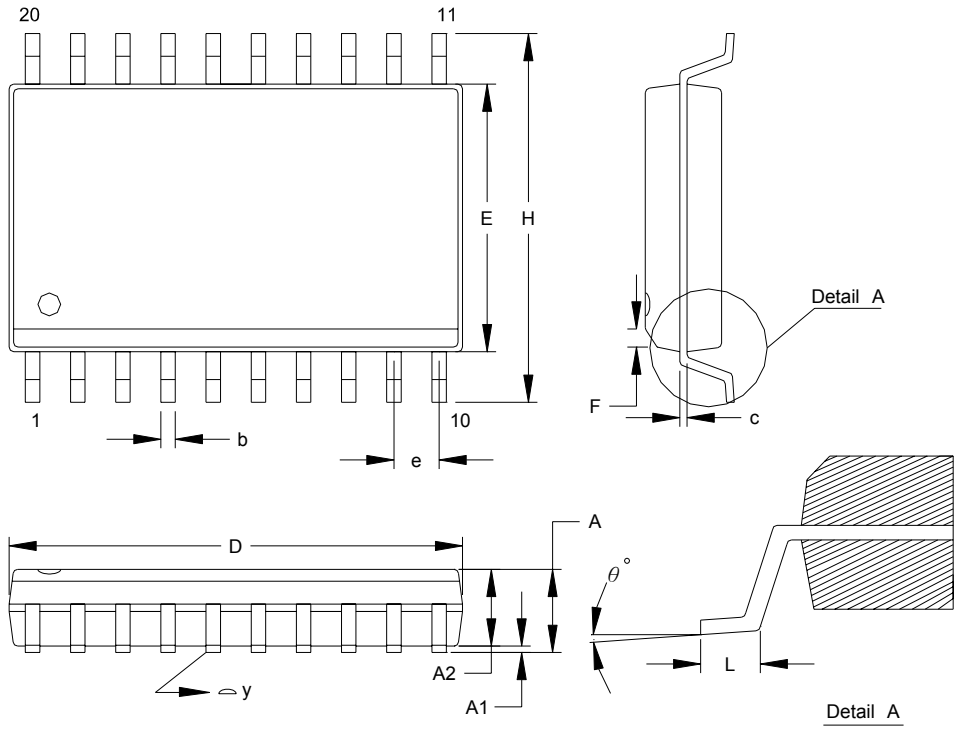
20 PINS – PLASTIC DIP (D)



Dimension:

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.334			0.210
A1	0.381			0.015		
A2	3.175	3.302	3.429	0.125	0.130	0.135
b		1.524			0.060	
b1		0.457			0.018	
D	24.892	26.162	26.924	0.980	1.030	1.060
E		7.620			0.300	
E1	6.223	6.350	6.477	0.245	0.250	0.255
e		2.540			0.100	
L	2.921	3.302	3.810	0.115	0.130	0.150
e_B	8.509	9.017	9.525	0.335	0.355	0.375
θ°	0°	7°	15°	0°	7°	15°

20 PINS – PLASTIC SOP (S)



Dimension:

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.362		2.642	0.093		0.104
A1	0.101		0.305	0.004		0.012
A2	2.260		2.337	0.089		0.092
b		0.406			0.016	
c		0.203			0.008	
D	12.598		12.903	0.496		0.508
E	7.391		7.595	0.291		0.299
e		1.270			0.050	
H	10.007		10.643	0.394		0.419
L	0.406		1.270	0.016		0.050
F		0.508X45°			0.020X45°	
y			0.101			0.004
θ°	0°		8°	0°		8°

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