HDMI Transmitter Port Protection and Interface Device

Features

- 0.05pF matching capacitance between the TMDS intra-pair
- Overcurrent output protection
- Level shifting circuitry, including ±8kV ESD protection on all TMDS lines
- Matched 0.5mm trace spacing (TSSOP)
- Simplified layout for HDMI connectors
- Backdrive protection

Applications

- PC
- Consumer Electronics
- Set Top Box
- Displays and Digital Television

Product Description

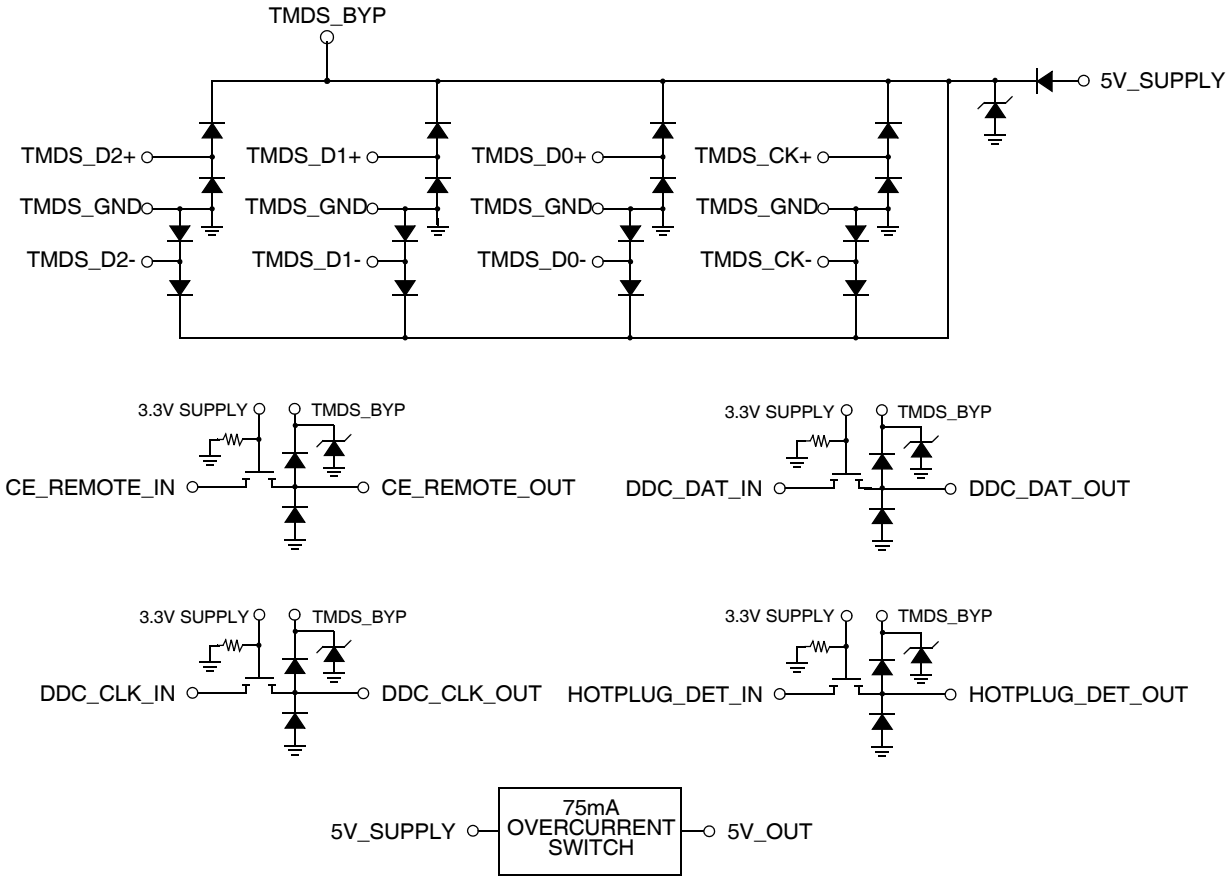
The CM2020 HDMI Transmitter Port Protection and Interface Device is specifically designed for next generation HDMI Host interface protection.

An integrated package provides all ESD, level shift, overcurrent output protection and backdrive protection for an HDMI port in a single 38-Pin TSSOP package.

The CM2020 part is specifically designed to complement the CM2021 protection part in HDMI receivers (Displays, CE devices, etc.)

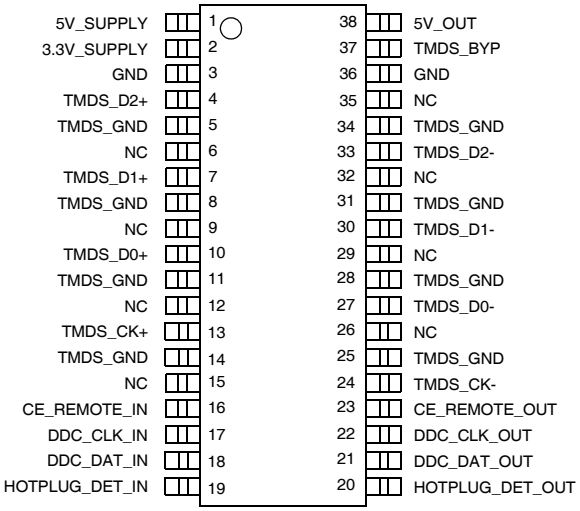
The CM2020 also incorporates a silicon overcurrent protection device for +5V supply voltage output to the connector.

Electrical Schematic



PACKAGE / PINOUT DIAGRAM

TOP VIEW



38-PIN TSSOP PACKAGE

Note: This drawing is not to scale.

PIN DESCRIPTIONS

PINS	NAME	DESCRIPTION
37	TMDS_BYP	This input pin is used to connect an optional external 0.1uF ceramic bypass capacitor only to enhance the ESD protection level. Note: Do not connect this pin to GND or any power rail.
4	TMDS_D2+	TMDS 0.9pF ESD protection.
33	TMDS_D2-	TMDS 0.9pF ESD protection.
7	TMDS_D1+	TMDS 0.9pF ESD protection.
30	TMDS_D1-	TMDS 0.9pF ESD protection.
10	TMDS_D0+	TMDS 0.9pF ESD protection.
27	TMDS_D0-	TMDS 0.9pF ESD protection.
13	TMDS_CK+	TMDS 0.9pF ESD protection.
24	TMDS_CK-	TMDS 0.9pF ESD protection.
16	CE_REMOTE_IN	3.3V_SUPPLY referenced logic level in.
23	CE_REMOTE_OUT	5V_SUPPLY referenced logic level out plus 3.5pF ESD.
17	DDC_CLK_IN	3.3V_SUPPLY referenced logic level in.
22	DDC_CLK_OUT	5V_SUPPLY referenced logic level out plus 3.5pF ESD.
18	DDC_DAT_IN	3.3V_SUPPLY referenced logic level in.
21	DDC_DAT_OUT	5V_SUPPLY referenced logic level out plus 3.5pF ESD.
19	HOTPLUG_DET_IN	3.3V_SUPPLY referenced logic level in.
20	HOTPLUG_DET_OUT	5V_SUPPLY referenced logic level out plus 3.5pF ESD.
2	3.3V_SUPPLY	Bias for CE / DDC / HOTPLUG level shifters.
1	5V_SUPPLY	Current source for 5V_OUT.
38	5V_OUT	75mA minimum overcurrent protected 5V output.
3, 5, 8, 11, 14, 25, 28, 31, 34, 36	GND / TMDS_GND	GND reference.
6, 9, 12,15, 26, 29, 32, 35	NC	No Connect.

Ordering Information

PART NUMBERING INFORMATION					
		Standard Finish		Lead-free Finish	
Pins	Package	Ordering Part Number[1]	Part Marking	Ordering Part Number[1]	Part Marking
38	TSSOP-38	CM2020-00TS	CM2020-00TS	CM2020-00TR	CM2020-00TR

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	RATING	UNITS
V_{CC5}, V_{CC3}	6.0	V
DC Voltage at any Channel Input	[GND - 0.5] to [VCC + 0.5]	V
Storage Temperature Range	-65 to +150	°C
Operating Temperature Range	-40 to +85	°C

STANDARD (RECOMMENDED) OPERATING CONDITIONS					
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
5V_SUPPLY	Operating Supply Voltage		5	5.5	V
3.3V_SUPPLY	Bias Supply Voltage	1	3.3	5.5	V

Specifications (cont'd)

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
I_{CC5}	Operating Supply Current	5V_SUPPLY = 5.0V		110	130	µA
I_{CC3}	Bias Supply Current	3.3V_SUPPLY = 3.3V		1	5	µA
V_{DROP}	5V_OUT Overcurrent Output Drop	5V_SUPPLY= 5.0V, I_{OUT}=55mA		65	100	mV
I_{SC}	5V_OUT Short Circuit Current Limit	5V_SUPPLY= 5.0V, 5V_OUT = GND	90	135	175	mA
I_{OFF}	OFF state leakage current, level shifting NFET	3.3V_SUPPLY = 0V		0.1	5	µA
$I_{BACKDRIVE}$	Current conducted from output pins to V_SUPPLY rails when powered down	5V_SUPPLY < V_{CH_OUT}; Signal pins: TMDS_[2:0]+/-, TMDS_CK+/-, CE_REMOTE_OUT, DDC_DAT_OUT, DDC_CLK_OUT, HOTPLUG_DET_OUT, 5V_OUT Only		0.1	5	µA
V_{ON}	VOLTAGE drop across level shifting NFET when ON	3.3V_SUPPLY = 2.5V, V_S = GND, I_{DS} = 3mA	75	95	140	mV
V_F	Diode Forward Voltage Top Diode Bottom Diode	I_F = 8mA, T_A = 25°C, Note 2	 0.6 0.6	 0.85 0.85	 0.95 0.95	 V V
V_{ESD}	ESD Withstand Voltage (IEC)	Pins 4, 7, 10, 13, 20, 21, 22, 23, 24, 27, 30, 33; Notes 2 and 3	±8			kV
V_{ESD}	ESD Withstand Voltage (HBM)	Pins 1, 2, 16, 17, 18, 19, 37, 38; Notes 2 and 4	±2			kV
V_{CL}	Channel Clamp Voltage @ 8kV HBM ESD Positive Transients Negative Transients	T_A = 25°C, Notes 2 and 4		 9.0 -9.0		 V V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	I = 1A, T_A = 25°C, Note 5		 3.0 1.5		 Ω Ω
I_{LEAK}	TMDS Channel Leakage Current	T_A = 25°C, Note 2		0.01	1	µA
$C_{IN,}$ TMDS	TMDS Channel Input Capacitance	5V_SUPPLY= 5.0V, Measured at 1MHz, V_{BIAS}=2.5V, Note 2		0.9	1.2	pF
$\Delta C_{IN,}$ TMDS	C_{IN} Matching Capacitance	5V_SUPPLY= 5.0V, Measured at 1MHz, V_{BIAS}=2.5V, Note 2, 6		0.05		pF
C_{MUTUAL}	Mutual Capacitance between signal pin and NC pin	5V_SUPPLY= 0V, Measured at 1MHz, V_{BIAS}=2.5V, Note 2		0.07		pF

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)						
$C_{IN,}$ DDC	Level Shifting Input Capacitance, Capacitance to GND	5V_SUPPLY= 0V, Measured at 100KHz, V_{BIAS}=2.5V, Note 2		3.5	4	pF
$C_{IN,}$ CEC	Level Shifting Input Capacitance, Capacitance to GND	5V_SUPPLY= 0V, Measured at 100KHz, V_{BIAS}=2.5V, Note 2		3.5	4	pF
$C_{IN,}$ HP	Level Shifting Input Capacitance, Capacitance to GND	5V_SUPPLY= 0V, Measured at 100KHz, V_{BIAS}=2.5V, Note 2		3.5	4	pF

Note 1: Operating Characteristics are over Standard Operating Conditions unless otherwise specified.
Note 2: This parameter is guaranteed by design and verified by device characterization.
Note 3: Standard IEC 61000-4-2, $C_{DISCHARGE}$=150pF, $R_{DISCHARGE}$=330Ω
Note 4: Human Body Model per MIL-STD-883, Method 3015, $C_{DISCHARGE}$=100pF, $R_{DISCHARGE}$=1.5kΩ
Note 5: These measurements performed with no external capacitor on TMDS_BYP.
Note 6: Intra-pair matching, each TMDS pair (i.e. D+, D-)

Performance Information

Typical Filter Performance (T_A=25°C, DC Bias=0V, 50 Ohm Environment)

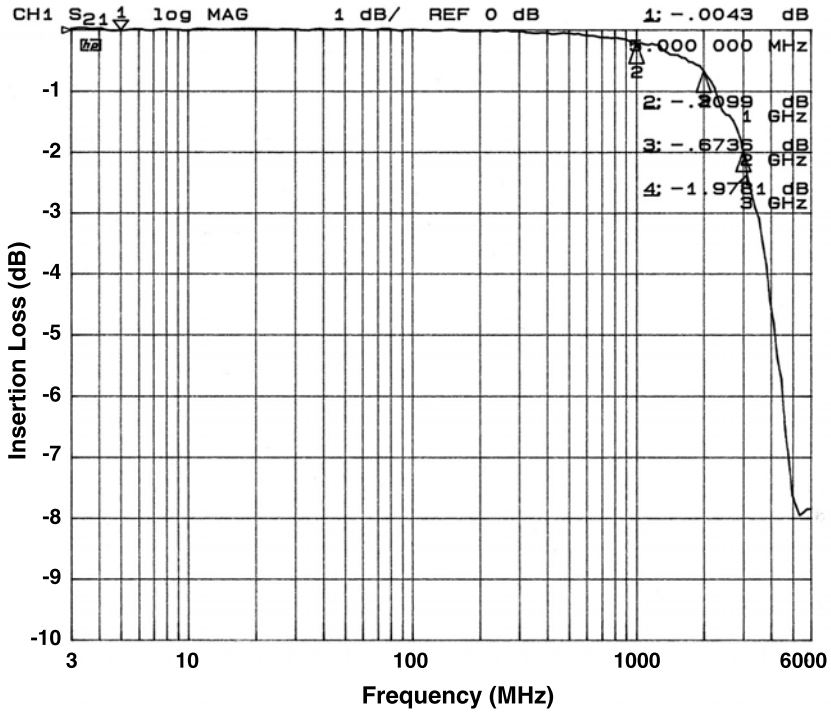


Figure 1. Insertion Loss vs. Frequency (TMDS_D1- to GND)

Application Information

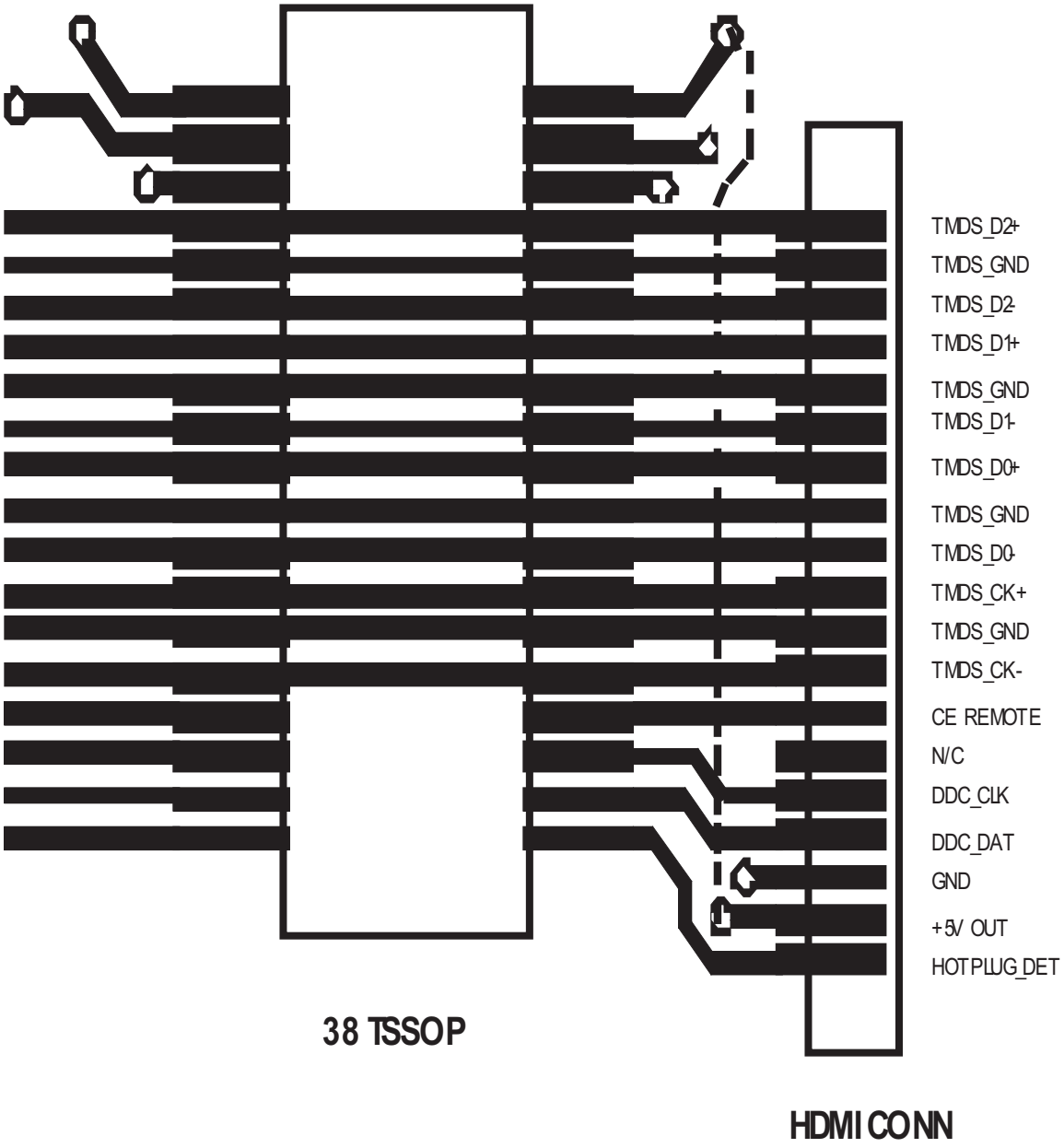


Figure 2. Typical Application for CM2020

Mechanical Details

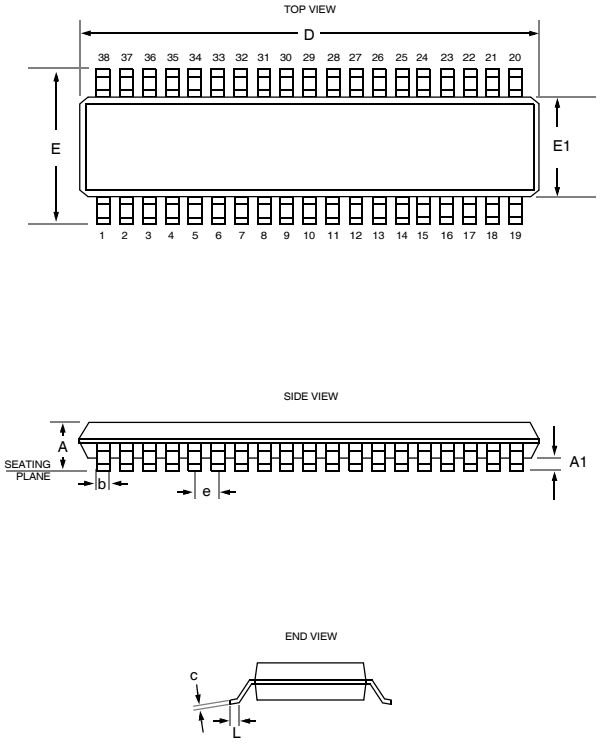
TSSOP-38 Mechanical Specifications

CM2020 devices are supplied in 38-pin TSSOP packages. Dimensions are presented below.

For complete information on the TSSOP-38, see the California Micro Devices TSSOP Package Information document.

PACKAGE DIMENSIONS				
Package	TSSOP			
JEDEC No.	MO-153 (Variation BD-1)			
Pins	38			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006
b	0.17	0.27	0.007	0.011
c	0.09	0.20	0.004	0.008
D	9.60	9.80	0.378	0.386
E	6.40 BSC		0.252 BSC	
E1	4.30	4.50	0.169	0.177
e	0.50 BSC		0.020 BSC	
L	0.45	0.75	0.018	0.030
# per tape and reel	2500 pieces			
Controlling dimension: millimeters				

Mechanical Package Diagrams



Package Dimensions for TSSOP-38