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APPLICATION NOTE 842

Mathcad Calculates Input Capacitor for Step-Down Buck Regulator

Step-down buck regulators are extremely popular in a variety of portable and non-portable equipment. These buck converters are terminated with an input capacitor, C_{IN} and an output capacitor, C_O, at the output. C_{IN} provides high-frequency filtering, so that V_{IN} has low ripple. This application note helps a system designer to set-up Mathcad and compute C_{IN} for a particular step-down DC-DC regulator design.

Step-down buck regulators are used in portable and non-portable equipment, such as PDAs, cell phones, computers, telcom/networks, and consumer products. These buck converters are terminated with an input capacitor, C_{IN}, at the input, and an output capacitor, C_O, at the output. The function of both capacitors is to provide high-frequency filtering, so that V_{IN} and V_O are close to pure DC, with little ripple noise.

A capacitor is often represented by a series combination of R, L, and C. R is the equivalent series resistance (ESR) and L is the equivalent series inductance (ESL). The term C is equal to the ideal capacitor value.

Figure 1 shows a typical schematic of a synchronous buck power stage and the associated waveforms to be used for the derivations and calculations.

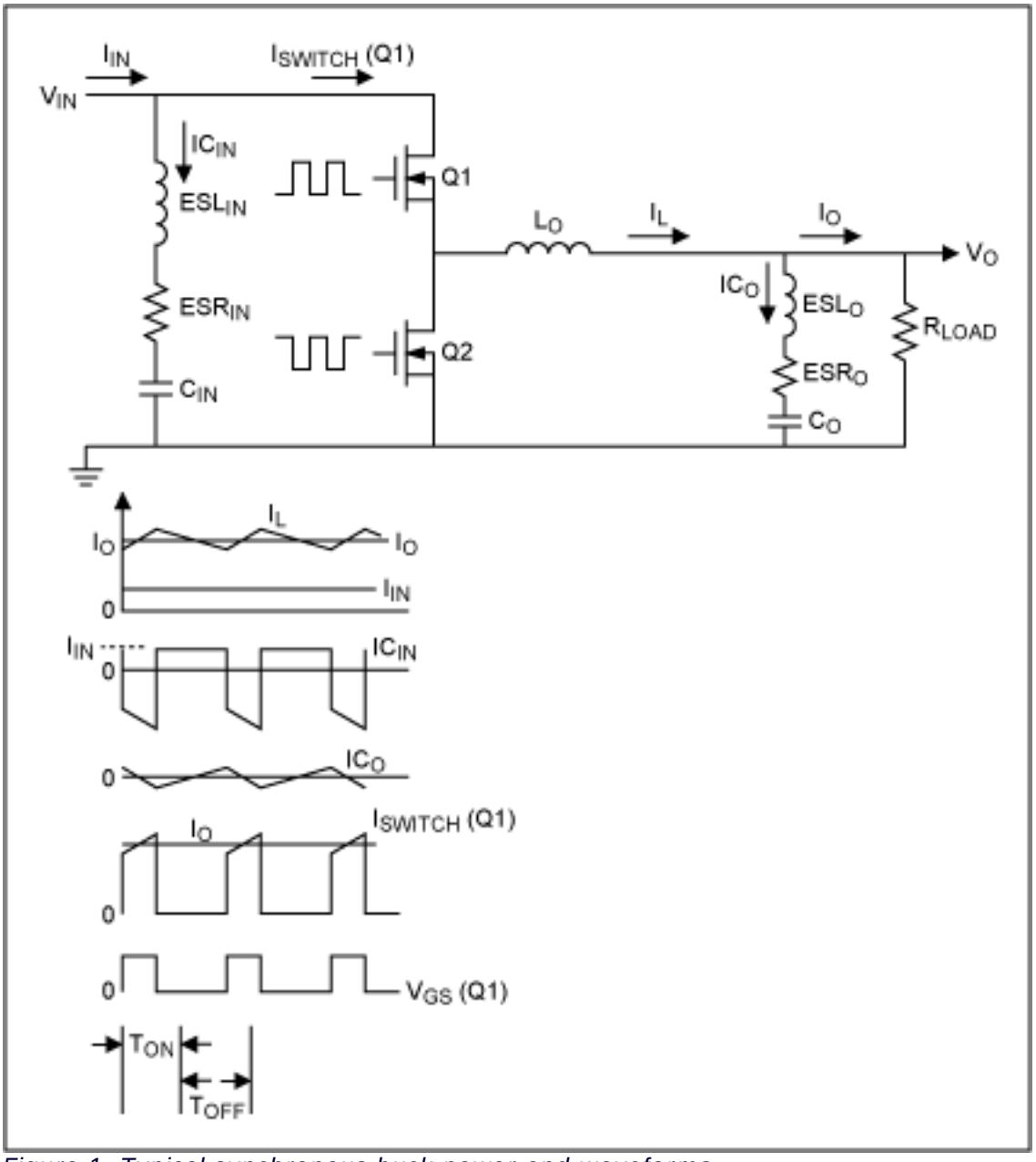

Figure 1. Typical synchronous buck power and waveforms

Setting up variables and data for example calculation in MathCad:

Input Voltage	$V_I := 12$	$n := 10^{-9}$
Output Voltage	$V_O := 3.3$	$u := 10^{-6}$, $k := 10^{3}$
Output Current	$I_O := 25$	$m := 10^{-3}$
High-Side Switch Drop	$V_{HS} := 0.227$	
Low-Side Switch Drop	$V_{LS} := 0.113$	
Switching Current Rise Time	$T_{RS} := 25 \cdot n$	
Switching Current Fall Time	$T_{FS} := 25 \cdot n$	
Switching Frequency	$F_S := 600 \cdot k$	

Duty Cycle	$D := (V_O + V_{LS}) / (V_I - V_{HS} + V_{LS})$	$D = 0.287$
Switch(Q1) On Time	$T_{ON} := D / F_S$	
Switch(Q1) Off Time	$T_{OFF} := 1 / F_S - T_{ON}$	
Converter Efficiency	$\eta := 0.9$	
Input Current	$I_{IN} := V_O \cdot I_O / \eta \cdot V_I$	$I_{IN} := 7.639$
Output Inductor Pk-Pk Ripple Current	$I_{RPL} := 0.3 \cdot I_O$	
Input Capacitor	$C_{IN} := 40 \cdot u$	(4 x 10uF ceramic of ESR = 10mΩ each and ESL = 2.5nH each)
Input Capacitor ESR	$ESR_{CIN} := 2.5 \cdot m$	
Input Capacitor ESL	$ESL_{CIN} := 0.625 \cdot n$	

As seen in Figure 1, the output ripple current through the input capacitor results in voltage across C_{IN} that reflects the values of ESR, ESL, and C. The ESR and ESL cause fast step voltage rise and fall, whereas C has a linear voltage rise and fall due to the fact that the capacitor charges and discharges. At the start of T_{ON}, C_{IN} sees a negative step current, which will produce a negative step voltage given by the following equation:

$$V_{STEP} = ESR_{CIN}(I_O - 0.5\, I_{RPL}) + ESL_{CIN}(I_O - 0.5\, I_{RPL}) / T_{RS}$$

During T_{ON}, the capacitor discharges an average current of $(I_O - I_{IN})$, which causes a linear ΔV of:

$$\Delta V_{CDIS} := (I_O - I_{IN}) \cdot T_{ON} / C_{IN}$$

The total voltage deviation from the start of T_{ON} to the end of T_{ON} is the summation of the above:

$$\Delta V_{ON}R := ESR_{CIN}(I_O - 0.5\, I_{RPL}) \qquad \Delta V_{ON}R := 0.053 \qquad I_{IN}T_{OFF} := 9.076 \cdot 10^{-6}$$

$$\Delta V_{ON}L := ESL_{CIN} \frac{(I_O - 0.5\, I_{RPL})}{T_{RS}} \qquad \Delta V_{ON}L := 0.531 \qquad (I_O - I_{IN})T_{ON} = 8.309 \cdot 10^{-6}$$

$$\Delta V_{ON}C := (I_O - I_{IN}) \frac{T_{ON}}{C_{IN}} \qquad \Delta V_{ON}C := 0.208$$

$$\Delta V_{ON} := \Delta V_{ON}R + \Delta V_{ON}L + \Delta V_{ON}C \qquad \Delta V_{ON} := 0.792$$

Similarly, but with opposite polarity, at the start of T_{OFF} and during T_{OFF}, the following voltage deviations are calculated:

$$\Delta V_{OFF}R := ESR_{CIN}(I_O + 0.5\, I_{RPL}) \qquad \Delta V_{OFF}R := 0.072$$

$$\Delta V_{OFF}L := ESL_{CIN}\frac{(I_O + 0.5\, I_{RPL})}{T_{FS}} \qquad \Delta V_{OFF}L := 0.719$$

$$\Delta V_{OFF}C := I_{IN}\frac{T_{OFF}}{C_{IN}} \qquad \Delta V_{OFF}C := 0.227$$

$$\Delta V_{OFF} := \Delta V_{OFF}R + \Delta V_{OFF}L + \Delta V_{OFF}C \qquad \Delta V_{OFF} := 1.018$$

The peak-to-peak ripple is equal to the higher of the two, which is ΔVOFF~1V. As seen from the above, most of the ripple is caused by ESL and the fast di/dt. Di/dt of 1A/nS is very realistic in today's MHz DC-DC converters. Therefore, to reduce the ripple, more capacitors would need to be placed in parallel. Lower value ceramic capacitors, such as 0.1uF in the 0805 or 1206 package, have half the ESL of the 10uF, or ~1.2nH. Place the 0.1uF as close as possible to the sensitive decoupling points.

Another parameter that needs to be determined is the RMS current through the input capacitor, so that the capacitor I_{RMS} rating is not exceeded. From the I_{CIN} waveform, the RMS current can be approximated (since the peak-to-peak inductor ripple current is usually 20-30% of I_O max) to be:

$$I_{CINRMS} := \sqrt{\left[(I_O - I_{IN}) \cdot \sqrt{D}\right]^2 + \left(I_{IN} \cdot \sqrt{1 - D}\right)^2}$$

Where $D = (V_O + V_{LS}) / (V_{IN} + V_{LS} + V_{HS})$, and $I_{IN} = (V_O \cdot I_O) / \eta \cdot V_{IN}$

$$I_{CINRMS} := 11.32$$

To simplify further, let $D = V_O/V_{IN}$ (since $V_0 >> V_{LS}$, and $V_{IN} + V_{LS} - V_{HS} \sim V_{IN}$), and $I_{IN} = V_O \cdot I_O/V_{IN}$ (since efficiency $\eta \sim 1$), so that the I_{CINRMS} equation above becomes:

$$I_{CINRMS} := \frac{I_O}{V_I}\left[\sqrt{V_O \cdot (V_I - V_O)}\right]$$

$$I_{CINRMS} := 11.163$$

The simplified version produces only ~1.4% error, and involves only three known parameters: V_I, V_O, and I_O. V_O is fixed, and I_O, V_I can have a specified range, depending on the application. However, I_{CINRMS} always has a maximum value of $I_O/2$, which happens at $V_I = 2V_O$, and decreases the value for $V_I < 2I_O$ and $V_I > 2L_O$. The plot in **Figure 2** below illustrates this:

$$V_I := 1.1\ V_O, 1.2\ V_O .. 4V_O$$

$$I_{CINRMS}(V_I) := \frac{I_O}{V_I}\left[\sqrt{V_O \bullet (V_I - V_O)}\right]$$

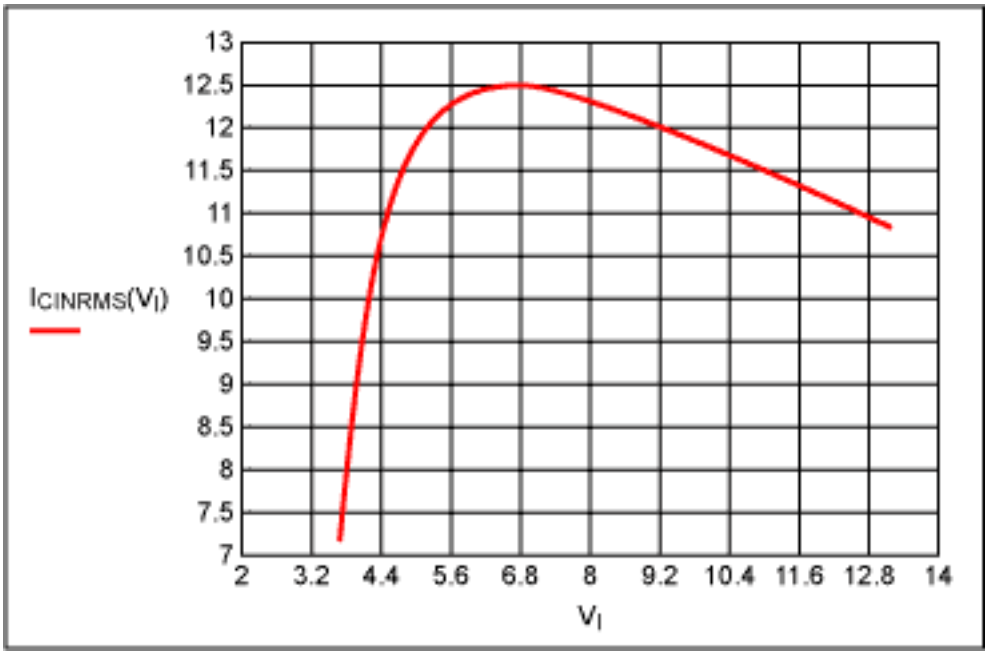

Figure 2.

Due to the high di/dt and pulsating current, a ceramic capacitor is chosen, for its low ESR and ESL. A higher ripple current rating is required at high-frequency to contain the switching spikes. Make sure the RMS current rating of the capacitor is well above the maximum operating RMS current. For long-term reliability, choose a capacitor that will exhibit less than a 10°C temperature rise. Most capacitor manufacturers provide plots that show RMS current vs. temperature rise.

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