Preliminary

EN5336Q

3A Voltage Mode Synchronous Buck PWM DC-DC Converter with Integrated Inductor Resistor Programmable Output

Description

This Enpirion solution is a Power System on Silicon DC-DC converter. It is specifically designed to meet the precise voltage and fast transient requirements of present and future high-performance, low-power processor, DSP, FPGA, memory boards and system level applications in a distributed power architecture. Advanced circuit techniques, ultra high switching frequency, and very advanced, high-density, integrated circuit and proprietary inductor technology deliver high-quality, ultra compact, non-isolated DC-DC conversion. This device requires only an input, output, and small soft-start programming capacitor and a resistor divider.

The Enpirion solution significantly helps in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, a reduction in the number of vendors required for the complete power solution helps to enable an overall system cost savings.

All Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

Typical Application Circuit

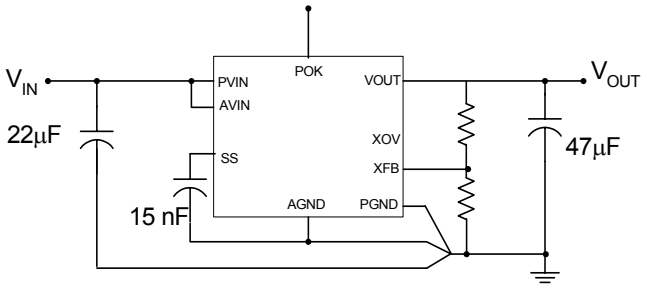

Figure 1. Simple Layout.

Features

- Greater than 10W output power
- INDUCTOR NOT REQUIRED
- Total solution footprint less than 130mm2
- Minimal external components
- 5MHz operating frequency for small external capacitors and excellent transient response
- High efficiency, greater than 90%
- 2% accuracy over line, load and temp
- Internal compensated with option to optimize with minimal external components.
- Wide input voltage range of 2.375V to 5.5V
- Resistor divider Output Voltage Select
- Output enable pin and Power OK signal
- Programmable soft-start time
- Programmable over-current protection
- Programmable over-voltage protection
- Thermal shutdown, short circuit, over-voltage and under-voltage protection
- RoHS compliant, MSL level 3, 260C reflow

Applications

- Point of load regulation for low-power processors, network processors, DSPs, FPGAs, and ASICs
- Notebook computers, servers, workstations
- Broadband, networking, LAN/WAN, optical
- Low voltage, distributed power architectures with 2.5V, 3.3V or 5V rails

Ordering Information

Part Number	Temp Rating (°C)	Package
EN5336QI	-40 to +85	44-pin QFN
EN5336QI-T	-40 to +85	44-pin QFN T&R
EN5336QC-E	QFN Evaluation Board	

Pin Configuration

Below is a top view diagram of the EN5336Q package.

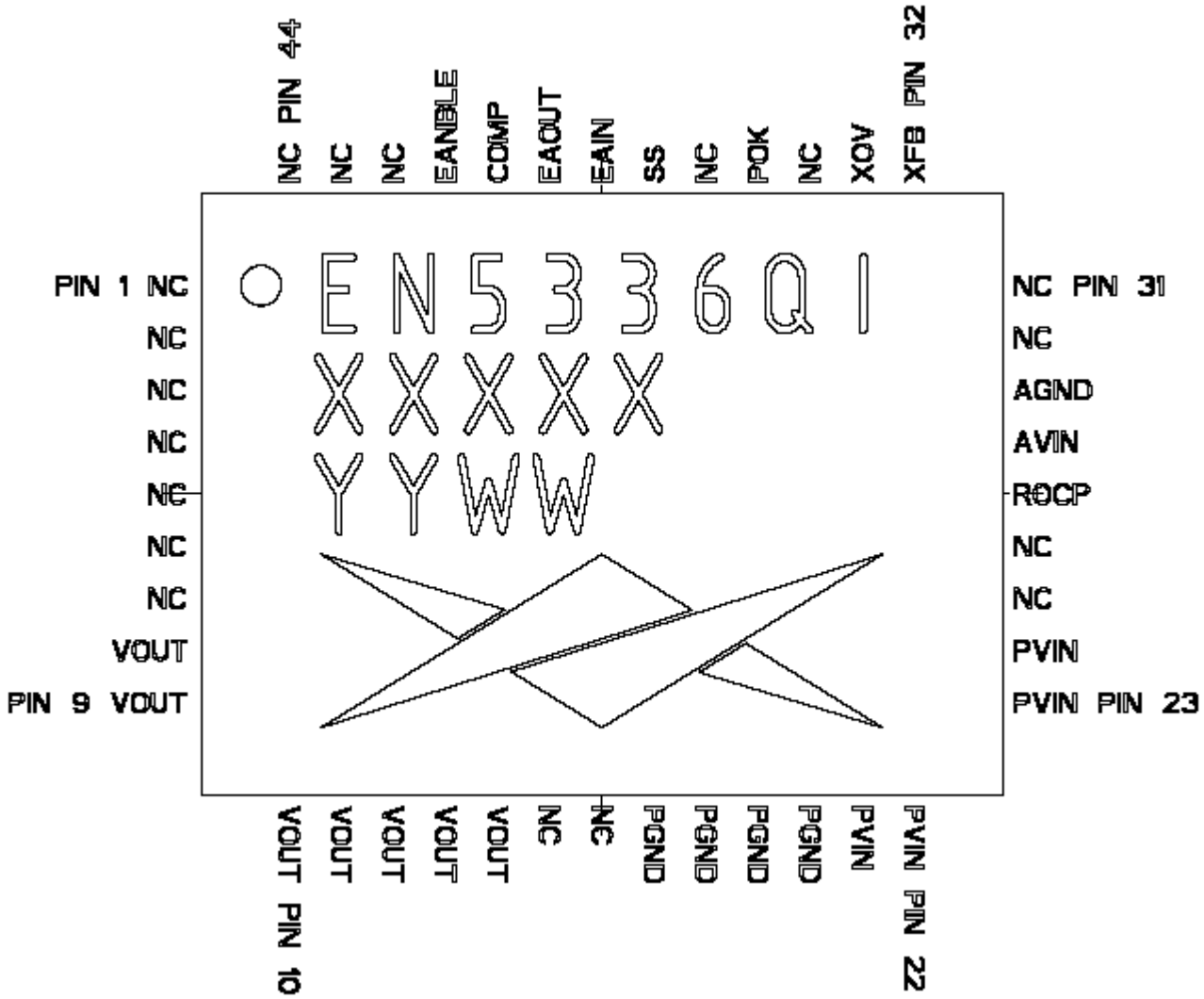

Figure 2. Pin Diagram, top view.

NOTE: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. Failure to follow this guideline may result in part malfunction or damage.

NOTE: All perimeter pins must be soldered to PCB.

Pin Descriptions

PIN	NAME	FUNCTION
1-7	NC	NO CONNECT – Do not electrically connect these pins to each other or to any other electrical signal. CAUTION!: May be internally connected.
8-14	VOUT	Regulated converter output. Connect these pins to the load and place output capacitor from these pins the PGND pins 17-18
15-16	NC	NO CONNECT – Do not electrically connect these pins to each other or to any other electrical signal. CAUTION!: Internally connected to switching node. Take care to route signals away from these pins.
17-20	PGND	Input/Output power ground. Connect these pins to the ground electrode of the Input and output filter capacitors. Refer to layout guideline section for details.
21-24	PVIN	Input power supply. Connect to input power supply. Decouple with input capacitor to PGND.
25-26	NC	NO CONNECT – Do not electrically connect these pins to each other or to any other electrical signal. CAUTION!: May be internally connected.
27	ROCP	Optional Over Current Protection adjust pin. Place ROCP resistor between this pin and AGND (pin 40) to adjust the over current trip point.
28	AVIN	Analog voltage input for the controller circuits. Connect this pin to the input power supply.
29	AGND	Analog ground for the controller circuits.
30-31	NC	NO CONNECT – Do not electrically connect these pins to each other or to any other electrical signal. CAUTION!: May be internally connected.
32	XFB	Feedback pin for external voltage divider network.
33	XOV	Over voltage programming feedback pin.
34	NC	NO CONNECT – Do not electrically connect this pin to any electrical signal. CAUTION!: May be internally connected.
35	POK	Power OK is an open drain transistor for power system state indication. POK is a logic high when VOUT is with -10% to +20% of VOUT nominal.
36	NC	NO CONNECT – Do not electrically connect this pin to any electrical signal. CAUTION!: May be internally connected.
37	SS	Soft-Start node. The soft-start capacitor is connected between this pin and AGND. The value of this capacitor determines the startup time.
38	EAIN	Optional Error Amplifier input. Allows for customization of the control loop response.
39	EAOUT	Optional Error Amplifier output. Allows for customization of the control loop response.
40	COMP	Optional Error Amplifier Buffer output. Allows for customization of the control loop response.
41	ENABLE	Input Enable. Applying a logic high, enables the output and initiates a soft-start. Applying a logic low disables the output.
42-44	NC	NO CONNECT – Do not electrically connect these pins to each other or to any other electrical signal. CAUTION!: May be internally connected.

Block Diagram

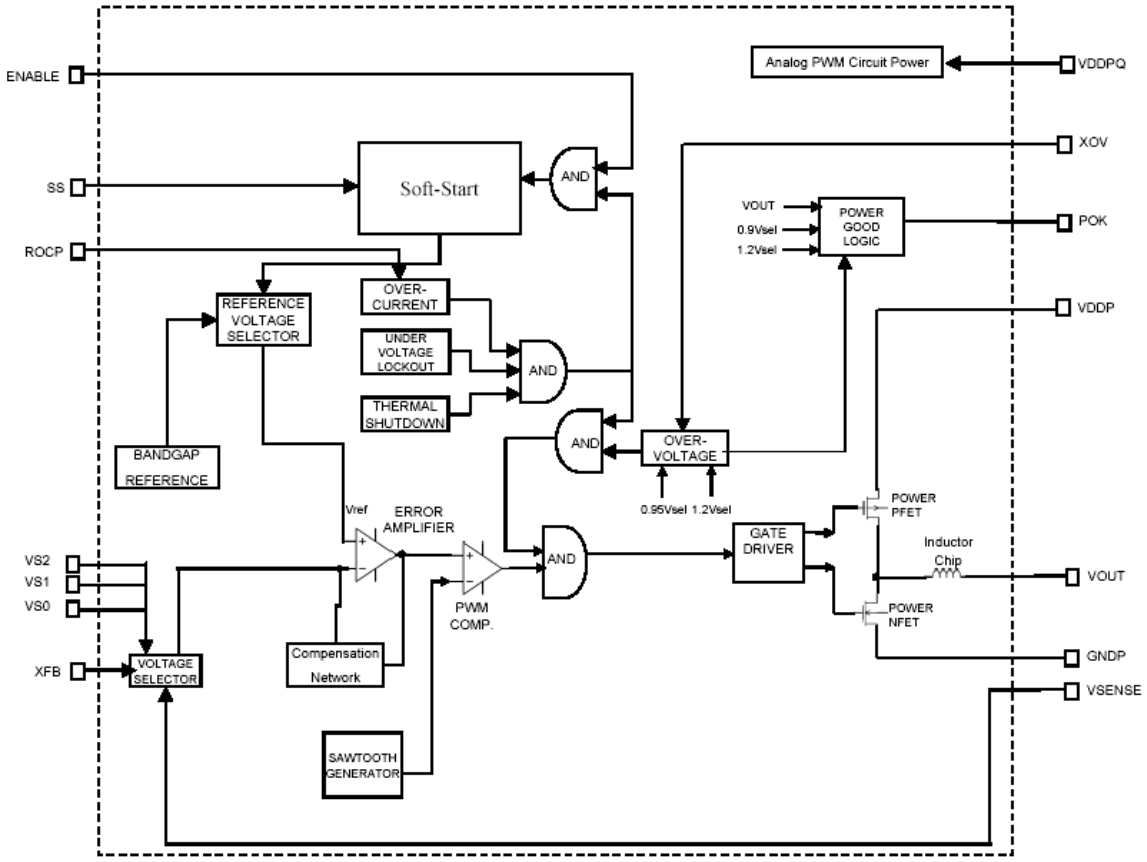

Figure 3. System block diagram.

Absolute Maximum Ratings

CAUTION: Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Maximum Electrical Ratings	Min	Max
Voltages on: V_{IN}, V_{OUT}	-0.3V	7.0V
Voltages on: XFB, XOV	-0.3V	2.7V
Voltages on: EAIN, EAOUT, COMP	-0.3V	2.7V
Voltages on: ENABLE, ROCP	-0.3V	V_{IN} + 0.3V
Maximum Thermal Ratings		
Ambient operating range	-40°C	+85°C
Storage Temperature Range	-65°C	+150°C
Reflow Peak Body Temperature MSL3 (10 Sec)		+260°C

Thermal Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Operating Junction Temp	T_J	-40		+125	°C
Thermal Shutdown	T_{SD}		160		°C
Thermal Shutdown Hysteresis	T_{SDH}		15		°C
Thermal Resistance: Junction to Case	θ_{JC}		3		°C/W
Thermal Resistance: Junction to Ambient	θ_{JA}		24		°C/W

Electrical Characteristics

NOTE: V_{IN}=3.3V over operating temperature range unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}		2.375		5.5	V
Shut-Down Supply Current	I_S	ENABLE=low		50		µA
Switching Frequency	F_{OSC}			5		MHz
Thermal Overload Trip Point	T_J			160		°C
V_{OUT}						
Regulated Feedback voltage	V_{XFB}			0.75		V
Overvoltage programming feedback pin voltage	V_{XOV}			0.90		
Range	V_{OUT}	Using external voltage divider	0.75		V_{IN}-0.6	V
Accuracy	V_{OUT}	Over line, load and temperature			2.0	%
Line Regulation	□V_{OUT}	V_{IN} = 2.5 to 5.0 volts		TBD		%/V
Load Regulation	□V_{OUT}	I_{LOAD} = 0 to 6A		TBD		%/A
Temperature Regulation	□V_{OUT}	T_A= 0 to 70ºC		TBD		mV
	□V_{OUT}	T_A= -40 to 85ºC		TBD		mV
Maximum Continuous Output Current						
Output Current	I_{OUT}				3	A
Enable Operation						
Disable Threshold	$V_{DISABLE}$	Max voltage to ensure the converter is disabled			0.8	V
Enable Threshold	V_{ENABLE}	2.375V ≤ V_{IN} ≤ 5.5V 5.5V < V_{IN}	1.8 2.0			V
Power OK Operation						
POK Low threshold		Vout rising Vout falling		90% 87%		
POK High threshold		Vout rising Vout Falling		Prog. 95%		
POK low voltage	V_{POK}				0.4	V
POK high voltage	V_{POK}				V_{IN}	V
ESD Rating						
PGND, VIN, VOUT						
AVIN, AGND						
EN, ROCP						
EAIN, EAOUT, COMP						
XFB, XOV						

Theory of Operation

Synchronous Buck Converter

The EN5336 is a synchronous, programmable power supply with integrated power MOSFET switches and integrated inductor. The nominal input voltage range is 2.4-5.5V. The output voltage is programmed using an external resistor divider network. The feedback control loop is a voltage-mode controller with a type III compensation network. The part uses a low-noise PWM topology. Up to 3A of continuous output current can be drawn from this converter. The 5MHz operating frequency enables the use of small-size input and output capacitors, and a wide controller bandwidth.

The power supply has the following protection features:

- Programmable over-current protection (to protect the IC from excessive load current)
- Thermal shutdown with hysteresis.
- Over-voltage protection
- Under-voltage lockout circuit to disable the converter output when the input voltage is less than approximately 2.2V

Additional features include:

- Soft-start circuit, limiting the in-rush current when the converter is powered up.

Power good circuit indicating whether the output voltage is within 90% and the programmed OVP trip-point percentage of the programmed voltage.

Device Programming Options

The EN5336 output voltage is programmed using a simple resistor divider network. Figure 4 shows the resistor divider configuration.

The EN5336 output voltage and over voltage thresholds are determined by the voltages presented at the XFB and XOV pins respectively. These voltages are set by way of resistor dividers between V_{OUT} and AGND with the midpoint going to XFB and XOV.

It is recommended that Rb1 and Rb2 resistor values be ~2kΩ. Use the following equation to set the resistor Ra1 for the desired output voltage:

$$Ra1 = \frac{(Vout - 0.75V) * Rb1}{0.75V}$$

If over-voltage protection is desired, use the following equation to set the resistor Ra2 for the desired OVP trip-point:

$$Ra2 = \frac{(OVPtrip - 0.90V) * Rb2}{0.90V}$$

By design, if both resistor dividers are the same, the OV trip-point will be 20% above the nominal output voltage.

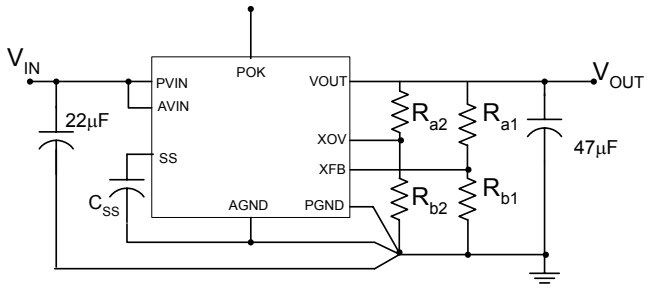

Figure 4. V_{OUT} and OVP resistor divider networks.

NOTE: if no OVP divider is present, there will be no over-voltage protection and POK will remain "high" as long as V_{OUT} remains above 90% of the nominal V_{OUT} setting.

Over-Voltage Protection

The Over-Voltage trip point is set as described above. When the output voltage exceeds the OV trip point, the PWM operation stops, the lower N-MOSFET is turned on and the POK signal goes low. When the output voltage drops below 95% of the programmed output voltage, normal PWM operation resumes and POK returns to its high state.

Input Capacitor Selection

The input capacitance requirement is approximately 22uF. In some applications, lower value capacitors are needed in parallel with the larger, capacitors in order to provide high frequency decoupling.

The input capacitor must be a X5R or X7R or equivalent dielectric formulation. Y5V or equivalent dielectric formulations lose capacitance with frequency, bias, and with temperature, thus are not suitable for switch-mode DC-DC converter input and output filter applications.

Output Capacitor Selection

The EN5366 has been optimized for use with approximately 50µF of output capacitance.

The output capacitor must be a X5R or X7R or equivalent dielectric formulation. Y5V or equivalent dielectric formulations lose capacitance with frequency, bias, and with temperature, thus are not suitable for switch-mode DC-DC converter input and output filter applications.

Output ripple voltage is determined by the aggregate output capacitor impedance. Output impedance, denoted as Z, is comprised of effective series resistance, ESR, and effective series inductance, ESL:

Z = ESR + ESL.

Placing output capacitors in parallel reduces the impedance and hence result in lower ripple voltage.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + ... + \frac{1}{Z_n}$$

Typical ripple versus capacitance is given below:

Output Capacitor Configuration	Typical Output Ripple (mV)
1 x 47uF	30
3 x 22 uF	20
5 x 10 uF	11

Enable Operation

The ENABLE pin provides a means to shut down the device, or enable normal operation. A logic low will disable the converter and cause it to shut down. A logic high will enable the converter into normal operation. When the ENABLE pin is asserted high, the device will go through a normal soft start. Enable may alternatively be tied to V_{IN}

Soft-Start Operation

Soft start is a method to reduce in-rush current when the device is enabled. The output voltage is ramped up slowly at start-up. The output rise time is controlled by the choice of a soft-start capacitor, which is placed between the SS pin (pin 37) and the AGND pin (pin 29).

Rise Time: $T_R = C_{ss} * 80K\Omega$

During start-up of the converter, the reference voltage to the error amplifier is gradually increased to its final level by an internal current source of typically 10uA charging the soft-start capacitor. Typical soft-start rise time is 1mS to 3mS. Typical SS capacitor values are in the range of 15nF to 30 nF.

POK Operation

The POK signal is an open drain signal indicating the output voltage is within the specified range. The POK signal will be a logic high when the output voltage is within 90% - 120% of the programmed output voltage. If the output voltage goes outside of this range, the POK signal will be a logic low until the output voltage has returned to within this range. In the event of an over-voltage condition the POK signal will go low and will remain in this condition until the output voltage has dropped to 95% of the programmed output voltage before returning to the high state (see also: Over Voltage Protection)

Over-Current Protection

The current limit function is achieved by sensing the current flowing through the P-MOSFET. When the sensed current exceeds the current limit, both NFET and PFET switches are turned off for the remainder of the clock cycle and the soft-start capacitor will begin to discharge. If the over-current condition is removed, the over-current protection circuit will enable the PWM operation. If the over-current condition persists, the soft start capacitor will eventually discharge and cause the converter to go through a full soft-start cycle.

It is possible to adjust the over-current set point by connecting a resistor between ROCP (pin 27) and GND (increase the trip point) or PVIN (decrease the trip point). The nominal over current trip point is set to 4.5A. The bias at ROCP pin is typically 0.8V.

In some cases, such as the start-up of FPGA devices, it is desirable to blank the over-current protection feature. In order to disable over-current protection, the ROCP pin should be tied to PVIN.

Thermal Overload Protection

Thermal shutdown will disable operation once the Junction temperature exceeds approximately 160ºC. When the junction temperature drops to approximately 135ºC, the converter will re-start with a normal soft-start.

Input Under-voltage Lock-out

Circuitry is provided to ensure that when the input voltage is below the specified UVLO voltage range, the converter will not start-up.

Compensation

The EN5336 is internally compensated through the use of a type 3 compensation network and is optimized for use with about 47µF of output capacitance and will provide excellent loop bandwidth and transient performance for most applications. (See the section on Capacitor Selection for details on recommended capacitor types.) Voltage mode operation provides high noise immunity at light load.

Specific applications may require modifications to the compensation. Terminals are provided to accommodate this need. For more information, contact Enpirion Applications Engineering support.

Design Considerations for Lead-Frame Based Modules

Exposed Metal on Bottom Of Package

Lead frame offers many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package.

Only the large thermal pad and the perimeter pads are to be mechanically or electrically connected to the PC board. PWB solder mask must be used to prevent connection to the other pads. Figure 4 shows the shape and location of these metal pads as well as the mechanical dimension of the large thermal pad and the pins. The “grayed-out” area represents the area that should be protected by solder mask on the PWB.

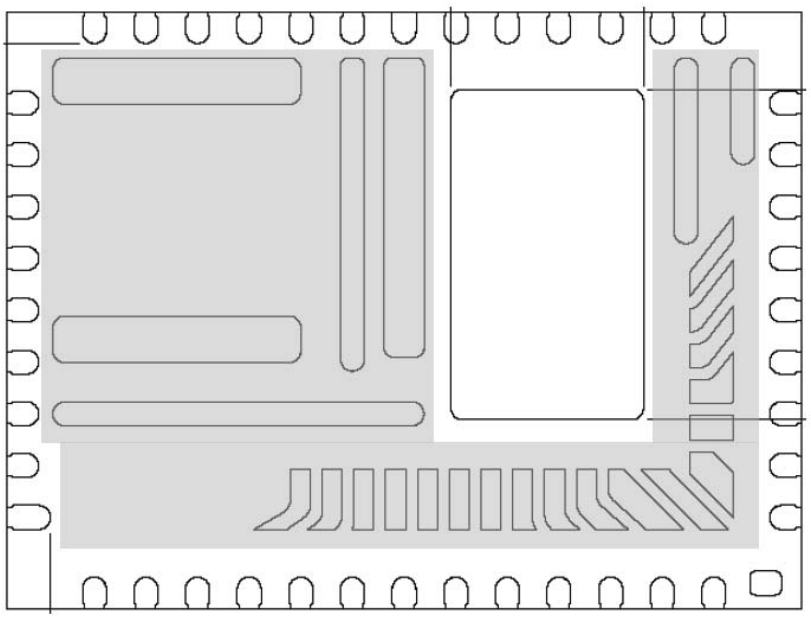

Figure 4. Lead-Frame exposed metal. Grey area highlights exposed metal that is not to be mechanically or electrically connected to the PWB.

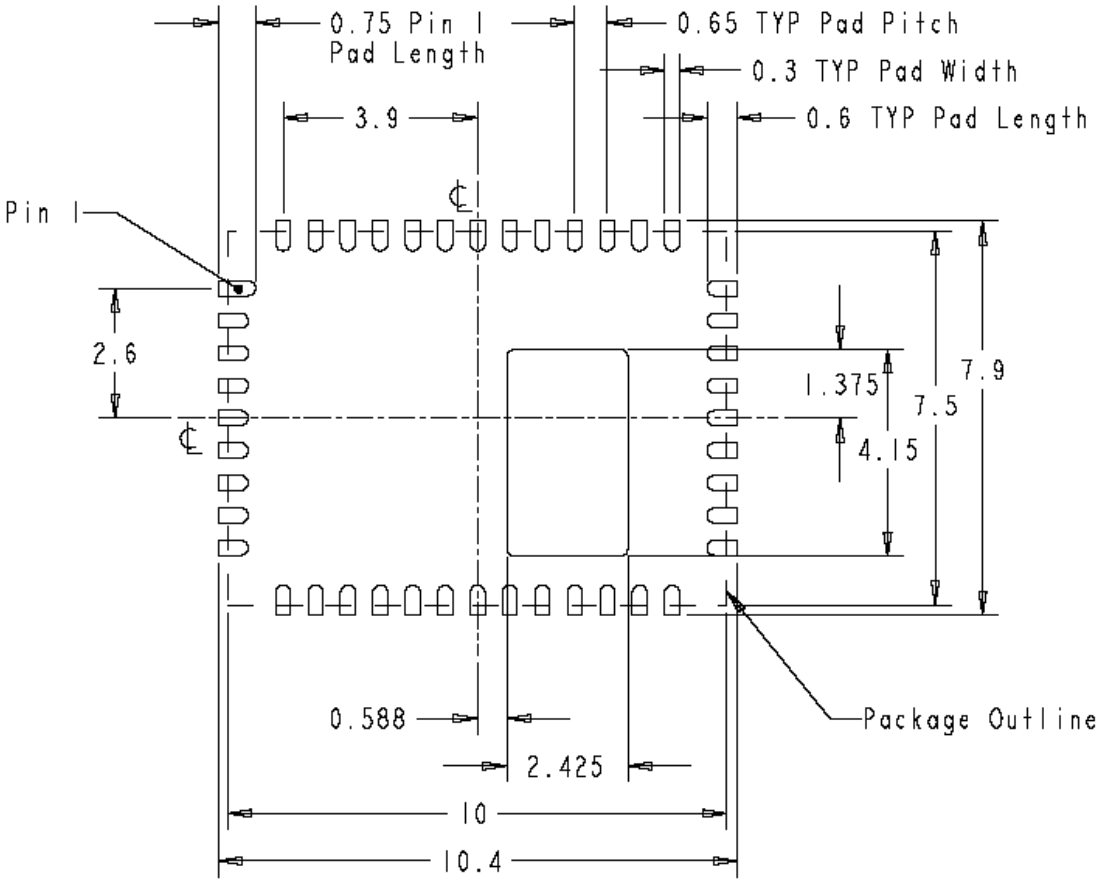

Figure 5. Recommended solder mask opening for PWB.

Package Dimensions

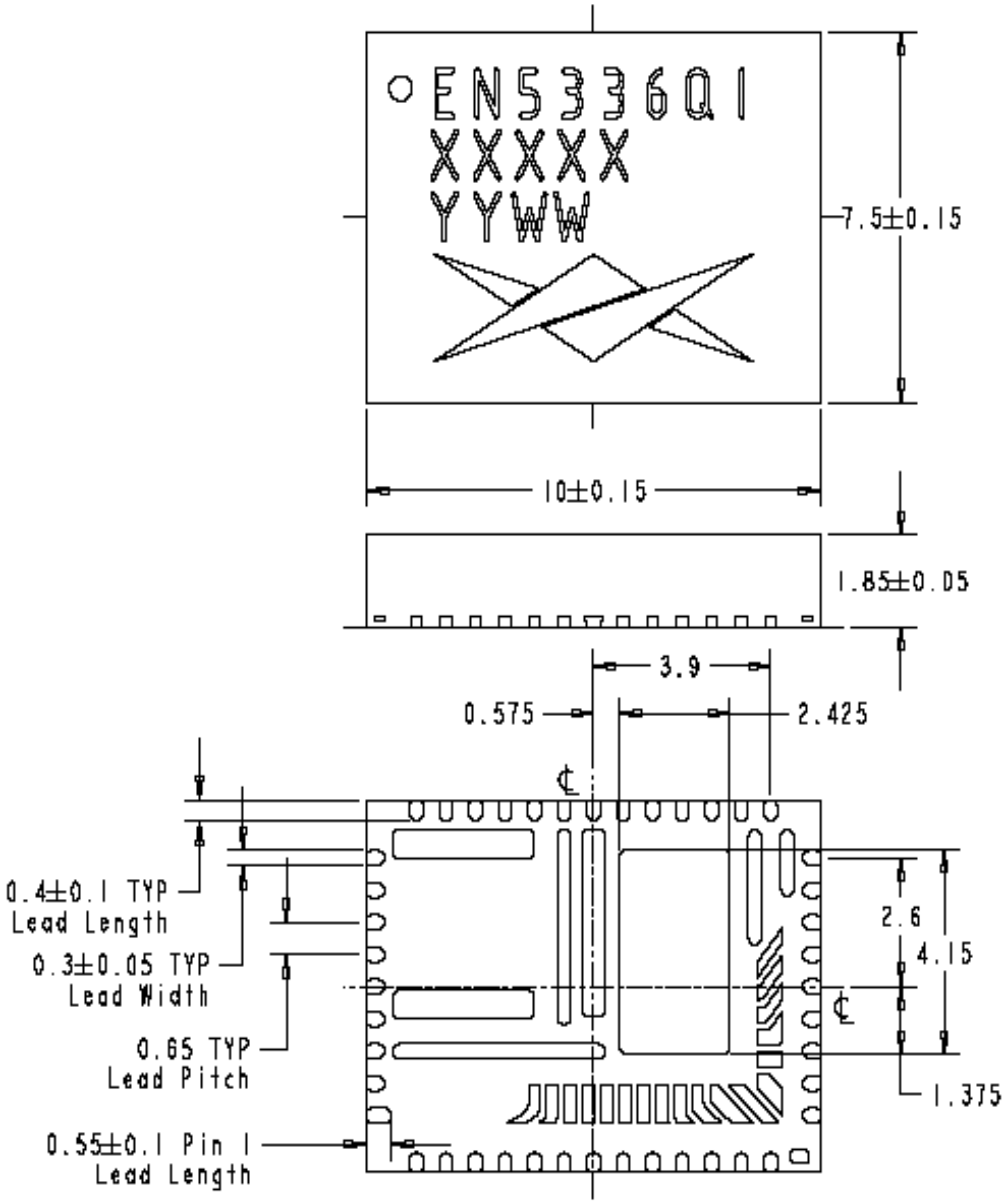

Figure 6. Package dimensions.

Contact Information

Enpirion, Inc.
685 Route 202/206
Suite 305
Bridgewater, NJ 08807
Phone: 908-575-7550
Fax: 908-575-0775