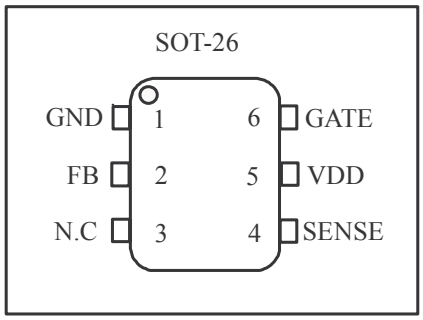
ABSTRACT

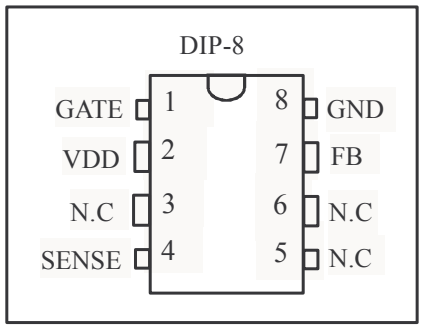
This highly integrated PWM controller, SG6849, offers several features to enhance the performance of a flyback converter for low power applications. Using the controller reduces costs of battery chargers and AC adapters. The no-load power consumption can be less than 200mW for universal AC input voltage range to meet the power conservation requirement.

FEATURES

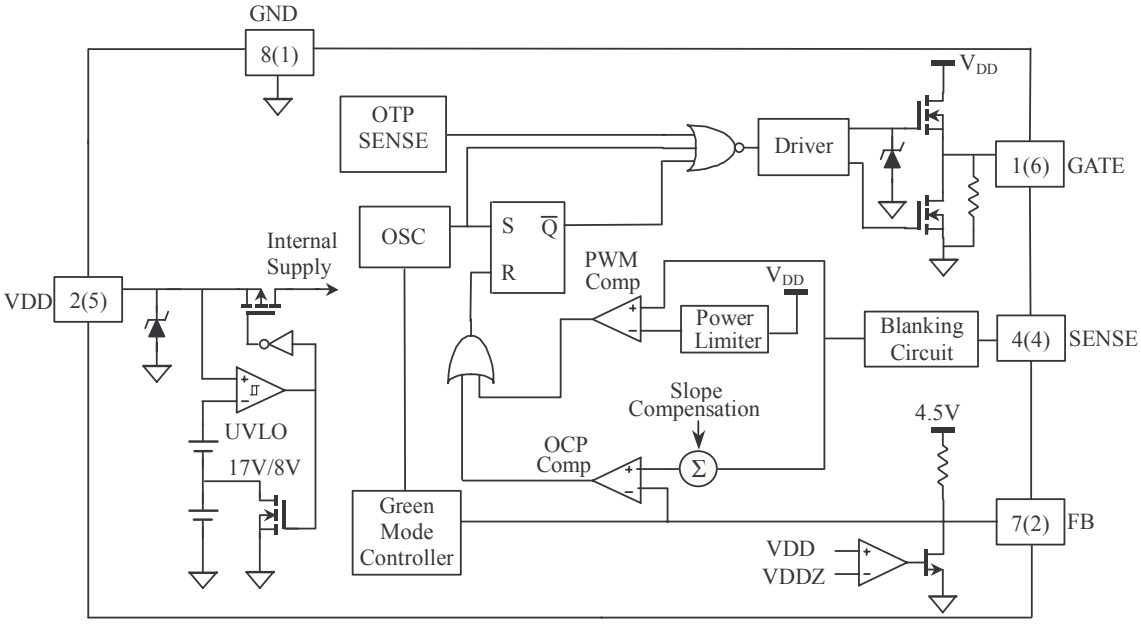
- Constant-voltage (CV) and constant-current control (CC) without secondary feedback
- Green-mode operation with linearly decreasing PWM frequency
- Burst mode
- Low start up current 5uA
- Low operation current 3.6mA
- Leading-edge blanking
- Fixed PWM frequency at 65kHz or 100kHz
- Constant output power limit for universal input
- Built-in synchronized slope compensation
- Current mode operation
- Cycle-by-cycle current limiting
- Under voltage lockout (UVLO)
- Programmable PWM frequency
- VDD over-voltage clamping
- Clamped gate output voltage 16.7V
- Built-in OTP sensor with hysteresis
- Few external components
- SOT-26 and DIP-8 packages available

PIN CONFIGURATION





BLOCK DIAGRAM



Parenthesis number is for SOT-26 pin assignment. Otherwise is for DIP-8 pin assignment

Description

This highly integrated PWM controller provides several features to enhance the performance of low power flyback converters. To minimize standby power consumption, the proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency under light-load and zero-load conditions. This green-mode function enables the power supply to easily meet international power conservation requirements. The supply voltage VDD is also used for feedback compensation, to regulate the output voltage without requiring a conventional TL431 and a photo-coupler. Typical start-up current is only 5uA and operating current is around 3.6mA. To further improve power conservation, a large start-up resistance can be used. Built-in synchronized slope compensation maintains the stability of peak current-mode control. Proprietary internal compensation provides a constant output power limit over a universal line input range (90Vac to 264Vac).

The SG6849 provides many protection functions. Pulse-by-pulse current limiting ensures safe operation even during short-circuits. Also, the internal protection circuit will disable PWM output, if VDD exceeds 22.7V. The gate output is clamped at 16.7V to protect the power MOSFET from damage due to high VDD voltage. The built-in over temperature protection (OTP) function will shutdown the controller at 150°C with a 20°C hysteresis. The SG6849 is designed to provide a low-cost total solution for flyback converters. It is available in 8-pin DIP and 6-pin SOT-26 packages.

Start-up Circuitry

When the power is turned on, the input rectified voltage Vdc charges the hold-up capacitor C1 via a start-up resistor R_{IN}. As the voltage of VDD pin reaches the start threshold voltage $V_{TH(ON)}$, the SG6849 activates and drives the entire power supply to work.

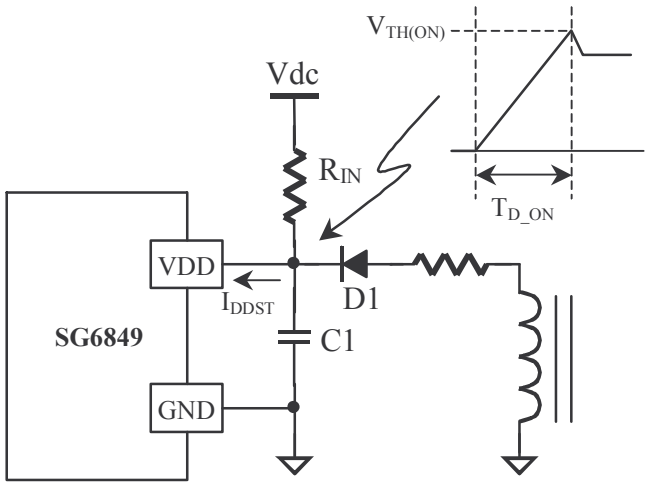


Figure 1. Circuit of providing power to SG6849

The maximum power-on delay time is determined as follows,

$$V_{TH(ON)} = (V_{dc} - I_{DDST} \cdot R_{IN}) \left[1 - e^{-\frac{T_{D\_ON}}{R_{IN} \cdot C1}} \right] \quad (1)$$

where

I_{DDST} is the start-up current of SG6849;

T_{D_ON} is the power-on delay time of the power supply.

Due to the low start-up current, a large R_{IN} such as 1.5Mohm can be used. Also with a hold-up capacitor of 10uF/50V, the power-on delay T_{D_ON} is less than 2.8sec for 90Vac input.

Constant Voltage (CV) Operation

The SG6849 can regulate the output voltage without secondary-side feedback signal. As shown in Figure 2, an internal VDD feedback comparator (VDD comp) is used to modulate the PWM output pulses when FB pin is floating. The primary VDD voltage will be maintained at 22.7V due to internal feedback compensation circuit. The output voltage is proportional to VDD voltage according to the ratio between transformer aux winding and secondary winding. A typical output characteristic using SG6849 is shown in Fig.3. If precise output voltage regulation is required, secondary feedback circuitry should be used.

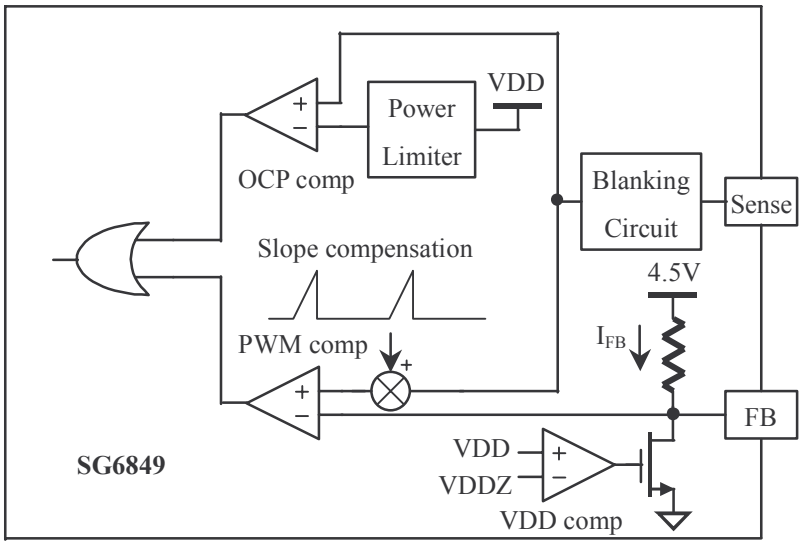


Figure 2. Voltage regulated by VDD feedback

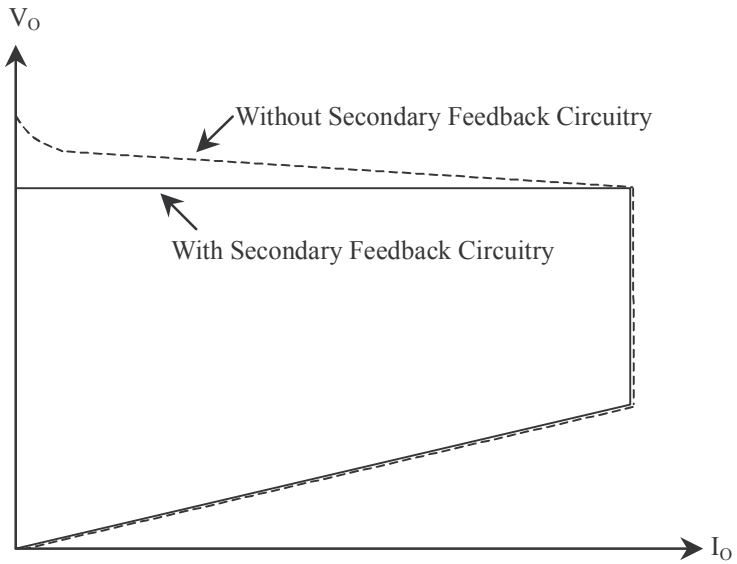


Figure 3. Different output characteristics with or without secondary feedback circuitry

A typical secondary feedback circuitry mainly consisting of a shunt regulator and an opto-coupler is shown in Figure 4. R1 and R2 form a voltage divider for the output voltage regulation. R3 and C1 are adjusted for control-loop compensation. A small-value RC filter (e.g. R_{FB}= 47ohm, C_{FB}= 1nF) placing from FB pin to GND can increase stability. The maximum sourcing current of FB pin is 1.4mA. The phototransistor must be capable of sinking this current to pull FB level down at no load. Thus, the value of biasing resistor Rb is determined as follows,

$$\frac{V_o - V_D - V_Z}{Rb} \cdot K \geq 1.4mA \quad (2)$$

where V_D is the drop voltage of photodiode, about 1.2V;
V_Z is the minimum operating voltage of the shunt regulator, typical value is 2.5V;

K is the current transfer rate (CTR) of the opto-coupler.

For an output voltage Vo=5V, with CTR=100%, the maximum value of Rb is around 910ohm.

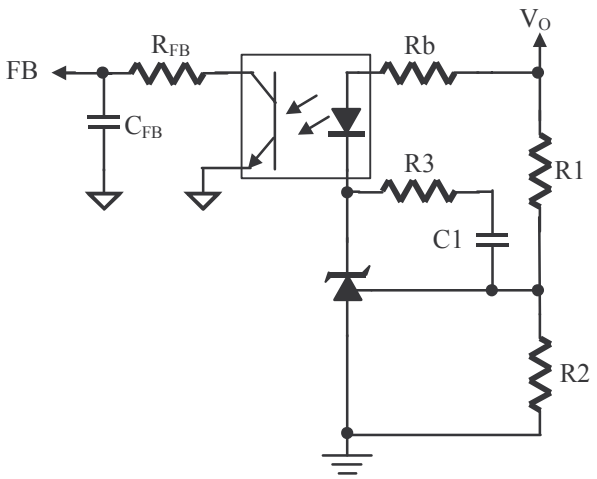


Figure 4. Feedback circuit.

Using secondary feedback circuitry, the primary VDD voltage should be maintained lower than 20V. Otherwise, the internal VDD feedback circuitry may activate with heavy output loading. The transformer aux turn number should be reduced compared with primary feedback application. When the secondary feedback circuitry is open loop, the primary feedback circuitry will act as a back up protection to prevent the VDD exceeding 22.7V.

Constant Current (CC) Operation

For a discontinuous-current mode flyback converter in constant current operation, the output power is proportional to the square of the peak primary current, and also to the output voltage. When the output voltage reduces to half, the primary current will drop to 0.707 times of the original one.

Inside the SG6849, the VDD voltage is used to modulate the level of the SAW current limiting threshold voltage. As shown in Figure 5, the valley voltage of the SAW current limiting curve reduces to 0.707 times of the original one when the VDD voltage reduces to half. With a good coupling of the transformer, the ratio of the VDD voltage to the output voltage is almost constant. A constant current operation is therefore achieved.

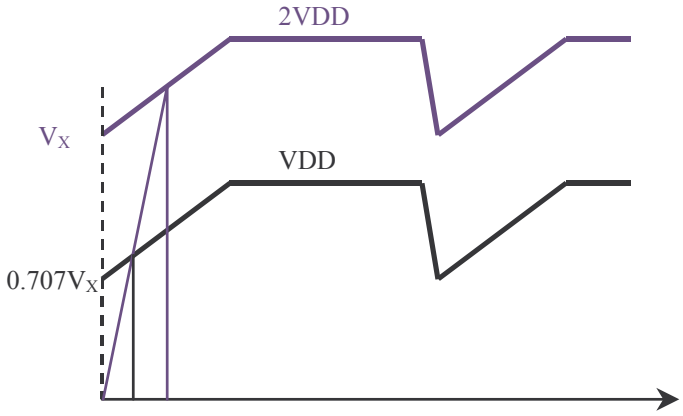


Figure 5. Voltage controlled SAW current limiting curves.

Oscillator & Green Mode Operation

The oscillation frequency is fixed at 65kHz for the SG6849-65, and at 100kHz for the SG6849-100. In normal loading conditions, the PWM frequency is fixed at 65KHz or 100KHz. The patented green-mode function provides off-time modulation to reduce the PWM frequency at light-load conditions. The sink current I_{FB} as shown previously in Figure 2 determines the green mode operation. As the load decreases, I_{FB} will increase. When I_{FB} is larger than 0.8mA, the PWM frequency starts to decrease. The green mode operation can reduce the power consumption of the power supply in light-load conditions. To further reduce the power consumption, the SG6849 enters into burst mode as I_{FB} over 1 mA.

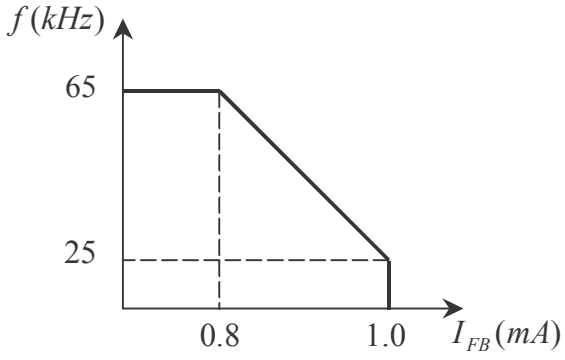


Figure 6. PWM frequency versus FB current.

Built-in Slope Compensation

A flyback converter can be operated in either discontinuous current mode (DCM) or continuous current mode (CCM). There are many advantages to operate in CCM. With the same output power, a converter in CCM exhibits

smaller peak inductor current than the one in DCM. Therefore, a small sized transformer and a low-rating MOSFET can be applied. On the secondary side of the transformer, the rms output current of DCM can be up to twice of CCM. Larger wire gauge and output capacitors with larger ripple current rating are required. DCM operation also results in higher output voltage spike. A large LC filter has also to be added. Therefore, a flyback converter in CCM achieves better performance with lower component cost.

Despite the above advantages of CCM operation, there is one concern – stability issue. In CCM operation, the output power is proportional to the average inductor current, while the peak current is controlled. This causes the well-known sub-harmonic oscillation when the PWM duty cycle exceeds 50%. Adding slope compensation (reducing the current-loop gain) is an effective way to prevent oscillation. SG6849 introduces a synchronized positive-going ramp (V_{SLOPE}) in every switching cycle to stabilize the current loop. The sensed voltage plus this slope compensation signal (V_{SLOPE}) is fed into the non-inverting input of the PWM comparator. The resulted voltage is compared with the FB signal to adjust the PWM duty cycle such that the output voltage is regulated. Therefore, users can use SG6849 to design a cost effective, highly efficient and compact sized flyback power supply operating in CCM without adding any external component.

The positive ramp added is,

$$V_{SLOPE} = V_{SL} \cdot D \quad (3)$$

where
V_{SL} = 0.33V;

D: Duty cycle

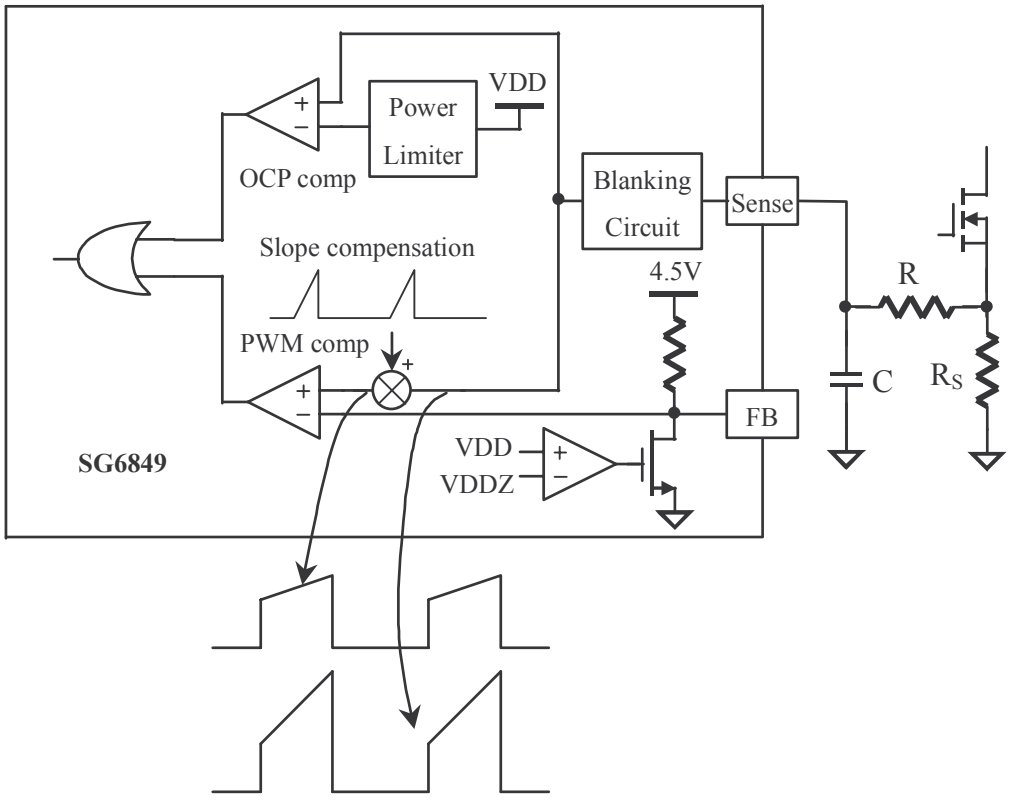


Figure 7. Synchronized slope compensation

Constant Output Power Limit

The maximum output power of a flyback converter can be generally designed by the current-sense resistor R_S. When the load increases, the peak inductor current increases accordingly. When the output current arrives at the

protection value, the OCP comparator dominates the current control loop. OCP happens when the current-sense voltage reaches the threshold value. The output GATE driver is turned off after a small propagation delay td. The delay time results in unequal power-limit level under universal input. In SG6849, a saw-tooth power-limiter is designed to solve the unequal power-limit problem. As shown in Figure 8, the power limiter is designed as a positive ramp signal and is fed to the inverting input of OCP comparator. This results in a lower current limit at high-line input than that at low-line. However, with fixed propagation delay td, the peak primary current would be the same for various line input voltage. Therefore the maximum output power can be almost limited to a constant value within a wide input voltage range without adding any external circuit.

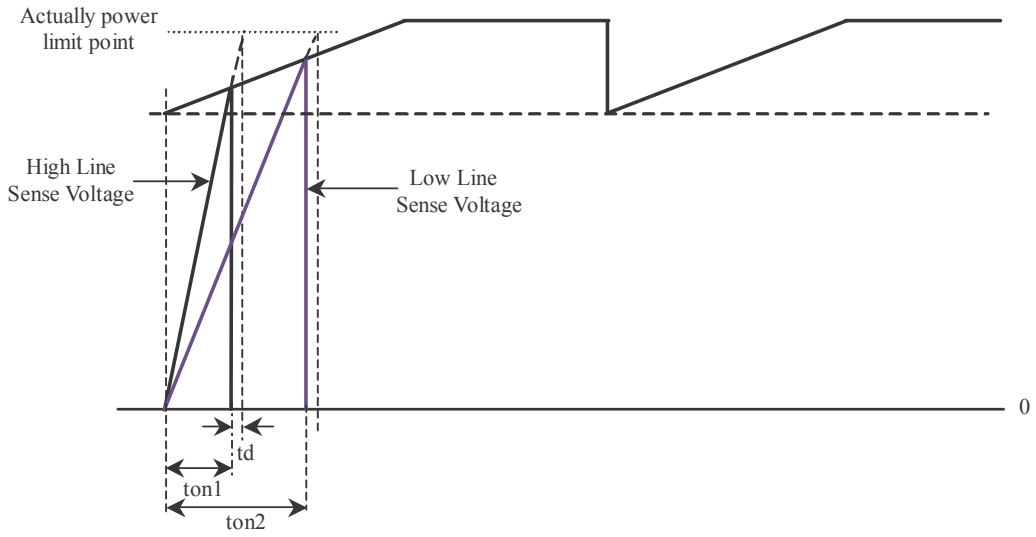


Figure 8. Constant power limit compensation

Over Temperature Protection

The SG6849 has a built-in temperature sensing circuit to shut down PWM output once the junction temperature exceeds 150°C. While PWM output is shut down, the VDD voltage will gradually drop to the UVLO voltage (around 8V). Then VDD will be charged up to the start-up threshold voltage of 17V through the start-up resistor until PWM output is restarted. This hiccup mode protection will happen repeatedly as long as the temperature remains above 130°C. The temperature hysteresis window for the OTP circuit is 20°C.

Leading Edge Blanking

A voltage signal proportional to the MOSFET current develops on the current-sense resistor R_S. Each time the MOSFET turned on, a spike, which is induced by the diode reverse recovery and by the output capacitances of the MOSFET and diode, inevitably appears on the sensed signal. Inside SG6849, a leading edge blanking time about 310nsec is introduced to avoid premature termination of MOSFET by the spike. Therefore, only a small-value RC filter (e.g. 100ohm + 470pF) is required between the SENSE pin and R_S. Still, a non-inductive resistor for the R_S is recommended.

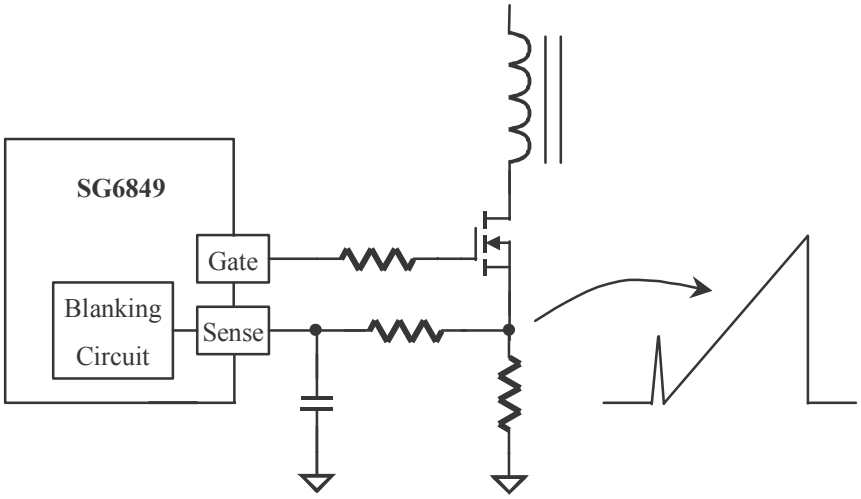


Figure 9. Turn on spike

Gate Drive

SG6849's output stage is a fast totem pole driver that can directly drive MOSFET gate. It is also equipped with a voltage clamping Zener diode to protect MOSFET from damage caused by undesirable over drive voltage. The output voltage is clamped at 16.7V. An internal pull down resistor is used to avoid floating state of gate before startup. A gate drive resistor in the range of 47 to 100 ohm is recommended. This resistor limits the peak gate drive current and provides damping to prevent oscillations at the MOSFET gate terminal.

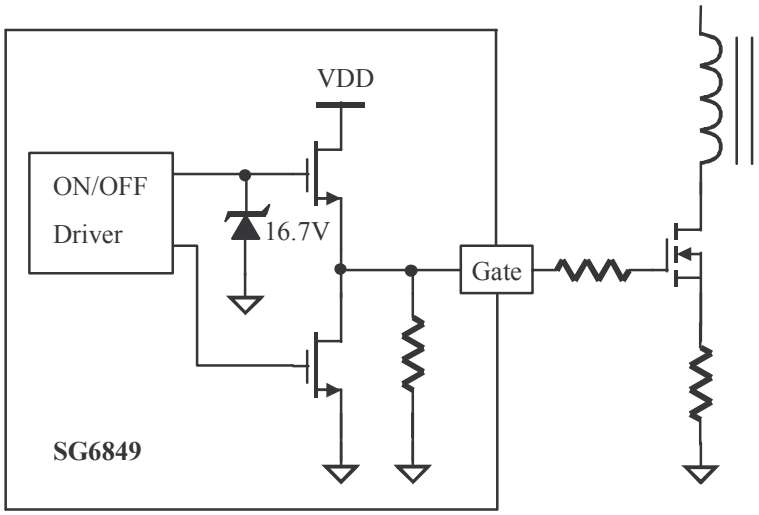


Figure 10. Gate drive

Lab Note

Before rework or solder/desolder on the power supply, it is suggested to **discharge primary capacitors by external bleeding resistor**. Otherwise the PWM IC may be destroyed by external high voltage during solder/desolder.

This device is sensitive to ESD discharge. To improve production yield, production line should be ESD protected in according to ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1.

Printed Circuit Board Layout

High frequency switching current/voltage make printed circuit board layout a very important design issue. Good PCB layout minimizes excessive EMI and helps the power supply survive during surge/ESD tests. Here, we give some common guidelines:

(A) In order to get better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitor C1 first, and then to the switching circuits.

(B) The high frequency current loop is in **C1 – Transformer – MOSFET – R_S – C1**. The area enclosed by this current loop should be as small as possible. Keep the traces (especially 4→1) short, direct, and wide. High voltage traces related the drain of MOSFET and RCD snubber should be kept far way from control circuits to prevent unnecessary interference. If heatsink is used for MOSFET, it's better to connect this heatsink to ground.

(C) As indicated by 3, the ground of control circuits should be connected first and then to other circuitry.

(D) As indicated by 2, the area enclosed by **transformer aux winding, D1, and C2** should also be kept small. Place C2 close to SG6849 for good decoupling.

(E) Two suggestions with different pro and cons for ground connections are recommended.

I. GND3→2→4→1: This could avoid common impedance interference for sense signal.

II. GND3→2→1→4: This could be better for ESD test where the earth ground is not available on the power supply. Regarding the ESD discharge path, the charges go from secondary through the transformer stray capacitance to GND2 first. And then the charges go from GND2 to GND1 and go back to mains. It should be noted that control circuits should not be placed on the discharge path. Point discharge for common choke can decrease high frequency impedance and help to increase ESD immunity.

(F) Should a Y-cap between primary and secondary is required, it is suggested to connect this Y-cap to the **positive terminal of C1 (Vdc)**. If this Y-cap is connected to primary GND, it should be connected to the **negative terminal of C1 (GND1)** directly. Point discharge of this Y-cap also helps for ESD. However, the creepage between these two pointed ends should be at least 5mm according to safety requirements.

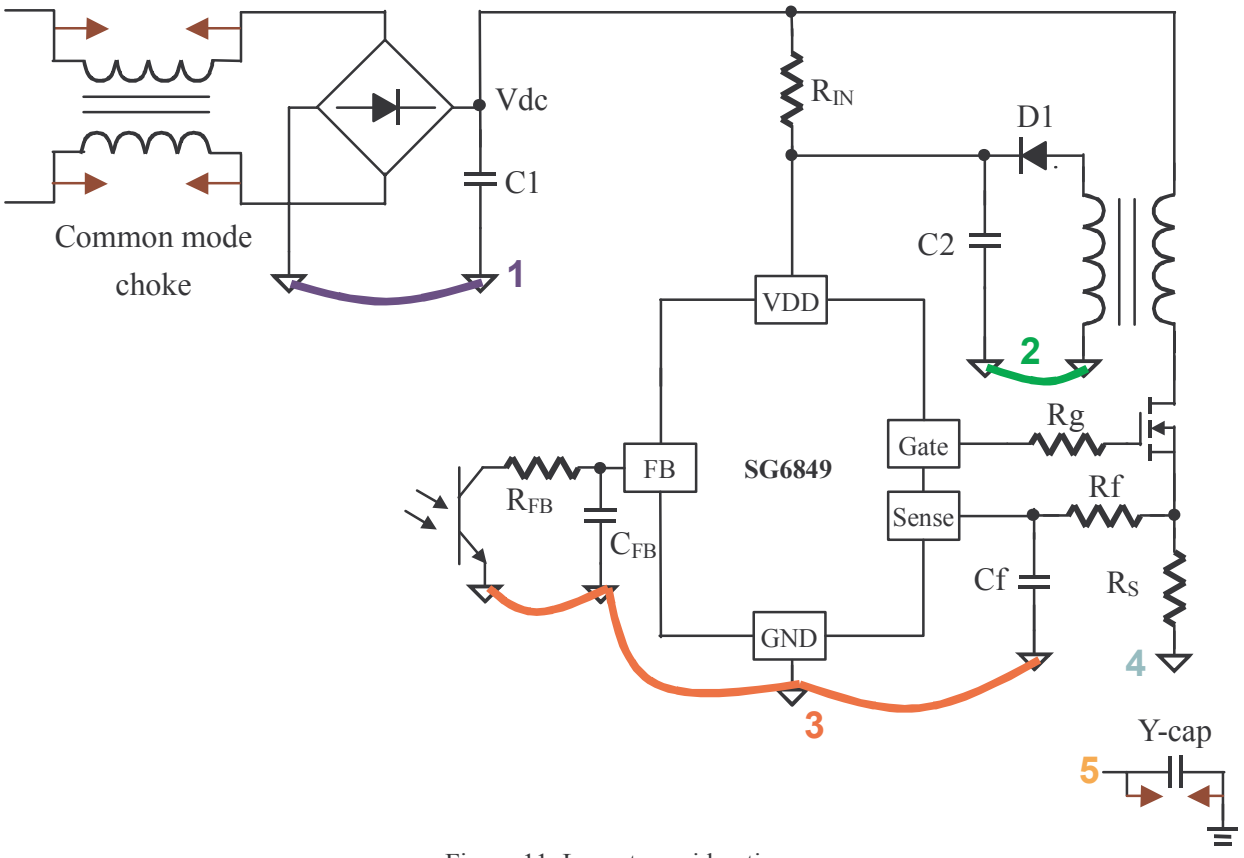


Figure 11. Layout considerations