Fixed Frequency Resonant Converter for High Voltage High Density Applications

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Abstract - A series resonant converter with nearly ZVS and fixed frequency phase-shift control is described. The circuit's ability to utilize component parasitics is used in a high voltage high density DC/DC converter. The topology has dual slope output characteristics with current limiting property. A computer simulation and prototype measurements are presented.

Introduction

This paper describes a nearly zero voltage switching (ZVS) operation of a clamped-mode series resonant converter with clamped capacitor voltage [1]. The topology has dual-slope output characteristics with a current-limiting property. The converter operating either above or below resonance has an ability to utilize integral MOSFET diodes at high frequency despite their long recovery time.

Reference [1] dealt primarily with static performance characteristics and component stress data. Power components' parasitics, which strongly influence converter performance at high frequency weren't considered. References [2] and [3] showed that analysis of this topology is very complex and identified nine topological modes corresponding to different conduction patterns of the clamping diodes. State-space representation and boundary conditions for each mode were also given in [3].

This paper shows that zero voltage turn-on of all four switches is achievable if the circuit is operated above resonance and a fixed delay is introduced between the gate drive pulses of switching transistors in both legs of the bridge. It is also shown that the circuit's current limiting output characteristics and its ability to utilize component parasitics eliminate the need for snubbers or other commutation-aid networks.

A special purpose computer program written to analyze the circuit is also described in the paper. Experimental results based on a 3.9 kV, 300W DC/DC converter used in the Microwave Power Module (MPM) demonstrate performance of this topology in a high voltage, high density application.

Circuit Operation

A schematic diagram of the clamped-mode series resonant converter with clamped capacitor voltage is shown in Figure 1. This topology was created from a conventional clamped-mode series resonant converter [4] by adding clamping diodes across the resonant capacitor and by dividing the resonant inductor and transformer primary winding into two equal sections.

The gate drive waveforms and the resultant tank voltage are also shown in FIgure 1. Q1 and Q2 are alternately switched with a 50% duty cycle; Q3 and Q4 are similarly switched. Control of the circuit is achieved by delaying the turn-on of the transistor Q4 with respect to Q1 by an angle PHI and delaying the turn-on of the transistor Q3 with respect to Q2 by the same angle. The tank voltage duty cycle increases with decreasing PHI, thus, modulation of the phase angle PHI results in PWM control of the output.

Output characteristics of the converter are shown in Figure 2. Expressions for normalized output voltage and current are listed in Table 1. Two different slopes of the maximum power curve (PHI = 1 Deg) correspond to two different modes of operation. For the values of normalized output current $I_o^* < 0.6$ the converter behaves as a voltage source; for high output currents the diodes D1-D4 clamp the tank capacitor to the input DC line, and the circuit operates as a current source.

Table 1
Normalized and Base Values

I_o	Output Current
V_o	Output Voltage
V_{IN}	Input Voltage
N=2n1/n2	Transformer Turns Ratio
$I_o^* = I_o/I_{base}$	Normalized Output Current
$I_{base} = N V_{in} /(\sqrt{(L1+L2)/C})$	Base Current
$V_o^* = V_o/V_{base}$	Normalized Output Voltage
$V_{base} = V_{in}/N$	Base Voltage

As described in [1], this topology can efficiently operate within a range of switching frequency $0.8\ f_o < f_s, < 1.5\ f_o$, where f_o is the resonant tank frequency, $f_o = 1/(2\pi\sqrt{((L1 + L2)C)})$. However, zero voltage turn-on of all four transistors is achieved only if the circuit operates either at ($f_s = f_o$), or above ($f_s > f_o$) resonance. Another condition is that at the rated load, the quality factor of the resonant tank ($Q = (\sqrt{((L1 + L2)/C)})/N^2 R_L$), shall exceed 0.3.

Also, a fixed time delay shall be introduced between the gate drive pulses of Q1, Q2, and Q3, Q4. During this dead time, the current flows through the anti-parallel diode and discharges the transistor's equivalent output capacitance. Because conduction of any transistor is preceded by conduction of its antiparallel diode, the diodes are commutated naturally, and MOSFETs' body diodes can be used despite their long recovery time.

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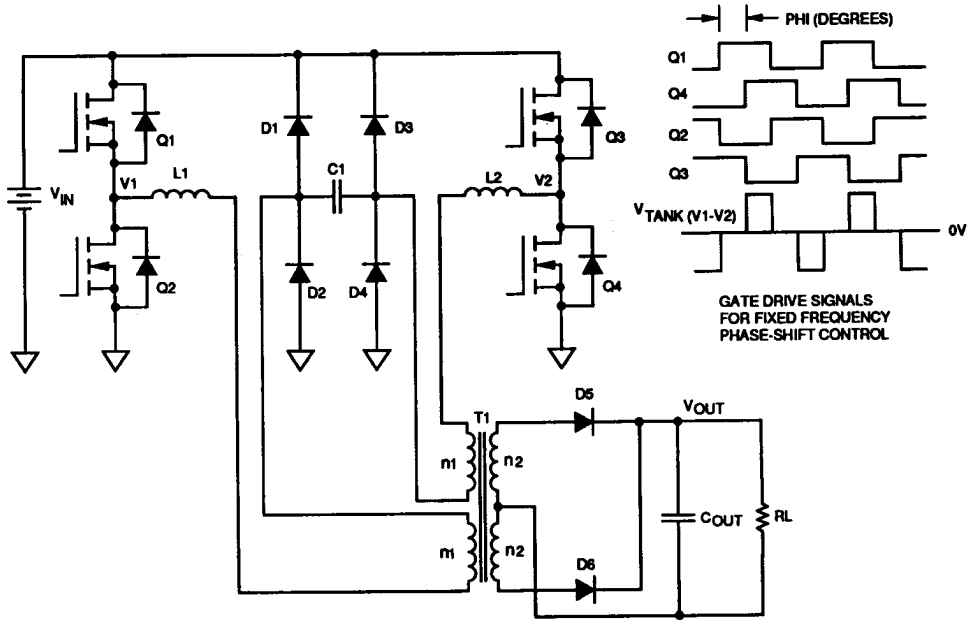


Figure 1 - Series Resonant Converter With Clamped Capacitor Voltage

Waveforms for a nearly-ZVS operation with 92% efficiency are shown in Figure 3. The conditions are as follows: $f_s = f_o = 300$ kHz, Q = 0.47, $P_{out} = 1000W$ (rated output), $V_{in} = 250$ VDC, $V_{out} = 50V$.

Additional parasitic components affecting operation of the converter include leakage inductance and equivalent capacitance of the transformer. It is well established that the leakage inductance of the transformer can be absorbed into the resonant inductor of a series resonant converter.

While the influence of the equivalent capacitance of a low voltage transformer is minimal, this is not the case with a high voltage transformer [5]. This capacitance (primarily layer-to-layer of the high voltage winding) slows down the rate of change of the secondary voltage. During the time interval when this voltage is switched from $V_{positive}$ to $V_{negative}$, the secondary current is diverted from the output to the transformer capacitance, thereby increasing the primary currents and the reactive power consumed by the inverter.

Transformer capacitance reflected to the primary side of the transformer changes the phase angle between the voltages and currents of transistors Q3 and Q4. As a result of this, antiparallel diodes CR3 and CR4 start conducting after their respective transistors, and currents in both diodes are no longer naturally commutated.

If the value of the quality factor Q is increased above 1, the circulating current will increase and the natural commutation of the diodes will be restored. This represents a design trade-off between the value of the circulating current and commutation losses in the antiparallel diode. It was also found that reducing magnetizing inductance of the transformer helps to improve commutation conditions.

Figure 4 shows transistor voltages and currents for a high voltage converter operating in this mode. The output voltage is 3.9 kV, the output power is 330W, the efficiency is 88.3% and the value of the quality factor Q is 1.4. Although the turn-on switching losses are relatively higher than those for the operation shown in Figure 3, the simulated converter efficiency is 89% @ 250 kHz.

One positive effect of a high transformer capacitance is the elimination of voltage overshoots and ringing across the secondary winding. This significantly reduces stress for the high voltage rectifier diodes.

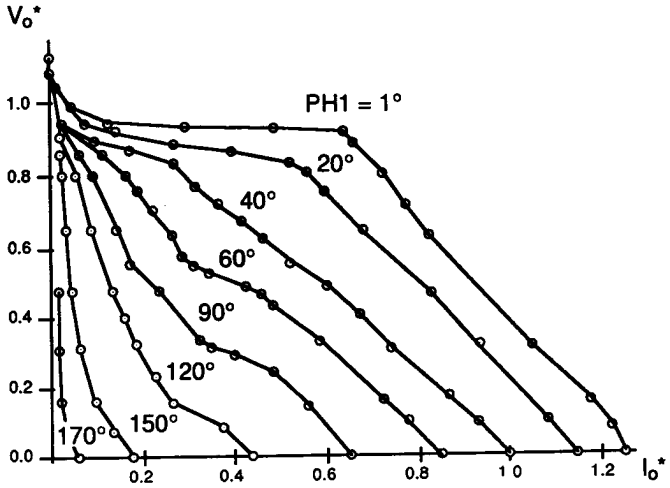


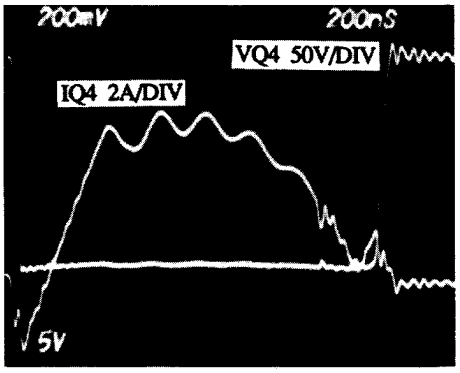
Figure 2 - Output Characteristics $f_s = f_o$

Experimental Results

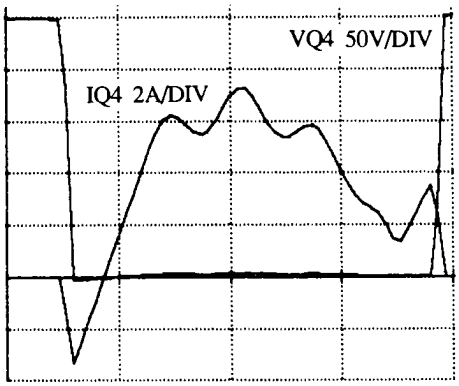
A 3.9 kV, 300W DC/DC converter was used in the Microwave Power Module (MPM). The MPM is a self-contained unit comprising a vacuum power booster (a "micro" TWT), a Monolithic Microwave Integrated Circuit Amplifier (MMIC), and a power conditioner. A block diagram and a photograph of the prototype module are shown in Figures 5 and 6, respectively. The volume of the prototype module is 40 cubic inches.

A schematic diagram of the converter's power stage is shown in Figure 7. It features a high voltage transformer with a four-section secondary winding, series-connected rectifier diodes, and a two-stage output filter. No snubbers or commutation-aid networks were used.

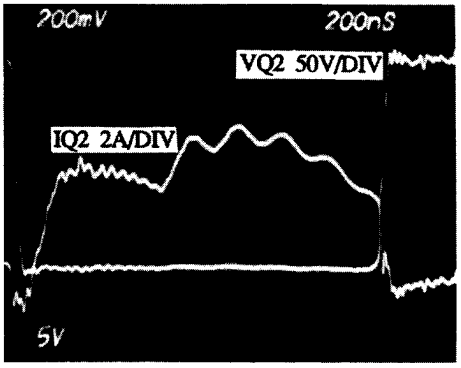
The 262 kHz operating frequency of the converter is limited primarily by the reverse recovery time t_{rr} of the high voltage rectifier diodes ($t_{rr} = 35$ ns for 1N6622 type diodes used in the prototype). Both steady-state and transient output voltage waveforms are shown in Figures 8 and 9. Cathode voltage ripple of less than 2V peak-to-peak (0.05% of 3.9 kV) is combined with a fast voltage run-up time. Dynamic behavior of the converter operating with such a highly non-linear load as the "micro" TWT is well-controlled and stable.



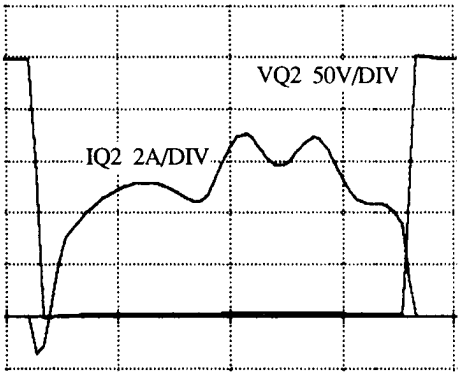
Time Scale 200 nS/div
Experimental IQ4, VQ4



Time Scale 500 uS/div
Simulated IQ4, VQ4



Time Scale 200 nS/div
Experimental IQ2, VQ2



Time Scale 500 uS/div
Simulated IQ2, VQ2

Figure 3 - Transistor Voltage and Current Waveforms at 300 kHz

Arcing of the tube (equivalent to applying a random short circuit to the output) didn't cause any damage to the converter. It should be noted that the control circuit included only a slow average current limit; dual-slope volt-ampere characteristics of the converter provided an adequate short term overload protection.

Voltage and current for one of the transformer secondary windings are shown in Figure 10 for two values of the input line voltage. Notice the low dV/dt that results from charging of the equivalent capacitance of the transformer.

Measured distribution of power losses is given in Table 2. The experimental data compares very well with the 89% efficiency of the DC/DC converter predicted by the computer model.

Table 2
Distribution of Power Losses at 270 Vin

1.	Collector Power	- 265.4W
2.	Helix Power	- 11.7 W
3.	Filament Power	- 3.4W
4.	MMIC Power	- 21.5W
5.	Bias Power Supply Power Losses	- 15W
6.	High Voltage Converter Control Circuit Power	- 6.2W
7.	High Voltage Converter Power Losses	- 31.5W
8.	Input Power	- 354.7W
	Bias Power Efficiency - 66%	
	High Voltage Converter Efficiency - 88%	

Computer Model and Circuit Analysis

The power circuit is analyzed by determining the differential equations for the state variables for the reactive elements and then iterating these variables with the use of a digital computer. Expressions for the state variables are determined by analysis of the equivalent circuit model shown in Figure 11. The following definitions apply:

dT	=	Incremental Time Step
VD	=	Diode Forward Voltage Drop
RD	=	Diode On Resistance
RDQ	=	MOSFET Intrinsic Diode On Resistance
RQ	=	MOSFET On Resistance

All other circuit parameters are defined by Figure 11.

Circuit equations are obtained from mesh and nodal analysis. All element voltages and currents must be determined. The technique for developing the simultaneous differential equations is to obtain expressions for the voltage across each inductor and the current thru each capacitor. This yielding the popular state-space representation of the higher order system, all equations are listed below.

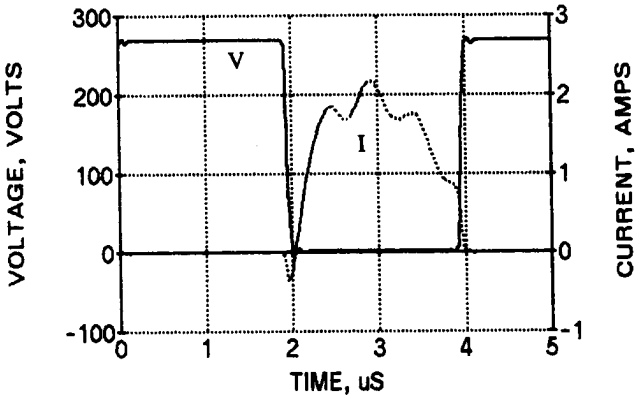
$$ELI = V1 - V3 - I1 * RT1 - VP \quad (1)$$
$$dILI = (EL1/L1) * dT \quad (2)$$
$$EL2 = V4 - V2 - I2 * RT1 - VP \quad (3)$$
$$dIL2 = (EL2/L2) * dT \quad (4)$$
$$I2 = IL2 + EL2/RL2 \quad (5)$$
$$I1 = IL1 + EL1/RL1 \quad (6)$$
$$dILM = (VP/LM) * dt \quad (7)$$
$$ID1 = (V3 - E1 - VD)/RD1 \quad (8)$$
$$ID2 = - (V3 + VD)/RD2 \quad (9)$$
$$ID3 = (V4 - E1 - VD)/RD3 \quad (10)$$
$$ID4 = - (V4 + VD)/RD4 \quad (11)$$

Definition: IA1 = I1 - ID1 + ID2 (12)
Definition: IB1 = ID3 + I2 - ID4 (13)
ICD1 = (IA1 * (.5 + CD/C1) - IB1/2)/(2* (1 + CD/C1)) (14)
See Appendix 1 for Derivation of Equation 14 (15)
dV3 = (ICD1/CD) * dT
dVC1 = ((IA1 - 2 * ICD1)/C1) * dT (16)
IS1 = (E1 - V1)/RQ (17)
IDQ1 = (V1 - E1 - VD)/RDQ (18)
IS2 = V1/RQ (19)
IDQ2 = - (V1 + VD)/RDQ (20)
ICQ1 = 0.5 * (IS2 - IS1 + IDQ1 - IDQ2 + I1) (21)
ICQ2 = ICQ1 (22)
dV1 = (ICQ1/CQ) * dT (23)
IS3 = (E1 - V2)/RQ3 (24)
IDQ3 = (V2 - E1 - VD)/RDQ (25)
IS4 = V2/RQ (26)
IDQ4 = - (V2 + VD)/RDQ (27)
ICQ3 = 0.5 * (IS4 - IS3 + IDQ3 - IDQ4 - I2) (28)
ICQ4 = ICQ3 (29)
dV2 = (ICQ3/CQ) * dT (30)

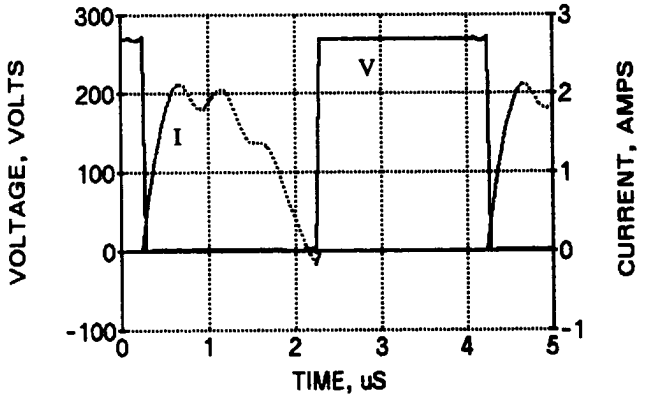
Circuit Connected to Transformer Secondary

IS = (I1 + I2 -2 * ILM) * N (31)
ICS = IS - VSC/RC (For IVR = 0) (32)
dVCS = (ICS/CS) * dT (33)
IVR = IS - VCS/RC (For ICS = 0) (34)
IC2 = IVR - VC2/RL (35)
dVC2 = (IC2/C2) * dT (36)

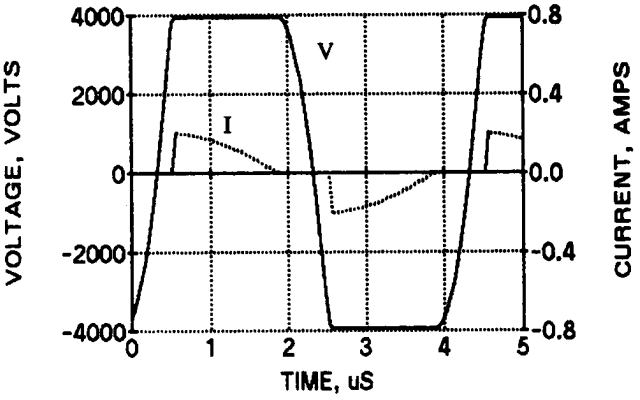
After each iteration of the state variables, capacitor voltages and inductor currents are updated. This is done by adding the incremental change to the previous value. All required node voltages and branch currents are then calculated and the next iteration begins. This method of numerical analysis is known as the forward Euler's Method, wherein the derivative of the function at step J is used to determine the value of the function at step J + 1. This simple approach was found to be less susceptible to numerical instability problems than implicit (matrix inversion) or multi-step integration techniques.



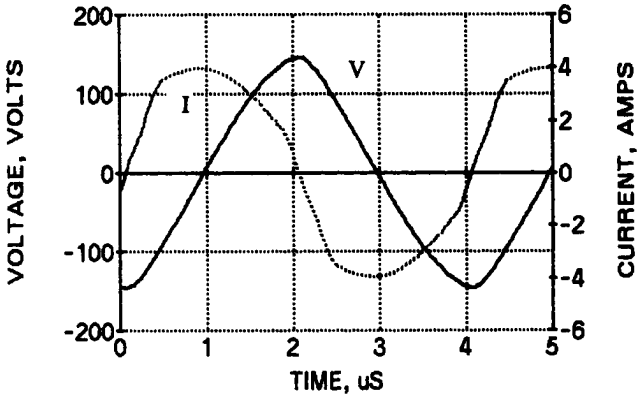
a) Transistor Q2 Voltage and Current



b) Transistor Q4 Voltage and Current



c) Secondary Winding Voltage and Current



d) Resonant Tank Capacitor Voltage and Current

Figure 4 - High Voltage Converter Switching Waveforms

The number of iterations per inverter period for this analysis is 25,000. The analysis is quite accurate if the time step, dT, is small compared to the shortest circuit time constant. The model includes a time delay between the turn-off of one transistor and turn-on of another in the same leg of the bridge.

Circuit diodes are modeled with IF statements. If the voltage across the diode exceeds the specified junction voltage, then the diode on resistance is set to a predetermined low value.

Because of the repetitive nature of this numerical technique, it is well suited for computations by a digital computer. A 486/33 PC was used to compute data for this paper.

High gain closed loop operation forces the output to settle in less than 10 cycles of the inverter frequency.

An effective way to check simulation accuracy is to compare the sum of the element dissipations with input power. These two values should correlate to within a few percent.

While iterating the equations, the program can be set up to track and compute various parameters so that peak, average, and RMS values of current, voltage, and power for any element can be easily computed.

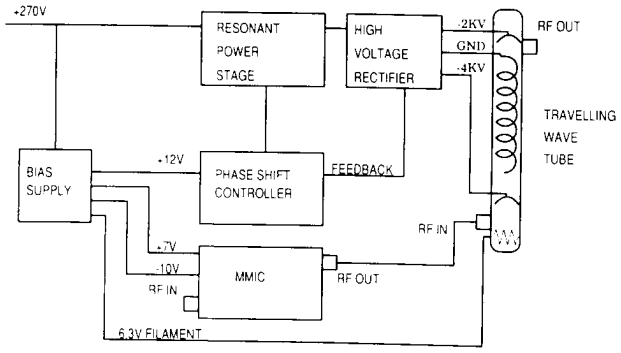


Figure 5 - Prototype Block Diagram

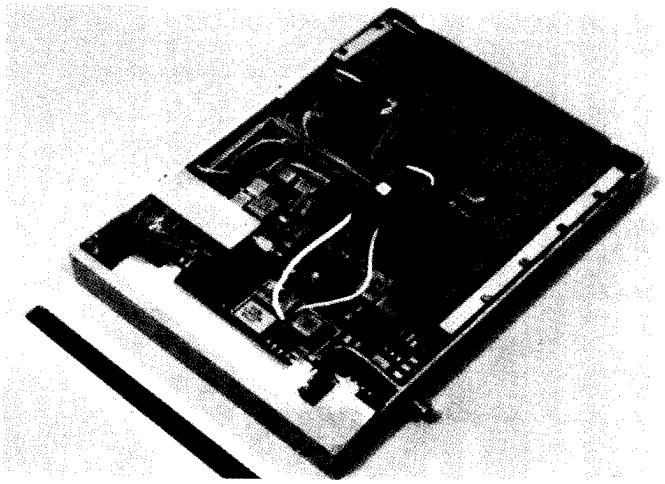


Figure 6 - Prototype MPM

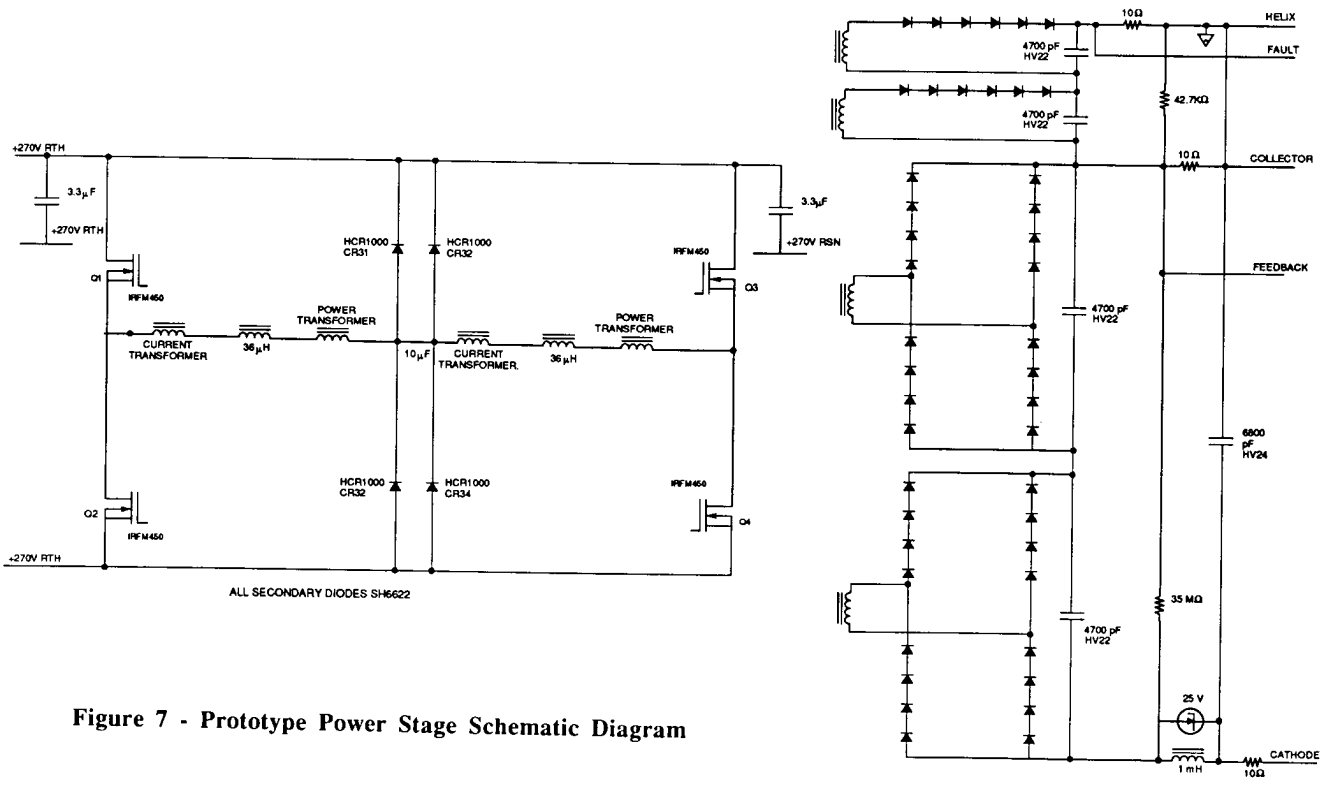


Figure 7 - Prototype Power Stage Schematic Diagram

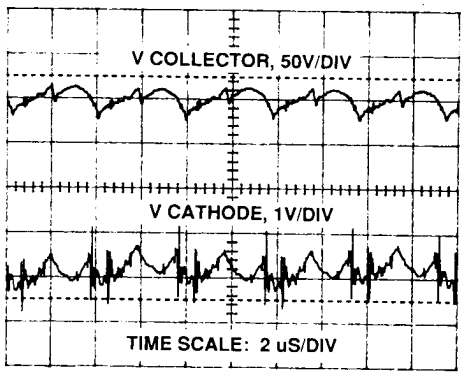


Figure 8 - High Voltage Power Supply Output Ripple

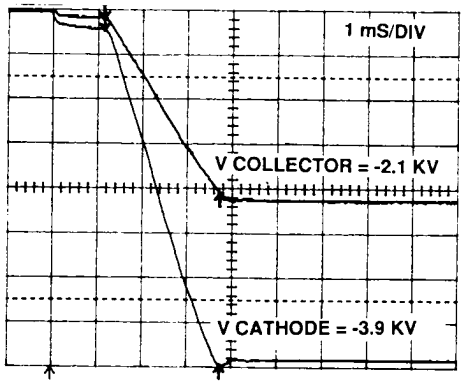


Figure 9 - High Voltage Power Supply Turn-On Transient Waveforms

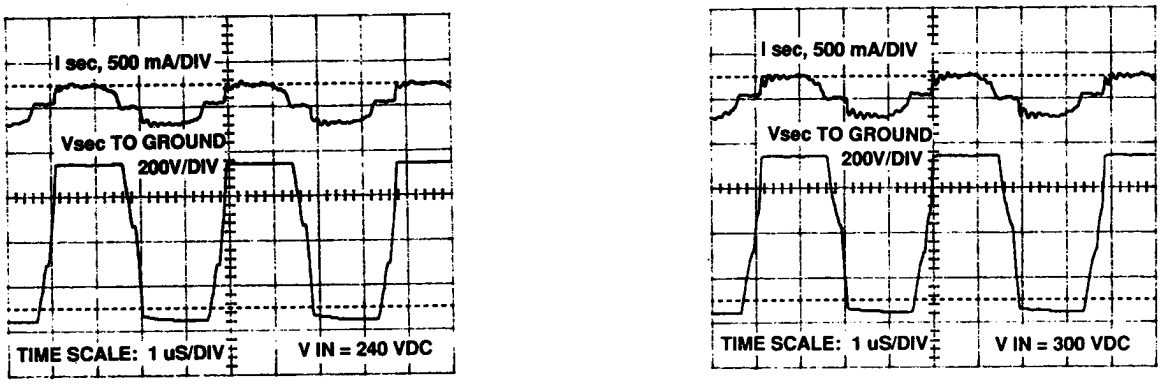


Figure 10 - High Voltage Transformer Secondary Voltage and Current Switching Frequency f_s = 262 kHz

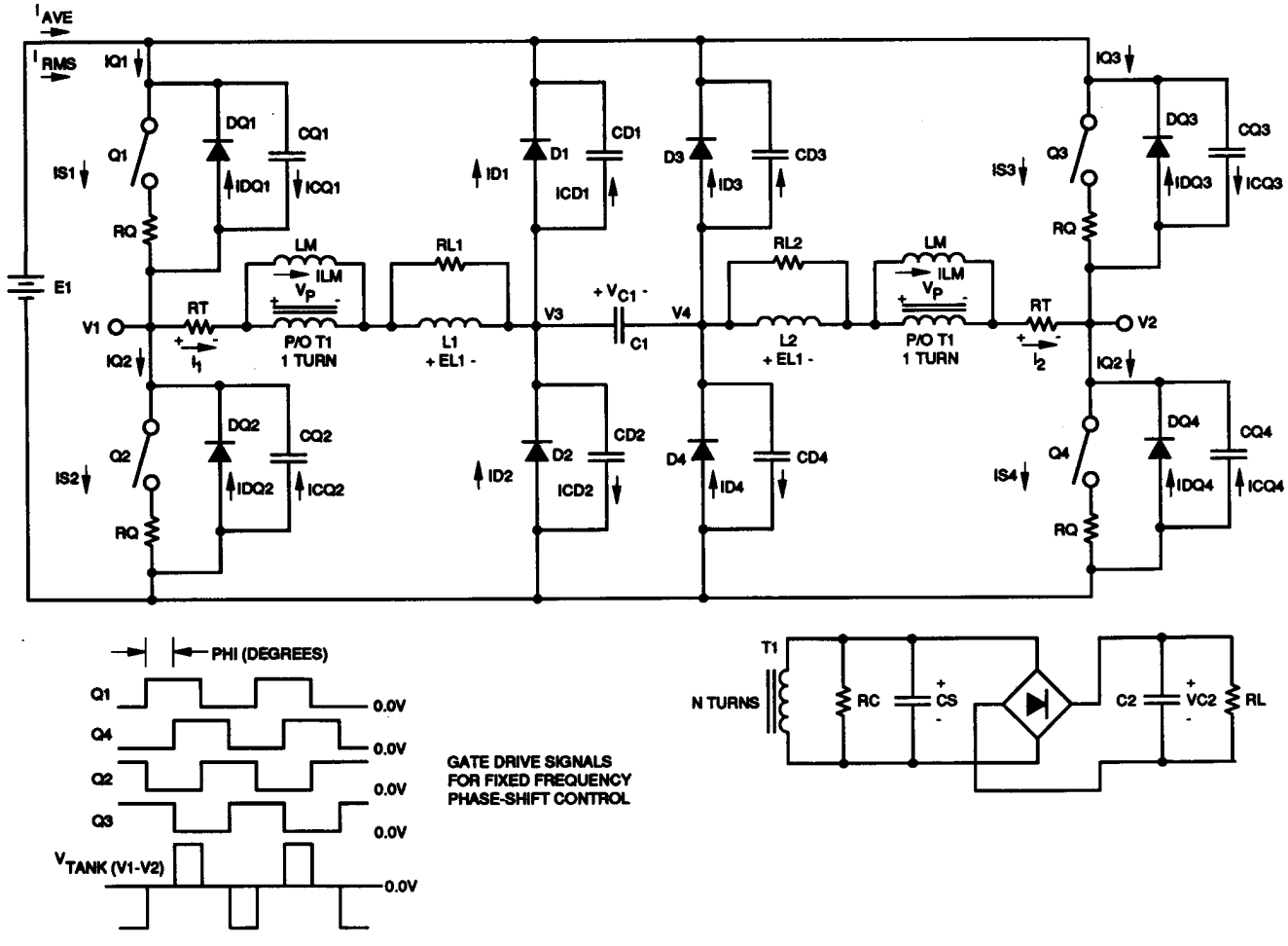


Figure 11 - Equivalent Circuit Model

Conclusions

A clamped-mode series resonant converter with clamped capacitor voltage for a high voltage application has been simulated and tested.

A near-zero voltage turn-on operation of all four transistors is described.

A simple and accurate computer model of the converter proved to run faster and provide more insight into the circuit's operation than packaged circuit analysis programs.

Future research will concentrate on improving the transistor commutation and analytic investigation of the dynamic properties of the converter.

Appendix - Derivation of Equation 14
(Formulation for Circuits Containing Capacitor Loops)

Equation 14 determines the current in the parasitic capacitance CD1.

This current is then used to calculate the incremental voltage changes at V3, across VC1 and V4.

This Appendix shows the derivation of Equation (14). CD1 thru CD4 form a capacitor bridge as show below:

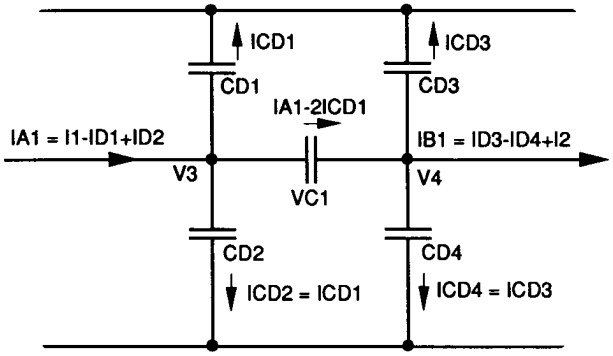


Figure A1 - Capacitor Loop

Figure A1 - Capacitor Loop

The instantaneous current, ICD1, is derived from the fact that the incremental voltage change at V4 is equal to the incremental voltage change at V3 minus the incremental voltage change across VC1:

(A1) $dV4 = dV3 - dVC1$

(A2) $dV4 = ((IA1 - 2 * ICD1 - IB1)/2* CD) * dt$

(A3) $dV3 = (ICD1/CD) * dt$

(A4) $dVC1 = ((IA1 - 2*ICD1)/C1) * dt$

Substituting equations A2, A3, and A4 into equation A1, dividing by dt and solving for ICD1 yields:

(A5) $ICD1 = (IA1 * (0.5 + CD/C1) - IB1 * 0.5)/(2(1+ CD/C1))$

which is identical to equation (14) in the Computer Model and Circuit Analysis Section.

References

[1] B. S. Jacobson, R. A. DiPerna, "Series Resonant Converter with Clamped Tank Capacitor Voltage", IEEE APEC, PP. 137-146, 1990.

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