High Power Factor Preregulator Using the SEPIC Converter

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Summary:

The SEPIC converter combines the best features of the boost and flyback topologies, making it especially advantageous in high power factor preregulator applications.

In addition, ripple current can be steered away from the input, dramatically reducing input noise filtering requirements.

This paper discusses the design of the SEPIC converter, design of the coupled inductor to achieve ripple current steering, and Zero Voltage Transition circuitry to minimize switching losses.

The SEPIC Preregulator:

A Single-Ended Primary Inductance Converter (SEPIC) is shown in Fig. 1, configured as a non-isolated high power factor preregulator.

The SEPIC converter uses two inductances. The input inductor *L1* together with the switch resembles a simple boost topology, whereas the shunt inductor *L2* location is similar to a buck-boost, or flyback topology.

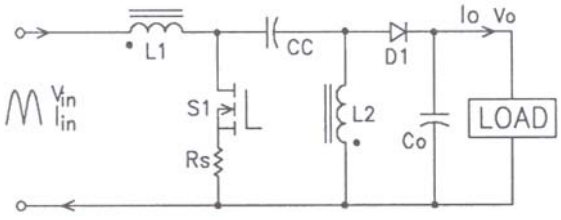


Fig 1. - SEPIC Power Circuit

In a conventional SEPIC converter, inductors *L1* and *L2* are independent. This paper will show that improved dynamic performance is obtained by coupling these inductors. More importantly, if the coupled inductor is designed so that its leakage inductance (*LL*) is located in series with *L1* in the input, the high frequency ripple current is steered *away* from *L1* and into *L2*, thus greatly easing input noise filtering requirements.

The main advantages and disadvantages of the SEPIC high power factor preregulator are:

PROs:

- Single switch
- Continuous input current (like Boost)
- Any output voltage (like Flyback).
- Ripple current can be steered away from input, reducing the need for input noise filtering.
- Inrush/overload current limiting capability.
- Switch location facilitates MOSFET gate drive.
- Outer loop control scheme identical to Boost—UC3854 can be used in same manner.
- Possibility of isolation/step down using secondary inductor winding, if a way can be found to avoid leakage inductance problems.

CONs:

- Higher switch/diode peak voltages and currents compared to boost topology.
- Bulk capacitor size/cost will be greater if operated at lower voltage than boost.

SEPIC Circuit Operation

In most high power factor preregulator applications, the switching frequency is very much greater than the 50-60Hz line frequency. Except for the bulk filter capacitor, the inductor and capacitor values in the power circuit are based upon switching frequency (HF) considerations, Their impedances are negligible at line frequency (LF). Thus, instantaneous values along the rectified line waveform are regarded as "dc" values when analyzing HF operation.

High Power Factor SEPIC Preregulator

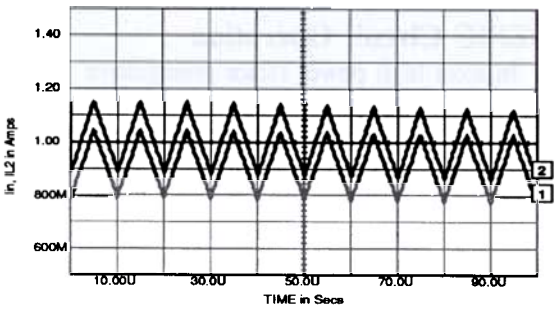
Coupling capacitor *Cc* is an important element in the SEPIC topology. Its voltage offset allows the SEPIC's boost-like inductor input to coexist with an output voltage which may be less than V_{IN}.

The steady-state average voltage across *Cc* always equals V_{IN}. To demonstrate this, look at the circuit mesh including V_{IN}, *Cc*, and inductances *L1* and *L2*. Since the steady-state average voltage across all inductor windings must equal zero, $V_{CC(avg)}$ must equal V_{IN}. In a practical SEPIC pre-regulator, *Cc* is small (≈0.5µF for 200W), so that $V_{CC(avg)}$ tracks the rectified line voltage. A small triangular HF ripple voltage also appears across *Cc*.

Fig. 2 shows the inductor currents in a conventional 200 Watt SEPIC converter operating at 100kHz with V_{IN}=220V, $I_{IN(avg)}$=0.9A, and V_O=200V. Inductors *L1* and *L2* are equal (4mH) and independent (not coupled). Input ripple is $250mA_{p-p}$.

Circuit explanation: Refer to the waveforms of Fig. 2 and the circuit of Fig. 1 with the inductors independent. When the switch is ON, the instantaneous rectified line voltage, V_{IN}, is applied to *L1*, with its dotted end positive. At the same time, V_{CC} = V_{IN} is applied to *L2*, with its dotted end also positive. Since *L1* = *L2*, I_{L1} and I_{L2} ramp upward at the same rate: V_{IN}/L. The switch current is the sum of I_{L1} (input current) and I_{L2}. The rectifier reverse voltage equals V_{IN} plus V_O.

When the switch is OFF, the currents flowing through *L1* and *L2* force their voltages to reverse until the output rectifier conducts current (I_{L1}+I_{L2}), previously conducted by the switch. *L2* is clamped directly across V_O with its dotted end negative. V_{IN} and V_{CC} cancel, so that V_O also appears across *L1*, with its dotted end also negative. I_{L1} and I_{L2} both ramp downward at the same rate: V_O/L.



- SEPIC Waveforms, Independent Inductors [1]-I_{IN} , [2]-I_{L2}

While the switch is OFF, I_{IN} charges *Cc*. While the switch is ON, *Cc* is discharged by I_{L2}. Although the steady-state average V_{CC} equals V_{IN}, the nearly rectangular current waveform through *Cc* results in a triangular ripple voltage across *Cc*.

By inspection, note that although the switch and rectifier conduct alternately, both block (V_{IN}+V_O), and both conduct (I_{IN}+I_{L2}). Also, if D is the switch duty cycle,

$$I_O = (I_{IN}+I_{L2})(1-D) \quad (1)$$

Since steady-state (and LF) I_{CC} must equal zero,

$$I_O = I_{L2} \quad (2)$$

Obviously, by inspection,

$$I_{IN} = I_{L1} \quad (3)$$

Assuming 100% efficiency, V_OI_O = $V_{IN}I_{IN}$, and

$$I_{L2} = I_O = I_{IN}(V_{IN}/V_O) \quad (4)$$

Thus with V_{IN} = 220V, V_O = 200V and 200W, Fig. 2 shows $I_{O(avg)}$ = 1A and $I_{IN(avg)}$ = 0.9A.

Since the steady-state (and LF) voltage across any inductor must equal zero, the volt-seconds applied to *L2* (and *L1*) during the ON time must be opposed by equal volt-seconds during the off time. Thus:

$$V_{IN}D = V_O(1-D); \quad D = \frac{V_O}{(V_{IN}+V_O)} \quad (5)$$

Note that the duty cycle relationship above for the SEPIC converter is identical to the buck-boost (flyback) topology, even though the input current characteristic closely resembles a boost converter.

Ripple Current Steering

Identical voltages are applied to *L1* and *L2* at all times throughout the switching period. This permits the inductors to be coupled by winding them (with equal turns) on a single magnetic core. (In order to maintain the same total ripple current and same total inductive energy storage, the coupled inductance value is halved: 2mH.) Referring to Fig. 3,

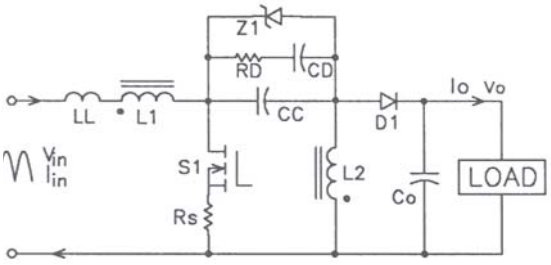
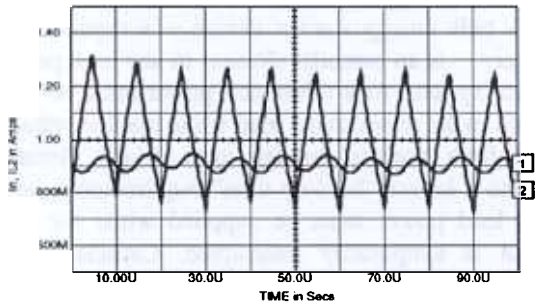


Fig. 3 - SEPIC with Coupled Inductors

the coupled inductor is designed so that its leakage inductance, L_L, is located in series with winding *L1* in the input. In this example, L_L is 10% of the 2mH mutual inductance, or 0.2mH. The high impedance of L_L in series with *L1* opposes the ripple current, forcing most of it into winding *L2*, which has only the relatively low impedance of *Cc* in opposition. As shown in Fig. 4, the triangular HF ripple current through *L2* is increased to $500mA_{p-p}$. The input ripple is reduced to only $50mA_{p-p}$ (mostly at the 100kHz fundamental), greatly diminishing the input noise filtering requirements.[1]



SEPIC Waveforms, Coupled Inductors [1]-I_{IN} , [2]-I_{L2} .

The design of the coupled inductor to achieve this important result is given in a separate paper.[2]

To summarize, the diversion of ac ripple from *L1* to *L2* occurs because (a) although the *total* current in coupled windings *L1* and *L2* is difficult to change, current can easily transfer from one winding to the other, and (b) the high impedance of L_L opposes the ac ripple current in input winding *L1* while the low impedance of *Cc* provides an easy path for the HF ripple current through winding *L2*.

The single coupled inductor is also smaller and costs less than two independent inductors with the same energy storage capability.

Design Considerations: The coupled inductance value *L1* = *L2* is made as small as possible to reduce cost/size and improve frequency response, limited by the amount of ripple current that can be tolerated. In this application, 2mH results in a worst-case ripple of $0.65A_{pp}$ at highest V_{IN} = $365V_{pk}$. This is best calculated during the OFF time when $\Delta I_{L2}/t_{OFF} = V_O/L$. Max t_{OFF} can be calculated at max V_{IN} using Eq. 5.

A large $L_L \cdot C_C$ product results in low input ripple, but impairs frequency response and increases cost. It is better to make *Cc* small to reduce inrush surge and cost. L_L should be correspondingly large provided it can be integrated into the design of the coupled inductor to eliminate its size/cost.

Worst-case input ripple (and EMI) is at the low line peak and full load. A near-rectangular current waveform passes through *Cc*: I_{IN} when the switch is OFF, and I_{L2} (=I_O) in the other direction when the switch is ON. This current waveform produces a triangular ripple voltage across *Cc*. This is best calculated during the ON time when $\Delta V_{CC}/t_{ON} = -I_O/C_C$. I_O = 2A at $400W_{pk}$, 200V out. Max t_{ON} can be calculated from Eq. 5 at min V_{IN}. In this application, a *Cc* of 0.5µF results in $25.6V_{pp}$ worst-case at low-line V_{INpk} = 113V, and 400W.

The triangular ripple voltage across *Cc* appears directly across L_L. L_L integrates this triangular voltage into a quasi-sinusoidal waveform (which is the input ripple). The peak-peak fundamental is $\sqrt{2}/\sqrt{3}$ of a peak-peak triangular waveform, or $21V_{pp}$ in this application. Dividing by X_{LL} = 130Ω (0.2mH at 100kHz) obtains $0.16A_{pp}$ input ripple at 400Wpk and low-line V_{INpk}. (Fig. 4 shows 50mA ripple at 220V input and 200W.)

Resonance problems: The coupled-inductor SEPIC topology has an unusual high-Q resonance effect involving leakage inductance L_L and coupling capacitor *Cc*. In Fig. 3, examine the circuit mesh involving V_{IN}, the inductances, and *Cc*. The ac impedance of V_{IN} is quite low (an input noise filter capacitor). Inductors *L1* and *L2* are tightly coupled in opposition, so their impedances cancel. The only significant ac impedances in this loop are L_L and

C_C. With 0.5µF and 0.2mH used in this example, they will resonate with high Q at 16KHz. L_L and C_C are tightly coupled to each other at all times during the switching period. Even when the switch is closed, L_L and C_C are coupled through the tightly coupled *L1* and *L2* windings.

Unless damped, shock-excited oscillations will send considerable 16KHz ripple back through the input. Theoretically, damping would be achieved if the input current control loop had significant gain at the 16KHz resonant frequency. However, a crossover frequency well above 16 KHz is not practical, as will be explained later. So damping is accomplished by the "brute-force" method using damping network R_D and C_D in shunt with C_C. (Series damping is impractical because of high losses due to the high ac current through C_C.)

To achieve critical damping requires a shunt R_D equal to 1/2 of the resonant impedance. But this requires a large blocking capacitor C_D, increasing cost and reducing the resonant frequency. As a compromise in this application, R_D of 10 Ohms is in series with C_D of 2.5µF, resulting in Q ≈ 1, underdamped but adequate. C_D reduces the self-resonant frequency to 8KHz, but at the 100KHz switching frequency, the coupling network is still effectively 0.5µF. Normal operating loss in R_D is less than 2W, but may be 6W with output shorted.

Output Voltage Level

In a boost preregulator, there is little choice — in order to function, the output voltage must be greater than the highest peak V_{IN}. Thus for a dual range (110/220V) input, the output voltage is normally 385V to 400V.

For the SEPIC converter, no such constraint exists. Theoretically, the output voltage can be any value — above or below the input voltage. However, there are several practical considerations.

Voltage and current ratings: In general, the SEPIC converter is "most comfortable" when $V_O = V_{IN}$, and D = 0.5. When V_O is much greater or much smaller than V_{IN}, peak voltages and peak currents become extreme. Peak switch and rectifier voltage is $V_{IN}+V_O$. Peak current through these devices (neglecting HF ripple) is $I_{IN}+I_O$. Substituting I_O from Eq. 4:

$$I_{IN}+I_O = I_{IN}\frac{V_{IN}+V_O}{V_O} = \frac{I_{IN}}{D} \qquad (6)$$

From this viewpoint alone, V_O in the range of 100–150V is probably optimum for 120V line input, resulting in peak switch and rectifier voltages of 300–350V. For single range 220V, or for 120V/220V input, V_O of 200V results in peak voltages approaching 600V at high 220V line.

Bulk capacitor size and cost: For the same bulk energy storage capability, electrolytic capacitor size and cost tend to vary inversely with voltage rating (more about this later). This consideration alone favors a high V_O, limited by capacitor reliability considerations.

Bus voltage requirements: Power distribution bus voltage will probably *not* be a factor in this decision. This SEPIC converter does not provide the line isolation usually dictated by safety requirements. Because an additional stage is required to obtain isolation, the bulk energy can be stored at any voltage, based on the previous considerations.

Bulk Energy Storage Requirements:

A bulk energy storage device — a capacitor or battery — is an essential element in any high power factor system. At a minimum, power must be provided to the downstream load while the line voltage waveform transits through zero. Many systems define a longer "hold-up time" requirement where full load power must be supplied while the line input is temporarily interrupted. Capacitors are normally used for bulk energy storage when hold-up time requirements are in the tens or hundreds of milliseconds. For longer hold-up times, capacitor size and cost becomes prohibitive, so batteries are used.

When holdup requirements are minimal, a small bulk capacitor may provide the required energy storage, but other factors may then become dominant:

1. The trade-off between voltage control loop dynamics and input third harmonic distortion becomes severe with a small bulk capacitor.
2. The capacitor current rating (120Hz ripple current plus 100kHz switched current) can be

inadequate — this relates to its Equivalent Series Resistance.

3. 120Hz ripple voltage becomes large.

These concerns are discussed in Ref. [3] and [4].

Capacitor size and cost: Electrolytic capacitors are "formed" by the manufacturer to various dielectric thicknesses. Thus several different voltage ratings and capacitance values are available in a single case size. The voltage rating is proportional to the dielectric thickness, but the capacitance value is inversely proportional. Therefore, for a given case size, C·V tends to be a constant value. A capacitor rated for 200V operation will have twice the capacitance as its 400V counterpart in the same case size.

However, at 200 Volts, *4 times* the capacitance value is required as at 400V to achieve the same energy storage ($\frac{1}{2}CV^2$) holdup capability, the same loop dynamics vs. harmonic distortion tradeoff, and the same percent 120Hz ripple. Thus, twice the physical volume (and cost) is required at 200V. For a given application, capacitor size and cost tends to vary inversely with voltage. *Storing bulk energy at 48V vs. 385V can require 8 times the capacitor size, weight, and cost.*

Current Control Loop Design

The control characteristic of the SEPIC converter is complex. Fortunately, in a high power factor preregulator application, the current loop control characteristic is simplified because: (a) Input current, rather than output current, is controlled, (b) V_O is essentially constant because of the large output bulk capacitor which buffers the current control loop against rapid load changes, and (c) the outer voltage control loop requires very low bandwidth to minimize line current distortion and thus does not contribute to current loop instability.

Conventional (peak) current mode control depends upon a current waveform with a linearly increasing ramp. However in this SEPIC converter, ripple current is steered away from the input, leaving only the small amplitude quasi-sinusoidal waveform shown in Fig. 4. This waveform is totally unsuited for peak CMC of input current.

Average current mode control, using a current error amplifier as embodied in the UC3854A, could handle this situation, but there is an additional serious complication: Resonance between L_L and C_C puts two poles in the control-to-input-current characteristic. There is also a pole due to coupled inductor *L1/L2*, which varies with load. Thus there are three active poles (one variable) above the L_L-C_C resonant frequency (10-15 kHz). This makes it impractical to achieve a crossover frequency, *fc*, above resonance. But with a lower crossover frequency there is insufficient loop gain to dampen the high Q L_L-C_C resonant peak.

The solution to this problem is to use average CMC of the average *switch* current. The switch current waveform is chopped, whereas the input current is continuous with a very small ripple. Even though their waveshapes are radically different, *average switch current equals average input current* (at frequencies below L_L-C_C resonance). The control-to-switch-current characteristic is identical to the control-to-input-current characteristic, except the switch current characteristic does not have the extra two resonant poles. Thus it is easy to control the switch current using average CMC. (Peak CMC won't do—the peak current is *much* greater than the average.) Since the L_L-C_C resonant circuit is now outside the control loop, it would ring if not for the damping network, R_D and C_D.

An additional important benefit of controlling average switch current: Switch current is discontinuous, allowing the use of a current transformer (CT) for current sensing. This is not possible with input current, nor is there any apparent way to synthesize the input current waveform.

The optimized average CMC method is well suited to any high power factor preregulator topology. It provides input voltage feedforward to rapidly adapt to instantaneous line voltage changes. It eliminates the peak-to-average error which contributes to distortion with peak CMC. It provides sufficient gain and bandwidth in the discontinuous mode to adequately track the sudden reversal of current required at the cusp of the rectified voltage waveform.

Figure 5 shows the SEPIC preregulator with average CMC control loop. Optimization of the current control loop is covered in a separate Seminar topic[5], which includes the derivation of a

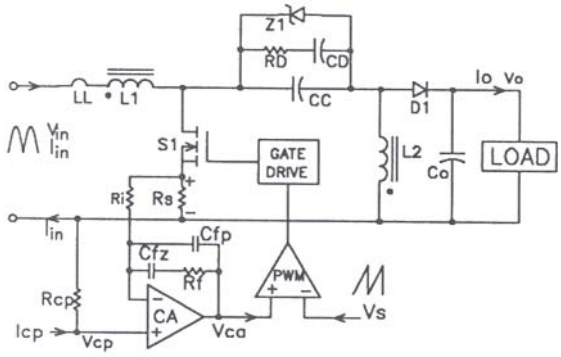


Fig 5. - SEPIC with Average CMC

small-signal model of the coupled-inductor SEPIC converter.

Figure 6 demonstrates the ability of the SEPIC power circuit with average CMC to track a change in input current demand from 1A to 50mA, and its stability. The max. rate of input current change is determined by L_L and C_C, and is much faster than the most severe requirement of the actual application. Note that portions of the I_{L2} waveform go negative, yet operation is not discontinuous because total inductor current $I_{L1}+I_{L2}$ is *not* negative.

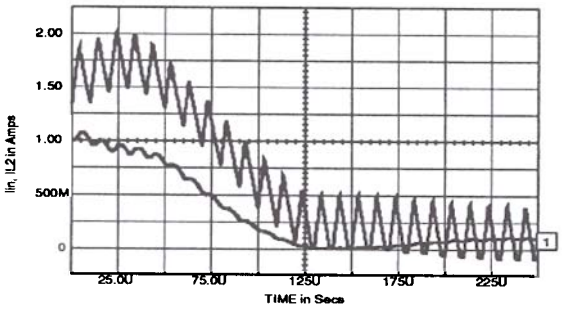


Fig 6. - Change in Current Demand

Input Current Sensing

With most high power factor preregulator techniques, input current must be sensed in order to make it conform to the desired waveshape. It is more difficult to sense input current in the SEPIC converter than in most other topologies, because input current is continuous, ruling out current sense transformers, and because the resonant L_L-C_C characteristic is associated with the input current. However because of the unique identity between average switch current and input current, the discontinuous switch current can be used as a substitute, eliminating both problems.

A current sense resistor is certainly the easiest current sense method at the low end of the power range, where the sense resistor power loss is not too serious. At least 1 Volt sense voltage at full rated input current is required to achieve current loop optimization with low-bandwidth amplifiers such as in the UC3854. A smaller sense voltage reduces the sense resistor loss, but requires a higher amplifier bandwidth such as in the UC3854A. The switch current should be sensed. This enables the sense resistor to be located in series with the MOSFET source terminal which maintains the IC current amplifier input at positive potential, eliminating problems with substrate diode conduction.

A current sense transformer (CT) cannot be used to sense input current directly because the waveform is continuous, giving no opportunity to reset the core. Fortunately, it is better to sense switch current for reasons discussed earlier, thus facilitating the use of a CT. The current transformer can provide a relatively high sense voltage to the current amplifier, reducing its required bandwidth. The CT reduces the power loss involved in direct current sensing, and eliminates the cost and difficulty of using a low resistance value, high wattage precision resistor.

Locating the CT primary in series with the MOSFET drain may reduce current spikes through the CT when the switch turns on.

Voltage Control Loop Design

Once the current loop has been optimized and properly closed, the specific power circuit topology is "buried" within the current loop. External to the closed current loop, the voltage control loop functions in exactly the same way, with the same design considerations whether the power circuit topology is boost, flyback, or SEPIC. The voltage loop establishes the desired amount of input current, but the current loop controls the specific power circuit topology to make it happen. Any HPF control circuit with a current amplifier can be used for

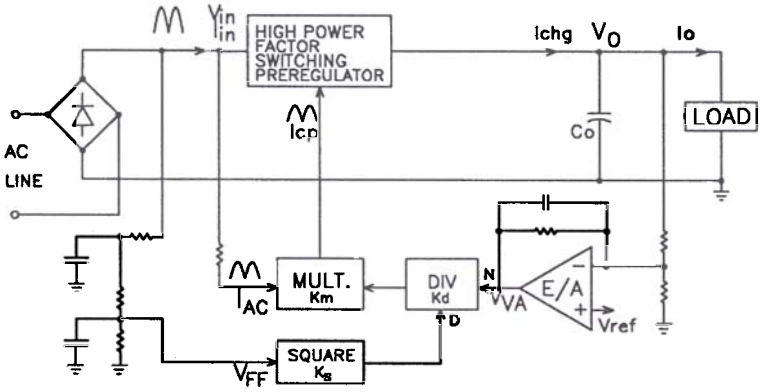


Fig 7. - HPF Preregulator Voltage Loop and Current Programming, any Topology, using the UC3854A

average CMC of the SEPIC preregulator. As shown in Figure 7, the UC3854A can be used, following the same procedure described in Reference [4] for a boost preregulator. (Reprinted in the back of this Seminar manual.)

Overcurrent Limiting

In normal operation, the outer voltage control loop programs an input current consistent with the power demand of the load, and sets an average input current *limit* consistent with the maximum power rating of the supply. However, when the output voltage is well below normal, either during the startup process or during severe overload, if the control circuit tries to maintain full rated power, an unacceptably high current level results.

For example, a 200 Watt preregulator must provide 400W at the line peak. Assume 100% efficiency, $P_{IN} = P_{OUT}$. At V_O = 200V and V_{IN} = 113V (peak input at 80V low line), I_{IN} = 3.55A and $I_{L2} = I_{O(avg)}$ = 2A. Peak current through switch *S1* and rectifier *D1* is 2A + 3.55A = 5.55A. But if *Vo* is pulled down to 10V by a severe overload, 400W at the input is still 3.55A, but the same 400W delivered to the output is now 40A! Peak current through S1 and D1 is now an intolerable 43.55A. This same total current through the coupled inductor requires it to be grossly overdesigned to prevent saturation.

The solution to this problem, effective for start-up or short-circuit conditions, is to incorporate in the control circuit an absolute limit on the peak *switch* current. This causes input current and power to be reduced in line with the reduced output power. In other words, the peak switch current limit translates into foldback input current limiting.

Peak switch current, peak rectifier current and total inductor current are the same: $I_{IN} + I_O$. So absolute current limiting is achieved by sensing the current through *S1* and shutting the switch off whenever the absolute limit is reached.

Switch current sensing already exists for use with the average current mode control loop. This same sense voltage can be used for peak current limiting. The UC3854 HPF control IC has a peak current limit input, but it requires a negative-going signal, opposite to the polarity used for average CMC in this application. Both polarities can be easily obtained from one sense transformer by seriesing two resistors across the CT secondary, and ground referencing the junction of the two resistors.

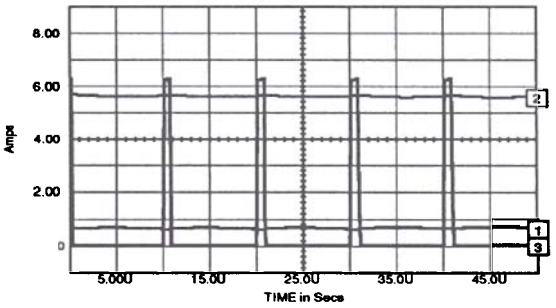


Fig 8. - Overload [1]-I_{IN}, [2]-I_{L2}, [3]-I_{SW}

Fig. 8 shows the SEPIC converter operating in equilibrium with V_{IN} at 113V and *Vo* pulled down to only 10V. The normal control circuit would call for 400W, but the peak switch current limit takes over control. When *S1* turns on, its current is the sum of I_{IN} plus I_{L2}. It does not take long for the current to ramp up to the 6.25A limit. When *S1* turns off, the 6.25A transfers to the output through *D1* (not shown) for the remainder of the switching period. Note that $I_{L2} = I_{O(avg)}$ = 5.65A, delivering 62.2W to the 10V output plus 1V diode drop. I_{IN} is

only 0.6A, taking 67.8W from the 113V line. The 5.6W power difference is due to loss in the damping network (which is worst case under this condition). Without the absolute switch current limit, the 400W power limit would force I_{L2} to 40A at 10V out, or even greater current with lower V_O.

Setting the current limit: The limit must be set high enough to provide full power at low line in normal operation with V_O=200V. For a 200W application, assume 80Vrms minimum, requiring 2.5Arms. Peak power is twice the average power at peak voltage and current — 400W at V_{IN}=113V and I_{IN}=3.55Apk. From Eq. 6:

$$I_{IN}+I_O = I_{IN}\frac{V_{IN}+V_O}{V_O} = 3.55\frac{113+200}{200} = 5.55A$$

Allowing for superimposed HF ripple current, a peak switch current limit of 7A would be appropriate. The inductor must be designed not to saturate at this current limit.

Start-up

Inrush surge: In normal operation, the voltage across coupling capacitor C_C is always equal to the instantaneous rectified line voltage. But at initial startup, C_C and the bulk output capacitor are both discharged. When the power supply is turned on, an inrush current surge charges C_C and C_D rapidly through the series inductor windings. This inrush surge is actually of little consequence because this capacitance is small (3µF in the 200W preregulator) and charges rapidly. The much larger bulk capacitor (800µF) is then charged slowly to V_O, under current limit control. This behavior of the SEPIC converter contrasts sharply with a boost converter, whose inrush surge charge is orders of magnitude greater because it charges the huge bulk capacitor directly.

Referring to Fig. 3 it can be seen that the inrush current flows *into* the dotted end of *L1* but *out* of the dotted end of *L2*. Thus the ampere-turns of these coupled windings cancel. *The core will not saturate no matter how large the inrush current is.* Only the leakage inductance L_L (in addition to the line impedance) limits the inrush surge. Since the leakage inductance flux is located in the non-magnetic region in and between windings *L1* and *L2*, *there is no danger of saturating* L_L.

There is one serious problem: C_C *resonantly* charges through L_L to a voltage much higher than the instantaneous line voltage when the supply is turned on. Without damping, if the instantaneous line happens to be at the peak 220V high line condition (365V) when the supply is turned on, C_C would charge to nearly 730V, considerably more than 365 plus 200 = 565V worst case under normal operation. The damping network helps considerably, but because it is underdamped, the overshoot may still be excessive, increasing the voltage rating requirements of MOSFET *S1* and rectifier *D1*.

If the damping does not limit the overshoot sufficiently, V_{CC} can be limited with a 400V Zener diode — a little greater voltage than the maximum peak V_{IN} of 365V, so the Zener will not interfere with normal operation. In most cases, the Zener diode should not be needed.

Figure 9a shows the inrush surge current with V_{IN} at 300V when the supply is turned on, and Fig. 9b shows the voltage across switch *S1* as V_{CC} resonantly charges, clamping at 400V.

The inrush surge amplitude and pulse width can be estimated from the resonant frequency and resonant impedance of the inrush circuit (neglecting line and input rectifier impedance):

$$f_R = \frac{1}{2\pi\sqrt{L_L C_{eff}}}, \quad Z_R = \sqrt{\frac{L_L}{C_{eff}}}$$

With the circuit conditions of Fig. 9, L_L = 0.2mH, C_C = 0.5µF, C_D = 2.5µF and R_D = 10Ω. The effective capacitance at resonance is 2µF, resulting in f_R = 8kHz and Z_R = 10Ω. The peak undamped inrush current would be 300V/10Ω=30A, but damping reduces this to 25A peak. The half-cycle resonant pulse width is 60µsec, lengthened somewhat by the action of the 400V clamp. Compared to the startup surge to charge 800µF directly, this surge is insignificant.

Fig. 9a shows that the inrush surge ends at 85µsec. During the surge, the switch turns on periodically, which applies V_{CC} momentarily across *L2*. Thus when I_{IN} reaches zero at the end of the surge, I_{L2} is already at 3A in the positive direction.

Following the inrush surge: From 85 to 190 µsec, each time the switch turns on, C_C gives up a

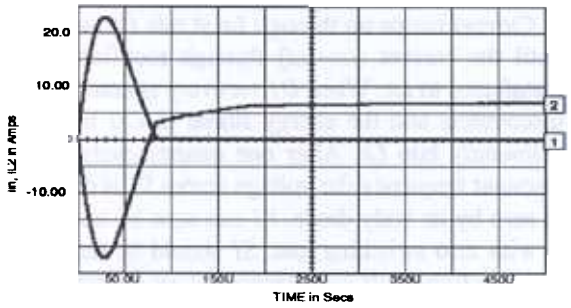


Fig. 9a - Startup [1]-IIN, [2]-IL1

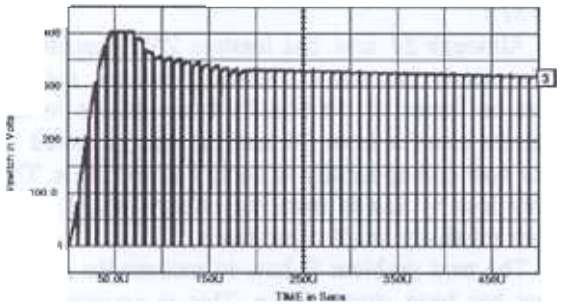


Fig. 9b - Startup VSWITCH

little of its energy into *L2*, causing *VCC* (seen across the switch) to slowly fall towards *VIN* (300V), and *IL2* to slowly rise. Most of the time, the switch is off, and *IL2* is delivered through *D1* to output capacitor *CO*. *IIN* remains at zero as long as *VCC* is greater than *VIN*, because when the switch turns on, *VCC* is applied to *L2*, inducing *VCC* > *VIN* across *L1* as well. Since *VIN* is still at 300V, the input rectifiers (not shown in Fig. 3) block all current flow.

At 190µsec, *IL2* reaches 6.5A and the switch current limit becomes effective. When the switch turns on, *VCC* applied to *L1* causes *IL1* to rise rapidly until the 6.5A switch current limit is reached. When the switch turns off, *IL1 slowly* discharges into *CO* (*VCO* is almost zero). The duty cycle thus is extremely short at the current limit.

With *CO* = 800µF, the output voltage rises at a rate less than 1V/100µsec!! So during the entire time shown in Fig. 8, the output is essentially shorted, and energy is being transferred from *CC* (and *CD*) to *CO*, and *IIN* = 0.

At approximately 1000µsec, *VCC* has decreased to equal *VIN*, which is still near 300V. (*VCC* subsequently tracks *VIN* along the rectified line waveform). Now, for the first time since the end of the surge, the input rectifiers can conduct and *IIN* starts to rise. The rate of rise is not determined by winding *L1*, but by leakage inductance *LL*. Since *L1* and *L2* are coupled, whatever current is demanded by *LL* is easily diverted away from winding *L2* into winding *L1*. As *IIN* starts to rise, *IL2* falls in a complementary manner. The total current *IIN*+*IL2* through the switch remains at the current limit.

During this last phase of the start-up process, when *VCC* = *VIN*, current limited operation is identical to the situation described earlier with severe overload. The output will rise slowly as the bulk capacitor charges at the current limited level. When *VO* rises to the point where *VO* times the current limited charging current equals the power limit for normal operation, the current backs away from the current limit and normal power-limited operation takes over.

Note that the foldback limiting characteristic of the peak switch current limit requires that constant power loads (such as downstream switching power converters) be disabled when *VO* is low, using undervoltage lockout. Otherwise, the reduced power input will not be able to pull up the preregulator output during start-up or after an overload has cleared. With resistive loads, this is not a problem, because load power is automatically reduced.

When *VO* is at or very close to zero, the very small duty cycle required to maintain the current at the limit may require an ON time less than the system can provide, for various reasons including ZVT circuitry. To prevent loss of control, if the current is already over the current limit when the clock pulse occurs, the current limiting circuit should inhibit the ON pulse completely, skipping pulses until the current falls below the limit.

ZVT Circuitry

Zero Voltage Transition capability is an important addition to any high power factor preregulator. High voltage circuits store significant energy in circuit parasitic capacitances. High voltage rectifier recovery characteristics are far from ideal, especially at higher power levels. With "hard" switching, these characteristics translate into high losses,

severe component stress, and radiated EMI. ZVT circuitry facilitates nearly lossless transitions and reduces noise.

Zero Voltage Transitions occur naturally whenever the power switch *S1* turns off. Current $I_{IN}+I_{L2}$ transfers from the switch to the capacitance of the switch, rectifier, and circuit parasitics (lumped together as C_{S1} in Fig. 10a) while the capacitance holds the voltage near zero. Then the capacitance charges as the voltage rises until clamped by the output rectifier conduction. Thus, turn-off loss is quite small without any special design effort.

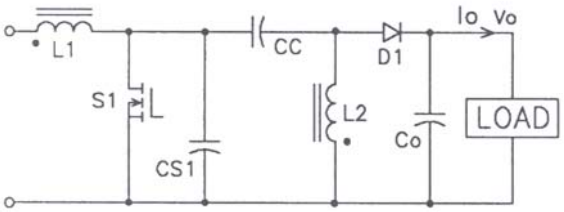


Fig 10a - Non-ZVT SEPIC Circuit

Turn-on is a different matter. *S1* is clamped at high voltage ($V_{IN}+V_O$) while the current makes its transition, causing power loss in the switch. This loss is worsened by the high voltage rectifier's reverse recovery current, especially if the switch turn-on is fast to minimize the transition time. No matter how fast *S1* turns on, the very significant energy stored in C_{S1} is translated into switch loss.

The first step in achieving turn-on ZVT is to connect a small inductor L_R in series with an auxiliary switch *S1a* across main power switch *S1* as shown in Fig. 10b.[6] *S1a* is a much smaller device than main power switch *S1*, with much lower *Coss*. When the control IC calls for switch turn-on, *S1a* is turned on first. *S1* turn-on is delayed.

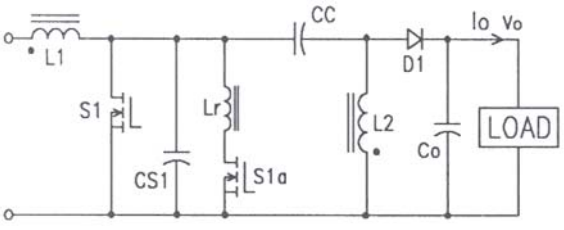


Fig. 10b - ZVT Inductor and Aux. Switch

Current ramps up through L_R at rate $(V_{IN}+V_O)/L_R$ until the current ($I_{IN}+I_{L2}$) through rectifier *D1* is transferred to L_R. When *D1* recovery is complete, it disconnects and the energy stored in C_{S1} transfers *resonantly* into L_R. After one quarter cycle at the resonant frequency the voltage across *S1* is clamped at zero by its body diode. *S1* can now be turned on — with zero switching loss. *S1* should be turned on and *S1a* turned off simultaneously, or as quickly as possible to transfer the current away from the much smaller *S1a* with its higher static losses. (As long as *S1a* remains on, L_R will prevent the current transfer to *S1*.)

Although *S1* now has lossless ZVT transitions, *S1a* clearly has turn-on losses. However, the big turn-on losses of the non-ZVT circuit due to the current transfer from D1 and the energy stored in C_{S1} now end up mostly as energy stored in L_R. The only loss in *S1a* is from the energy stored in its own relatively small capacitance.

The next problem is how to recover the energy that has been stored in L_R. This is accomplished with a second tightly coupled winding on L_R, as shown in Fig. 10c. The two windings have the same number of turns, bifilar wound. When *S1a* turns off, current transfers to the second winding and passes through the diode to any convenient voltage sink -- V_{CC} or V_O, where the energy stored in L_R is recovered.

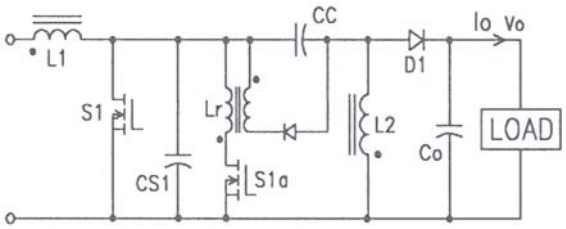


Fig 10c - Energy Recovery

The ON time of the ZVT switch *S1a* becomes the minimum ON time of the SEPIC converter. In normal operation, this is not a problem. As shown by Eq. 5, the minimum duty cycle occurs at max V_{IN} and never approaches zero with normal values of V_O. But D *does* approach zero when V_O is zero during start-up or short-circuit load conditions. The control circuit must then skip pulses to reduce the

duty cycle and retain control in spite of the fixed minimum ON time.

Design Considerations: Two things must be defined: (1) the inductor L_R value, and (2) the delay time for turning on S1 after S1a has been turned on (which will be the minimum ON time of the converter).

There are three sequential times involved:

1. The time for current to ramp up in L_R and transfer away from *D1*:

$$t_{RAMP} = L_R(I_{IN}+I_O)/(V_{IN}+V_O)$$

2. *D1* recovery time
3. Resonant quarter cycle when energy transfers from C_{S1} to L_R:

$$t_{RES} = \pi\sqrt{L_R C_{S1}}/2$$

A small L_R value reduces t_{RAMP} and t_{RES} but worsens the diode recovery current and peak resonant current. One approach is to consider what would be a reasonable delay time (minimum ON time). A ramp time of 200ns is 2% of the 10µsec switching period. Worst case is at peak low line, full power. Applying the values developed earlier for this specific application to the t_{RAMP} equation above:

$$L_R = 200ns(113V+200V)/(3.55A+2A)$$

$$L_R = 11.27\mu H$$

For L_R = 10µH, $t_{RAMPmax}$ is 171nsec.

Assuming a total capacitance C_{S1} of 500pF, the resonant frequency is 2.4 MHz, resulting in a time t_{RES} of 104ns for 1/4 cycle. This time is independent of V_{IN} or load. Resonant impedance Z_R = $(L/C)^{1/2}$ = 141Ω. At high line peak of 365V, this results in a peak resonant current of (365+200)/141 = 4A (in addition to 3A I_O+I_{IN} at high line peak).

A total *S1a* ON time of 300nsec, resulting in a minimum duty cycle of .03 is reasonable and adequate for this application.

Switching losses in high power factor applications are especially severe because of the high voltages being switched. ZVT techniques are unusually advantageous. The biggest implementation problem at this date is that existing HPF control ICs do not provide the delayed driver function, forcing it to be accomplished with outboard components.

Line Isolation

It is theoretically possible to incorporate line isolation in the SEPIC converter by adding an additional winding *L3*, as shown in Fig. 11.

Insulation for 3750Vrms isolation must be incorporated between windings *L2* and *L3*. Unfortunately, the high voltage insulation prevents close coupling between these windings. The resulting leakage inductance is large and its circuit location (directly in series with either *L2* or *L3*) causes delays, voltage spikes and difficulty energy recovery problems.

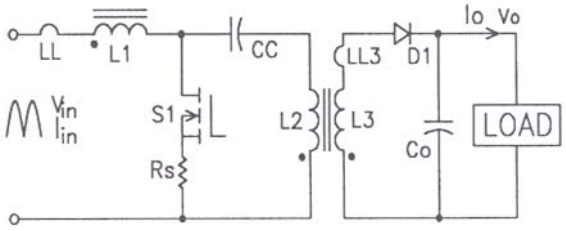


Fig 11. - SEPIC Converter with Isolation

To date, there are no known practical solutions to this problem. If a way can be found, this would considerably enhance the usefulness of the SEPIC high power factor topology. Bear in mind that if an isolation technique is also used to step down to an isolated 48V bus, for example, there is a substantial penalty in bulk capacitor size and cost vs. energy storage at 200V.

A suggestion for anyone who would attempt to solve this problem: If *L1* and *L2* are also coupled to maintain ripple current steering as discussed earlier, it is important to use the following winding sequence, starting from the gapped core center leg: *L3*, HV insulation, *L2*, *L1*. Otherwise the leakage inductances L_L in the input and L_{L3} in the output will be coupled to each other, with (probably) disastrous results.

Conclusions

The SEPIC converter has many advantages for high power factor preregulator applications. Steering the high frequency ripple current away from the input can dramatically reduce the size and cost of th input noise filter. This advantage, the very small start-up surge, and the inherent current-limiting capability become more and more significant as the power level rises.

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[6] G.C.Hua, C.S.Leu, Y.M.Jiang, F.C.Lee "Novel Zero-Voltage Transition PWM Converters," *VPEC Power Electronics Seminar Proceedings, p33*, 1992

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