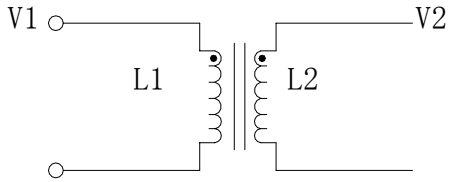
测试原理

本章的目的是了解一些常见测试参数的定义。

1. 什么是 T\R?



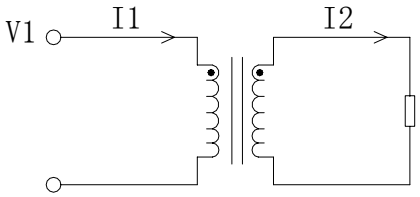
T\R 是一个绕组到另一个绕组的电压比 TR=V1/V2

对于一个电源变压器，它的有效输出电压是 V2=V1*TR

对于一个电流传感变压器，它的有效测量电流是 I2=I2/TR

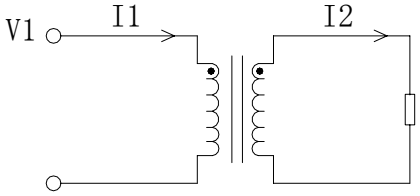
对于一个阻抗匹配变压器，它的有效变压器阻抗是 Z1=Z1/(2)

2. 什么是 OCL?



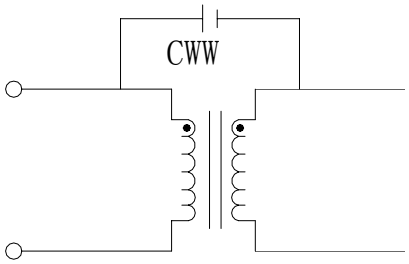
变压器初级电感指次级开路时初级绕组的有效电感，即 I2=0 时。

3. 什么是 LL?



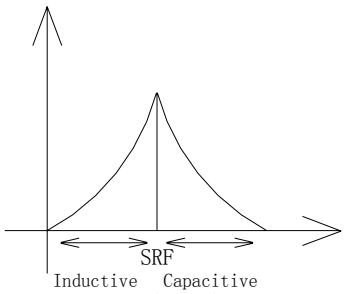
初级漏感是指变压器次级所有绕组短路时在次级测得的电感，即 I2=最大时（短路）。

4. 什么是 CWW?



将变压器绕组各自短路，然后用电桥测量绕组间的电容。

5. 什么是 SRF?



在某个频率下输出的阻抗最大时称为 SRF。

6. 什么是 DCR?

直流条件下的阻抗。

7. 什么是 OCL BALANCE/DCR BALANCE/CWW BALANCE/LL BALANCE?

两个绕组间的 OCL 匹配，叫 OCL BALANCE。

两个绕组间的 DCR 匹配，叫 DCR BALANCE。

绕组间的 CWW 匹配，叫 CWW BALANCE。

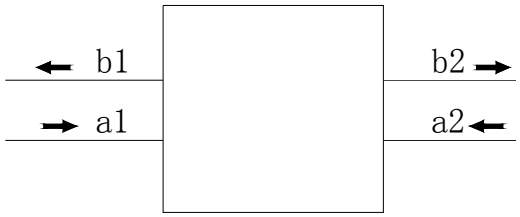
绕组间的 LL 匹配，叫 LL BALANCE。

8. 什么是 Q 值?

在给定频率下，每个周期里最大贮存能量与损耗能量之比的 2 倍定义为品质因数。

9. 什么是 IL?

定义：The ratio of transmitted to incident power is call the insertion loss。



两个端口的网络 S-PARAMTERS 公式如下：

b1=S11*a1+S12*a2　　eqs1

b2=S21*a1+S22*a2　　eqs2

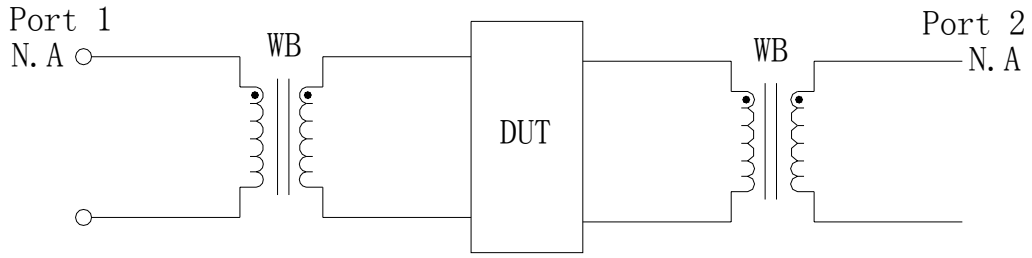
S12=b1/a2　　当 a1=0 时

S22=b2/a1　　当 a2=0 时

端口 1 to 端口 2 的 Insertion Loss(dB)=-20log(|S21|)

端口 2 to 端口 1 的 Insertion Loss(dB)=-20log(|S21|)

IL 测试设置如下：



10. 什么是 RL?

定义：The ratio of reflected to incident signal is call the return loss。

两个端口的网络 S-PARAMTERS 公式如下：

b1=S11*a1+S12*a2　　eqs1

b2=S21*a1+S22*a2　　eqs2

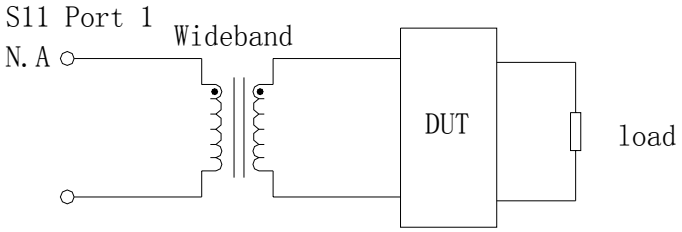
S12=b1/a1　　当 a2=0 时

S22=b2/a2　　当 a1=0 时

端口 1 the return loss (dB)=-20log(|S11|)

端口 2 the return loss (dB)=-20log(|S22|)

RL 测试设置如下：



11. 什么是 DD（Differential Delay 微分延迟）？

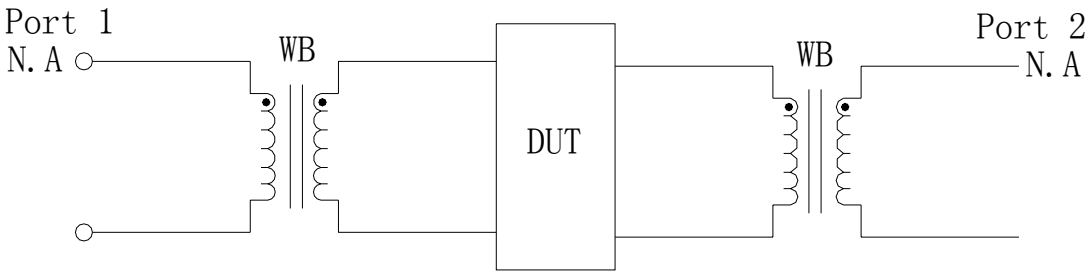
定义：在不同频率下两个信号的延迟差。

公式：DD=∅1/（f1*360）-∅2/(f2*360)。

其中：f1、f2 是测试信号的频率；∅1，∅是测试信号的相位。

对于一个理想的产品 DD=0

DD 测试设置如下：

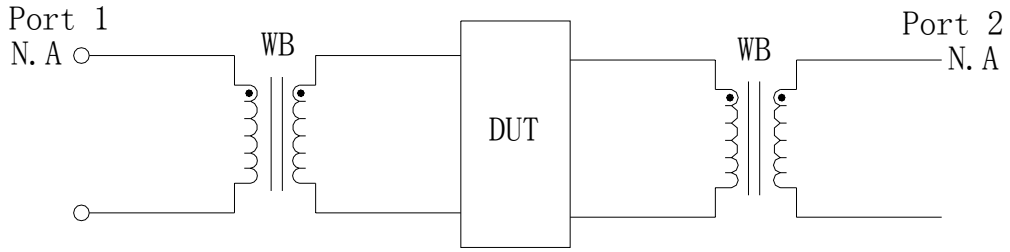


12. 什么是 GD?

定义：信号通过一个测试设备的转接时间。

Group delay=the derivative of the phase characteristic with respect to frequency。

GD 测试设置如下：

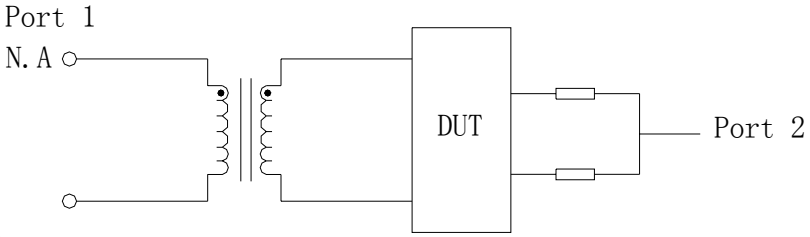


13. 什么是 DCMR?

The common mode response of the balanced device, when it is stimulated with the differential mode signal.

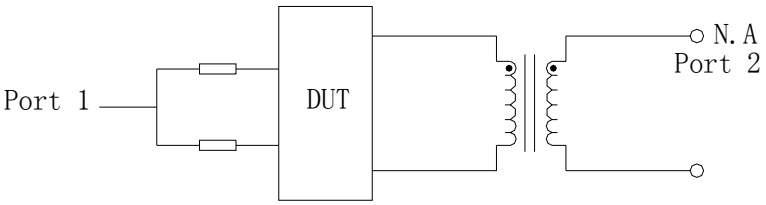
DCMR indicates the devise capability of preventing producing interference to the other devise.

DCMR 测试设置如下：



The differential mode response of the balanced device, when it is stimulated with the common mode signal.

CDMR 测试设置如下：

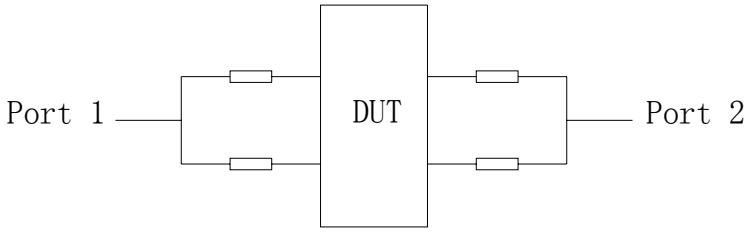


14. 什么是 CMRR?

The common mode response of the balanced device, when it is stimulated with the common mode signal.

CMRR indicates the devise capability to block the interference from transmitting.

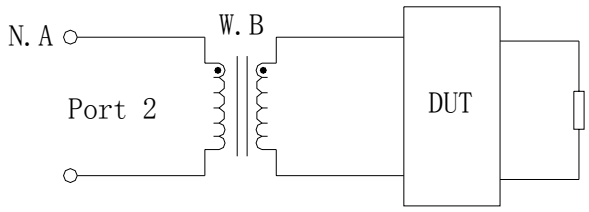
CDMR 测试设置如下：



15. 什么是 CT?

Cross talk indicates the devise susceptibility to interference by another channel signal。

CT 测试设置如下：



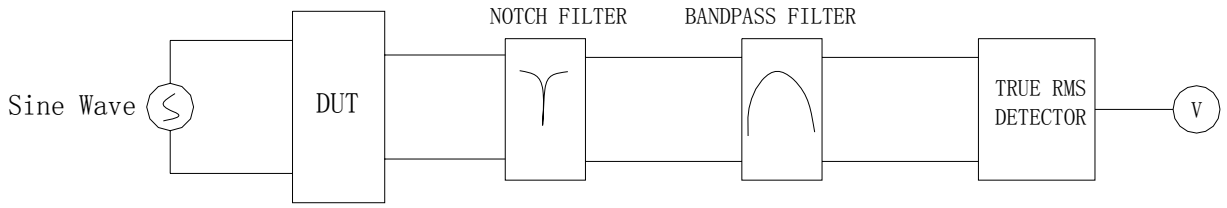
16. 什么是 THD+D?

THD indicates the linearity of the device。

A sinewave signal is input to the device,THD is the square root of the sum of the squares of the individual harmonic amplitudes。

The following figure is a simplified block diagram of the THD+N setup.The key functional blocks is a tunable notch filter(band-reject filter).In operation,this is turned to the fundamental sinewave frequency,so that the fundamental is greatly attenuated.The filter is designed to have virtually on insertion loss a second harmonic and higher,so harmonics are passed essentially unattenuated.Wind band noise,AC mains-related hum,and an other interfering signals below and above the notch filter frequency are also passed unattenuated;hence the (N9plus noise) portion of the name.

THD 测试设置如下：



17. 什么是 LB?

The imbalance of the devise will transform the common mode signal to differential mode signal. Longitudinal balance indicates the devise susceptibility to the interference.

18.

19.