Section 4   Power Transformer Design

Power Transformer Design

This Section covers the design of power transformers used in buck-derived topologies: forward converter, bridge, half-bridge, and full-wave center-tap. Flyback transformers (actually coupled inductors) are covered in a later Section. For more specialized applications, the principles discussed herein will generally apply.

Functions of a Transformer

The purpose of a power transformer in Switch-Mode Power Supplies is to transfer power efficiently and instantaneously from an external electrical source to an external load. In doing so, the transformer also provides important additional capabilities:

- The primary to secondary turns ratio can be established to efficiently accommodate widely different input/output voltage levels.
- Multiple secondaries with different numbers of turns can be used to achieve multiple outputs at different voltage levels.
- Separate primary and secondary windings facilitate high voltage input/output isolation, especially important for safety in off-line applications.

Energy Storage in a Transformer

Ideally, a transformer stores no energy–all energy is transferred instantaneously from input to output. In practice, all transformers do store some undesired energy:

- Leakage inductance represents energy stored in the non-magnetic regions between windings, caused by imperfect flux coupling. In the equivalent electrical circuit, leakage inductance is in series with the windings, and the stored energy is proportional to load current squared.
- Mutual inductance (magnetizing inductance) represents energy stored in the finite permeability of the magnetic core and in small gaps where the core halves come together. In the equivalent circuit, mutual inductance appears in parallel with the windings. The energy stored is a function of the volt-seconds per turn applied to the windings and is independent of load current.

Undesirable Effects of Energy Storage

Leakage inductance delays the transfer of current between switches and rectifiers during switching transitions. These delays, proportional to load current, are the main cause of regulation and cross regulation problems. Reference (R4) included in this manual explains this in detail.

Mutual inductance and leakage inductance energy causes voltage spikes during switching transitions resulting in EMI and damage or destruction of switches and rectifiers. Protective snubbers and clamps are required. The stored energy then ends up as loss in the snubbers or clamps. If the loss is excessive, non-dissipative snubber circuits (more complex) must be used in order to reclaim most of this energy.

Leakage and mutual inductance energy is sometimes put to good use in zero voltage transition (ZVT) circuits. This requires caution–leakage inductance energy disappears at light load, and mutual inductance energy is often unpredictable, depending on factors like how well the core halves are mated together.

Losses and Temperature Rise

Transformer loss is sometimes limited directly by the need to achieve a required overall power supply efficiency. More often, transformer losses are limited by a maximum "hot spot" temperature rise at the core surface inside the center of the windings. Temperature rise (°C) equals thermal resistance (°C/Watt) times power loss (Watts).

$$\Delta T = R_T \times P_l$$

Ultimately, the appropriate core size for the application is the smallest core that will handle the required power with losses that are acceptable in terms of transformer temperature rise or power supply efficiency.

Temperature Rise Limit

In consumer or industrial applications, a transformer temperature rise of 40-50°C may be acceptable, resulting in a maximum internal temperature of 100°C. However, it may be wiser to use the next size larger core to obtain reduced temperature rise and reduced losses for better power supply efficiency.

Losses

Losses are difficult to predict with accuracy. Core loss data from core manufacturers is not always dependable, partly because measurements are made under sinusoidal drive conditions. Low frequency winding losses are easy to calculate, but high frequency eddy current losses are difficult to determine accurately, because of the high frequency harmonic content of the switched rectangular current waveshape. Section 3 discusses this problem extensively. Computer software can greatly ease the difficulty of calculating the winding losses, including high order harmonics[1].

Thermal Resistance

Temperature rise depends not only upon transformer losses, but also upon the thermal resistance, R_T (°C/Watt), from the external ambient to the central hot spot. Thermal resistance is a key parameter, unfortunately very difficult to define with a reasonable degree of accuracy. It has two main components: internal thermal resistance R_I between the heat sources (core and windings) and the transformer surface, and the external thermal resistance R_E from the surface to the external ambient.

Internal thermal resistance depends greatly upon the physical construction. It is difficult to quantify because the heat sources are distributed throughout the transformer. R_I from surface to internal hot spot is not relevant because very little heat is actually generated at that point. Most of the heat generated in the core (other than in toroids) is near the transformer surface. Heat generated within the winding is distributed from the surface to the internal core. Although copper has very low thermal resistance, electrical insulation and voids raises the R_T within the winding. This is a design area where expertise and experience is very helpful. Fortunately, internal thermal resistance is considerably smaller than external R_E (except with high velocity forced air cooling), and while R_I shouldn't be ignored, it usually is not critically important compared with R_E.

External R_E is mainly a function of air convection across the surface of the transformer–either natural convection or forced air. R_E with natural convection cooling depends greatly upon how the transformer is mounted and impediments to air flow in its vicinity. A transformer mounted on a horizontal surface and surrounded by tall components, or mounted in a relatively small enclosure will have considerably greater R_E than if it were mounted on a vertical surface, benefiting from the "chimney effect". With forced air cooling, R_E can be driven down to a very small value, depending on air velocity, in which case internal R_I becomes the primary concern. With forced air cooling, thermal resistance and temperature rise often become irrelevant, because an absolute loss limit to achieve power supply efficiency goals becomes dominant.

For the average situation with natural convection cooling, a crude "rule of thumb" can be used:

$$R_E = \frac{800°C \cdot cm^2 / Watt}{A_S \cdot cm^2} \quad °C / Watt$$

Where A_S is the total surface area of the transformer, excluding the mounting surface. Calculating A_S is time-consuming, but another rule of thumb simplifies this, as well. For a given class of cores, such as E-E cores in the ETD or EC series, the relative proportions are quite similar for all core sizes. Thus for all cores in the ETD or EC series, the usable surface area, A_S, is approximately 22 times the winding window area, A_W. Combining this with the equation above enables the window area, A_W, from the core data sheet, to be used to directly calculate the external thermal resistance:

$$R_E = \frac{36}{A_W \ in \ cm^2} \quad °C / Watt$$

For pot cores or PQ cores, window areas are proportionately smaller, and not as consistent. A_S/A_W may range from 25 to 50, so that R_E may range from $16/A_W$ to $32/A_W$ °C/W.

Experience is a great help in minimizing and crudely quantifying thermal resistance. In the final analysis, an operational check should be conducted with a thermocouple cemented at the hot spot near the middle of the centerpost, with the transformer mounted in a power supply prototype or mockup.

Worst Case Losses

Transformer losses should be examined under worst-case conditions that the power supply is expected to operate over long periods of time, not under transient conditions.

Transformer losses can be put into three major categories: core hysteresis losses, core eddy current losses, and winding losses.

Core hysteresis losses are a function of flux swing and frequency. In all buck-derived applications under steady-state conditions, VIN•D = n•VO. Under fixed frequency operation, volt-seconds and therefore flux swing are constant. *Hysteresis loss is therefore constant*, regardless of changes in VIN or load current.

Core eddy current loss, on the other hand, is really I^2R loss in the core material. If VIN doubles, Peak I^2R loss quadruples, but since D is halved, average I^2R loss doubles. Thus core eddy current loss is proportional to VIN. *Worst case is at high VIN.*

Winding losses: In buck-derived regulators, peak secondary current equals load current and peak primary current equals load current divided by the turns ratio:

$$I_{Spk} = I_L \;\; ; \;\; I_{Ppk} = I_L / n$$

Peak currents are independent of VIN. But at constant peak currents (constant load), *rms current squared (and I^2R loss) is proportional to duty cycle D and inversely proportional to VIN..* (With constant peak current, high order harmonics depend mostly on switching transitions and do not vary significantly with D.)

In buck-derived regulators, winding loss is always greatest at low VIN.

Ferrite cores: In most ferrite materials used in SMPS applications, hysteresis losses dominate up to 200-300kHz. At higher frequencies, eddy current losses take over, because they tend to vary with frequency squared (for the same flux swing and waveshape).

Thus, *at frequencies up to 200-300kHz, worst case is at low VIN and full load* because of high winding losses. Once core eddy current losses become significant, they rise rapidly with frequency, especially at high VIN. (The increase in eddy current loss with high VIN, small D, is not shown in core manufacturer's loss curves because they assume sinusoidal waveforms.) Winding losses also rise with frequency, especially at low VIN. To maintain a reasonable R_{AC}/R_{DC}, Litz wire with more strands of finer wire must be used, raising R_{DC} because increased insulation and voids reduce the copper area. Thus, *at frequencies where core eddy current losses dominate, core loss worst case is at high VIN, full load. Winding loss worst case is always at low VIN, full load..*

Laminated metal alloy and powdered metal cores: Core eddy current losses dominate, hence worst case is at high VIN, full load. Winding losses are worst case at low VIN, full load.

Balancing Core and Winding Losses

At SMPS operating frequencies, when the core is usually loss-limited, not saturation limited, total losses are at a broad minimum when core losses are approximately equal to or a little less than winding losses. Likewise, winding losses are at a minimum and well distributed by making the rms current density approximately equal in all windings. With a bridge or half-bridge primary, which has good winding utilization, and center-tapped secondaries which have poor utilization, rms current densities will be approximately equalized when the primary conductor cross-section area is 40% and the secondaries 60% of the available area. In most other cases, primary and secondary conductor areas should be 50%/50%, including: Forward converter (single-ended primary/secondary SE/SE), C.T. primary/C.T. secondary, bridge-half bridge primary/bridge secondary.

The above allocations can be impossible to achieve because the number of turns in each winding must be an integral number. In a low voltage secondary, 1.5 turns may be required for optimum balance between core and winding losses. With one turn, the flux swing and core loss may be much too large; with two turns the winding loss becomes too great. At either extreme, it may be impossible to meet temperature rise or absolute loss limits. A larger core may be required to resolve this problem.

Window Utilization

This subject is discussed extensively in Section 3. As a reminder:

- Safety isolation requirements impose minimum dimensional limits for creepage and insulation thickness which can waste a high percentage of window area, especially in a small transformer. A bobbin also reduces the area available for windings.

    Triple insulated wire satisfies the insulation thickness requirement and eliminates the creepage requirement. It is worth considering, especially for small transformers where creepage distances take up a large percentage of window area.

- In the reduced window area that is available for the windings, much of the actual winding area is taken up by voids between round wires and by wire insulation. In a winding consisting of many turns of single, round, insulated wires, only 70 - 75% of the area available for that winding is likely to be conductor metal -- "copper". With Litz wire, the copper area is reduced further. For every level of twisting , an additional 0.75 factor (approximate) applies. For example, with Litz wire 7 strands of 7 strands (49 total wires), the copper area would be .75•.75•.75 = 42% of the area available for that winding. On the other hand, a winding consisting of layers (turns) of copper foil or strap, there are no voids, only the insulation between turns. Winding area utilization could be as much as 80 - 90% copper area.

Topology

The choice of circuit topology obviously has great impact on the transformer design, but a detailed discussion is beyond the scope of this topic.

There is a great deal of overlap in topology usage. Flyback circuits (flyback transformers are covered in Section 5) are used primarily at power levels in the range of 0 to 150 Watts, Forward converters in the range of 50 to 500 Watts, half-bridge from 100 to 1000 Watts, and full bridge usually over 500 Watts.

Full bridge and half-bridge topologies with full bridge secondaries have the best transformer efficiency because the core and the windings are fully utilized. With center-tapped secondaries, winding utilization and efficiency are reduced. With center-tapped primary *and* secondaries, winding utilization and efficiency are further reduced. All of the push-pull topologies have the further advantage that for a given switching frequency, giving the same output ripple filtering and closed loop capability, the frequency at which the transformer core and windings operate is halved, reducing core and ac winding losses.

Forward converter transformers have the poorest utilization and efficiency because neither the core nor the windings are used during the lengthy core reset interval.

Frequency

There are several meanings to the term "frequency" in switching power supply applications, and it is easy for confusion to arise.

In this paper, "switching frequency", f_S, is defined as the frequency at which switch drive pulses are generated. It is the frequency seen by the output filter, the frequency of the output ripple and input ripple current, and is an important concept in control loop design. In a single-ended power circuit such as the forward converter, the power switch, the transformer, and the output rectifier all operate at the switching frequency and there is no confusion. The transformer frequency and the switching frequency are the same.

"Clock frequency" is the frequency of clock pulses generated in the control IC. Usually, the switching frequency is the same as the clock frequency, but not always. Occasionally, the control IC may divide the clock frequency to obtain a lower switching frequency. It is not unusual for a push-pull control IC to be used in a single-ended forward converter application, where only one of the two switch

drivers is used, to guarantee 50% max. duty cycle. In this case the switching frequency is half the clock frequency.

Confusion often arises with push-pull topologies. Think of the push-pull power circuit as a 2:1 frequency divider, with the transformer and the individual switches and individual rectifiers operating at a "transformer frequency", f_T, which is one-half of the switching frequency. Collectively, the switches and rectifiers operate at the switching frequency, but the transformer operates at the transformer frequency. Some designers define "switching frequency" as the frequency that the individual switch and the transformer operate at, but this requires redefining the term "switching frequency" when dealing with output ripple and in control loop design.

Duty Cycle

Duty cycle, D, is defined as the amount of time the power switch is on in relation to the switching period: $D = t_{ON}/T_S$.

In a single-ended forward converter, this is clearly understood, but in a push-pull circuit, ambiguity often arises. For example, in a half-bridge circuit operating at minimum V_{IN}, the duty cycle is likely to be in the vicinity of 90% (D = 0.9). The transformer is delivering power to the output 90% of the time, there is a voltage pulse applied to the filter input 90% of the time, etc. But individual power switches and individual rectifiers, which conduct only during alternate switching periods, can be said to operate at a duty cycle of 45%. That is true, but it is better tothink of them as operating at D/2, retaining a consistent definition of D throughout the power supply design.

Maximum Duty Cycle

In normal steady-state operation of a buck-derived regulator, $V_{IN}\cdot D$ is constant. The control loop changes duty cycle D inversely proportional to V_{IN} to maintain a constant output voltage, V_O. ($V_{IN}D = n\cdot V_O'$), where n is the turns ratio N_P/N_S, and V_O' equals output voltage V_O plus diode forward voltage drop at full load.

At a fixed switching frequency and *with normal steady-state operation, the volt-seconds applied to the transformer windings are constant*, independent of line voltage or load current.

$$V_{IN}t_{on} = \frac{V_{IN}D}{f_S} = \frac{nV_O'}{f_S}$$

The maximum duty cycle, Dmax, associated with minimum V_{IN} in normal steady-state operation, is limited by a variety of considerations:

In a forward converter, a substantial portion of each switching period must be allowed for core reset. If the voltage backswing during reset is clamped to V_{IN}, the duty cycle must be limited to less than 50% because the time required for reset equals the switch ON time.

In a push-pull converter (bridge, half-bridge, PPCT) duty cycle can approach 100% at the switching frequency (always think of D at the switching frequency, not the transformer frequency). However, it may be necessary to limit D to less than 90% to allow a current transformer to self-reset.

Often the control IC limits the duty cycle for several reasons including allowing time for delays in turning off the switch.

At low V_{IN}, if normal Dmax is right at the duty cycle limit, the regulator has no reserve volt-second capability and cannot respond rapidly to a sudden load increase occuring when V_{IN} is low. It may be desirable to make the "normal" Dmax less than the absolute limit, Dlim, to provide a little headroom in this situation.

A potentially serious problem needs to be considered: During initial start-up of the power supply, or following a sudden large increase in load current which temporarily pulls down Vout, the control loop calls for full current, pushing the duty cycle to its absolute maximum limit, Dlim. The output filter inductor limits the current rate of rise, so that for several switching frequency periods, the duty cycle is at the limit, Dlim. During the transient event described above, Dlim could occur when V_{IN} is maximum. Thus, the volt-seconds applied to the transformer windings could be several times larger than normal:

Limit $V_{IN}D = V_{IN}maxDlim$
Normal $V_{IN}D = V_{IN}minDmax$

The flux swing, also several times greater than normal, could saturate the core. (The increased core loss is not a problem–it is only temporary.)

This may not be a problem if the ratio limit/normal VIND is small and/or if the normal flux density swing, limited by core loss, is a small fraction of Bsat (Bsat - Br for a forward converter). For example, if limit/normal VIND is 3:1, and if normal ΔB is 0.08T, then with Bsat greater than 0.24T, there is no problem.

If this problem exists, soft-start circuitry can eliminate it during start-up, but soft-start has no effect when the load increases rapidly. A few IC control circuits have volt-second limiting capability, but the vast majority do not. The soft saturation characteristic of power ferrite material may be forgiving enough to allow the core to saturate, with the absolute current limit providing protection, but with sharp-saturation core materials, this is a likely disaster. If all else fails, the normal flux swing must be reduced to the point where the abnormal flux swing does not reach saturation.

Restrictions on Number of Turns

Choices regarding the number of turns and turns ratios are often severely limited by low voltage secondaries. For a 5 Volt output the alternatives might be a 1-turn or a 2-turn secondary–a 2 to 1 step in the number of turns in every winding. For the same size core and window, this doubles the current density in the windings and accordingly increases the loss.

Choices may be further restricted when there are multiple low voltage secondaries. For example, a 2.5 to 1 turns ratio may be desirable between a 12 Volt and a 5 Volt output. This is easily accomplished with a 2-turn 5V secondary and a 5-turn 12V winding. But if the 5V secondary has only 1 turn, the only choice for the 12V secondary is 3 turns, which may result in excessive linear post-regulator loss. This problem could be handled by the use of fractional turns -- see reference (R6).

There are no hard and fast rules to follow in establishing the optimum turns for each winding, but there is some general guidance. First, define the ideal turns *ratios* between windings that will achieve the desired output voltages with the normal VIND established earlier. Later, when a specific core has been tentatively selected, the turns ratios will translate into specific turns, but these are not likely to be the integral numbers required in practice. It then becomes a juggling act, testing several approaches, before reaching the best compromise with integral turns. The lowest voltage secondary usually dominates this process, because with small numbers the jumps between integral turns are a larger percentage. Especially if the lowest voltage output has the greatest load power, which is often the case, the lowest voltage secondary is rounded up or down to the nearest integral. Rounding down will increase core loss, rounding up will increase winding loss. If the increased loss is unacceptable, a different core must be used that will require less adjustment to reach an integral number of turns. The low voltage output is usually regulated by the main control loop.

Higher voltage secondaries can be rounded up to the next integral with less difficulty because they have more turns. However, it is unlikely that accuracy or load regulation will be acceptable, requiring linear or switched post-regulation.

Since the primary is usually higher voltage, the primary turns can usually be set to achieve the desired turns ratio without difficulty.

Once the turns have been established, the initial calculations must be redefined.

Flux Walking

Faraday's Law states that the flux through a winding is equal to the integral volt-seconds per turn. This requires that the voltage across any winding of any magnetic device must average zero over a period of time. The smallest dc voltage component in an applied ac waveform will slowly but inevitably "walk" the flux into saturation.

In a low frequency mains transformer, the resistance of the primary winding is usually sufficient to control this problem. As a small dc voltage component pushes the flux slowly toward saturation, the magnetizing current becomes asymmetrical. The increasing dc component of the magnetizing current causes an IR drop in the winding which eventually cancels the dc voltage component of the drive waveform, hopefully well short of saturation.

In a high frequency switchmode power supply, a push-pull driver will theoretically apply equal and opposite volt-seconds to the windings during alternate switching periods, thus "resetting" the core (bringing the flux and the magnetizing current back to its starting point). But there are usually small volt-second asymmetries in the driving waveform due to inequalities in MOSFET R_{DSon} or switching speeds. The resulting small dc component will cause the flux to "walk". The high frequency transformer, with relatively few primary turns, has extremely low dc resistance, and the IR drop from the dc magnetizing current component is usually not sufficient to cancel the volt-second asymmetry until the core reaches saturation.

Flux walking is not a problem with the forward converter. When the switch turns off, the transformer magnetizing current causes the voltage to backswing, usually into a clamp. The reverse voltage causes the magnetizing current to decrease back to zero, from whence it started. The reverse volt-seconds will exactly equal the volt-seconds when the switch was ON. Thus the forward converter automatically resets itself (assuming sufficient reset time is allowed, by limiting the maximum duty cycle).

The flux walking problem is a serious concern with any push-pull topology (bridge, half-bridge or push-pull CT), when using voltage mode control..

One solution is to put a *small* gap in series with the core. This will raise the magnetizing current so that the IR drop in the circuit resistances will be able to offset the dc asymmetry in the drive waveform. But the increased magnetizing current represents increased energy in the mutual inductance which usually ends up in a snubber or clamp, increasing circuit losses.

A more elegant solution to the asymmetry problem is an automatic benefit of using current mode control (peak or average CMC). As the dc flux starts to walk in one direction due to volt-second drive asymmetry, the peak magnetizing current becomes progressively asymmetrical in alternate switching periods. However, current mode control senses current and turns off the switches at the same peak current level in each switching period, so that ON times are alternately lengthened and shortened. The initial volt-second asymmetry is thereby corrected, peak magnetizing currents are approximately equal in both directions, and flux walking is minimized.

However, with the half-bridge topology this creates a new problem. When current mode control corrects the volt-second inequality by shortening and lengthening alternate pulse widths, an ampere-second (charge) inequality is created in alternate switching periods. This is of no consequence in full bridge or push-pull center-tap circuits, but in the half-bridge, the charge inequality causes the capacitor divider voltage to walk toward the positive or negative rail. As the capacitor divider voltage moves away from the mid-point, the volt-second unbalance is made worse, resulting in further pulse width correction by the current mode control. A runaway situation exists, and the voltage will walk (or run) to one of the rails. This problem is corrected by adding a pair of diodes and a low-power winding to the transformer, as detailed in the Unitrode Applications Handbook.

Core Selection: Material

Select a core material appropriate for the desired *transformer* frequency.

With power ferrites, higher frequency materials have higher resistivity, hence lower eddy current losses. However, the permeability is generally lower, resulting in greater magnetizing current, which must be dealt with in snubbers and clamps.

With metal alloy cores, the higher frequency materials have higher resistivity and require very thin laminations. Although saturation flux density is usually very much greater than with ferrite materials, this is usually irrelevant because flux swing is severely limited by eddy current losses.

Ferrite is the best choice in transformer applications except for mechanical ruggedness.

Core Selection: Shape

The window configuration is extremely important. The window should be as wide as possible to maximize winding breadth and minimize the number of layers. This results in minimized Rac and leakage inductance. Also, with a wide window, the fixed creepage allowance dimension has less impact. With a wider window, less winding height is required, and the window area can be better utilized.

Pot cores and PQ cores have small window area in relation to core size, and the window shape is almost square. The creepage allowance wastes a large fraction of the window area, and the winding breadth is far from optimum. These cores are not as well suited for high frequency SMPS applications. One advantage of pot cores and PQ cores is that they provide better magnetic shielding than E-E cores, reducing EMI propagation.

EC, ETD, LP cores are all E-E core shapes. They have large window area in relation to core size, and the window has the desirable wide configuration.

Toroidal cores, properly wound, must have all windings distributed uniformly around the entire core. Thus the winding breadth is essentially the circumference of the core, resulting in the lowest possible leakage inductance and minimizing the number of winding layers. There is no creepage allowance because there is no end to the windings. (But there is a problem bringing the leads out.) Stray magnetic flux and EMI propagation are also very low.

The big problem with toroidal cores is the winding difficulty, especially with the shapes and gauge of conductors used in SMPS transformers. How can a 1-turn secondary be spread around the entire toroid? Automatic winding is virtually impossible. For this reason, toroidal shapes are seldom used in SMPS transformers.

Planar cores with their low profile are becoming more popular as SMPS frequencies progressively increase. Planar cores introduce a new set of unique problems which are beyond the scope of this discussion. Be assured that Faraday's and Ampere's Laws still apply, but in a planar core, flux density and field intensity change considerably throughout the important regions, making calculation much more difficult.

Core Selection: Size

A novice in the art of transformer design usually needs some guidance in making an initial estimate of the core size appropriate for the application requirements. One widely used method, with many variations, is based on the core Area Product, obtained by multiplying the core magnetic cross-section area by the window area available for the winding.

There are many variables involved in estimating the appropriate core size. Core power handling capability does not scale linearly with area product or with core volume. A larger transformer must operate at a lower power density because heat dissipating surface area increases less than heat-producing volume. The thermal environment is difficult to evaluate accurately, whether by forced air or natural convection.

Some core manufacturers no longer provide area product information on their data sheets, often substituting their own methodology to make an initial core size choice for various applications.

The following formula provides a crude indication of the area product required:

$$AP = A_W A_E = \left(\frac{P_O}{K \, \Delta B \, f_T} \right)^{4/3} \quad cm^{\cdot}$$

where:

P_O	= Power Output
ΔB	= Flux density swing, Tesla
f_T	= *Transformer* operating frequency
K	= .014 (Forward converter, PPCT)
	= .017 (Bridge, half bridge)

This formula is based on current density of $420 A/cm^2$ in the windings, and assumes a window utilization of 40% copper. At low frequencies, the flux swing is limited by saturation, but above 50kHz (ferrite), ΔB is usually limited by core losses. Use the ΔB value that results in a core loss of $100 mW/cm^3$ (2 times the "flux density" given in the core loss curves).

These initial estimates of core size are not very accurate, but they do reduce the number of trial solutions that might otherwise be required. In the final analysis, the validity of the design should be checked with a prototype transformer operated in the circuit and the environment of the application, with the hot spot temperature rise measured by means of a thermocouple cemented to the center of the centerpost.

Transformer Design Cookbook

The steps for designing a power transformer for SwitchMode Power Supplies is outlined below. A typical example is carried through to illustrate the process. There are many approaches to transformer design. The approach presented here appears the most logical and straightforward to the author.

It may be worthwhile to use software such as "Magnetic Designer" from Intusoft[2] for the initial design, using the approach defined herein for verification and tune-up. The author has not evaluated "Magnetic Designer" sufficiently to make an unqualified endorsement, but it should certainly make a good starting point and take a great deal of drudgery out of the process. It has the advantage of including an extensive core database.

Initial Preparation

The first few steps in this process define application parameters that should not change, regardless of subsequent iterations in the selection of a specific core type and size.

If the results are not acceptable, start over from the very beginning, if that seems appropriate. Great difficulty in achieving an acceptable forward converter transformer design may be a subtle message that a half-bridge topology is perhaps a better choice.

Step 1. Define the power supply parameters pertaining to the transformer design:

V_{IN} Range:	100 - 190 V
Output 1:	5 V, 50 A
Output 2:	none
Circuit Topology:	Forward Converter
Switching Freq, f_s:	200 kHz
Transformer Freq, f_T:	200 kHz
Max Loss (absolute):	2.5 W
Max °C Rise:	40°C
Cooling Method:	Natural Convection

Step 2. Define absolute duty cycle limit Dlim, tentative normal Dmax at low V_{IN} (to provide headroom for dynamic response), and normal $V_{IN}D$:

Absolute Limit, Dlim:	0.47
Normal Dmax:	0.42
Normal $V_{IN} \cdot D$:	$V_{IN}min \cdot Dmax = 42$ V

VINmaxDlim: 89.3 V

Step 3. Calculate output voltages plus diode and secondary IR drops at full load:

Vo1':	5.0 + 0.4 = 5.4 Volts
Vo2':	n/a

Step 4. Calculate desired turns ratios: P-S1; S1-S2, etc. Remember that choices with low voltage secondaries will probably be limited.

$n = N_P/N_{S1} = V_{IN}D/Vo1'$: 42/5.4 = 7.8
Possible choices: 8:1 ; 7:1 ; 15:2

Core Selection

Step 5: Tentatively select core material, shape and tentative size, using guidance from the manufacturer's data sheet or using the area product formula given previously in this paper. Will a bobbin be used?:

Core Material: Ferrite, Magnetics Type P
Core type, Family: ETD
Core Size: 34mm -- ETD34

Step 6: For the specific core selected, note:
Effective core Area, Volume, Path Length. (cm)

A_e:	0.97 cm^2
V_e:	7.64 cm^3
ℓ_e:	7.9 cm

Window Area, Breadth, Height, Mean Length per Turn (' indicates net with bobbin, creepage).

A_w / A_w': 1.89 / 1.23 cm^2
bw / bw': 2.36 / 1.5 cm
hw / hw': 0.775 / 0.6 cm
MLT: 5.8 / 6.1 cm

Define R_T and Loss Limit

Step 7: Obtain thermal resistance from data sheet or calculate from window area (not bobbin area) from formula for EC and ETD series:

$$R_E = \frac{800}{22 \cdot A_W \, in \, cm^2} = \frac{36}{1.89} = 19 \text{ °C/Watt}$$

Calculate loss limit based on max. temperature rise:

$$P_{lim} = {}^{\circ}C_{rise}/R_T: \qquad = 40/19 = 2.1 \text{ Watts}$$

The 2.1W limit applies, since it is less than the absolute limit from Step 1. Tentatively apportion half to core loss, half to winding loss.

     PClim: 1 Watt
     Pwlim: 1.1 Watt

Step 8: Loss Limited Flux Swing

Calculate max. core loss per cm^3
     PClim/Ve = 1/7.64 = 131 mw/cm^3 (= kW/m^3)

Using this core loss value, enter the core loss curve for the P material selected. At the *transformer* frequency, find "flux density" (actually peak flux density). Double it to obtain the loss-limited peak-peak flux density swing, ΔB:

At 131 mw/cm^3 and 200kHz:
$\Delta B = 2 \cdot 800$ Gauss = 1600G = 0.16 Tesla
Normal $\Delta\phi = \Delta B \cdot A_e$

Step 9: Using Faraday's Law, calculate the number of secondary turns:

$$\int E_{S1}\, dt = Vpk_{S1}t_{ON} = V_{O1}' \cdot T_S$$

$$N_{S1} = \int E_{S1}dt/\Delta\phi = V_{O1}' \cdot T_S /\Delta\phi$$

$$N_{S1} = \frac{V_{O1}' T_S}{\Delta B \times A_E} = \frac{5.4 \times 5 \times 10^{-6}}{.16 \times .97 \times 10^{-4}} = 1.74 \text{ Turns}$$

Rounding down to 1 turn will greatly increase the volts/turn, flux swing and core losses. Rounding up to 2 turns reduces core losses but increases winding loss. Since the result above is much closer to 2 turns, this will be adopted.

Step 10: Recalculate flux swing and core loss at 2 turns:

$$\Delta B(2 \text{ turns}) = 0.16T\frac{1.74 \text{turns}}{2 \text{ turns}} = 0.14 \text{Tesla}$$

From the core loss curves, loss at 0.14T/2 (700 Gauss) is 110mw/cm^3 x 7.64cm^3

Core loss = 0.84 W

Step 11: Finalize the choice of primary turns. A larger turns ratio results in lower peak current, larger D (less reserve), and more copper loss. From the possibilities defined in Step 4, trial solutions show the best choice to be NP = 15 turns (7.5:1 turns ratio).

Recalculate normal VIND and flux swing under worst case VINmaxDlim conditions:

$$V_{IND} = nV_O' = 7.5 \cdot 5.4 = 40.5 \text{ V}$$

$$\Delta B_{lim} = 0.14T \cdot 89.3/40.5 = 0.31T \text{ -- OK}$$

Step 12: Define the winding structure.

An interleaved structure will be used, as shown in Figure 4-1, to minimize leakage inductance and winding losses.
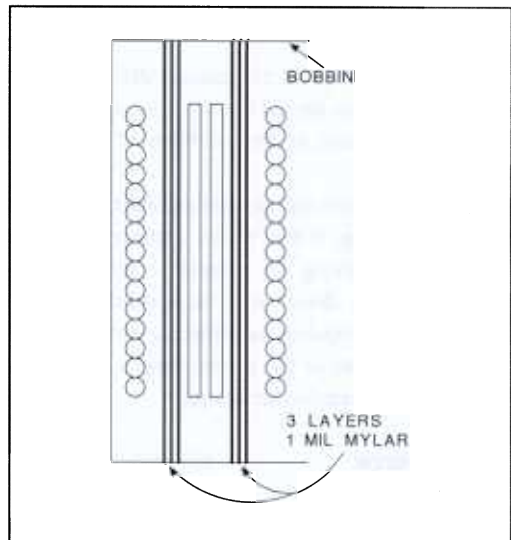

Figure 4-1

The interleaved structure results in two winding sections. Primary windings of 15 turns in each section are connected in parallel. Primary current divides equally in the two paralleled windings because this results in the lowest energy transfer. Secondary windings of 1 turn copper foil in each section are connected in series, resulting in a 2-turn secondary. With only one turn in each section, the secondary windings can be much thicker than DPEN to minimize dc resistance without increasing the ac resistance.

Step 12: Calculate DPEN at 200 kHz:

$$Dpen = 7.6/\sqrt{f} = 7.6/\sqrt{200,000} = .017 \text{ cm}$$

Step 13: Calculate dc and rms ac currents in each winding at VINmin and Dmax. (Ref. Section 3):

$$Isdc = 50A \cdot Dmax = 50 \cdot 0.405 = 20.25A$$

$$Isac = Isdc((1-D)/D)^{1/2} = 24.5A$$

$$Ipdc = Isdc/n = 20.25/7.5 = 2.7A$$

$$Ipac = Isac/n = 24.5/7.5 = 3.27A$$

Primary current in each of the two paralleled sections is one-half the total primary current: 1.35Adc and 1.65Aac.

Step 14: Define the primary winding:

One layer of 15 turns spread across the available winding breadth of 1.3cm allows a maximum insulated wire diameter of 0.87mm. AWG 21 – 0.72mm copper will be used.

From Ref R2, pg 9, the effective layer thickness equals $0.83 \cdot dia(dia/spacing)^{1/2}$.

$$Q = (\text{layer thickness})/DPEN$$
$$Q = 0.83 \cdot .072(.072/.087)^{1/2}/.017 = 3.19$$

From Dowell's curves, Rac/Rdc for 1 layer is 3.1. This will result in unacceptable ac losses.

A Litz wire consisting of 100 strands #42 wire has a diameter of 0.81mm and a resistance of 0.545mΩ/cm.

The dc resistance of the single layer is:

$$Rdc = \Omega/cm \cdot MLT \cdot Ns = .00055 \cdot 6.1 \cdot 15 = .05\Omega$$

Multiplying by $(1.35Adc)^2$, dc power loss is .091W in each section, for a total primary dc loss of 0.18W.

The diameter of each #42 wire is .064mm, but there are effectively ten layers of fine wire in the single layer of Litz wire. This is because the 100 strands are roughly equivalent to a 10 x 10 array, thus ten

wires deep. Q is approximately 1/10 the value for solid wire, or 0.3, resulting in Rac/Rdc of 1.2. Thus, Rac = Rdc•1.2, or .06Ω.

Multiplying by 1.65A squared, the ac loss is 0.16W in each section, for a total primary ac loss of 0.32W. Adding the 0.18W dc loss,

Total primary power loss = 0.5 Watts.

Step 15: Define the secondary winding.

The secondary consists of two turns (two layers) of copper strip or foil, 1.3cm wide (full available winding breadth), and 0.13cm thick. There is one secondary layer in each of the two sections of the interleaved winding structure. This permits the thickness of the copper strip to be much greater than DPEN to minimize dc losses, without increasing ac losses. This is because ac current flows only on the outer side of each turn. As the conductor is made thicker, Rac/Rdc becomes larger, but Rdc decreases and Rac remains the same.

With a solid copper secondary, the layer thickness is the same as the conductor thickness, 0.1cm.

$$Q = \text{Layer thickness}/DPEN = 0.13/.017 = 7.6$$
$$Rac/Rdc = 7.5$$

This will be acceptable because the dc resistance is very low.

$$Rdc = \rho \cdot MLT \cdot Ns/(bw'h)$$
$$Rdc = 2.3 \cdot 10^{-6} \cdot 6.1 \cdot 2/(1.3 \cdot 0.13) = 166\mu\Omega$$
$$Pdc = 166\mu\Omega \cdot 20.25^2 = .068 \text{ W}$$
$$Pac = Rdc \cdot Rac/Rdc \cdot Iac^2 = 166\mu\Omega \cdot 7.5 \cdot 24.5^2$$
$$Pac = 0.75 \text{ W}$$

Total secondary loss:
$$.068W + 0.75W = 0.82 \text{ W}$$
Total copper loss:
$$0.82W + 0.5W = 1.32 \text{ W}$$
Total core plus copper loss:

$$0.84W + 1.32W = 2.16 \text{ Watts}$$

Thus, the total power loss is under the absolute limit of 2.5Watts, but slightly over the 2.1 Watt limit based on the desired max. temperature rise of 40°C.

References:

(R2)   "Eddy Current Losses in Transformer Windings and Circuit Wiring," *Unitrode Seminar Manual SEM600*, 1988 (reprinted in the Reference Section at the back of this Manual)

(R4)   "The Effects of Leakage Inductance on Switching Power Supply Performance," *Unitrode Seminar Manual SEM100*, 1982 (reprinted in the Reference Section at the back of this Manual)

(R6)   "How to Design a Transformer with Fractional Turns," *Unitrode Seminar Manual SEM500*, 1987 (reprinted in the Reference Section at the back of this Manual)

(1)   PROXY -- Proximity effect analysis, KO Systems, Chatsworth, CA, 818-341-3864

(2)   "Magnetics Designer," Magnetics design software, IntuSoft, San Pedro, CA 310-833-0710

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