PWM CONTROL IC WITH SCP/DTC FUNCTION

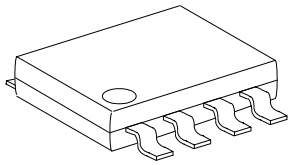
GENERAL DESCRIPTION

The FP5001, a 1-chip composed of open collector transistor output pulse-width-modulation control circuits with an error amplifier and dead-time comparators (DTC), the FP5001 contains a 1.0V precision voltage reference regulator, under-voltage lockout circuit (UVLO), short circuit protection circuit (SCP), applied to offer space and low cost in many applications such as the DC/DC converter and backlight inverter.

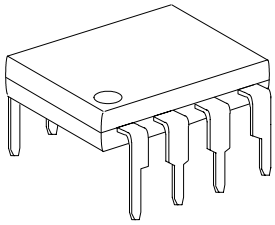
Using few external components, FP5001, a high performance integrated IC, is designed for a control circuit. The circuit diagram of the typical application example is as below.

FEATURES

- Reference Voltage Precision: 5% (FP5001)
- Output sink current up to 100mA
- Low quiescent supply current
- Wide operating voltage range: 3.6~40V
- Variable dead-time control (DTC)
- UVLO protection function
- SCP protection function
- Oscillator Frequency: Max. 500KHz
- Package: PDIP8/ SOP8

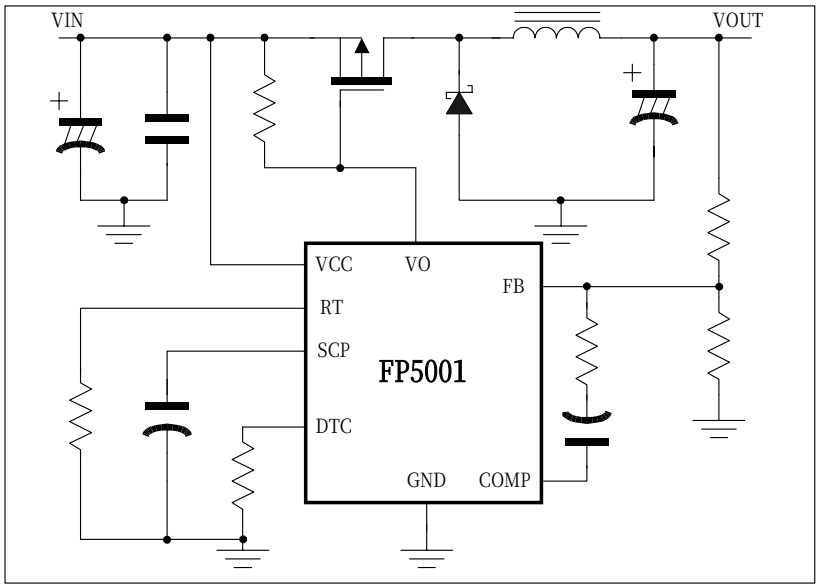


SOP8

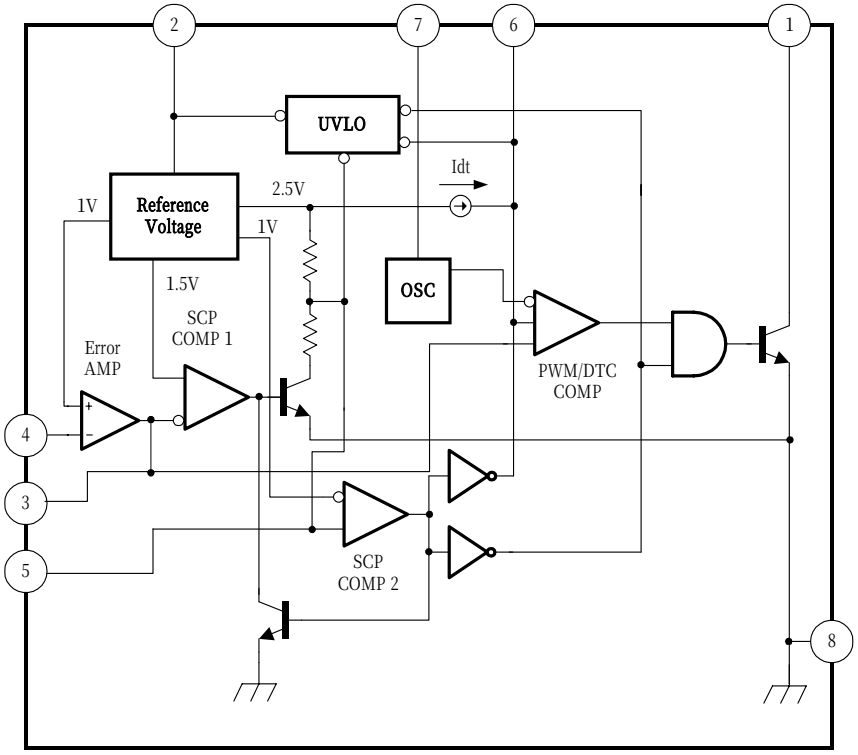


PDIP8

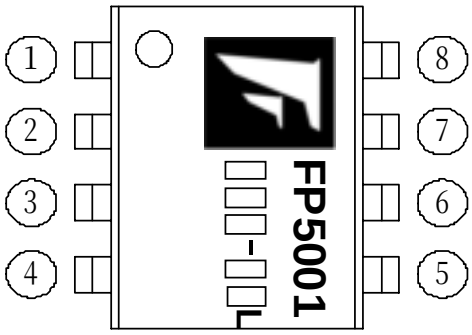
TYPICAL APPLICATION CIRCUIT



FUNCTIONAL BLOCK DIAGRAM



MARK VIEW



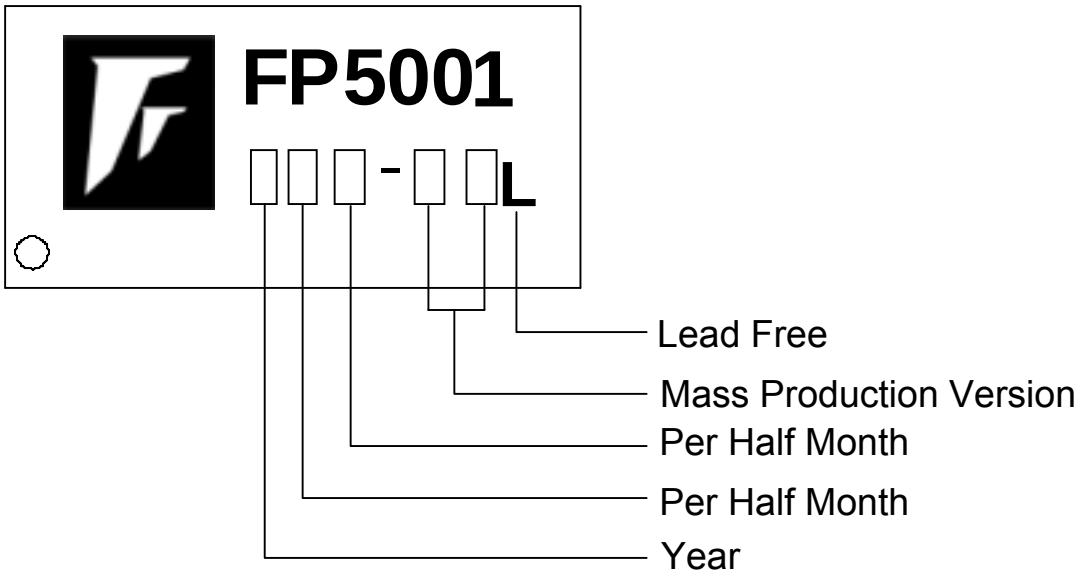
PIN DESCRIPTION

NAME	NO.	STATUS	DESCRIPTION
OUT	1	O	Open Collector Transistor Output
VCC	2	P	IC Power Supply
COMP	3	O	Error Amplifier Feedback Output
FB	4	I	Error Amplifier Inverting Input
SCP	5	I	Short Circuit Protection Input
DTC	6	I	Dead-Time Control Input
RT	7	I	A resistance of Oscillator
GND	8	P	IC Ground

ORDER INFORMATION

Part Number	Operating Temperature	Package	Description
FP5001D-LF	-20°C 85°C	SOP8	Tube
FP5001DR-LF	-20°C 85°C	SOP8	Tape & Reel
FP5001P-LF	-20°C 85°C	PDIP8	Tube (1%)

IC DATE CODE DISTINGUISH

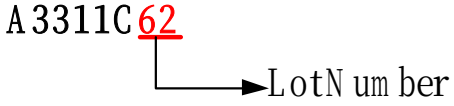


FOR EXAMPLE:

January A (Front Half Month), B (Last Half Month)
February C, D
March E, F ----------And so on.

Lot Number is the last two numbers

For Example:



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Vcc) ---------- +40V

Differential Input Voltage (V_{id}) ---------- +20V

Collector Output Voltage (Vo) ---------- +40V

Collector Output Current (Io) ---------- +150mA

Maximum Junction Temperature (T_j) ---------- +150°C

Thermal Resistance Junction to Ambient (SOP package)---------- 175°C/W

(PDIP package)---------- 100°C/W

Power Dissipation (SOP8 package)

Ta=25°C ---------- 650mW

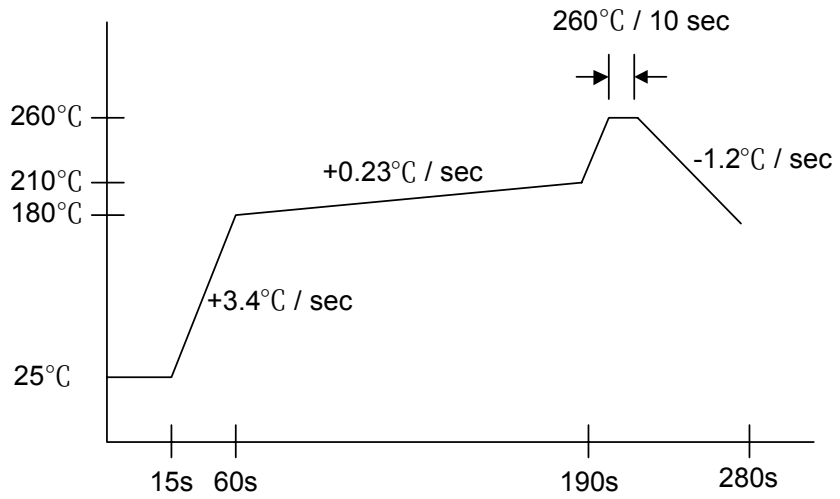
Ta=70°C ---------- 550mW

Operating Temperature Range ---------- -20°C 85°C

Storage Temperature Range ---------- -65°C 150°C

SOP8 Lead Temperature (soldering, 10 sec) ---------- +260°C

PDIP8 Lead Temperature (soldering, 20 sec) ---------- +260°C



DC ELECTRICAL CHARACTERISTICS

Electrical characteristics over recommended operating temperature range，VCC＝6V，fosc＝70KHz（unless otherwise noted）

Reference

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	V_{REF}	COMP connected to FB	0.95	1	1.05	V
Input regulation	$\triangle V_{REF}$	V_{CC}＝3.6 V to 40 V		2	12.5	mV
Output voltage change with temperature	$\triangle V_{REF}$ /V_{REF}	T_A＝-20℃ to 25℃	-10	-1	15	mV/V
		T_A＝ 25℃ to 85℃	-10	-2	10	

†All typical values are at T_A＝25℃.

Under voltage lockout

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Upper threshold voltage	V_{upper}	T_A＝25℃		3		V
Lower threshold voltage	V_{low}	T_A＝25℃		2.8		V
Hysteresis	V_{hys}	T_A＝25℃	100	200		mV
Reset threshold voltage	V_{reset}	T_A＝25℃	2.1	2.55		V

†All typical values are at T_A＝25℃.

Short-circuit protection

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCP threshold voltage	V_{TH}	T_A＝25℃	0.95	1.00	1.05	V
SCP voltage，latched	V_{LATCH}	No pullup		2.4		V
SCP voltage，UVLO operation	V_{OPR}		140	185	230	mV
SCP voltage，UVLO standby	$V_{STANDBY}$	No pullup		60	120	mV
Input source current	I_{SOURCR}	T_A＝25℃	-10	-15	-20	μA
SCP comparator 1 threshold voltage	$V_{COMP(TH)}$			1.5		V

†All typical values are at T_A＝25℃.

Oscillator

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency	f	R_t＝100K		70		KHz
Standard deviation of frequency	△f			15		KHz
Frequency change with voltage	△f/△V	V_{CC}＝3.6V to 40V		1		KHz
Frequency change with temperature	△f/△T	T_A＝-20℃ to 25℃	-4	-0.4	4	KHz
		T_A＝ 25℃ to 85℃	-4	-0.2	4	KHz
Voltage at RT	V_{RT}			1		V

†All typical values are at T_A＝25℃.

DC ELECTRICAL CHARACTERISTICS (Cont.)

Electrical characteristics over recommended operating temperature range，VCC＝6V，fosc＝70KHz（unless otherwise noted）（continued）

Dead-time control

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output（source）current	I_{SOURCE}	$V_{(DT)}$＝1.5V	0.9×I_{RT}‡		1.2×I_{RT}	μA
Input threshold voltage	V_{TH}	Duty cycle＝0%	0.5	0.7		V
		Duty cycle＝100%		1.3	1.5	

†All typical values are at T_A＝25°C.

‡Output source current at RT

Error amplifier

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage		V_{IN}	V_{CC}＝3.6V to 40V	0		1.5	V
Input bias current		V_{BIAS}			-160	-500	nA
Output voltage swing	Positive	V_{POS}		1.5	2.3		V
	Negative	V_{NEG}			0.3	0.4	V
Open-loop voltage amplification		A_{VO}			80		dB
Unity-gain bandwidth		BW_U			1.5		MHz
Output（sink）current		I_{SINK}	$V_{I(FB)}$＝1.2V，COMP＝1V	600	1100		μA
Output（source）current		I_{SOURCE}	$V_{I(FB)}$＝0.8V，COMP＝1V	-45	-70		μA

†All typical values are at T_A＝25°C.

Output

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output saturation voltage	V_{SAT}	I_O＝10mA		0.8	1.2	V
Off-state current	I_{OFF}	V_O＝40V， V_{CC}＝0			10	μA
		V_O＝40V			10	
Short-circuit output current	I_{SC}	V_O＝6V		40		mA

†All typical values are at T_A＝25°C.

Total device

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Standby supply current	Off state	$I_{STANDBY}$			1	1.5	mA
Average supply current		I_{AVE}	R_t＝100k		1.2	1.5	mA

†All typical values are at T_A＝25°C.

DETAILED DESCRIPTION

Voltage reference

A 2.5-V regulator operating from VCC is used to power the internal circuitry of the FP5001.

A resistive divider provides 1-V reference for the error amplifier and SCP circuits.

Error amplifier

The error amplifier compares a sample of the dc-to-dc converter output voltage to the 1V reference and generates an error signal for the PWM comparator. The dc-to-dc converter output voltage is set by selecting the error-amplifier gain (see Figure 1), using the following expression:

$$Vo = (1 + R1/R2) \times (1\ V)$$

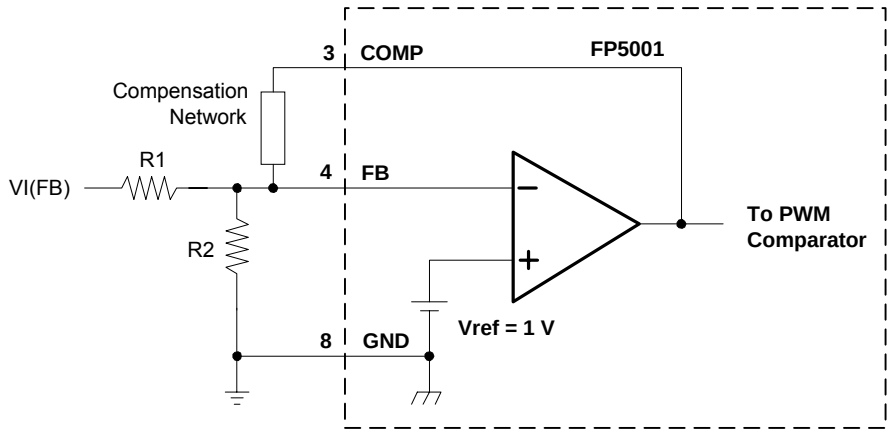


Figure 1. Error-Amplifier Gain Setting

The error-amplifier output is brought out as COMP for use in compensating the dc-to-dc converter control loop for stability. Because the amplifier can only source 45 uA, the total dc load resistance should be 100 kΩ or more.

Oscillator/PWM

The oscillator frequency (fosc) can be set between 20 kHz and 500 kHz by connecting a resistor between RT and GND. Acceptable resistor values range from 15 kΩ to 250 kΩ. The oscillator frequency can be determined by using the graph shown in Figure 5.

The oscillator output is a triangular wave with a minimum value of approximately 0.7 V and a maximum value of approximately 1.3 V. The PWM comparator compares the error-amplifier output voltage and the DTC input voltage to the triangular wave and turns the output transistor off whenever the triangular wave is greater than the lesser of the two inputs.

Dead-time control (DTC)

DTC provides a means of limiting the output-switch duty cycle to a value less than 100%, which is critical for boost and flyback converters. A current source generates a reference current (I_{DT}) at DTC that is nominally equal to the current at the oscillator timing terminal, RT. Connecting a resistor between DTC and GND generates a dead-time reference voltage (V_{DT}), which the PWM/DTC comparator compares to the oscillator triangle wave as described in the previous section. Nominally, the maximum duty cycle is 0% when V_{DT} is 0.7 V or less and 100% when V_{DT} is 1.3 V or greater. Because the triangle wave amplitude is a function of frequency and the source impedance of RT is relatively high (1250 Ω), choosing R_{DT} for a specific maximum duty cycle, D, is accomplished using the following equation and the voltage limits for the frequency in question as found in Figure 11 (V_{osc}max and V_{osc}min are the maximum and minimum oscillator levels):

$$R_{DT} = (R_t + 1250) [D (V_{osc}max - V_{osc}min) + V_{osc}min]$$

Where

R_{DT} and R_t are in ohms, D in decimal

Soft start can be implemented by paralleling the DTC resistor with a capacitor (C_{DT}) as shown in Figure 2. During soft start, the voltage at DTC is derived by the following equation:

$$V_{DT} \approx I_{DT} R_{DT} \left(1 - e^{\left(- t / R_{DT} C_{DT} \right)} \right)$$

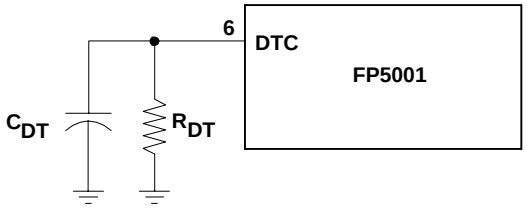


Figure 2. Soft-Start Circuit

If the dc-to-dc converter must be in regulation within a specified period of time, the time constant, $R_{DT}C_{DT}$, should be $t_0/3$ to $t_0/5$. The FP5001 remains off until $V_{DT} \approx 0.7$ V, the minimum ramp value. C_{DT} is discharged every time UVLO or SCP becomes active.

Undervoltage-lockout (UVLO) protection

The undervoltage-lockout circuit turns the output transistor off and resets the SCP latch whenever the supply voltage drops too low (approximately 3 V at 25°C) for proper operation. A hysteresis voltage of 200 mV eliminates false triggering on noise and chattering.

Short-circuit protection (SCP)

The FP5001 includes short-circuit protection (see Figure 3), which turns the power switch off to prevent damage when the converter output is shorted. When activated, the SCP prevents the switch from being turned on until the internal latching circuit is reset. The circuit is reset by reducing the input voltage until UVLO becomes active or until the SCP terminal is pulled to ground externally.

When a short circuit occurs, the error-amplifier output at COMP rises to increase the power-switch duty cycle in an attempt to maintain the output voltage. SCP comparator 1 starts an RC timing circuit when COMP exceeds 1.5V. If the short is removed and the error-amplifier output drops below 1.5V before time out, normal converter operation continues. If the fault is still present at the end of the time-out period, the timer sets the latching circuit and turns off the FP5001 output transistor.

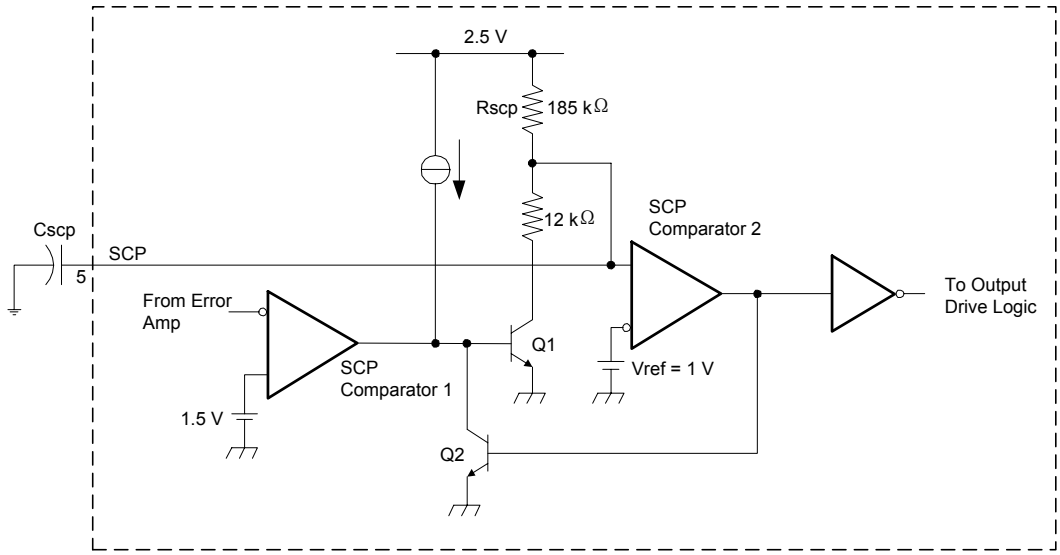


Figure 3. SCP Circuit

The timer operates by charging an external capacitor (C_{SCP}), connected between the SCP terminal and ground, towards 2.5V through a 185-kΩ resistor (R_{SCP}). The circuit begins charging from an initial voltage of approximately 185 mV and times out when the capacitor voltage reaches 1V. The output of SCP comparator 2 then goes high, turns on Q2, and latches the timer circuit. The expression for setting the SCP time period is derived from the following equation:

$$V_{SCP} = (2.5 + 0.185)(1 - e^{-t/\tau}) + 0.185$$

Where

$$\tau = R_{SCP}C_{SCP}$$

The end of the time-out period, t_{SCP}, occurs when V_{SCP} = 1 V. Solving for C_{SCP} yields:

$$C_{SCP} = 12.46 \times t_{SCP}$$ Where t is in seconds, C in μF.

t_{SCP} must be much longer (generally 10 to 15 times) than the converter start-up period or the converter will not start.

Output transistor

The output of the FP5001 is an open-collector transistor with a maximum collector current rating of 100mA and a voltage rating of 40V. The output is turned on under the following conditions: the oscillator triangle wave is lower than both the DTC voltage and the error-amplifier output voltage, the UVLO circuit is inactive, and the short-circuit protection circuit is inactive.

PARAMETER MEASUREMENT INFORMATION

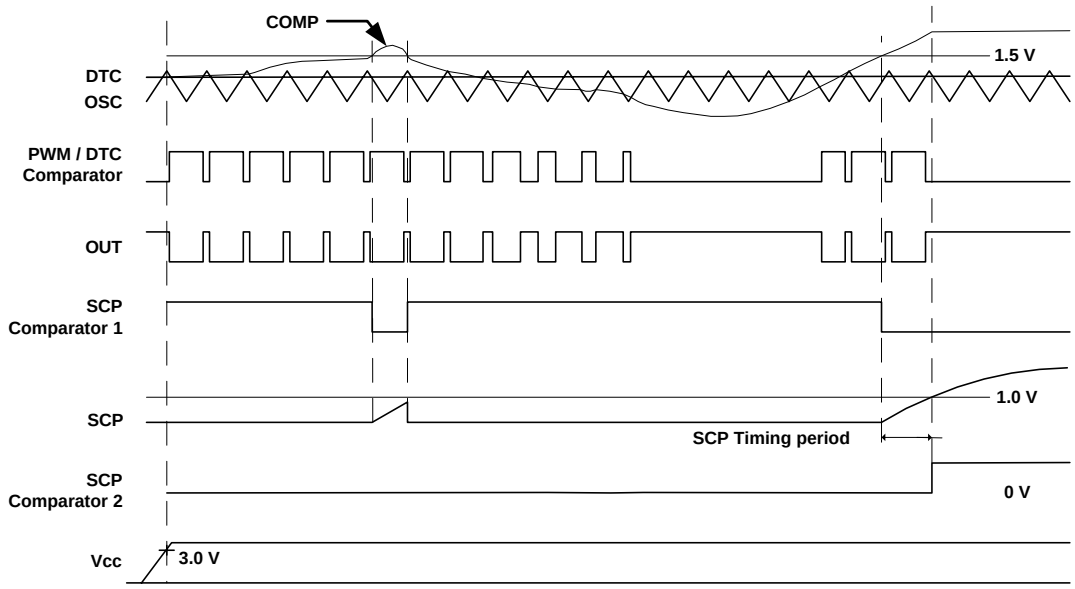


Figure 4. PWM Timing Diagram

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY
VS
TIMING RESISTANCE

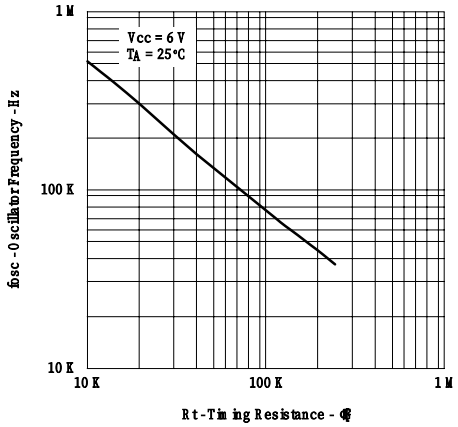


Figure 5

OSCILLATOR FREQUENCY
VS
AMBIENT TEMPERATURE

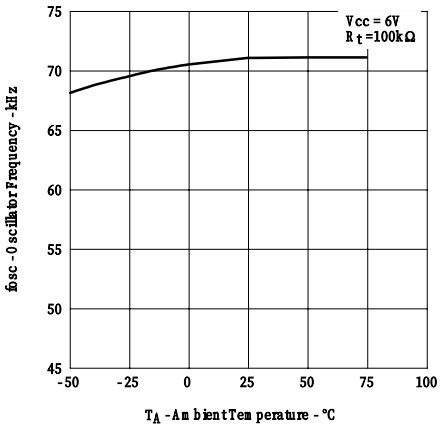


Figure 6

REFERENCE OUTPUT VOLTAGE
VS
POWER-SUPPLY VOLTAGE

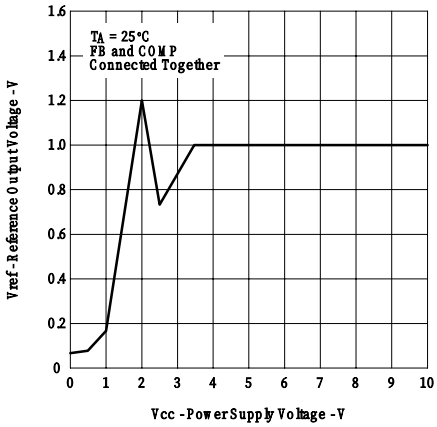


Figure 7

REFERENCE OUTPUT VOLTAGE FLUCTUATION
VS
AMBIENT TEMPERATURE

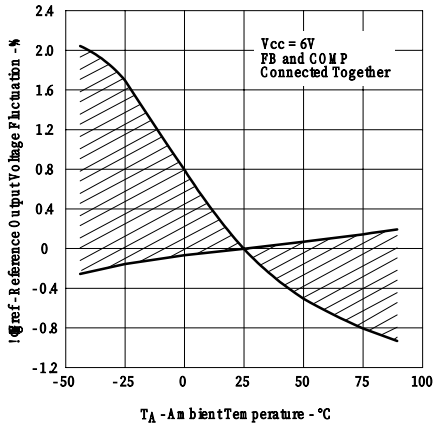


Figure 8

AVERAGE SUPPLY CURRENT
VS
POWER-SUPPLY VOLTAGE

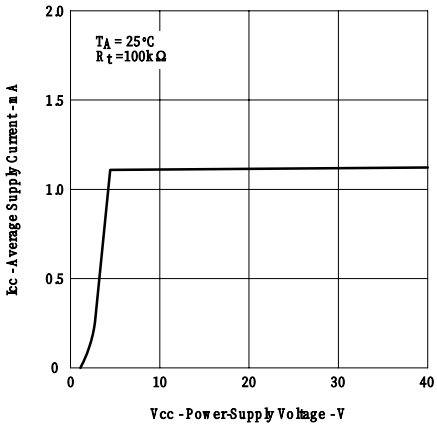


Figure 9

AVERAGE SUPPLY CURRENT
VS
AMBIENT TEMPERATURE

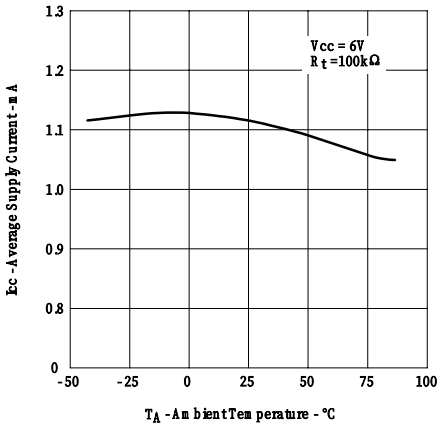


Figure 10

TYPICAL CHARACTERISTICS (Cont.)

PWM TRIANGLE WAVE AMPLITUDE VOLTAGE
VS
OSCILLATOR FREQUENCY

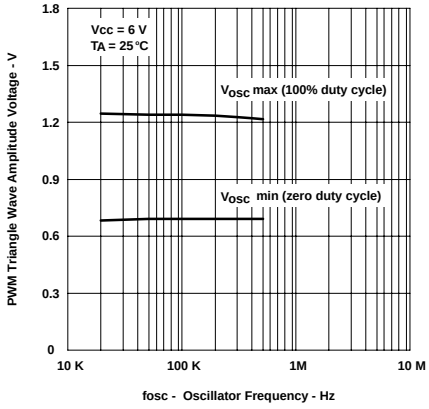


Figure 11

ERROR AMPLIFIER OUTPUT VOLTAGE
VS
OUTPUT (SINK) CURRENT

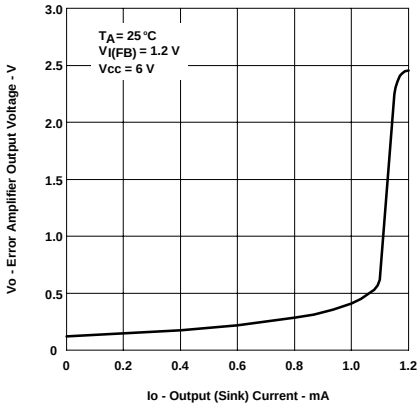


Figure 12

ERROR AMPLIFIER OUTPUT VOLTAGE
VS
OUTPUT (SOURCE) CURRENT

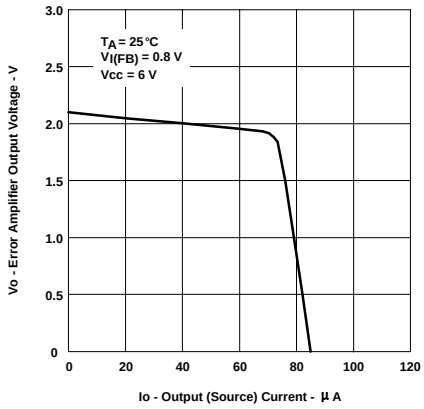


Figure 13

ERROR AMPLIFIER OUTPUT VOLTAGE
VS
AMBIENT TEMPERATURE

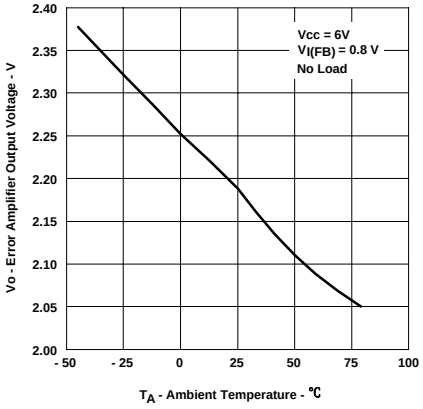


Figure 14

ERROR AMPLIFIER OUTPUT VOLTAGE
VS
AMBIENT TEMPERATURE

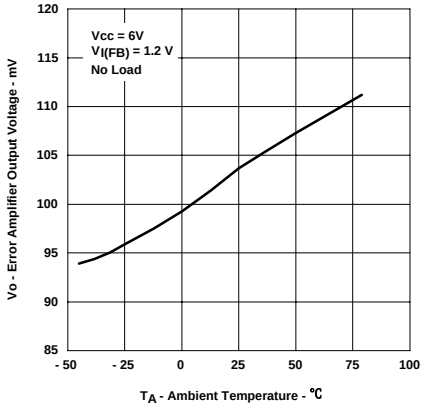


Figure 15

OUTPUT DUTY CYCLE
VS
DTC VOLTAGE

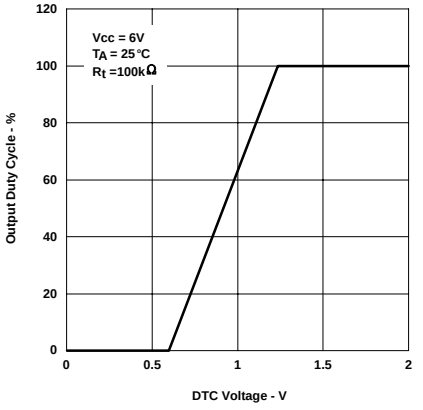


Figure 16

TYPICAL CHARACTERISTICS (Cont.)

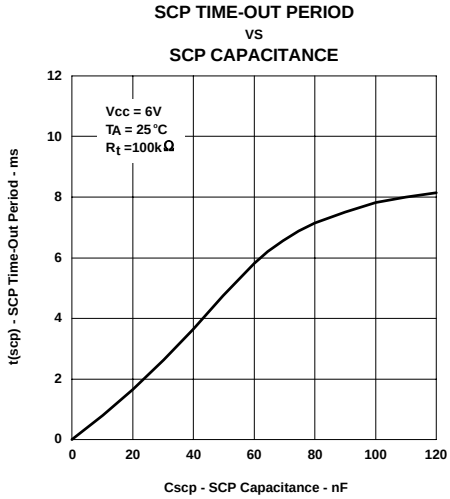


Figure 17

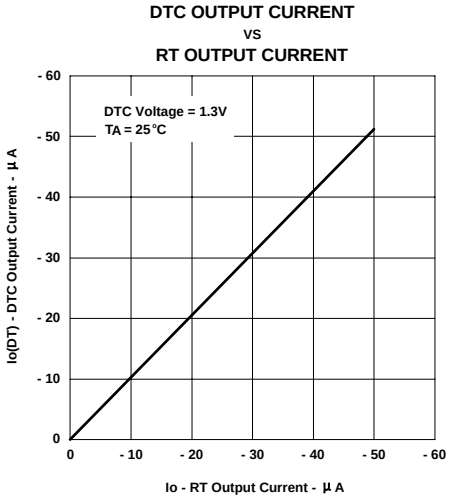


Figure 18

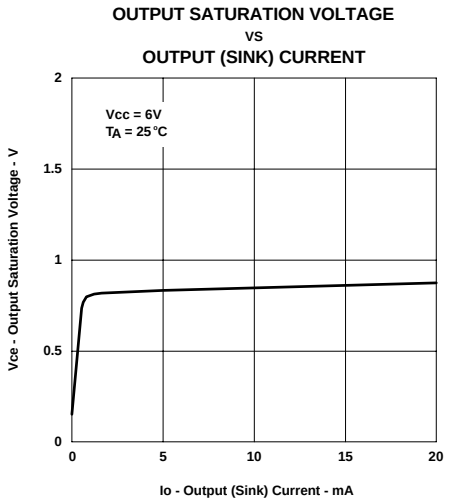
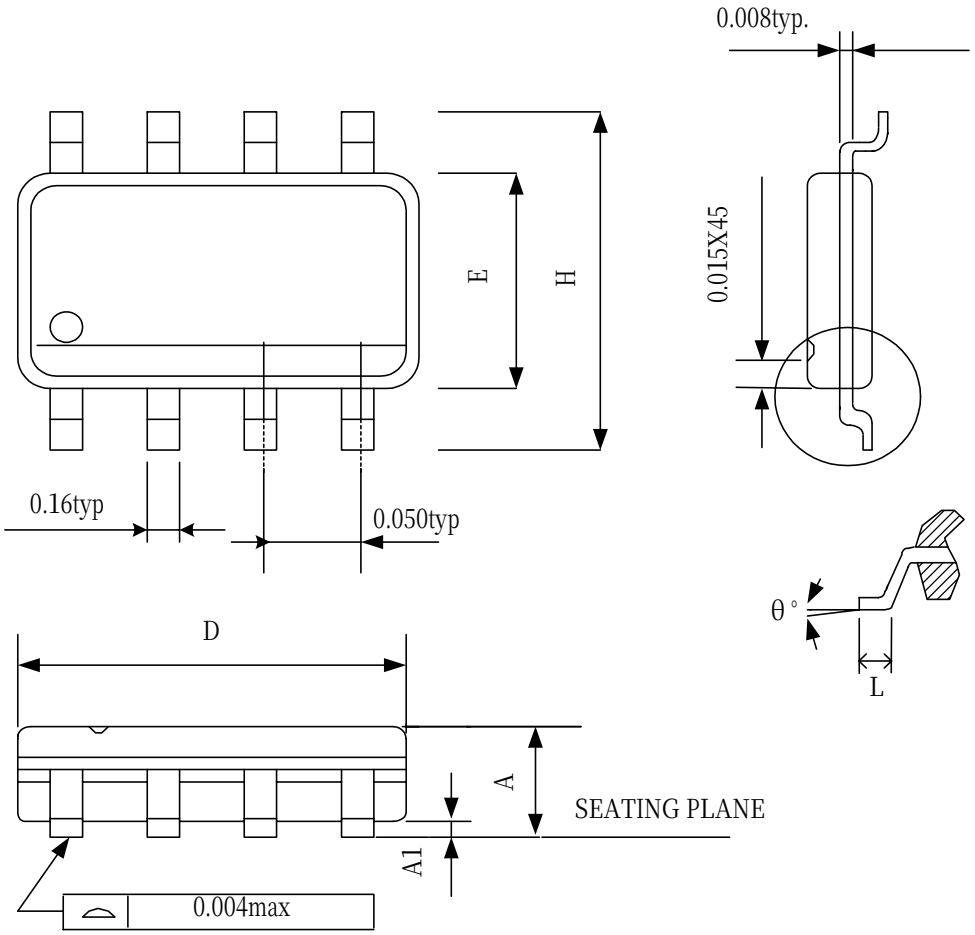


Figure 19

PACKAGE OUTLINE

SOP 8

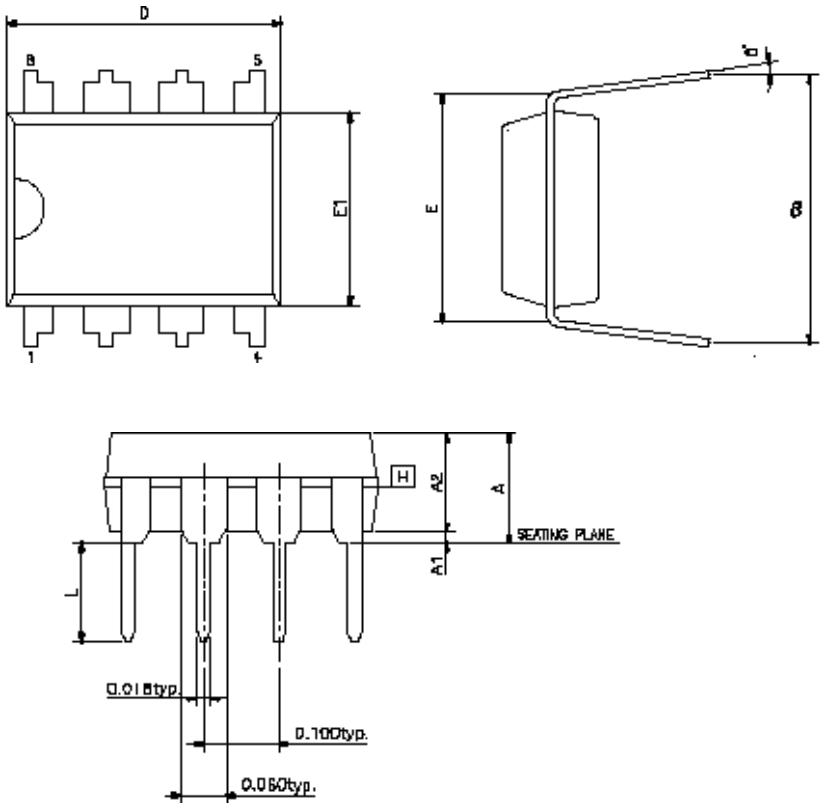


SYMBOLS	MIN	MAX
A	0.053	0.069
A1	0.004	0.010
D	0.189	0.196
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ °	0	8

NOTE:

1. JEDEC OUTLINE:MS-012 AA
2. DIMENSIONS “D” DOES NOT INCLUDE MOLD FLASH,PROTRUSIONS OR GATE BURRS.MOLD FLASH,PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.0.06in) PER SIDE
3. DIMENSIONS “E” DOES NOT INCLUDE INTER-LEAD FLASH,OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.0.10in) PER SIDE.

PDIP 8



SYMBOLS	MIN	NOR	MAX
A	-	-	0.210
A1	0.015	-	-
A2	0.125	0.130	0.135
D	0.355	0.365	0.400
E		0.300BSC	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e_Θ	0.335	0.355	0.375
Θ °	0	7	15

Note:

0. JEDEC OUTLINE:MS-001 BA

1. “D””E1”DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH

2. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED

3. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTIDN

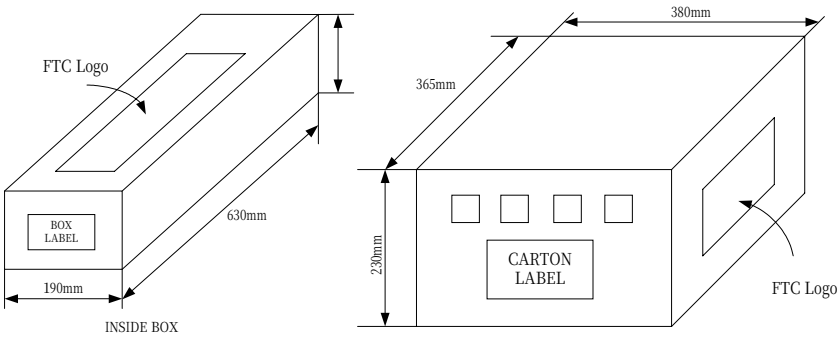
4. DISTANCE BETWEEN LEADSINCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MININUM

5. DATUM PLANE H CONINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

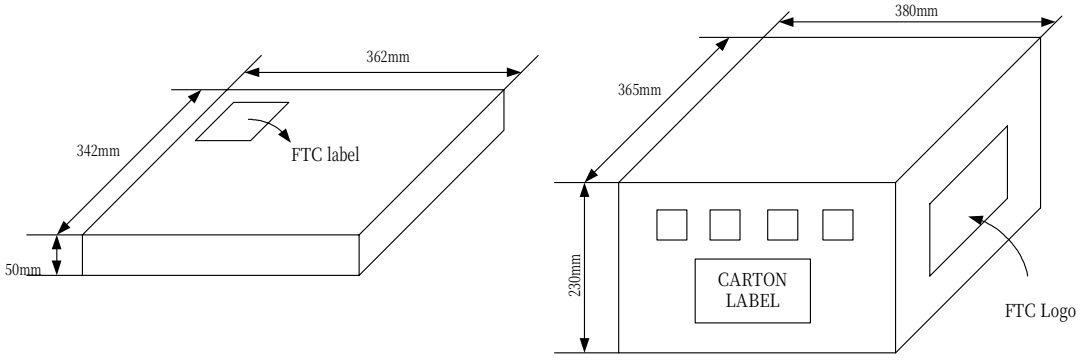
PACKING SPECIFICATIONS

BOX DIMENSION

TUBE INSIDE BOX AND CARTON



TAPE & REEL INSIDE BOX AND CARTON



PACKING QUANTITY SPECIFICATIONS

100 EA / TUBE	2500 EA / REEL
100 TUBES / INSIDE BOX	4 INSIDE BOXES / CARTON
4 INSIDE BOXES / CARTON	

LABEL SPECIFICATIONS

TAPPING & REEL

Feeling Technology Corp.
Product : FP5001
Lot No : A3311C62
D/C : 4Xx-XXL
Q'ty : ◎ ◎

無鉛
Lead Free

CARTON

Feeling Technology Corp.

Product Type: FP5001

Lot No: A3311C62

Date Code: 4Xx-XXL

Package Type: SOP-8L

Marking Type: Laser

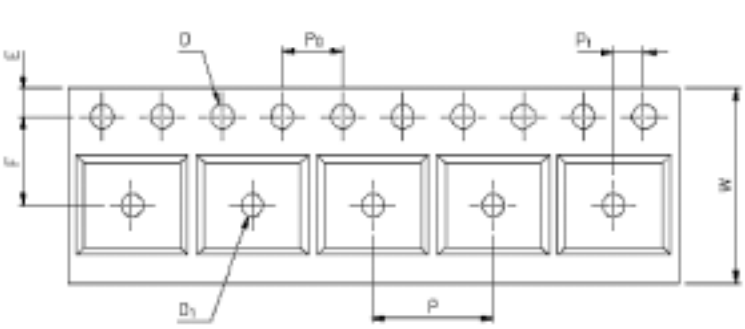
Total Q'ty: 10,000

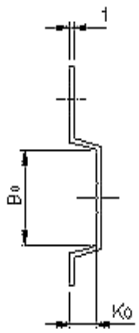
無鉛
Lead Free

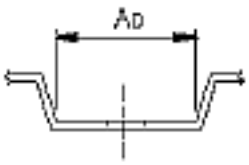
CARRIER TAPE DIMENSIONS

APPLICATION	W	P	E	F	D	D_1
SOP8	$12.0^{+0.3}_{-0.1}$	8.0±0.1	1.75±0.1	5.5±0.1	1.55±0.1	$1.5^{+0.25}$

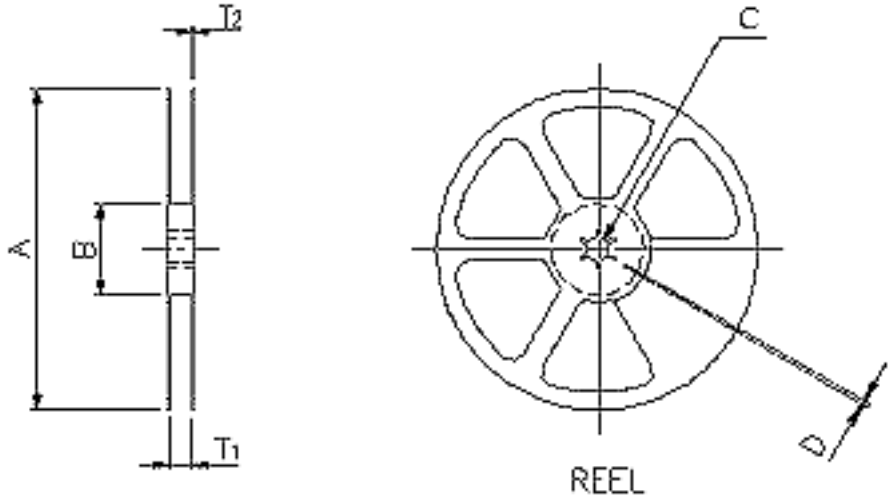
APPLICATION	P_0	P_1	A_0	B_0	K_0	t
SOP8	4.0±0.1	2.0±0.1	6.4±0.1	5.20±0.1	2.1±0.10	0.30±0.013







REEL DIMENISIONS



APPLICATION	MATERIAL	A	B	C	D	T_1	T_2
SOP8	PLASTIC REEL (WHILE)	330±0.1	62±1.5	12.75+0.15	2+0.6	12.4+0.2	2.0+0.2

SGS REPORT

SGS

Test Report

FEELING TECHNOLOGY CORP.
2F, NO.287, SEC.2, KUANG FU RD., SHIN-CHU CITY, TAIWAN, R.O.C.

Report No : CE/2003/81704
Date : 2003/08/28
Page : 1 of 1

The following merchandise was(were) submitted and identified by the client as :

Type of Product	:	POWER IC (FP5001D)
Style/Item No	:	SOP-8
Sample Received	:	2003/08/25.
Testing Date	:	2003/08/25 TO 2003/08/28

Test Result

PART NAME NO.1 : IC(MIX ALL PARTS)

Test Item(s):	Unit	Method	MDL	Result NO.1					Spec.
Lead (Pb)	ppm	ICP-AES After As per US EPA3050B or Acid digestion.	2	16.3					---

NOTE: (1) N.D. = Not detected.(<MDL)
(2) ppm = mg/kg
(3) MDL= Method Detection Limit
(4) " --" = Not Applicable
(5) *=Results shown are of the adjusted analytical results.

Auren Lee/M.R./ Supervisor
Signed for and on behalf of
SGS TAIWAN LTD.