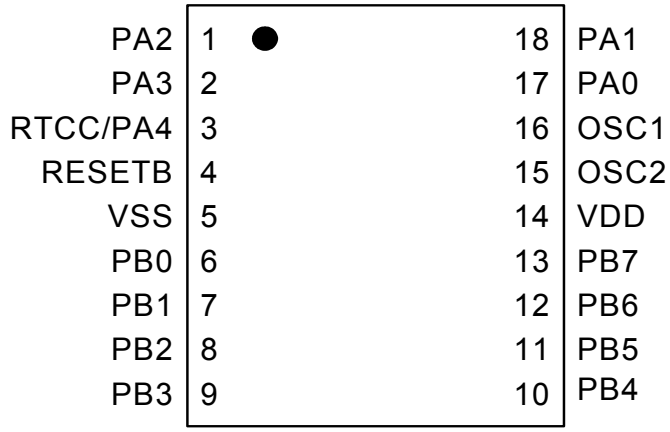
1. Feature

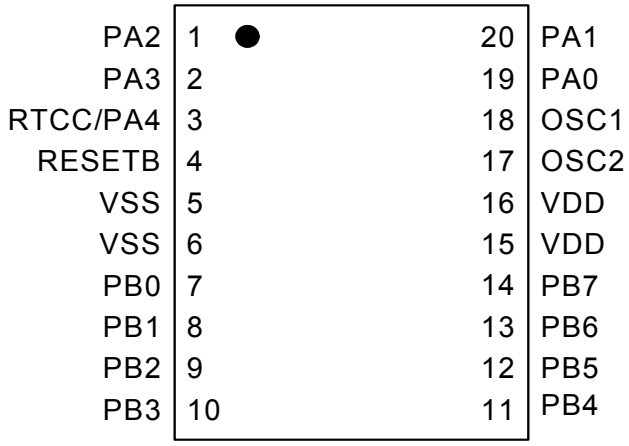
- ROM size: 1,024 Words OTP ROM
- RAM size: 25 Bytes
- 76 single word instruction
- Stack level: 2
- I/O ports: 13
  - Port B: 8 pull high I/O pin
  - Port A0~3: 4 normal I/O pin
  - RTCC/PA4: input pin
- Four kinds of external oscillation modes can be selected:
  RC, LS(Low Speed) Crystal, NS(Normal Speed) Crystal and HS(High Speed) Crystal
- Port B has signal toggle wake up function
- Built-in one 8 bit count up Timer/counter (TMR0) with 8 bit programmable prescaler
- Built-in Watchdog Timer
- Operation Voltage: 2.2V 5.5V
- Different Package Type:
  MK7A10PSS20C: 20 pin SSOP
  MK7A10PD18C: 18 pin DIP
  MK7A10PS18C: 18 pin SOP
  MK7A10PD14C: 14 pin DIP
  MK7A10PS14C: 14 pin SOP

2. Pin Assignment

2.1 18 Pin & 20 Pin

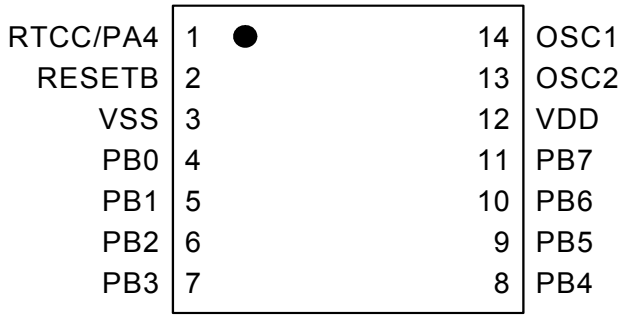


18 pin DIP or SOP package



20 pin SSOP package

2.2 14 Pin



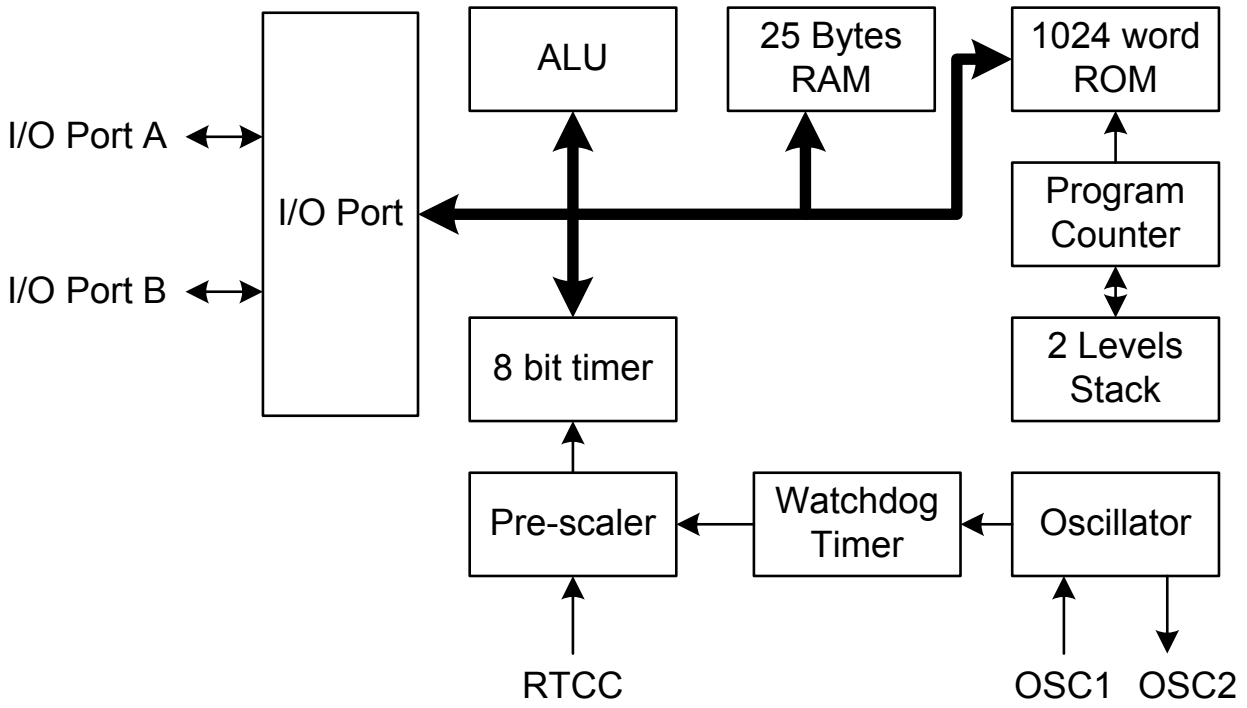
14 pin DIP and SOP package

3. Pin Description

Name	I/O	Description
RTCC/PA4	I	1.External clock or pulse input to TMR0 counter 2.PA4 input (When config. bit6 is set to1)
PA3~0	I/O	I/O Port A0~3
PB7~0	I/O	1.I/O Port B0~7 2.Signal toggle wake up (When config bit7 is set to1) 3.Pull-up resistor (When config bit7 is set to1)
RESETB	I	System reset signal
OSC1	I	Oscillator input
OSC2	O	Oscillator output
VDD	P	System power
VSS	P	Ground

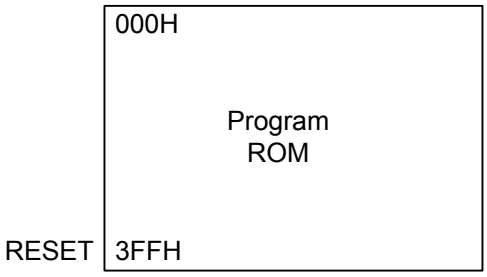
<Note> I: Input; O: Output; I/O: Input/Output; P: Power

4. System Block Diagram



5. Memory Map

5.1 Program memory



<Note> LCALL and LGOTO allow directly operate 1K word addressing.

5.2 Control Register

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CONFIG		TYPE	RTCE	LV1	LV0	CPT	WDTE	FOSC1	FOSC0
SELECT		X	X	SUR0	EDGE0	PSA	PS2	PS1	PS0
IAR	$00	X	X	X	A4	A3	A2	A1	A0
TMR0	$01	D7	D6	D5	D4	D3	D2	D1	D0
PC	$02	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	$03	X	X	SA0	TOB	PDB	Z	DC	C
BSR	$04	X	X	X	D4	D3	D2	D1	D0
I/O $Port_A$	$05	X	X	X	X	PA3	PA2	PA1	PA0
I/O $Port_B$	$06	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0

<Note> X: Reserved

5.3 Configuration Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CONFIG	TYPE	RTCE	LV1	LV0	CPT	WDTE	FOSC1	FOSC0

Bit 1	Bit 0	OSC Type	Frequency Range
0	0	LS (low speed)	32~455KHz
0	1	NS(Normal speed)	1M~8MHz
1	0	HS (high speed)	10~40MHz
1	1	RC	32K~ 10MHz

Bit 2	Description
0	Watchdog timer disable
1	Watchdog timer enable

Bit 3	Description
0	Code Protection ON
1	Code Protection OFF

Bit 5	Bit 4	Detected Voltage Level
0	0	4V
0	1	No use
1	0	2V
1	1	No use

Bit 6	Description
0	Timer Input Only
1	PA4 Input

Bit 7	Description
0	Port B has no signal toggle wake up function
1	Port B has signal toggle wake up function

<Note> When Port B is in input mode, it will has pull up resistor

5.4 Select Register

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SELECT	X	X	SUR0	EDGE0	PSA	PS2	PS1	PS0

Bit 2	Bit 1	Bit 0	Description	
PS2	PS1	PS0	TMR0 rate	WDT rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3	Description
0	Prescaler assigned to TMR0
1	Prescaler assigned to WDT

Bit 4	Description
0	increment when rising edge (Lo to Hi transition) on external clock
1	increment when falling edge (Hi to Lo transition) on external clock

Bit 5	Description
0	TMR0 clock source is (System Clock/4)
1	TMR0 clock source is RTCC input

5.5 Data memory (Register and RAM)

The Data memory is composed of Register and RAM, the address map is as below:

Address	Description
00	IAR
01	TMR0
02	PC
03	STATUS
04	BSR
05	PORTA
06	PORTB
07~1F	General Purpose Register(RAM)

5.5.1 IAR: Indirect Address Register. It is used with BSR to access a physical address.

5.5.2 TMR0: 8 bit count up timer register

5.5.3 PC: Program Counter. 10 bit counter register.

5.5.4 STATUS: Status Register.

<table>
<tr><th>Bit</th><th>Symbol</th><th colspan="3">Description</th></tr>
<tr><td rowspan="3">0</td><td rowspan="3">C</td><td colspan="3">Carry and Borrow bit:</td></tr>
<tr><td colspan="2">ADD instruction</td><td>SUB instruction</td></tr>
<tr><td colspan="2">1: a carry occurred from the MSB
0: no carry</td><td>1: no borrow (Note1)
0: a borrow occurred from the MSB</td></tr>
<tr><td rowspan="3">1</td><td rowspan="3">DC</td><td colspan="3">Nibble Carry and Nibble Borrow bit</td></tr>
<tr><td colspan="2">ADD instruction</td><td>SUB instruction</td></tr>
<tr><td colspan="2">1: a carry from the low nibble bits of the result occurred
0: no carry</td><td>1: no borrow
0: a borrow from the low nibble bits of the result occurred</td></tr>
<tr><td>2</td><td>Z</td><td colspan="3">Zero bit:
1: the result of a logic operation is zero
0: the result of a logic operation is not zero</td></tr>
<tr><td>3</td><td>PDB</td><td colspan="3">Power down flag bit: (Note2)
1: after power-on or by the CLRWDT instruction
0: execute SLEEP instruction</td></tr>
<tr><td>4</td><td>TOB</td><td colspan="3">Time out flag bit:
1: after power-on or by the CLRWDT or SLEEP instruction
0: Occur WDT time-overflow</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">SA0</td><td></td><td colspan="2">Page Location</td></tr>
<tr><td>0
1</td><td colspan="2">Page0 (000H~1FFH)
Page1 (200H~3FFH)</td></tr>
</table>

<Note1>: A SUB instruction is executed by adding the 2's complement of the subtrahend, so C = 1 represents positive result. The below table shows the relation between Carry and Borrow.

B0H－50H										50H－B0H									
	C	B7	B6	B5	B4	B3	B2	B1	B0		C	B7	B6	B5	B4	B3	B2	B1	B0
＋		1	0	1	1	0	0	0	0	＋		0	1	0	1	0	0	0	0
＝	1	1	0	1	0	0	0	0	0	＝	0	1	0	1	0	0	0	0	0

<Note2>: The TOB and PDB bits are active low that can be used to determine different causes of reset. The below table illustrates the value of TOB and PDB after the relative reset events.

TOB	PDB	Reset Event
0	0	WDT time out from sleep mode
0	1	WDT time out from normal mode
1	0	Input a “Low” at RESETB from sleep mode
1	1	Power on reset
Unchanged	Unchanged	Input a “Low” at RESETB from normal

5.5.5 BSR: Bank Select Register. It is used with IAR for indirect addressing data memory.

5.5.6 Port A~B are programmable I/O ports. All I/O pins were set to input mode in power on reset stage.

5.6 Reset

There are 3 kinds of condition will cause system reset:

5.6.1 Power-on
5.6.2 Input a Lo signal into RESETB
5.6.3 When WDTE flag is enabled and the timer escape

5.7 Reset condition of all the RAM

Address	Name	Cold Reset	Warm Reset
N/A	Accumulator	xxxx xxxx	pppp pppp
N/A	IODIR	1111 1111	1111 1111
N/A	Select	--11 1111	--11 1111
00h	IAR	---- ----	---- ----
01h	TMR0	xxxx xxxx	pppp pppp
02h	PC	111 1111 1111	111 1111 1111
03h	STATUS	0001 1xxx	000# #ppp
04h	BSR	111x xxxx	111p pppp
05h	PORTA	0000 xxxx	0000 pppp
06h	PORTB	xxxx xxxx	pppp pppp
07h~1Fh	General Purpose RAM	xxxx xxxx	pppp pppp

<Note> x: unknown; p: keep as previous data ; #: value depends on condition
-:unimplemented and read as"0".

5.8 Wake up function

The chip provide pin signal toggle wake up function. It will return from sleep mode when signal toggle in input port. In order to safely wake up from sleep mode, we suggest to read the input pin to store data before entering sleep mode. The sample program is as below:

```
MOVLA    FFh
IODIR    PORTB   ;// set bit0~7 of port B as input. Only input pin can be wake up
……       ……..
MOVM     PORTB,a ;//Store the data of input pin before sleep
SLEEP            ;// if doesn't perform the read instruction, then can not enter
                 ;// SLEEP mode
 NOP             ;//Add NOP instruction to delay a while when chip wake up
```

6. Instruction Set

<Note> Instruction cycle consist of 4 system clock

Mnemonic Operands	Instruction Code (Advance)	Cycles	Status Affected	OP-code
ADD M, m	(M)+(acc) → (M)	1	C, DC, Z	01 0101 1MMM MMMM
ADD M, a	(M)+(acc) → (acc)	1	C, DC, Z	01 0101 0MMM MMMM
AND M, m	(M). (acc) → (M)	1	Z	01 0100 1MMM MMMM
AND M, a	(M). (acc) → (acc)	1	Z	01 0100 0MMM MMMM
ANDLA I	Literal . (acc) → (acc)	1	Z	11 1001 iiii iiii
BC M, b0	Clear bit0 of (M)	1	None	00 1100 0MMM MMMM
BC M, b1	Clear bit1 of (M)	1	None	00 1100 1MMM MMMM
BC M, b2	Clear bit2 of (M)	1	None	00 1101 0MMM MMMM
BC M, b3	Clear bit3 of (M)	1	None	00 1101 1MMM MMMM
BC M, b4	Clear bit4 of (M)	1	None	00 1110 0MMM MMMM
BC M, b5	Clear bit5 of (M)	1	None	00 1110 1MMM MMMM
BC M, b6	Clear bit6 of (M)	1	None	00 1111 0MMM MMMM
BC M, b7	Clear bit7 of (M)	1	None	00 1111 1MMM MMMM
BS M, b0	Set bit0 of (M)	1	None	00 1000 0MMM MMMM
BS M, b1	Set bit1 of (M)	1	None	00 1000 1MMM MMMM
BS M, b2	Set bit2 of (M)	1	None	00 1001 0MMM MMMM
BS M, b3	Set bit3 of (M)	1	None	00 1001 1MMM MMMM
BS M, b4	Set bit4 of (M)	1	None	00 1010 0MMM MMMM
BS M, b5	Set bit5 of (M)	1	None	00 1010 1MMM MMMM
BS M, b6	Set bit6 of (M)	1	None	00 1011 0MMM MMMM
BS M, b7	Set bit7 of (M)	1	None	00 1011 1MMM MMMM
BTSC M, b0	If bit0 of (M) = 0, skip next instruction	1 + (skip)	None	00 0100 0MMM MMMM
BTSC M, b1	If bit1 of (M) = 0, skip next instruction	1 + (skip)	None	00 0100 1MMM MMMM
BTSC M, b2	If bit2 of (M) = 0, skip next instruction	1 + (skip)	None	00 0101 0MMM MMMM
BTSC M, b3	If bit3 of (M) = 0, skip next instruction	1 + (skip)	None	00 0101 1MMM MMMM
BTSC M, b4	If bit4 of (M) = 0, skip next instruction	1 + (skip)	None	00 0110 0MMM MMMM
BTSC M, b5	If bit5 of (M) = 0, skip next instruction	1 + (skip)	None	00 0110 1MMM MMMM
BTSC M, b6	If bit6 of (M) = 0, skip next instruction	1 + (skip)	None	00 0111 0MMM MMMM
BTSC M, b7	If bit7 of (M) = 0, skip next instruction	1 + (skip)	None	00 0111 1MMM MMMM

BTSS M, b0	If bit0 of (M) = 1, skip next instruction	1 + (skip)	None	00 0000 0MMM MMMM
BTSS M, b1	If bit1 of (M) = 1, skip next instruction	1 + (skip)	None	00 0000 1MMM MMMM
BTSS M, b2	If bit2 of (M) = 1, skip next instruction	1 + (skip)	None	00 0001 0MMM MMMM
BTSS M, b3	If bit3 of (M) = 1, skip next instruction	1 + (skip)	None	00 0001 1MMM MMMM
BTSS M, b4	If bit4 of (M) = 1, skip next instruction	1 + (skip)	None	00 0010 0MMM MMMM
BTSS M, b5	If bit5 of (M) = 1, skip next instruction	1 + (skip)	None	00 0010 1MMM MMMM
BTSS M, b6	If bit6 of (M) = 1, skip next instruction	1 + (skip)	None	00 0011 0MMM MMMM
BTSS M, b7	If bit7 of (M) = 1, skip next instruction	1 + (skip)	None	00 0011 1MMM MMMM
CLRA	Clear accumulator	1	Z	01 0001 0000 0000
CLR M	Clear memory M	1	Z	01 0001 1MMM MMMM
CLRWDT	Clear watch-dog register	1	TO, PO	01 0000 0000 0001
COM M, m	~(M) → (M)	1	Z	01 0010 1MMM MMMM
COM M, a	~(M) → (acc)	1	Z	01 0010 0MMM MMMM
DEC M, m	Decrement M to M	1	Z	01 0110 1MMM MMMM
DEC M, a	(M) - 1 → (acc)	1	Z	01 0110 0MMM MMMM
DECSZ M, m	(M) - 1 → (M), skip if (M) = 0	1 + (skip)	None	01 0111 1MMM MMMM
DECSZ M, a	(M) - 1 → (acc), skip if (M) = 0	1 + (skip)	None	01 0111 0MMM MMMM
INC M, m	(M) + 1 → (M)	1	Z	01 1000 1MMM MMMM
INC M, a	(M) + 1 → (acc)	1	Z	01 1000 0MMM MMMM
INCSZ M, m	(M) + 1 → (M), skip if (M) = 0	1 + (skip)	None	01 1001 1MMM MMMM
INCSZ M, a	(M) + 1 → (acc), skip if (M) = 0	1 + (skip)	None	01 1001 0MMM MMMM
IODIR M	Set i/o direction	1	None	01 0000 0000 0MMM
IOR M, m	(M) ior (acc) → (M)	1	Z	01 1111 1MMM MMMM
IOR M, a	(M) ior (acc) → (acc)	1	Z	01 1111 0MMM MMMM
IORLA I	Literal ior (acc) → (acc)	1	Z	11 0011 iiii iiii
LCALL I	Call subroutine. However, LCALL can addressing 1K address	2	None	10 0iii iiii iiii
LGOTO I	Go branch to any address	2	None	10 1iii iiii iiii
MOVAM m	Move data form acc to memory	1	None	01 0000 1MMM MMMM

MOVLA I	Move literal to accumulator	1	None	11 0001 iiii iiii
MOV M, m	(M) → (M)	1	Z	01 0011 1MMM MMMM
MOV M, a	(M) → (acc)	1	Z	01 0011 0MMM MMMM
NOP	No operation	1	None	01 0000 0000 0000
RET	Return	2	None	11 1111 0111 1111
RETI	Return and enable INTM	2	None	11 1111 1111 1111
RETLA I	Return and move literal to accumulator	2	None	11 1100 iiii iiii
RL M, m	Rotate left from m to itself	1	C	01 1100 1MMM MMMM
RL M, a	Rotate left from m to acc	1	C	01 1100 0MMM MMMM
RR M, m	Rotate right from m to itself	1	C	01 1110 1MMM MMMM
RR M, a	Rotate right from m to acc	1	C	01 1110 0MMM MMMM
SELECT	Set select register	1	None	01 0000 0000 0010
SLEEP	Enter sleep (saving) mode	1	TO, PO	01 0000 0000 0011
SUB M, m	(M)–(acc) → (M)	1	C, DC, Z	01 1010 1MMM MMMM
SUB M, a	(M) –(acc) → (acc)	1	C, DC, Z	01 1010 0MMM MMMM
SWAP M, m	Swap data from m to itself	1	None	01 1101 1MMM MMMM
SWAP M, a	Swap data from m to acc	1	None	01 1101 0MMM MMMM
XOR M, m	(M) xor (acc) → (M)	1	Z	01 1011 1MMM MMMM
XOR M, a	(M) xor (acc) → (acc)	1	Z	01 1011 0MMM MMMM
XORLA I	Literal xor (acc) → (acc)	1	Z	11 1000 iiii iiii

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Supply Voltage …. Vss-0.3V to Vss+5.5V Storage Temperature ……. –50℃ to 125℃
Input Voltage …… Vss-0.3V to VDD+0.3V Operating Temperature …. 0℃ to 70℃

7.2 DC Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VDD	Conditions				
VDD	Operating Voltage	---		2.2		5.5	V
V_{DVT}	Detect Voltage	5V	Low Voltage Detector (Idd = 3uA) Config bit5.bit4=00		3.8		V
		3V	Low Voltage Detector (Idd = 1uA) Config bit5.bi4=10		2.2		V
V_{IL}	Input Low Voltage	5V	I/O Port			0.8	V
I_{IL}	Input Leakage Current	5V	Vin=VDD, VSS		1		UA
I_{DD1}	Standby Current	5V	LV disable,WDT disable,		1		uA
			LV disable,WDT enable,		10		uA
		3V	LV disable,WDT disable,		1		
			LV disable,WDT enable,		2		
I_{IL}	Input Leakage Current	5V	Vin=VDD, VSS		1		uA
			Vol=01V		35		
			Vol=1.5V		50		
R_{PUHI}	Pull_Hi Pin Resister	5V	Set PortB input pin and Pull_Hi		60		KΩ
		3V	Set PortB input pin and Pull_Hi		100		

7.3 AC Characteristics

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
		VDD	Conditions				
f_{sys1}	System Clock	5V	LS Crystal mode	32		455	Khz
		3V		32		455	
f_{sys2}	System Clock	5V	NT Crystal mode	1		10	Mhz
		3V		1		10	
f_{sys3}	System Clock	5V	HS Crystal mode	10		20	Mhz
		3V		10		20	
f_{sys4}	System Clock	5V	RC mode	32K		10	Mhz
		3V		32K		10	
T_{wdt}	Watchdog Timer	5V			20		mS
		3V			25		
T_{rht}	Reset Hold Time	5V			20		mS
		3V			25		

7.4 External RC Table

R value	C value	RC frequency	R connect to (VDD,OSC1)
4.9 M	0.1u (need)	32 Khz	The capacitor is need for stabile frequency
250 K	0.1u (suggest)	455 Khz	
116 K	0.1u (suggest)	1 Mhz	
60 K	0.1u (suggest)	2 Mhz	
32 K	0.1u (suggest)	4 Mhz	
18 K	0.1u (suggest)	8 Mhz	
14 K	0.1u (suggest)	10 Mhz	