EN5366QI

6A Voltage Mode Synchronous Buck PWM DC-DC Converter with Integrated Inductor External Output Voltage Programming

RoHS Compliant

Description

The EN5366QI is a Power System on Silicon DC-DC converter. It is specifically designed to meet the precise voltage and fast transient requirements of present and future high-performance, low-power processor, DSP, FPGA, memory boards and system level applications in a distributed power architecture. Advanced circuit techniques, ultra high switching frequency, and very advanced, high-density, integrated circuit and proprietary inductor technology deliver high-quality, ultra compact, non-isolated DC-DC conversion. High switching frequency and integrated inductor reduce component count requiring only ceramic capacitors and small programming resistors.

The Enpirion solution significantly helps in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, a reduction in the number of vendors required for the complete power solution helps to enable an overall system cost savings.

All Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

Typical Application Circuit

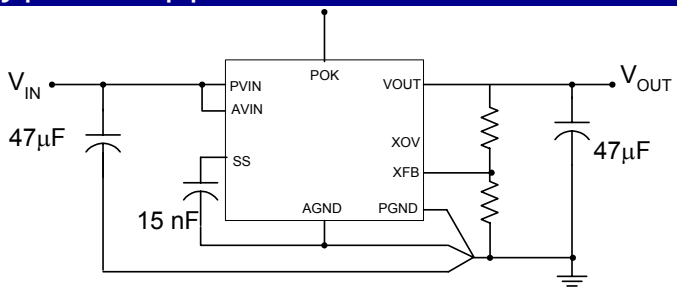


Figure 1. Simple Layout.

Features

- Integrated INDUCTOR, MOSFETS, Controller
- Footprint 1/3rd that of competing solutions.
- Minimal external components.
- Up to 20W continuous output power.
- Master/slave configuration for paralleling.
- 5MHz operating frequency.
- High efficiency, up to 93%.
- V_{OUT} accuracy 2% over line, load and temp.
- Wide input voltage range of 2.375V to 5.5V.
- External resistor divider output voltage select.
- Output enable pin and Power OK signal.
- Programmable soft-start time.
- Programmable over-current protection.
- Programmable over-voltage protection.
- Thermal shutdown, short circuit, and UVLO.
- RoHS compliant, MSL level 3, 260C reflow.

Applications

- Point of load regulation for low-power processors, network processors, DSPs, FPGAs, and ASICs
- Notebook computers, servers, workstations
- Broadband, networking, LAN/WAN, optical
- Low voltage, distributed power architectures with 2.5V, 3.3V or 5V rails
- DSL, STB, DVR, DTV, iPC
- Ripple sensitive applications

Ordering Information

Part Number	Temp Rating (°C)	Package
EN5366QI	-40 to +85	58-pin QFN
EN5366QI-T	-40 to +85	58-pin QFN T&R
EN5366QI-E	QFN Evaluation Board	

Pin Configuration

Below is a top view diagram of the EN5366Q package.

NOTE: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

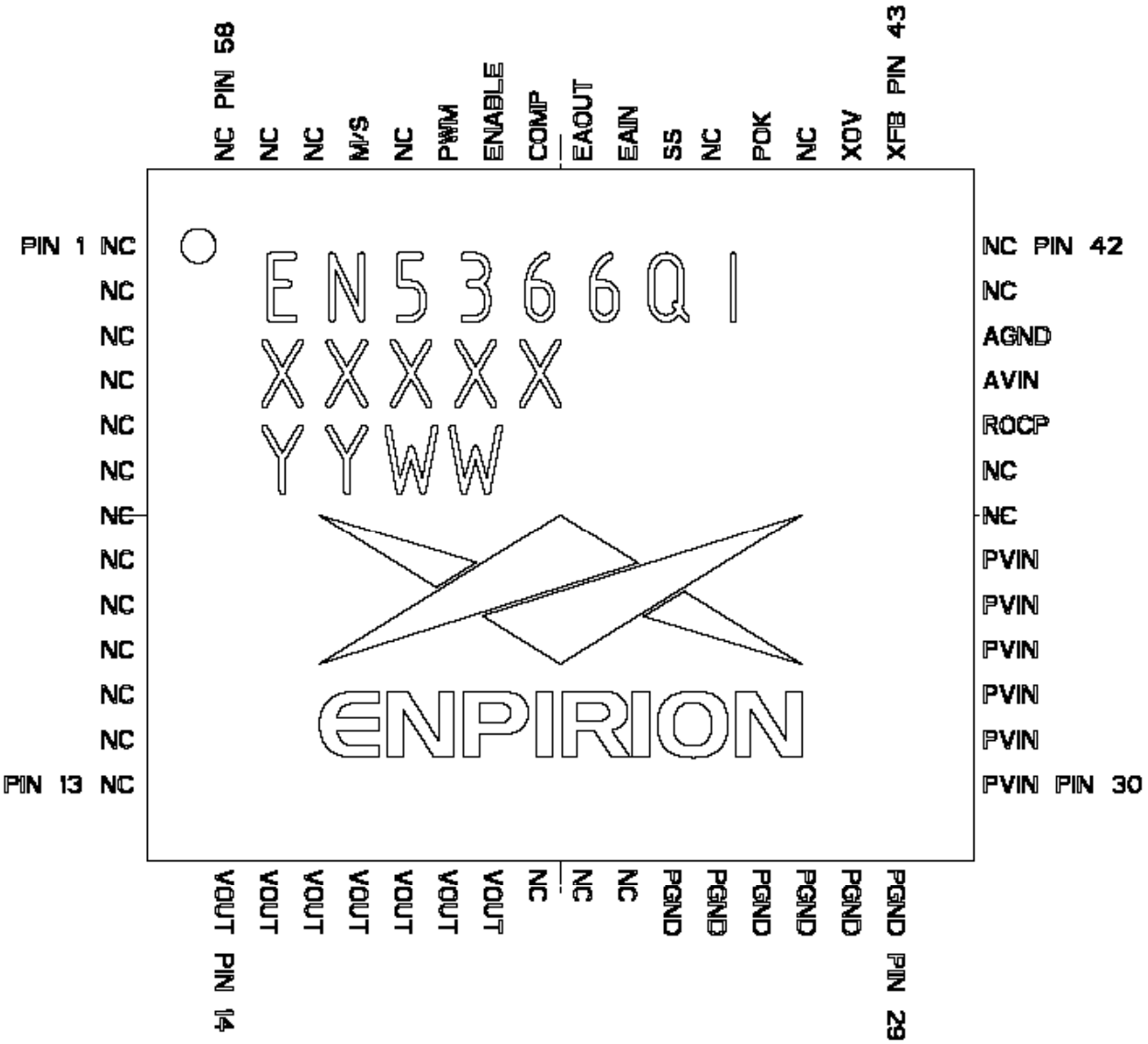


Figure 2. Pin Diagram, top view.

Pin Descriptions

PIN	NAME	FUNCTION
1-3	NC	NO CONNECT – Do not electrically connect these pins to each other or to any other electrical signal. CAUTION!: May be internally connected.
4-5	NC	NO CONNECT – Do not electrically connect these pins to each other or to any other electrical signal. CAUTION!: Internally connected to switching node. Take care to route signals away from these pins.
6-13	NC	NO CONNECT – Do not electrically connect these pins to each other or to any other electrical signal. CAUTION!: May be internally connected.
14-20	VOUT	Regulated converter output. Connect these pins to the load and place output capacitor from these pins the PGND pins 24-26.
21-23	NC	NO CONNECT – Do not electrically connect these pins to each other or to any other electrical signal. CAUTION!: Internally connected to switching node. Take care to route signals away from these pins.
24-29	PGND	Input/Output power ground. Connect these pins to the ground electrode of the Input and output filter capacitors. Refer to layout guideline section for details.
30-35	PVIN	Input power supply. Connect to input power supply. Decouple with input capacitor to PGND (pins 24-29).
36-37	NC	NO CONNECT – Do not electrically connect these pins to each other or to any other electrical signal. CAUTION!: May be internally connected.
38	ROCP	Optional Over Current Protection adjust pin. Place ROCP resistor between this pin and AGND (pin 40) to adjust the over current trip point.
39	AVIN	Analog voltage input for the controller circuits. Connect this pin to the input power supply.
40	AGND	Analog ground for the controller circuits.
41-42	NC	NO CONNECT – Do not electrically connect these pins to each other or to any other electrical signal. CAUTION!: May be internally connected.
43	XFB	Feedback pin for external voltage divider network.
44	XOV	Over voltage programming feedback pin.
45	NC	NO CONNECT – Do not electrically connect these pins to each other or to any other electrical signal. CAUTION!: May be internally connected.
46	POK	Power OK is an open drain transistor for power system state indication. POK is a logic high when VOUT is with -10% to +20% of VOUT nominal.
47	NC	NO CONNECT – Do not electrically connect these pins to each other or to any other electrical signal. CAUTION!: May be internally connected.
48	SS	Soft-Start. The soft-start capacitor is connected between this pin and AGND. The value of this capacitor determines the startup timing.
49	EAIN	Optional Error Amplifier input. Allows for customization of the control loop.
50	EAOUT	Optional Error Amplifier output. Allows for customization of the control loop.
51	COMP	Optional Error Amplifier Buffer output. Allows for customization of the control loop.
52	ENABLE	Input Enable. Applying a logic high, enables the output and initiates a soft-start. Applying a logic low disables the output.
53	PWM	PWM input/output. Used for optional master/slave configuration. When M/S pin is asserted “low”, PWM will output the gate-drive PWM waveform. When the M/S pin is asserted “high”, the PWM pin is configured as an input for PWM signal from the “master” device. PWM pin can drive up to 3 slave devices.
54	NC	NO CONNECT – Do not electrically connect these pins to each other or to any other electrical signal. CAUTION!: May be internally connected.
55	M/S	Optional Master/Slave select pin. Asserting pin “low” places device in Master Mode for current sharing. PWM pin (53) will output PWM drive signal. Asserting pin “high” will place the device in Slave Mode. PWM pin (53) will be configured to input (receive) PWM drive signal from “Master” device.
56-58	NC	NO CONNECT – Do not electrically connect these pins to each other or to any other electrical signal. CAUTION!: May be internally connected.

Block Diagram

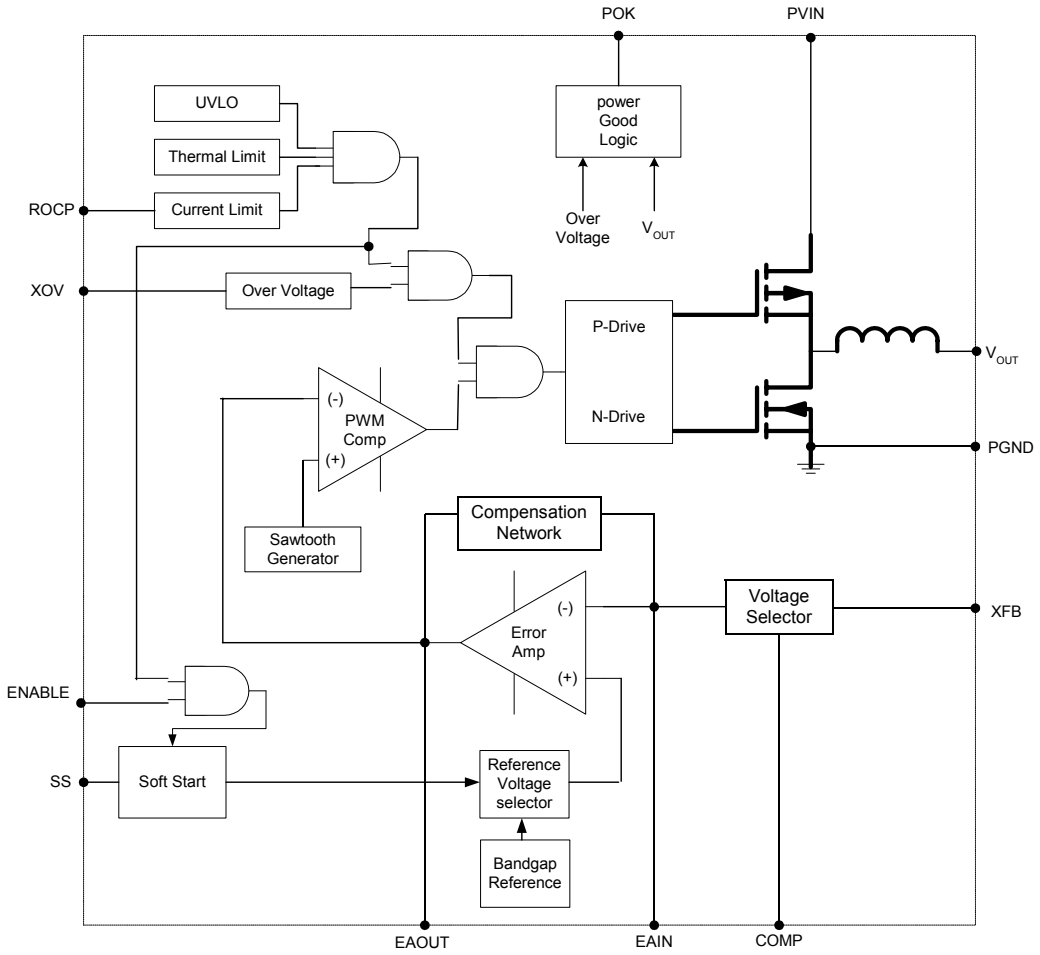


Figure 3. System block diagram.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond recommended operating conditions is not implied. Stress beyond Absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Supply Voltage	V_{IN}	-0.5	7.0	V
Input Voltage – Enable		-0.5	V_{IN}	V
Input Voltage – XFB, XOV		-0.5	V_{IN}	V
Voltages on: EAIN, EAOUT, COMP		-0.5	2.5	V
Voltages on: PWM, M/S		-0.5	2.5	V
Storage Temperature Range	T_{STG}	-65	150	°C
Maximum Operating Junction Temperature	$T_{J\text{-}ABS\ Max}$		150	°C
Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020A			260	°C
ESD Rating (based on Human Body Model)			2000	V

Thermal Characteristics

PARAMETER	SYMBOL	TYPICAL	UNITS
Thermal Resistance: Junction to Ambient (0 LFM)	θ_{JA}	20	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	1.5	°C/W
Maximum Recommended Operating Junction Temp.	T_J	+125	°C

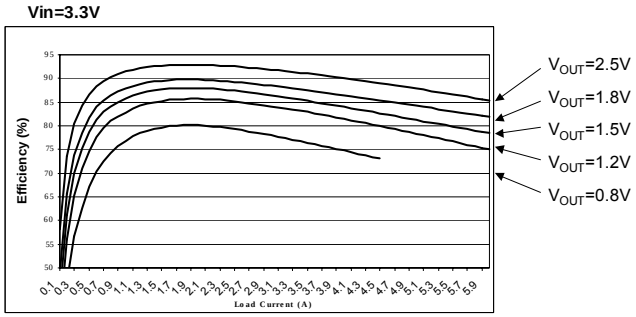
Electrical Characteristics

NOTE: V_{IN}=5.5V over operating temperature range unless otherwise noted.
Typical values are at T_A = 25°C.

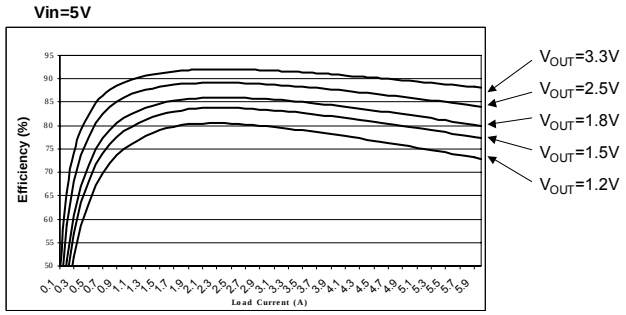
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}		2.375		5.5	V
Under Voltage Lock out threshold	V_{UVLO}	V_{IN} Increasing V_{IN} Decreasing		2.2 2.1		V
Regulated Feedback Voltage	V_{XFB}			0.75		V
V_{OUT} Accuracy	V_{OUT}	Over line, load and temperature	-2.0		2.0	%
Shut-Down Supply Current	I_S	ENABLE=0V		50		µA
Switching Frequency	F_{OSC}			5		MHz
Thermal Overload Trip Point	T_J			150		°C
Maximum Continuous Output Current	I_{OUT}		6			A
Enable Operation						
Disable Threshold	$V_{DISABLE}$	Max voltage to ensure the converter is disabled			0.8	V
Enable Threshold	V_{ENABLE}	2.375V ≤ V_{IN} ≤ 5.5V 5.5V < V_{IN}	1.8 2.0			V
Voltage Select Operation						
Logic Low Threshold	$V_{SX\text{-}Low}$	Threshold voltage for Logic Low			0.8	V
Logic High Threshold	$V_{SX\text{-}High}$	Threshold voltage for Logic High (internally pulled high; can be left floating to achieve logic high)	1.8		V_{IN}	V
Power OK Operation						
POK threshold High				[1]Prog		%
POK threshold low				90%		%
Parallel Operation						
Current Balance	ΔI_{OUT}	With 2 – 4 converters in parallel, the difference between any 2 parts. ΔV_{IN} < 50mV; R_{TRACE} < 10mΩ.		+/-10		%

Note 1: The upper POK threshold is set according to the programmable over-voltage trip-point.

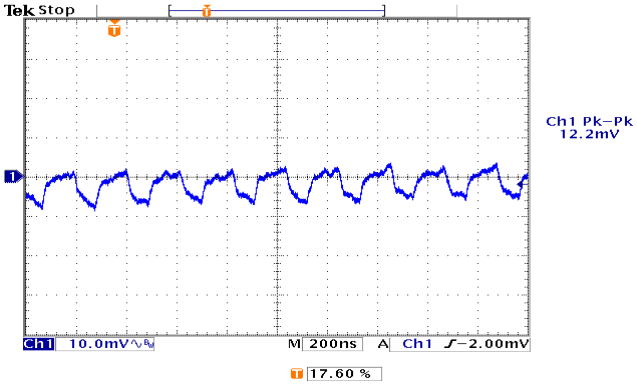
Typical Performance Characteristics



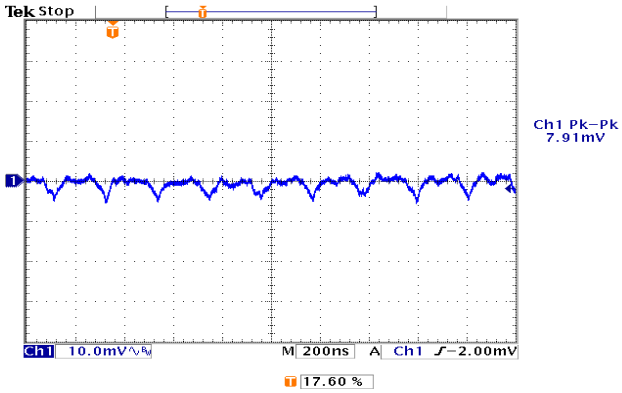
Efficiency vs. Load, V_{IN} = 5V



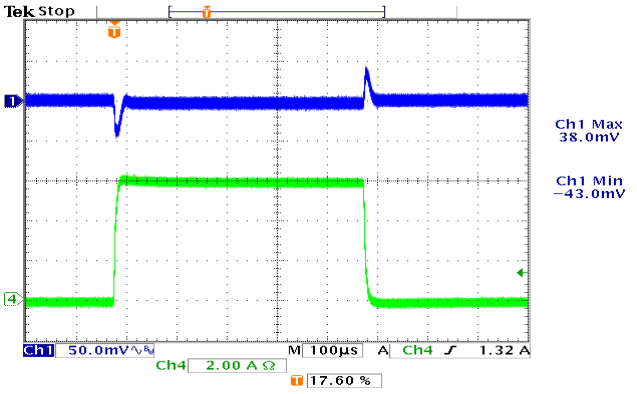
Efficiency vs. Load, V_{IN} = 3.3V



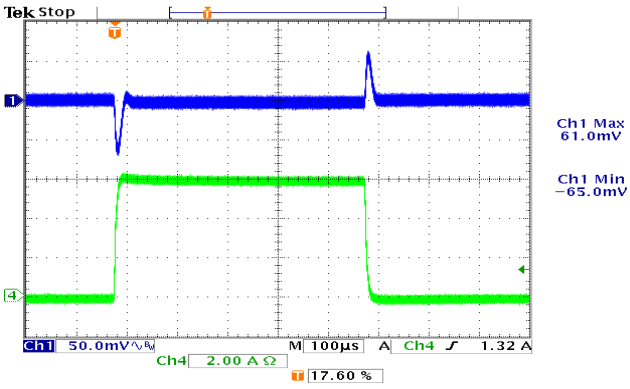
Ripple Voltage, 5.5V_{IN}/3.3V_{OUT}



Ripple Voltage, 3.3V_{IN}/2.5V_{OUT}



Transient Response 5.5V_{IN}/2.5V_{OUT}



Transient Response 5.5V_{IN}/3.3V_{OUT}

Theory of Operation

Synchronous Buck Converter

The EN5366 is a synchronous, programmable power supply with integrated power MOSFET switches and integrated inductor. The nominal input voltage range is 2.4-5.5V. The output voltage is programmed using an external resistor divider network. The feedback control loop is a type III voltage-mode and the part uses a low-noise PWM topology. Up to 6A of continuous output current can be drawn from this converter. The 5MHz operating frequency enables the use of small-size input and output capacitors.

The power supply has the following protection features:

- Programmable over-current protection (to protect the IC from excessive load current).
- Short Circuit protection.
- Thermal shutdown with hysteresis.
- Programmable over-voltage protection.
- Under-voltage lockout circuit to disable the converter output when the input voltage is less than approximately 2.2V

Additional features include:

- Soft-start circuit, to limit the in-rush current when the converter is powered up.
- Power good circuit (POK) indicating whether the output voltage is between 90% of nominal V_{OUT} and the OVP trip point.

Programming Output Voltage and OVP

The EN5366 output voltage is programmed using a simple resistor divider network. Figure 4 shows the resistor divider configuration.

The EN5366 output voltage and over voltage thresholds are determined by the voltages presented at the XFB and XOV pins respectively. These voltages are set by way of resistor dividers between V_{OUT} and AGND with the midpoint going to XFB and XOV.

It is recommended that Rb1 and Rb2 resistor values be ~2kΩ. Use the following equation to set the resistor Ra1 for the desired output voltage:

$$Ra1 = \frac{(Vout - 0.75V) * Rb1}{0.75V}$$

If over-voltage protection is desired, use the following equation to set the resistor Ra2 for the desired OVP trip-point:

$$Ra2 = \frac{(OVPtrip - 0.90V) * Rb2}{0.90V}$$

By design, if both resistor dividers are the same, the OV trip-point will be 20% above the nominal output voltage.

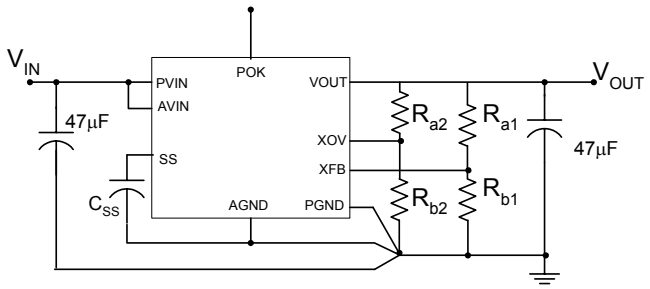


Figure 4. V_{OUT} and OVP resistor divider networks.

NOTE: if no OVP divider is present, there will be no over-voltage protection and POK will remain "high" as long as V_{OUT} remains above 90% of the nominal V_{OUT} setting.

Input Capacitor Selection

The EN5366QI requires between 40-80uF of input capacitance. Low ESR ceramic capacitors are required with X5R or X7R rated dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these loose capacitance with frequency, temperature and bias voltage.

In some applications, lower value capacitors are needed in parallel with the larger, capacitors in order to provide high frequency decoupling.

Table 2. Recommended input capacitors.

Description	MFG	P/N
22uF, 10V, X7R, 1210	Murata	GRM32ER71A226KE20L
	Taiyo Yuden	LMK325BJ226KM-T
47uF, 10V, X5R, 1210	Murata	GRM32ER71A476KE20L
	Taiyo Yuden	LMK325BJ476KM-T

Output Capacitor Selection

The EN5366QI has been optimized for use with approximately 50µF of output capacitance. Low ESR ceramic capacitors are required with X5R or X7R rated dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these loose capacitance with frequency, temperature and bias voltage.

Table 3. Recommended output capacitors.

Description	MFG	P/N
10uF, 6.3V, X7R, 1206	Murata	GRM319R60J106KE19D
	Taiyo Yuden	LMK316BJ106KD-T
22uF, 6.3V, X5R, 1206	Murata	GRM31CR60J226KE19L
	Taiyo Yuden	LMK316BJ226KL-T
47uF, 6.3V, X5R, 1206	Murata	GRM31CR71A476ME19L
	Taiyo Yuden	LMK316BJ476KL-T

Output ripple voltage is determined by the aggregate output capacitor impedance. Output impedance, denoted as Z, is comprised of effective series resistance, ESR, and effective series inductance, ESL:

Z = ESR + ESL.

Placing output capacitors in parallel reduces the impedance and will hence result in lower ripple voltage.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + ... + \frac{1}{Z_n}$$

Typical ripple versus capacitor arrangement is given below:

Output Capacitor Configuration	Typical Output Ripple (mVp-p) (as measured on EN5366QI Evaluation Board)
1 x 47uF	20
5 x 10 uF	9

Enable Operation

The ENABLE pin provides a means to shut down the device, or enable normal operation. A logic low will disable the converter and cause it to shut down. A logic high will enable the converter into normal operation. When the ENABLE pin is asserted high, the device will undergo a normal soft start.

Soft-Start Operation

Soft start is a method to reduce in-rush current when the device is enabled. The output voltage is ramped up slowly upon start-up. The output rise time is controlled by choice of a soft-start capacitor, which is placed between the SS pin (pin 48) and the AGND pin (pin 40).

Rise Time: $T_R = C_{ss} * 80K\Omega$

During start-up of the converter, the reference voltage to the error amplifier is gradually increased to its final level by an internal current source of typically 10uA. Typical soft-start rise time is 1mS to 3mS. Typical SS capacitor values are in the range of 15nF to 30 nF.

POK Operation

The POK signal is an open drain signal from the converter indicating the output voltage is within the specified range. The POK signal will be a logic high when the output voltage is within 90% - 120% of the programmed output voltage. If the output voltage goes outside of this range, the POK signal will be a logic low until the output voltage has returned to within this range. In the event of an over-voltage condition the POK signal will go low and will remain in this condition until the output voltage has dropped to 95% of the programmed output voltage before returning to the high state (see also: Over Voltage Protection)

Over-Current Protection

The current limit function is achieved by sensing the current flowing through the sense P-MOSFET. When the sensed current exceeds the current limit, both NFET and PFET switches are turned off. If the over-current condition is removed, the over-current protection circuit will enable the PWM operation. If the over-current condition persists, the soft start capacitor will eventually discharge and cause the converter to go through a full soft-start cycle. This circuit is designed to provide high noise immunity.

It is possible to adjust the over-current set point by connecting a resistor between ROCP (pin 38) and GND (increase the trip point) or PVIN (decrease the trip point). The nominal over current trip point is set to 9A. The voltage at the ROCP pin is designed to be 0.8V.
In some cases, such as the start-up of FPGA devices, it is desirable to blank the over-current protection feature. In order to disable over-current protection, the ROCP pin should be tied to PVIN.

Over-Voltage Protection

When the output voltage exceeds 120% of the programmed output voltage, the PWM operation stops, the lower N-MOSFET is turned on and the POK signal goes low. When the output voltage drops below 95% of the programmed output voltage, normal PWM operation resumes and POK returns to its high state.

Thermal Overload Protection

Thermal shutdown will disable operation once the Junction temperature exceeds approximately 150ºC. Once the junction temperature drops by approx 20ºC, the converter will re-start with a normal soft-start.

Input Under-voltage Lock-out

Circuitry is provided to ensure that when the input voltage is below the specified voltage range, the converter will not start-up. Circuits for hysteresis, input de-glitch and output leading edge blanking are included to ensure high noise immunity and prevent false tripping.

Compensation

The EN5366QI is internally compensated through the use of a type 3 compensation network and is optimized for use with about 50µF of output capacitance and will provide excellent loop bandwidth and transient performance for most applications. (See the section on Capacitor Selection for details on recommended capacitor types.) Voltage mode operation provides high noise immunity at light load.
In some cases modifications to the compensation may be required. The EN5366QI provides access to the internal compensation network to allow for customization. For more information, contact Enpirion Applications Engineering support.

Parallel Device Operation

In order to power a load that is higher than the rated 6A of the EN5366QI, from 2 to 4 devices can be placed in parallel for providing a single load with up to 24A of output current.

Paralleling more than 1 device is accomplished by selecting a master device and tying that M/S pin to AGND. All slave devices should have their M/S pin tied to AVIN. The PWM pin from the master device is connected to all slave device PWM pins. (See Figure 4.)

1. All master and slave devices should have identical placement and values of input, output and soft-start capacitors.
2. All master and slave devices should have their ENABLE pins tied together and should be operated simultaneously with a fast rising edge of 10 uSec or less, to ensure that devices start up at the same time. Startup imbalance could lead to OCP condition on first device to startup.
3. The XFB pins of the Master and Slave devices should all connect to the center tap of the output voltage programming resistor divider to ensure proper setting for

protection features.

4. The XOV pins of the Master and Slave devices should all connect to the center tap of the over-voltage set-point programming resistor divider to ensure proper setting for protection features
5. The maximum board trace resistance between any 2 devices VOUT pins should be less than 10mΩ.
6. The maximum difference of PVIN between any 2 devices should be less than 50mV.
7. POK pins should be connected together to ensure device error conditions are properly detected.

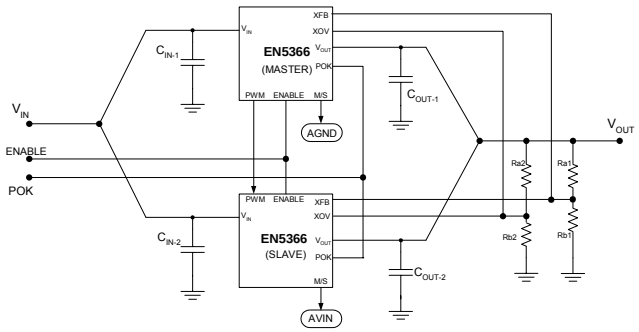


Figure 4 . Paralleling of two devices.

Layout Recommendations

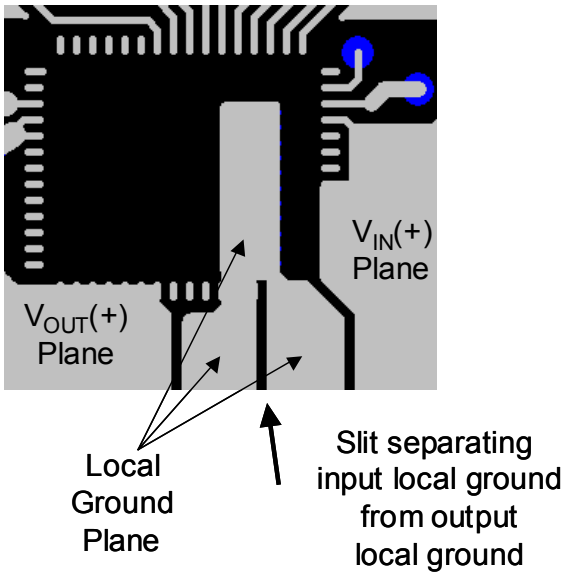


Figure 5. Layout of power and ground planes.

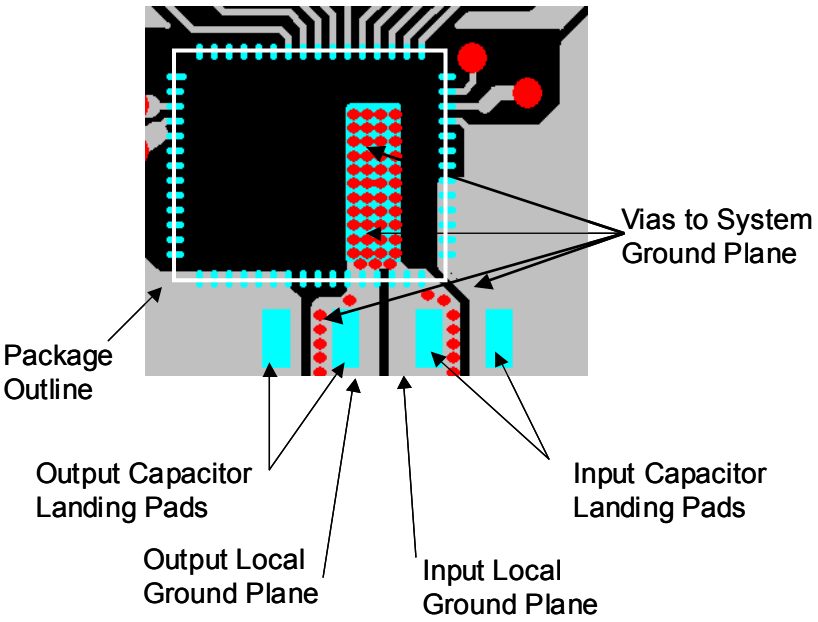


Figure 6. Use of vias connecting local and system ground.

Recommendation 1: Input and output capacitors should be placed as close to the EN5366QI package as possible to reduce EMI from input and output loop currents. This reduces the physical area of the Input and Output AC current loops.

Recommendation 2: Place a slit in the input/output capacitor ground plane just beyond the common connection point of the GND pins of the device as shown in figure 5.

Recommendation 3: Multiple small (0.25mm) vias should be used to connect ground terminal of the Input capacitor and the output capacitor to the system ground plane as shown in figure 6.

Recommendation 4: The large thermal pad underneath the component must be connected to the system ground plane through as many vias as possible. The diameter of the vias should be less than 0.3mm. This provides the quiet, or analog ground for the converter and also provides the path for heat dissipation from the converter. A later section of this note

makes a recommendation on the PCB footprint.

Recommendation 5: The system ground plane referred to in recommendations 3 and 4 should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input and output capacitors that carry large AC currents.

Recommendation 6: As with any switch-mode DC/DC converter, do not run sensitive signal or control lines underneath the converter package.

Design Considerations for Lead-Frame Based Modules

Exposed Metal on Bottom Of Package

Lead frame offers many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package.

Only the large thermal pad and the perimeter pads are to be mechanically or electrically connected to the PC board. The PCB top layer under the EN5366QI should be clear of any metal except for the large thermal pad. The “grayed-out” area in Figure 7 represents the area that should be clear of any metal (traces, vias, or planes), on the top layer of the PCB.

Figure 8 demonstrates the recommended PCB footprint for the EN5366QI. Figure 9 shows the shape and location of the exposed metal pads as well as the mechanical dimension of the large thermal pad and the pins.

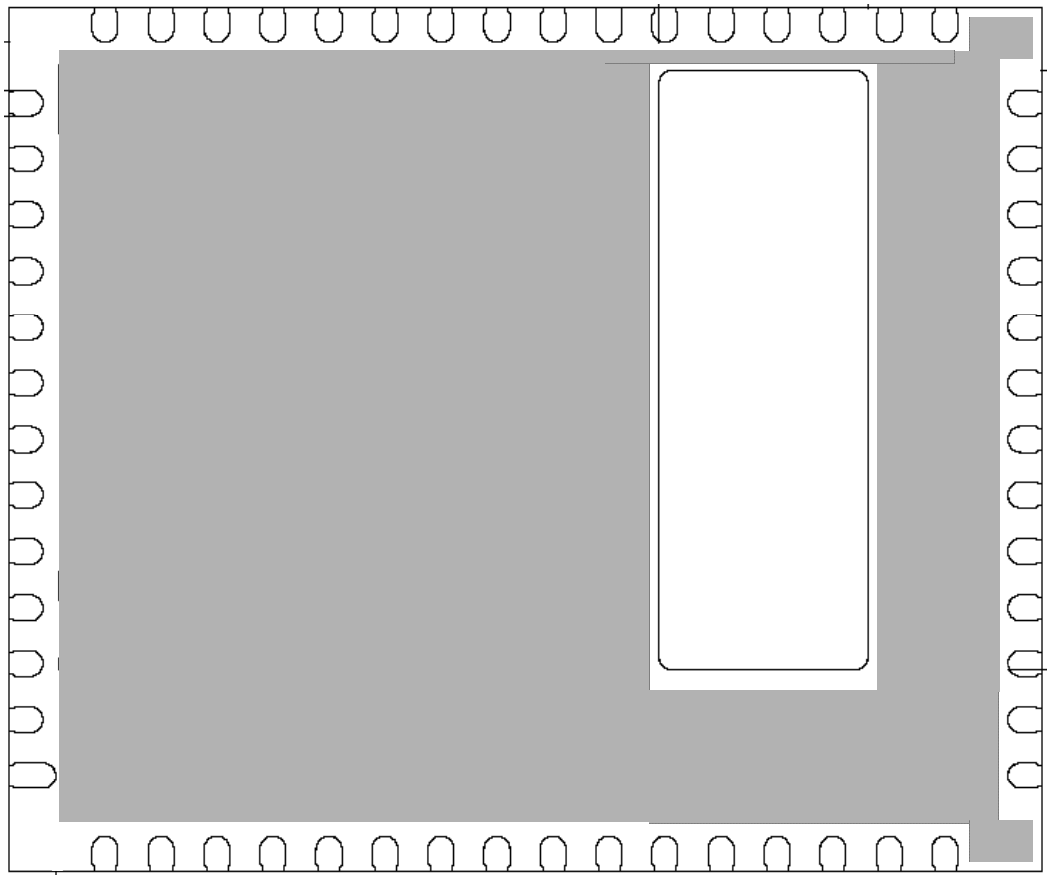


Figure 7. Lead-Frame exposed metal. Grey area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.

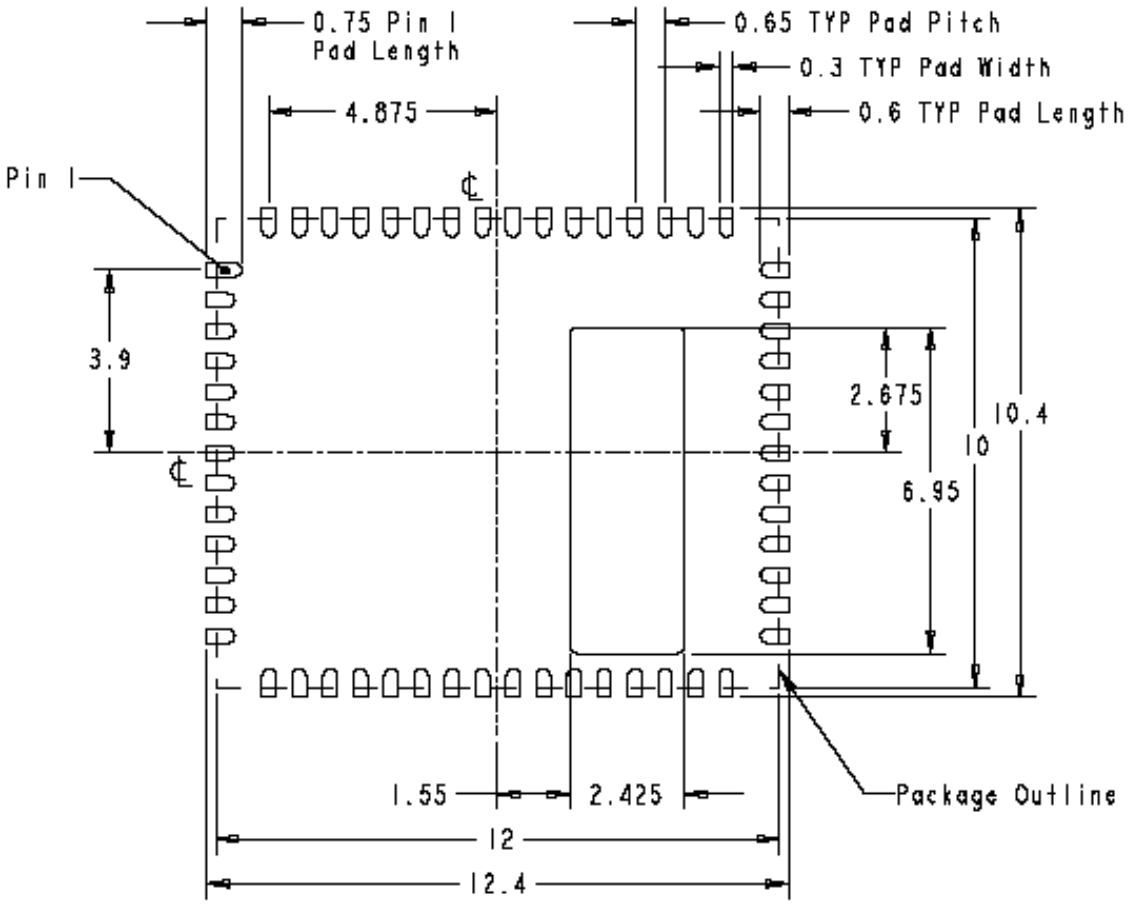


Figure 8. Recommended footprint for PCB.

Package Dimensions

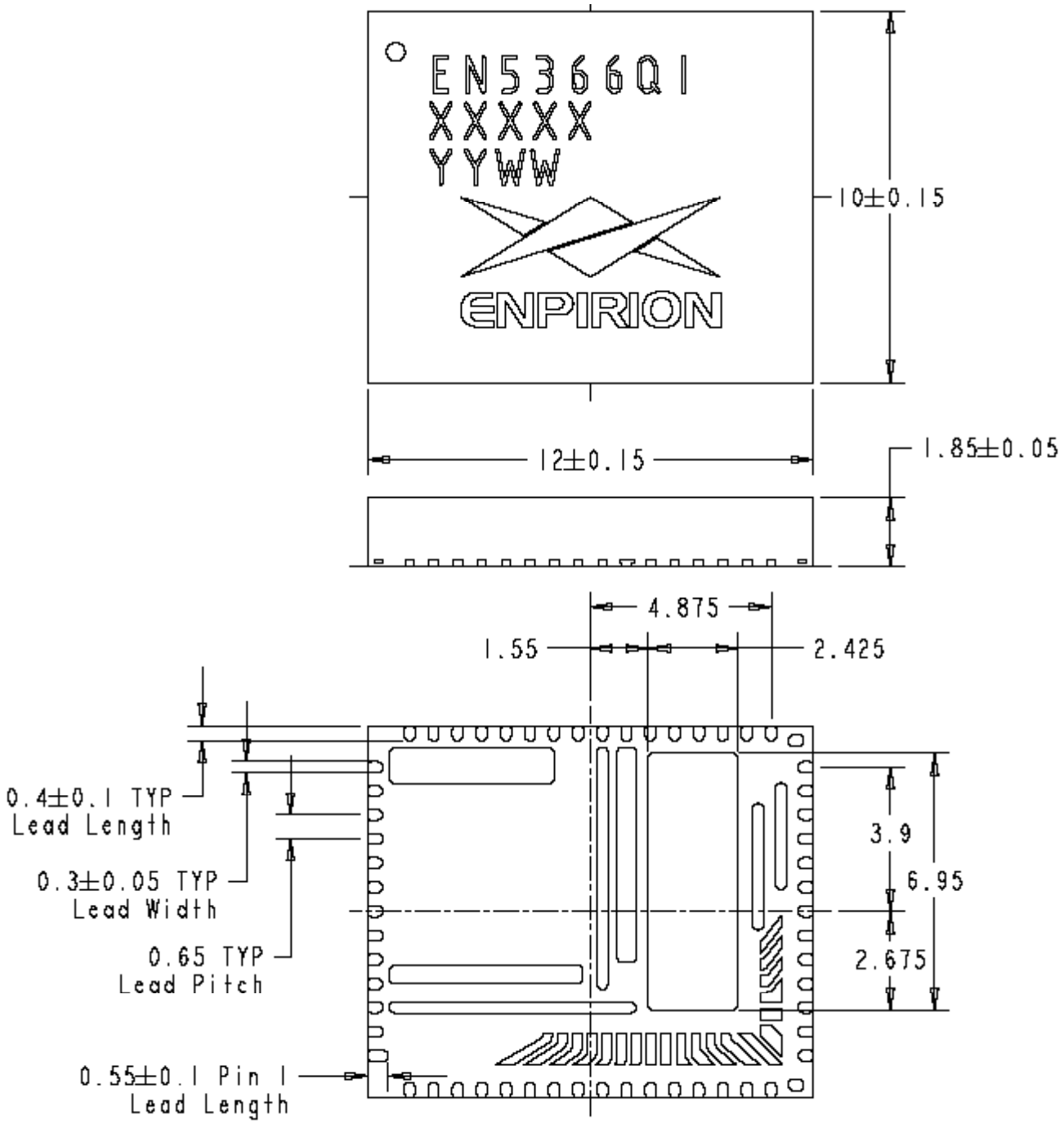
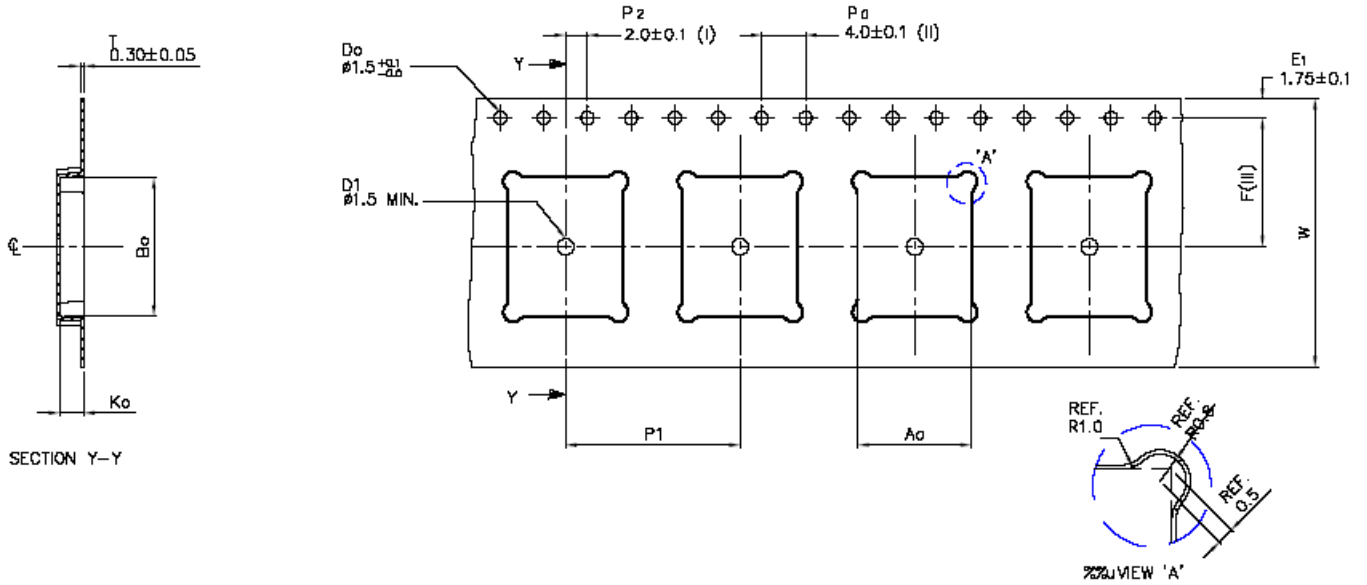


Figure 9. Package dimensions.

TAPE AND REEL SPECIFICATION



Ao	10.40	+/–	0.1
Bo	12.40	+/–	0.1
Ko	2.20	+/–	0.1
F	11.50	+/–	0.1
P1	16.00	+/–	0.1
W	24.00	+/–	0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Typical SR of form tape from 10^5 to 10^{11} OHM/SQ
ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Additional Products

Part Number	Description
EP5352QI	500mA DCDC with integrated inductor; 5mm x 4mm x 1.1mm package
EP5362QI	600mA DCDC with integrated inductor; 5mm x 4mm x 1.1mm package
EP5382QI	800mA DCDC with integrated inductor; 5mm x 4mm x 1.1mm package
EQ5352DI	500mA DCDC regulator; tiny 3mm x 2mm x 0.9mm DFN package
EQ5362DI	600mA DCDC regulator; tiny 3mm x 2mm x 0.9mm DFN package
EQ5382DI	800mA DCDC regulator; tiny 3mm x2mm x0.9mm DFN package
EN5312QI	1A DCDC with integrated inductor; 5mm x 4mm x 1.1mm package
EN5335QI	3A DCDC with integrated inductor; 10mm x 7.5mm x 1.85mm QFN package 3-Pin VID V_{OUT} programming
EN5336QI	3A DCDC with integrated inductor; 10mm x 7.5mm x 1.85mm QFN package External resistor divider V_{OUT} programming
EN5365QI	6A DCDC with integrated inductor; 12mm x 10mm x 1.85mm QFN package 3-Pin VID V_{OUT} programming; Parallel Capable

Contact Information

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