AND8105/D

Design of a 100 W DC-DC Converter for Telecom Systems Using the NCP1560

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APPLICATION NOTE

INTRODUCTION

The NCP1560 PWM controller contains all the features and flexibility needed to implement voltage−mode control for single−ended DC−DC converters. This IC operates from an input supply between 21.5 V and 150 V, commonly found in telecom and 42 V automotive systems.

The NCP1560 is the ideal choice for new generation isolated fixed switching frequency DC−DC converters using synchronous rectification to achieve extremely high conversion efficiency. This controller will help designers cope with their daily challenge, "small form factor highly protected module" through the following features:

- **Dual control outputs with adjustable overlap delay:** provide design flexibility. Output 1 (OUT1) controls the main switch in a forward or flyback converter topology. Output 2 (OUT2) can be used to control an active clamp/reset switch, a synchronous rectifier switch, or both. OUT2 has an adjustable overlap delay to prevent simultaneous conduction of the switching elements.

- **An Internal Startup Regulator:** provides power to the NCP1560 during startup. Once the system powers up, the regulator is disabled, thus reducing power consumption. The regulator can be powered directly from the input line.

- **Soft−Start:** allows the system to turn ON in a controlled manner and reduce stress on system components.

- **Maximum Duty Cycle:** circuit limits the duty cycle inversely proportional to line voltage. It allows for a tighter transformer design.

- **Line Feedforward:** adjusts the duty cycle inversely proportional to line voltage, allowing the controller to respond in the same cycle to line voltage changes. It provides the controller the same advantages of current−mode control, while eliminating noise susceptibility, low power jitter and the need for ramp compensation.

- **Dual Mode Overcurrent Protection Circuit:** handles momentary and hard short conditions differently to provide the best tradeoff in system performance and safety. The NCP1560 enters the cycle by cycle current limit mode if the system reaches the 1st current limit threshold. If the system reaches the 2nd current limit threshold, the controller enters the cycle skip current limit mode. While the converter is in the cycle skip mode, the outputs are disabled.

- **Line Under/Overvoltage Detector:** circuit enables the device when the line voltage is within the pre−selected voltage range. A resistor divider from the input line bias the under−overvoltage detector.

DESIGN SPECIFICATIONS

The flexibility of the NCP1560 is demonstrated in a DC−DC converter for the telecom system. The converter delivers up to 100 W at 3.3 V. The converter specifications are listed in Table 1.

Table 1. Converter Specifications

Parameter	Symbol	Min	Max
Input Voltage	V_{in}	32 V	78 V
Frequency	f	260 kHz	300 kHz
Full Load Efficiency	η	80%	−
Duty Cycle	DC	−	60%
Output Voltage	V_{out}	3.3 V ($\pm$5%)	
Output Current	I_{out}	3 A	30 A
Output Voltage Ripple	$V_{out(rip)}$	−	50 mV
Output Power	P_{out}	−	100 W

A forward converter topology is selected for our converter, as it provides low output voltage ripple and high efficiency.

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FORWARD CONVERTER

Figure 1 shows the forward converter topology. In a forward converter, current flows in the primary side when the switch turns ON. The dot end of the transformer primary side becomes positive with respect to the non–dot end. The dot end of the secondary side also becomes positive, forward biasing D1. When the switch turns OFF, the transformer opposes the current flow change and its polarity is reversed. While the polarity is reversed, the transformer is reset and the voltage needs to be clamped to prevent damage to the converter. This can be accomplished using a reset winding or an active clamp/reset circuit. During the OFF period, D1 is reverse biased, D2 is forward biased and power to the load is provided by C_{out}.
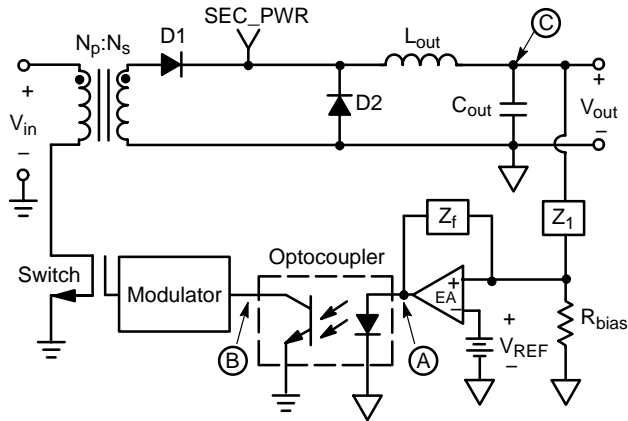

Figure 1. Forward Converter Topology

DESIGN PROCEDURE

The converter design is broken in several steps to ease the design process. The transformer design is the starting point as it determines most of the system components. The converter design follows the order below:

1. Transformer
2. Core Reset
3. Auxiliary Supply
4. Power Switch Selection
5. Output L–C Filter
6. Input EMI Filter
7. Synchronous Rectifier
8. Feedback Loop
9. Current Limit
10. Under/Overvoltage Lockout
11. Maximum Duty Cycle
12. Soft–start
13. Oscillator Frequency
14. Layout Considerations
15. Design Verification

TRANSFORMER DESIGN

A ferrite core is used for the transformer as it provides low core losses (compared to powder cores) at the target operating frequency of 275 kHz. The converter input to output power relationship is given in equation (1)

$$P_{in} = \frac{P_{out}}{\eta} = I_P \times V_{in} \tag{1}$$

where, I_P is the average primary current, η is the target efficiency and P_{in} and P_{out} are the input and output power, respectively. The input to output voltage relationship is described in equation (2).

$$V_{out} = \left[\frac{V_{in(min)} - V_{DS(on)}}{\frac{N_p}{N_s}} - V_{f(D2)} \right] DC \tag{2}$$

where, N_p and N_s are the primary and secondary winding turns, $V_{DS(on)}$ is the voltage drop across the switching element and $V_{f(D2)}$ is the voltage drop across D2. The converter is designed to operate at a 60% maximum duty cycle at 32 V. It provides a good compromise between transformer size and voltage stress on the switching element.

The secondary winding carries the higher current. Therefore, N_s is set to 1 to reduce conduction losses. Assuming a $V_{DS(on)}$ and $V_{f(D2)}$ drop of 0.5 V each, (2) is used to determine the primary winding turns as follows:

$$N_p = \frac{32\ V - 0.5\ V}{\frac{3.3\ V}{0.6} + 0.5\ V} \times 1 = 5.25 \approx 5$$

Once the primary winding turns are known, the required transformer effective area in cm^2, A_e, is calculated using (3)

$$A_e = \frac{V_{in(min)} \times t_{on}}{(B_{pk} - B_r) \times N_p \times 1x10^{-8}} \tag{3}$$

where, B_{pk} and B_r are peak and remanence flux density in Gauss, respectively. The peak and remanence fluxes are a function of the core material selected. Payton America R Material was selected.

The peak and remanence flux densities are set at 3000 G and 1000 G, respectively. As given in (3), operating the transformer at a high flux density reduces the core effective area (thus size). However, if B_{pk} is arbitrarily selected, the transformer may saturate. Solving (3),

$$A_e = \frac{32\ V \times \frac{0.6}{260\ kHz}}{(3000\ G - 1000\ G) \times 5 \times 1x10^{-8}} = 0.738\ cm^2$$

indicates that an effective area of 0.738 cm^2 is required. Payton America E18 core is used for our transformer. It has an effective area of 0.75 cm^2.1

The NCP1560 supply voltage needs to be biased above $V_{AUX(off)}$ (7.0 V) after initial turn ON to prevent the outputs from turning OFF. After a fault condition, V_{AUX} needs to be cycled between $V_{AUX(off)}$ and $V_{AUX(on)}$ (11 V) to re–enable the outputs. This is accomplished by biasing V_{AUX} from an auxiliary winding supply. The auxiliary winding is designed to generate a voltage above $V_{AUX(on)}$ during all input voltage conditions. The auxiliary winding turns (N_{AUX}) are calculated solving (4)

$$V_{AUX} = V_{in} \times \frac{N_{AUX}}{N_p} \qquad (4)$$

where, V_{AUX} is the auxiliary winding peak voltage. The auxiliary winding turns are set to 2 for a peak voltage range between 12.8 V and 31.2 V.

A reset winding is also built in our transformer and is discussed in the following section.

The final step in our transformer design is to select the wire size and determine if the required number of turns fit within the transformer window area.

The transformer design consists of a primary winding (terminals 1–2), a secondary winding (terminals 6,7–8,9), a reset winding (terminals 10–11) and an auxiliary winding (terminals 4–5). The transformer can be ordered from Payton America under part number 9452. Table 2 summarizes the specifications of our transformer.

Table 2. Transformer Specifications

Parameter	Terminals	Min	Max
Magnetizing Inductance	1–2	93.75 μH	156.25 μH
DC Resistance	1–2	–	7.5 mΩ
Magnetizing Inductance	6,7–8,9	3.75 μH	6.25 μH
DC Resistance	6,7–8,9	–	0.45 mΩ
Resonant Frequency	–	1 MHz	–
Leakage Inductance	1–2/6–8	170 nH (typ)	
Capacitance	1–2/6–8	250 pF (typ)	

Designing a transformer is an iterative process. It requires one to make certain assumptions, design the transformer and validate the original assumptions. Also, the operating frequency and temperature range needs to be considered to prevent the transformer from saturating.

CORE RESET

At the end of each cycle, the transformer can not have energy stored in it. Otherwise, the energy will increase in each subsequent cycle until the transformer saturates. The NCP1560 converter is designed to reset the transformer using a reset winding or an active clamp/reset circuit as shown in Figure 2.
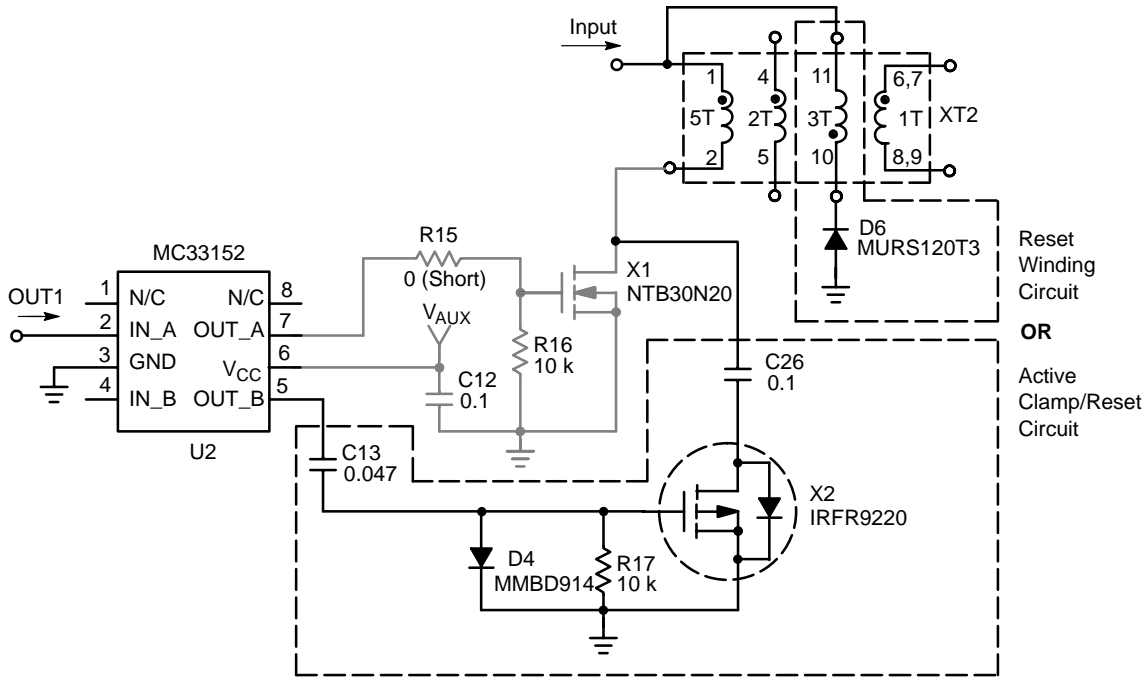

Figure 2. Core Reset Circuit Configuration

The reset winding with diode D6, clamps the reflected secondary to primary voltage. Saturation is avoided if the ON time volt−second (V−s_{on}) product is equal or smaller than the OFF time volt−second (V−s_{off}) product as given in equation (5).

$$\left(V_{in} \times \frac{DC}{f}\right) \leq \left(\frac{V_{in} \times (1 - DC)}{f} \times \frac{N_p}{N_{reset}}\right) \quad (5)$$

where, N_{reset} is the number of turns of the reset winding. Solving for N_{reset}, a maximum number of 3.33 turns are required. The number of turns is set at 3. A disadvantage of the reset winding method is the increased power loss and voltage stress on the main switch during the OFF time. The stress voltage on the main switch is calculated using (6).

$$V_{stress} = V_{in} + \left(V_{in} \times \frac{N_p}{N_{reset}}\right) \quad (6)$$

The active clamp/reset topology reduces power dissipation by recycling the transformer magnetizing energy using a resonant circuit. The active clamp/reset circuit in our converter is connected to the primary winding. The transformer magnetizing inductance, L_M, and storage capacitor, C26, form the resonant circuit.

A constant voltage across C26 is obtained by setting the resonant circuit time constant significantly greater than the converter OFF time. Equation (7) relates the latter constraint to system parameters. The voltage stress on the primary switch is reduced (compared to the reset winding method) and is given in equation (8).

$$\frac{(1 - DC)^2}{(2\pi f)^2 \times L_M} << C26 \quad (7)$$

$$V_{stress} = \frac{V_{in}}{1 - DC} \quad (8)$$

OUT2 controls the active clamp/reset circuit. A p−channel MOSFET, X2, instead of an n−channel MOSFET is used to eliminate the need of a gate driver.

Removing C26 configures the converter to operate using the reset winding. If the active clamp/reset circuit is used, D6 needs to be removed.

AUXILIARY SUPPLY REGULATOR

The auxiliary supply circuit schematic is shown in Figure 3. Using Equation (4), the auxiliary winding peak voltage is calculated between 12.8 V and 31.2 V over the input voltage range. The maximum voltage of the V_{AUX} pin is 16 V. Therefore, the auxiliary supply voltage needs to be regulated. A peak detector, comprised of D2 and C10, rectifies the output of the auxiliary winding. The Zener

voltage of D10 is 15 V. The V_{AUX} voltage is clamped at 13.6 V once the auxiliary winding voltage exceeds 15 V. Diode D8 prevents the NCP1560 startup regulator from sourcing current into the regulator.

Power to the NCP1560 while operating in the Dynamic Self Supply (DSS) Mode is provided by the capacitor (C7) connected on the V_{AUX} pin. Therefore, C7 must be sized such that once the outputs are enabled, a V_{AUX} voltage greater than 7.0 V is maintained while the converter reaches regulation. Also, the V_{AUX} discharge time (from 11 V to 7.0 V) must be greater that the soft−start charge period to assure the converter turns ON.

The output of a forward converter reaches regulation in a time given in equation (9)

$$t = \cos^{-1}\left(1 - \frac{V_{out} \times N_p}{DC \times V_{in} \times N_s}\right) \times \sqrt{L_{out}C_{out}} \quad (9)$$

where, L_{out} and C_{out} are the output inductor and capacitor respectively. Solving (9) using an L_{out} of 2 μH and C_{out} of 848 μF, a minimum time of 59 μs is calculated. Please note that (9) does not account for duty cycle modulation due to soft−start.

Ignoring soft−start, C_{AUX} (or C7) needs to be sized to bias the NCP1560 and any additional circuit powered from C_{AUX}. The required value for C_{AUX} is calculated using (10)

$$C_{AUX} = C7 = \frac{I_{C7} \times t}{4 V} \quad (10)$$

where, I_{C7} includes the NCP1560 bias current (I_{AUX3}) and any additional current supplied by C7. Capacitor C7 is set at 10 μF.
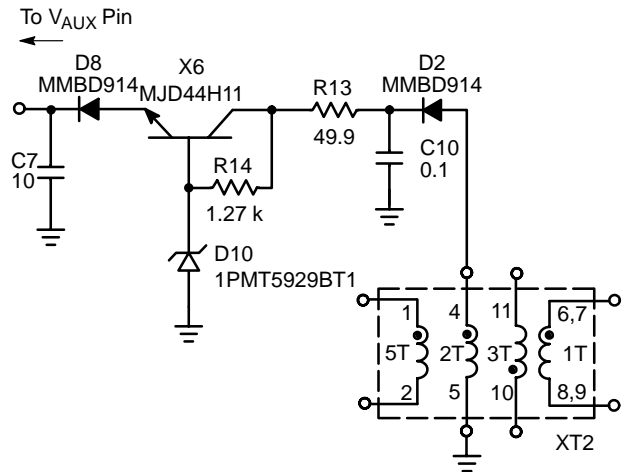

Figure 3. Auxiliary Supply Circuit Schematic

POWER SWITCH

A MOSFET is selected as the primary side switching element. Several factors, including current, voltage stress and power dissipation are considered for the MOSFET selection.

Once the average primary current and maximum duty cycle are determined, the peak primary current, $I_{P(PK)}$, is calculated using (11)

$$I_{P(PK)} = \frac{I_P}{DC_{(MAX)}} \tag{11}$$

$$I_{P(PK)} = \frac{3.54 \text{ A}}{0.6} = 5.9 \text{ A}$$

where, I_P is the average primary current calculated using (1).

The current capability of our MOSFET is selected at least twice the calculated $I_{P(PK)}$ to account for $R_{DS(on)}$ temperature variations and thermal dissipation limitations. In addition, a low $R_{DS(on)}$ MOSFET is selected to reduce power dissipation. The voltage stress on the MOSFET is calculated using (8). ON Semiconductor's NTB30N20 is selected for our design as it meets all our requirements.

The NCP1560 is not designed to drive a big capacitive load, such as the gate of the NTB30N20. Therefore, a gate driver is required to drive the NTB30N20. ON Semiconductor's MC33152 gate driver was selected as it provides the required drive capability and is compatible with the voltage level of the NCP1560 control outputs. The MC33152 is biased from the auxiliary supply discussed in the previous section.

OUTPUT FILTER

The output L−C filter averages the voltage at the cathode of D1. Figure 4 shows the output L−C filter. The output inductor determines the ripple current the output capacitor will absorb. The inductor value is selected such that the current will not go discontinuous at the minimum output current using (12)

$$L_{out} = \frac{V_{out} \times \left(\frac{1}{DC_{MIN}} - 1\right) \times t_{on(min)}}{2 \times I_{out(min)}} \tag{12}$$

$$L_{out} = \frac{3.3 \text{ V} \times \left(\frac{1}{0.22} - 1\right) \times \frac{0.22}{260 \text{ kHz}}}{2 \times 3 \text{ A}} = 1.65 \text{ μH}$$

where, $t_{on(min)}$ and DC_{MIN} are the ON time and duty cycle at the maximum input voltage. The peak to peak ripple current (I_{P-P}) across L_{out} is given in equation (13).

$$I_{P-P} = \frac{\left(V_{in}\frac{N_S}{N_P} - V_{out}\right) \times t_{on}}{2 \times L_{out}} \tag{13}$$

A maximum ripple current of 3.05 A is calculated at the maximum input voltage.

The output capacitor Equivalent Series Resistance, R_{ESR}, mostly determines the output voltage ripple. The ripple is the product of I_{P-P} and R_{ESR}. The required R_{ESR} to absorb 3.05 A and maintain $V_{out(rip)}$ below 50 mV is 16 mΩ. The output capacitor specification is relaxed by increasing L_{out} (or L2) to 2 μH. In addition, several capacitors in parallel are used to reduce R_{ESR}.
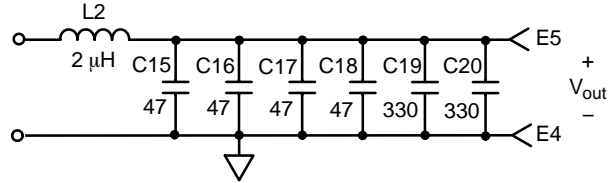

Figure 4. Output L−C Filter Schematic

The complete output inductor specifications are listed in Table 3. The output inductor can be ordered from Payton America under part number 9453.

Table 3. Output Inductor Specifications

Parameter	Nominal $T_A = 25°C$, $I_L = 0$ A	Minimum $T_A = 100°C$, $I_L = 30$ A
Inductance	2.0 μH	1.87 μH
DC Resistance	1.0 mΩ (max)	–
Turns	4	–
Width	25.02 mm	–
Length	24.99 mm	–
Height	8.89 mm (max)	–

INPUT FILTER

An L−C filter at the converter input is used to reduce EMI. The input L−C filter reduces noise and provides a fixed input voltage to the converter. The input L−C filter is shown in Figure 5. Capacitor C27 is used for common mode noise reduction.
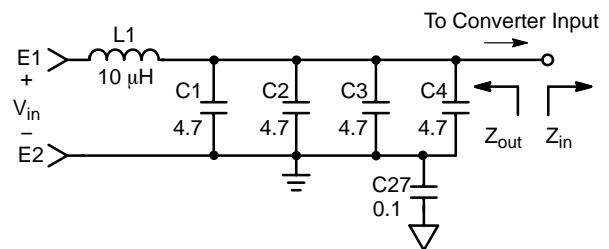

Figure 5. Input L−C Filter Schematic

Oscillation may occur if the converter input impedance, Z_{in}, is lower than the filter output impedance, Z_{out}. The converter closed loop input impedance is ultimately determined by the converter feedback loop as well as the open loop input impedance. However, the converter input impedance can be approximated as a negative resistor using (14).

$$Z_{in}(dB-Ohm) = -20 \log \left(\frac{V_{out}}{I_{out}} \right) \qquad (14)$$

The L–C filter output impedance is given by (15).

$$Z_{out} \approx (L_1) \parallel \left(4C_1 + \frac{R_{ESR}}{4} \right) \qquad (15)$$

The converter input impedance approximation will be used for our analysis. Figure 6 shows the L–C filter output impedance and the approximated converter input impedance over frequency. The filter output impedance exceeds the converter input impedance violating our original design constraint. However, the converter input impedance is only an approximation. The converter does not oscillate.

In general, if the system oscillates, the input filter output impedance can be decreased as in most cases the approximated converter input impedance is dictated by the system specifications. This can be accomplished adding more capacitance or reducing the inductor value.
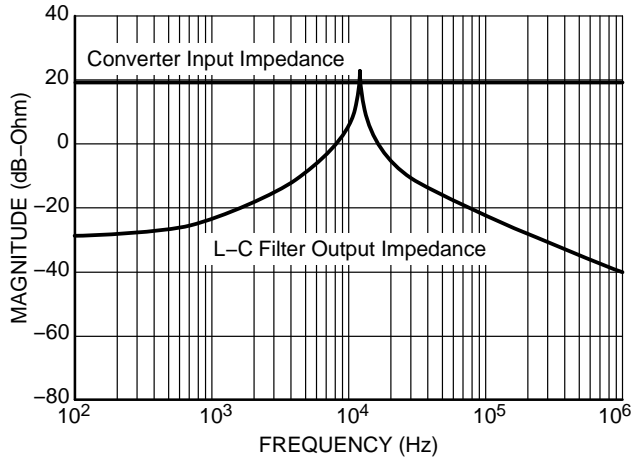
Figure 6. Input Filter Output Impedance and Approximated Converter Input Impedance

SYNCHRONOUS RECTIFICATION

The NCP1560 OUT2 can be easily configured to control a synchronous rectifier topology. Synchronous rectification uses MOSFETs as rectification elements instead of diodes D1 and D2 in Figure 1.

In the forward mode, the MOSFET internal body diode starts conducting current. Immediately after, the MOSFET is turned ON and current starts flowing through the channel of the MOSFET, instead of the body diode. The voltage drop is now significantly reduced, thus reducing power losses. In the reverse mode, the internal body diode blocks the current.

The synchronous rectifier topology can be operated in a self–driven or in an externally controlled mode. In either mode, care needs to be taken to prevent both MOSFETs from conducting simultaneously. If not, an excessive amount of current can be generated, possibly destroying the MOSFETs.

The nominal voltage across the secondary winding of TX2, V_{sec}, is calculated between 6.4 V and 15.6 V using (16). In addition, voltage spikes will be present during turn ON and turn OFF transitions due to parasitic elements.

$$V_{sec} = \left(V_{in} \times \frac{N_s}{N_p} \right) \qquad (16)$$

The minimum voltage of the secondary winding (6.4 V) is high enough to drive the gate of a logic level MOSFET. Therefore, X3 is moved to the bottom of the current path and operated in a self–driven configuration. X4 is controlled using OUT2. The secondary winding voltage determines the minimum breakdown voltage of MOSFETs X3 and X4. Also, it determines the minimum gate voltage of X3. The circuit schematic of the synchronous rectification circuit is shown in Figure 7 on the following page.
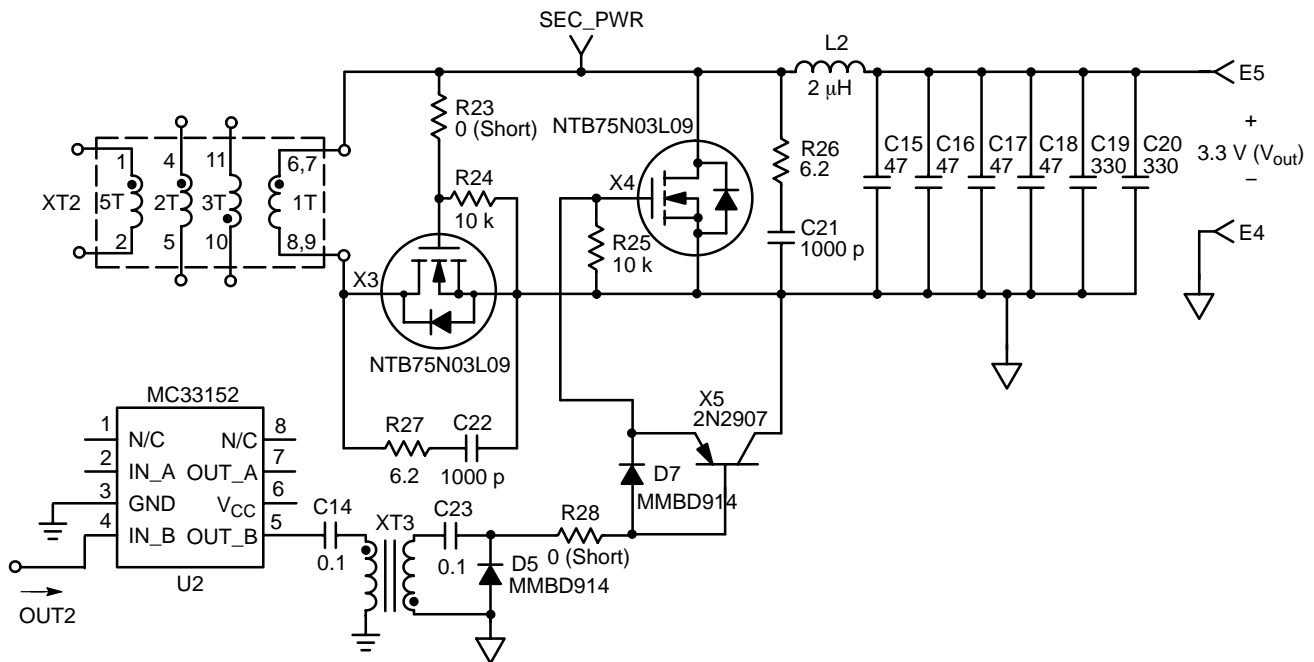
Figure 7. Synchronous Rectification Circuit

MOSFETs with a minimum breakdown voltage of 30 V, a maximum gate voltage of 20 V and a logic level input are required. The current capability of X3 and X4 need to be at least twice I_{out} to account for $R_{DS(on)}$ temperature variations and thermal limitations. In addition, a low $R_{DS(on)}$ MOSFET is preferred to reduce conduction losses. ON Semiconductor's NTB75N03L09 MOSFET is selected as it meets all the requirements.

The adjustable overlap delay of OUT2 prevents simultaneous conduction of the rectification elements. The maximum overlap delay, $t_{D(max)}$, is limited by the operating frequency and duty cycle as given in (17).

$$t_{D(max)} \le \frac{(1 - DC)}{2f} \qquad (17)$$

The propagation delay of the control signal and the response time of the synchronous rectifier circuit limit the minimum delay time. The overlap delay is set to approximately 100 ns by setting R5 to 110 kΩ.

Transformer TX3 transmits OUT2 across the isolation boundary. Also, OUT2 is inverted to turn ON X4 when the main switch is OFF. The control signal is AC coupled to TX3 using capacitors C14 and C23. Diode D5 clamps the output of TX3 at one diode drop below ground. The turn OFF response of X4 is improved using D7 and X5.

R−C snubbers are added across X3 and X4. The snubbers are comprised of C22 and R27, and R26 and C21.

OPTOCOUPLER AND V_{EA} CIRCUIT

The NCP1560 PWM Comparator modulates the duty cycle by comparing the Feedforward Ramp to the feedback signal from the error amplifier. The feedback signal is fed into the inverting input of the PWM Comparator through the V_{EA} pin. An optocoupler transmits the feedback signal across the isolation boundary.

The V_{EA} drive circuit is shown in Figure 8. It consists of a resistor divider from V_{REF} to ground. The low side resistor and a series diode are incorporated into the V_{EA} pin to reduce external component count. The series diode prevents the optocoupler from sinking current out the of V_{EA} pin.
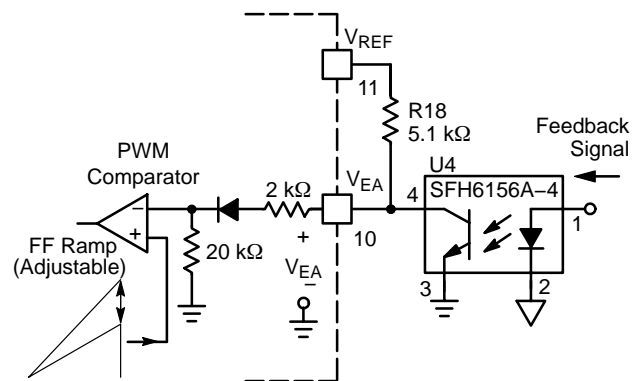

Figure 8. V_{EA} Drive Circuit

While the feedback signal is absent, the resistor divider sets the voltage on the V_{EA} pin. Once the feedback signal is present, the optocoupler, turns ON and the voltage on the V_{EA} pin is reduced.

The series diode and resistor divide the V_{EA} voltage before the signal is compared to the Feedforward Ramp. The minimum V_{EA} voltage is limited by the voltage drop of the series diode and is specified in the NCP1560 data sheet as $V_{EA(L)}$. The Feedforward Ramp limits the maximum V_{EA} voltage. Equation (18) shows the V_{EA} voltage range.

$$V_{EA(L)} \leq V_{EA} \leq \left(\frac{I_{FF} \times DC}{186.56 \text{ pF} \times f} \right) + V_{EA(L)} \quad (18)$$

FEEDBACK LOOP

The converter regulates the output voltage by adjusting the duty cycle using a negative feedback loop. If the loop is not stable, the converter will oscillate. To insure the loop is stable and has adequate transient response, the closed loop response should have a minimum phase margin of 45° under all line and load conditions. This is accomplished by shaping the open loop response using an error amplifier.

The block diagram shown in Figure 1 is used to evaluate the converter open loop frequency response.

The optocoupler sets the gain from point A to point B. The optocoupler anode is driven directly from the error amplifier output and the gain is measured at 30 dB with a pole at 10 kHz. If a limiting resistor, R33, is placed between the error amplifier output and the anode of the optocoupler, the gain is given in equation (19).

$$G_{OPTO} = \frac{R_{18} \times CTR}{R_{33}} \quad (19)$$

where, CTR is the optocoupler transfer ratio.

The optocoupler can be driven in an alternate configuration in which current is sink out instead of source in. To operate in that configuration, remove R9 and R33 and place R34 and D3.

The frequency response from the modulator input (point B) to the converter output (point C) is composed of 2 blocks, the modulator gain and the L−C Filter frequency response. The modulator gain is given in equation (20).

$$G_{MOD} = \frac{(C_{FF} \times f \times 125 \times (R_{FF} + 12 \text{ k}\Omega))}{\left(6.7 \times \frac{N_p}{N_s} \right)} \quad (20)$$

The L−C filter frequency response is given in equation (21).

$$H(f) = \frac{\left(s + \frac{1}{R_{ESR}C_{out}} \right)}{\left(s^2 \frac{L_{out}}{R_{ESR}} + s + \frac{1}{R_{ESR}C_{out}} \right)} \quad (21)$$

The L−C Filter has one zero and one double pole. The L−C filter corner frequency determines the pole location and is given in equation (22).

$$f_{p(LC)} = \frac{1}{2 \pi \sqrt{L_{out}C_{out}}} \quad (22)$$

The L−C filter zero frequency is given by (23). Using an ESR of 1 mΩ, the zero is calculated at 37.5 kHz.

$$f_{z(ESR)} = \frac{1}{2\pi R_{ESR}C_{out}} \quad (23)$$

The total open loop frequency response is the product (or the sum in dB) of the optocoupler gain, (20) and (21). The simulated open loop frequency response from A to C is shown in Figure 9.
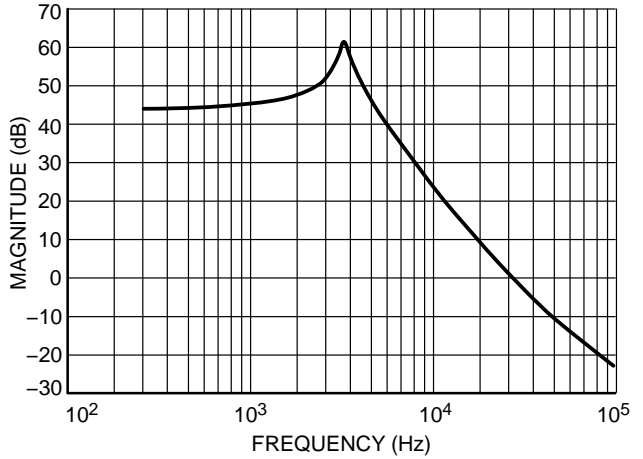

Figure 9. Simulated Open Loop Frequency Response

Several error amplifier configurations are available. A type III error amplifier, as the one shown in Figure 10, is selected for our converter as it provides adequate phase margin. A type III error amplifier has 3 poles and 2 zeros. One of the poles is at the origin. The frequency of the remaining poles and zeros are calculated using (24) through (27).
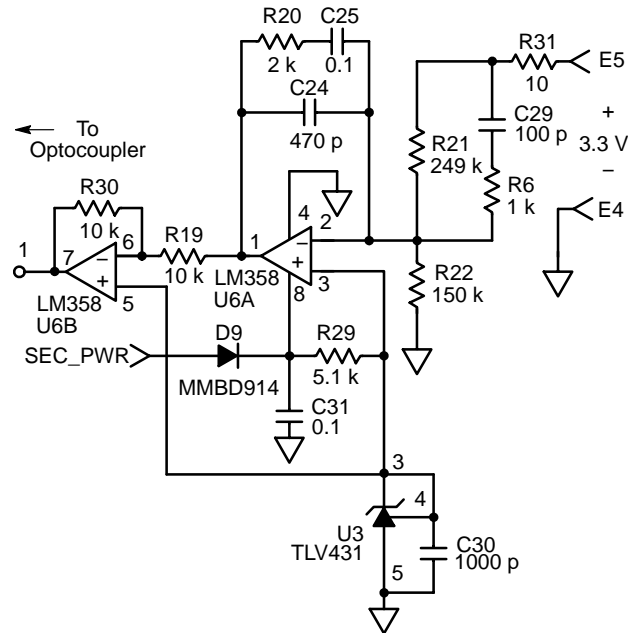

Figure 10. Type III Error Amplifier

The additional inverting stage is added to drive the optocoupler using the correct polarity. The error amplifier poles and zeros are selected to achieve the desired crossover frequency.

$$f_{p2} = \frac{1}{2\pi R_{20}(C_{24} \parallel C_{25})} \qquad (24)$$

$$f_{p3} = \frac{1}{2\pi C_{29} R_6} \qquad (25)$$

$$f_{z1} = \frac{1}{2\pi R_{20} C_{25}} \qquad (26)$$

$$f_{z2} = \frac{1}{2\pi C_{29}(R_6 + R_{21})} \qquad (27)$$

On Semiconductor's TLV431 is used to generate the error amplifier reference voltage, V_{REF}. The reference voltage is set at 1.25 V to eliminate the need of additional components.

The selection of the compensation network components begins by noting that the voltage on the node between R21 and R22 equals V_{REF} when the output is in regulation. The values selected for R21 and R22 are 249 kΩ and 150 kΩ, respectively. Resistor R31 is added to provide a test point to measure the open loop frequency response. It is set at 10 Ω to avoid disrupting the DC bias point.

The selected crossover frequency, f_{CO}, is 10 kHz. The error amplifier gain is set to –42 dB using (28) to achieve an approximated closed loop gain of 0 dB at f_{CO}.

$$G_{EA} = 20 \log\left(\frac{R_{20}}{R_{21}}\right) \qquad (28)$$

Resistor R20 is set to 2 kΩ. Zeros, f_{z1} and f_{z2}, are placed before and after the L–C filter corner frequency to cancel the phase lag and attenuation of the filter double pole. In addition, the zeros are placed before f_{CO} to cross 0 dB with a slope of –20 dB/dec. Poles f_{p2} and f_{p3} are used to cancel the ESR zero and attenuate high frequency noise, respectively. Table 4 summarizes the system gain, poles and zeros location.

Table 4. System Poles and Zeros Location

Parameter	Frequency (kHz)	Magnitude (dB)
$f_{p(LC)}$	3.867	–
$f_{z(ESR)}$	37.5	–
$f_{p(opto)}$	10	–
f_{p1}	0	–
f_{p2}	170.2	–
f_{p3}	1592.4	–
f_{z1}	0.796	–
f_{z2}	6.369	–
G_{MOD}	–	14.19
G_{OPTO}	–	30.0
G_{EA}	–	–41.9

The phase contribution of a zero and a pole at the crossover frequency are given in equations (29) and (30), respectively.

$$\theta_{zero} = \tan^{-1}\left(\frac{f_{CO}}{f_z}\right) \qquad (29)$$

$$\theta_{pole} = -\tan^{-1}\left(\frac{f_{CO}}{f_p}\right) \qquad (30)$$

The phase margin, θ_M, is evaluated taking into account the phase contribution of all the poles and zeros as shown below:

$$\theta_M = 180° - 2\theta_{LC} - \theta_{p1} + \theta_{z1} + \theta_{z2} + \theta_{opto} + \theta_{ESR} \quad (31)$$

$$\theta_M = 180° - 138° - 90° + 85.4° + 57.5° - 45° + 15°$$

$$= 65°$$

for a total phase margin of 65°. The poles and zeros 1 decade beyond f_{CO} do not contribute to the phase at the crossover frequency.

The error amplifier supply voltage (V_{CC}) is generated from node "SEC_PWR" using a peak detector comprised of D9 and C31. The voltage of node "SEC_PWR" is calculated between 6.4 V and 15.6 V using equation (16). The error amplifier is implemented using ON Semiconductor's LM358 as it can operate from the available single voltage supply. Also, the LM358 has a small input offset voltage and low input bias current.

The TLV431 supply current is generated using a resistor, R29, from V_{CC}. The minimum cathode current, assuming a voltage drop of 0.7 V across D9 is 1.1 mA. It exceeds the TLV431 recommended minimum current of 80 μA. A low pass filter, comprised of C30 and R29 reduces high frequency noise and voltage ripple.

CURRENT LIMIT CIRCUIT

The converter delivers 100 W under normal operating conditions. However, if a short circuit or fault is present, the current needs to be limited to protect the load and the converter. This is easily accomplished using the NCP1560 dual mode over−current protection. A current sense circuit is implemented using a current transformer. The transformer senses the primary current and generates a proportional voltage. The current sense circuit is shown in Figure 11.
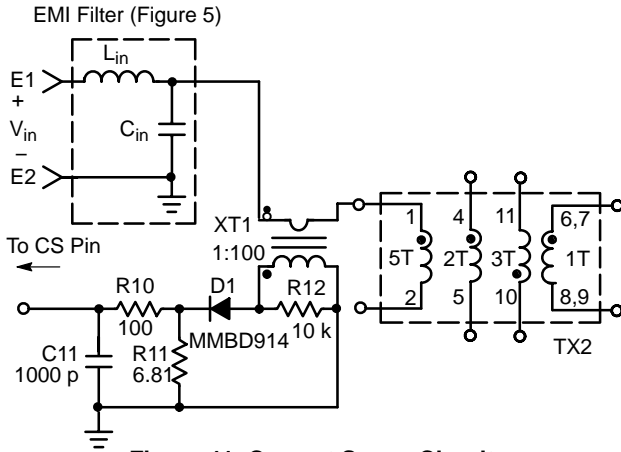

Figure 11. Current Sense Circuit

The target power dissipation, P_D, of the current sense circuit is 50 mW. Using $I_{P(PK)}$ calculated earlier, the turns of the current sense transformer are determined using (32)

$$n = \frac{I_{P(PK)}}{\left(\dfrac{P_D}{DC \times (V_f + I_{LIM1})}\right)} \qquad (32)$$

where, V_f is the forward drop of D1 and I_{LIM1} is the cycle by cycle current limit threshold. The sense voltage is generated across R11. The value of R11 is selected using (33). A load resistor, R12, is added to load the transformer during the OFF time.

$$R_{11} = \frac{I_{LIM1} \times n}{I_{P(PK)}} \qquad (33)$$

The converter will enter the cycle skip current mode if a severe overload or short is present. While in the cycle skip mode, the converter will not switch for a time period determined by the cycle skip timer. Switching is allowed once the cycle skip timer expires and V_{AUX} reaches 11 V. The cycle skip capacitor, C28, is set at 1000 pF for a minimum OFF time of 162 μs.

A low pass filter, comprised of R10 and C11, attenuates high frequency noise and avoids false triggering of the current limit circuit. The cutoff frequency of the filter is given in equation (34). The cutoff frequency is selected 5 times higher than the operating frequency of the converter to provide high frequency attenuation without interfering with the converter operation. It is set at 1.6 MHz.

$$f = \frac{1}{2\pi R_{10} C_{11}} \qquad (34)$$

UNDER/OVERVOLTAGE LOCKOUT

The NCP1560 eliminates the need for additional supervisory circuits by incorporating an internal under/ overvoltage (UV/OV) detector. The UV/OV detector enables the controller when the voltage on the UV/OV pin is within 1.52 V and 3.61 V. The UV/OV bias circuit is shown in Figure 12. A resistor divider, consisting of R1 and R4, bias the UV/OV detector.
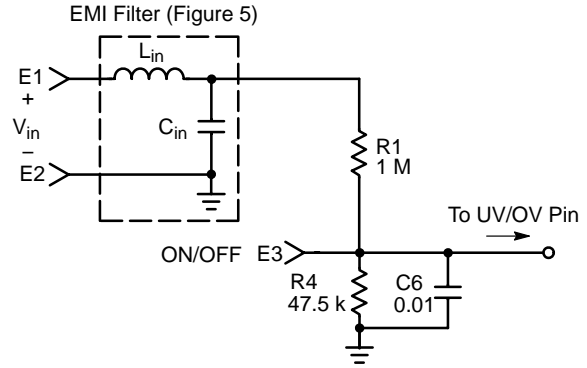

Figure 12. UV/OV Bias Circuit Network

A 10 nF capacitor, C6, across R4 reduces noise and provides a stable voltage during turn ON and turn OFF transitions. The UV detector turns ON the converter at 33.52 V. The turn OFF voltage (V_{in} decreasing) is determined by $V_{UV(H)}$. The turn OFF voltage is 31.31 V. The OV detector turns OFF the converter at 79.61 V. The turn ON voltage (V_{in} decreasing) is determined by $V_{OV(H)}$. The turn ON voltage is 76.3 V.

MAXIMUM DUTY CYCLE

The converter is designed to operate at a maximum duty cycle of 60%. However, under transient conditions as well as input voltage variations, the converter may require a higher duty cycle to quickly respond to load changes. If the duty cycle is not controlled, the transformer may saturate.

The internal NCP1560 duty cycle limit is configured without using additional components by using its preset limits. This is accomplished by grounding the DC_{MAX} pin and selecting the feedforward resistor, R_{FF}, accordingly (refer to ON Semiconductor's data sheet NCP1560/D). Grounding the DC_{MAX} pin sets $V_{DC(inv)}$ to 0.888 V. The feedforward current and resistor are calculated using (35) and (36), respectively.

$$I_{FF} = \frac{C_{FF} \times V_{DC(inv)} \times f \times 125\text{ k}\Omega}{6.7\text{ k}\Omega \times DC} \qquad (35)$$

$$I_{FF} = \frac{10\text{ pF} \times 0.8888\text{ V} \times 260\text{ kHz} \times 125\text{ k}\Omega}{6.7\text{ k}\Omega \times 0.6} = 71.86\text{ μA}$$

$$R_{FF} = \frac{V_{in(min)}}{I_{FF}} - (6.7\text{ k}\Omega + 5.6\text{ k}\Omega) \qquad (36)$$

$$R_{FF} = \frac{32\text{ V}}{71.86\text{ μA}} - (6.7\text{ k}\Omega + 5.6\text{ k}\Omega) \approx 433\text{ k}\Omega$$

The feedforward resistor is set to 487 kΩ to account for component and temperature variations.

SOFT−START

Soft−start allows the converter to turn ON in a controlled manner. The NCP1560 soft−start control is adjusted by placing an external capacitor, C_{SS}, between the SS pin and ground. The soft−start control is present while the C_{SS} voltage is below 2.0 V.

The converter will not turn ON if the soft−start period, t_{SS}, is longer than the time it takes C_{AUX} (C7) to discharge to 7.0 V. Once t_{SS} is determined, the soft−start capacitor is calculated using (37).

$$C_{SS} \leq \frac{6.2\ \mu A \times t_{SS}}{2\ V} \qquad (37)$$

The soft−start capacitor is set at 2200 pF, for a period of 0.71 ms.

OSCILLATOR FREQUENCY

The oscillator frequency is set at 275 kHz by setting R_T (R7) to 110 kΩ. The oscillator frequency varies linearly with the resistor value, therefore, the tolerance of R_T is set at 1%.

LAYOUT CONSIDERATIONS

Switching regulators can be noisy! However, with careful layout, noise is reduced. A few things to remember are:

1. Keep switching elements and high current traces away from the controller and sensitive nodes.
2. Keep trace lengths to a minimum, especially important for high current paths.
3. Use wide traces for high current paths.
4. Place bypass capacitors close to the components.
5. Use a ground plane if possible or a single point ground system.

The converter is built using a 4 layer FR4, single side board. The converter footprint is 2.5 in x 3.0 in. The components location within the board is shown in Figure 13 and the complete circuit schematic is shown in Figure 14. The Bill of Material is listed in Table 5.

The layout files are available. Please contact your sales representative for more information.
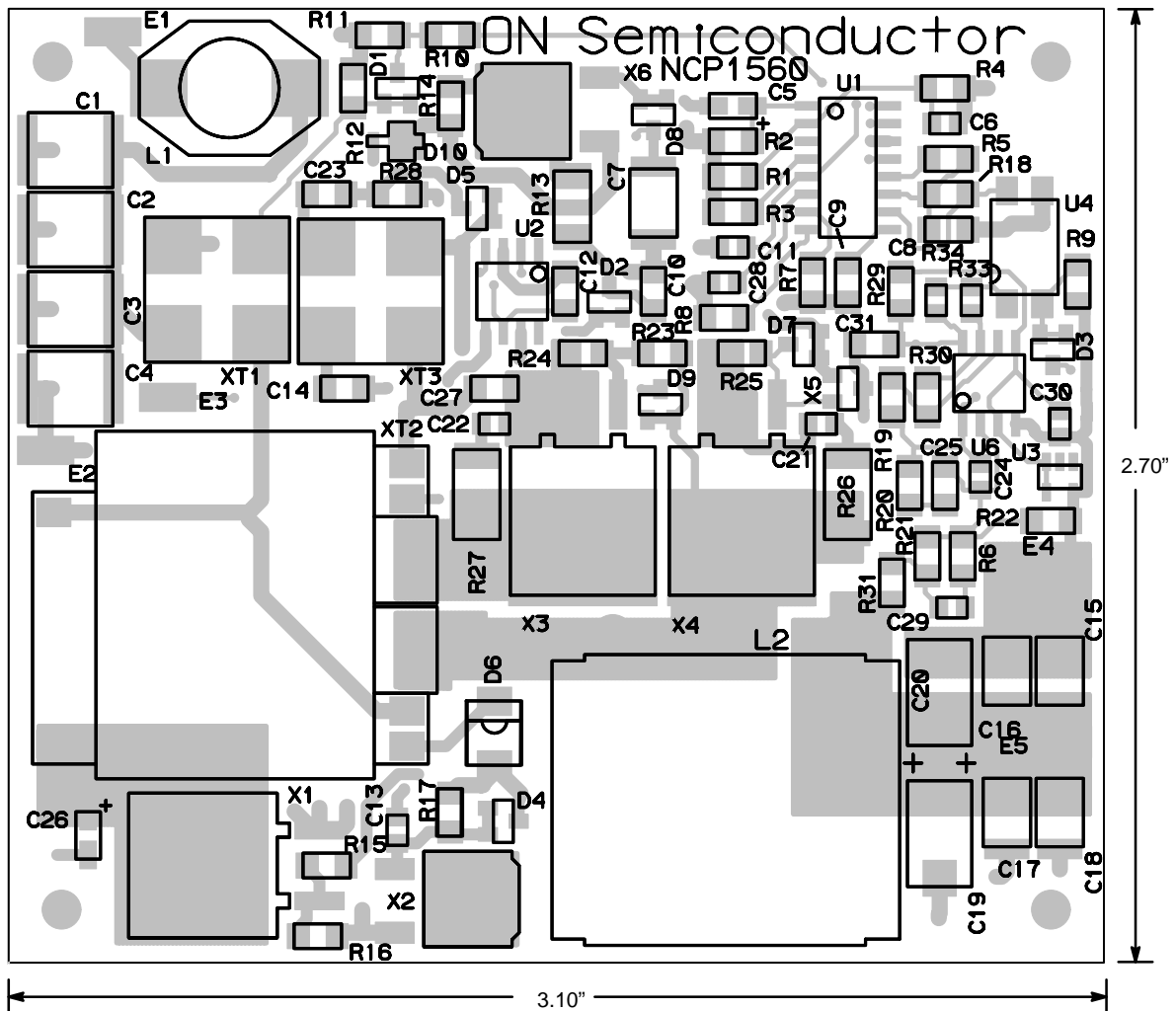
Figure 13. Board Arrangement

Figure 14. Complete Circuit Schematic
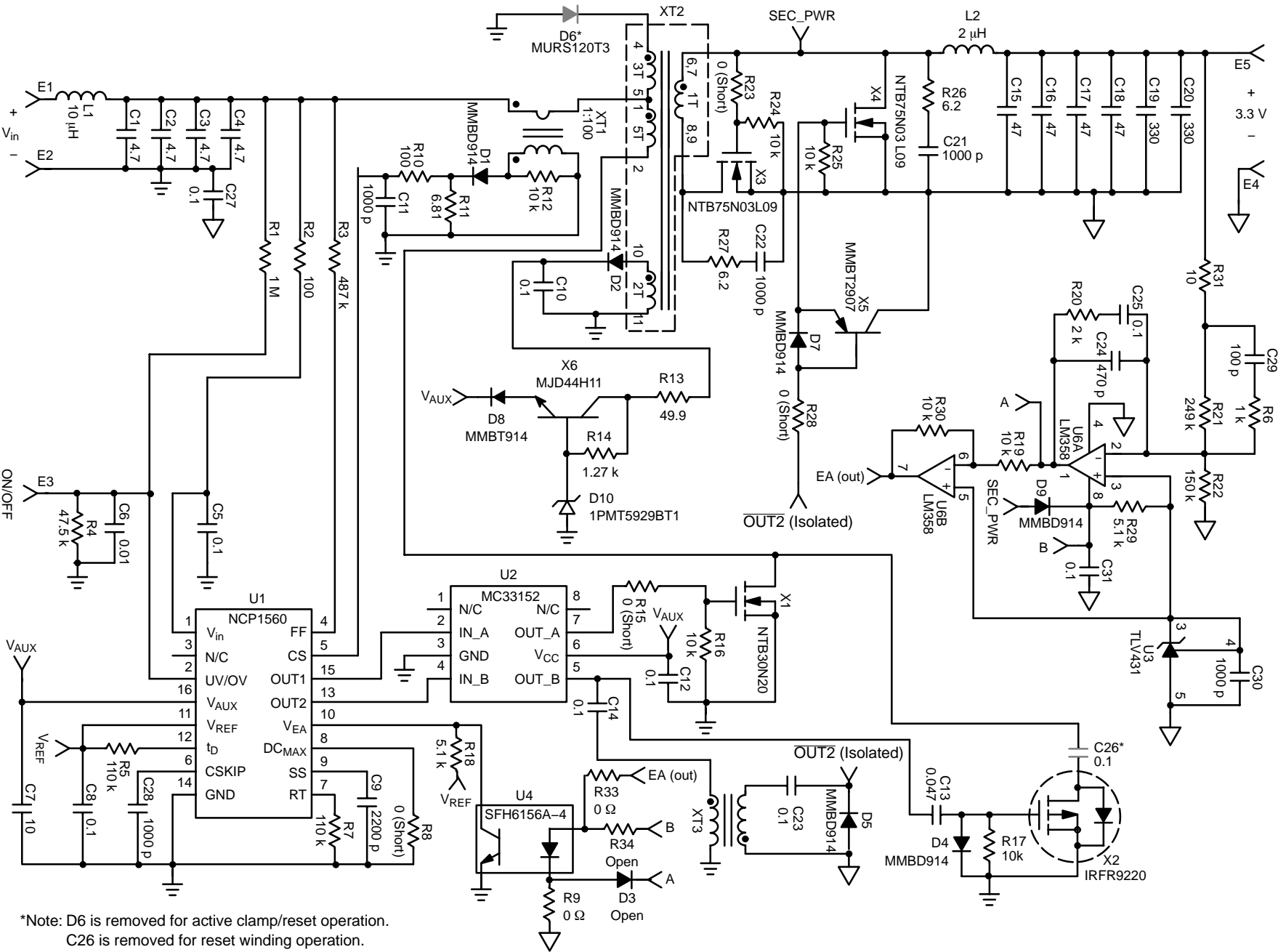
*Note: D6 is removed for active clamp/reset operation.
C26 is removed for reset winding operation.

Table 5. BILL OF MATERIALS

Quantity	Reference	Part/Description	Value	Vendor	Notes
4	C1 – C4	CKG5750DX7R2A475M	4.7 μF, 100 V	TDK (Note 1)	–
5	C11, C21, C22, C28, C30	C0805C102K1RAC	1000 pF, 100 V	KEMET	–
1	C5	C3216X7R2A104K	0.1 μF, 100 V	TDK (Note 1)	–
1	C6	C0805C103K5RAC	0.01 μF, 50 V	KEMET	–
1	C7	C4532X7R1E106M	10 μF, 25 V	TDK (Note 1)	–
8	C8, C10, C12, C14, C23, C25, C27, C31	C1206C104K5RAC	0.1 μF, 50 V	KEMET	–
1	C9	VJ1206Y222KXXA	2200 pF, 25 V	Vishay Vitramon (Note 2)	–
1	C13	C2012X7R2A473	0.047 μF, 100 V	TDK (Note 1)	–
4	C15 – C18	C4532X5R0J476M	47 μF, 6.3 V	TDK (Note 1)	–
2	C19 – C20	T495X337K006AS	330 μF, 6.3 V	KEMET	–
1	C24	C0805C471J1GAC	470 pF, 100 V	KEMET	–
1	C26	C3216X7R2E104M	0.1 μF, 250 V	TDK (Note 1)	–
1	C29	C0805C101J1GAC	100 pF, 100 V	KEMET	–
7	D1, D2, D4–D5, D7–D9	MMBD914LT1	–	ON Semiconductor	High Speed Diode
1	D3	MMBD914LT1	–	ON Semiconductor	Do not place
1	D10	1PMT5929BT1	–	ON Semiconductor	15 V Zener
1	D6	MURS120T3	–	ON Semiconductor	Do not place, 200 V
1	R1	CRCW1206105J	1.0 MΩ	Vishay Dale (Note 2)	–
2	R2, R10	CRCW1206101J	100 Ω	Vishay Dale (Note 2)	–
1	R3	CRCW12064873F	487 kΩ	Vishay Dale (Note 2)	–
1	R4	CRCW12064752F	47.5 kΩ	Vishay Dale (Note 2)	–
1	R5, R7	CRCW12061103F	110 kΩ	Vishay Dale (Note 2)	–
1	R6	CRCW1206102J	1.0 kΩ	Vishay Dale (Note 2)	–
4	R8, R9, R15, R23, R28	CRCW1206000ZJ	0 Ω	Vishay Dale (Note 2)	Short
1	R11	CRCW12066R81F	6.81 Ω	Vishay Dale (Note 2)	–
7	R12, R16, R17, R19, R24, R25, R30	CRCW12061002F	10 kΩ	Vishay Dale (Note 2)	–
1	R13	CRCW201249R9J	49.9	Vishay Dale (Note 2)	0.5 W
1	R14	CRCW12061271F	1.27 kΩ	Vishay Dale (Note 2)	–
2	R18, R29	CRCW1206512J	5.1 kΩ	Vishay Dale (Note 2)	–
1	R20	CRCW1206202J	2.0 kΩ	Vishay Dale (Note 2)	–
1	R21	CRCW12062493F	249 kΩ	Vishay Dale (Note 2)	–
1	R22	CRCW12061503F	150 kΩ	Vishay Dale (Note 2)	–
2	R26, R27	CRCW25126R2J	6.2 Ω	Vishay Dale (Note 2)	1.0 W
1	R31	CRCW1206100J	10 Ω	Vishay Dale (Note 2)	–
1	R33	CRCW0805000Z5	0 Ω	Vishay Dale (Note 2)	–
1	R34	CRCW1206512J	5.1 kΩ	Vishay Dale (Note 2)	Do not place
1	XT1	CS105	–	Vanguard Electronics	Current Transformer
1	XT2	9452 (Custom)	–	Payton America	Power Transformer
1	XT3	GD103	–	Vanguard Electronics	Isolation Transformer
1	U1	NCP1560HDR2	–	ON Semiconductor	PWM Controller
1	U2	MC33152D	–	ON Semiconductor	Dual MOSFET Driver
1	U3	TLV431ASNT1	–	ON Semiconductor	Voltage Regulator
1	U4	SFH6156–4	–	Vishay, Infineon (Note 2)	Optocoupler

1. TDK components can be ordered at 847–803–6100.
2. Vishay Components can be ordered at 402–563–6866.

Table 5. BILL OF MATERIALS (continued)

Quantity	Reference	Part/Description	Value	Vendor	Notes
1	U6	LM358D	–	ON Semiconductor	Dual Op Amp
1	X1	NTB30N20	–	ON Semiconductor	Power MOSFET, 200 V
1	X2	IRFR9220	–	International Rectifier	Power MOSFET, 200 V
2	X3, X4	NTB75N03L09	–	ON Semiconductor	Power MOSFET, 30 V
1	X5	MMBT2907AWT1	–	ON Semiconductor	PNP Transistor, 60 V
1	X6	MJD44H11	–	ON Semiconductor	NPN Transistor, 80 V
1	L1	DO3316–103	10 μH	Coilcraft	Input Choke
1	L2	9453 (Custom)	2.0 μH	Payton America	Output Choke

DESIGN VERIFICATION

The final step in our design includes validation and test of the converter. Before powering the converter, it should be inspected for potential problems. A few suggestions include:

1. Verify all connections. Check for shorts and opens, especially on the input and output terminals.
2. Verify component values.
3. Slowly increase the input voltage to 25 V while monitoring the input current. If the input current is above 25 mA, repeat steps 1 to 3.
4. Once the input voltage reaches 25 V, measure the voltage on critical nodes. The NCP1560 startup regulator should be ON. If the voltages are not correct, remove power and repeat steps 1 to 3.
5. Increase the input voltage to 36 V. Measure the output voltage. If it is not 3.3 V, repeat steps 1 to 3.
6. Increase the input voltage to 80 V. The output should turn OFF.

Please be careful when probing and testing the converter. High voltage may be present. Exercise CAUTION!

Once the converter functionality is verified, the board performance is evaluated and compared to our original goals. The evaluation criteria include:

1. Open loop frequency response.
2. Efficiency.
3. Line and load regulation.
4. Step load response.
5. Output voltage ripple.

The open loop response is measured injecting an AC signal across R31 using a network analyzer and an isolation transformer as shown in Figure 15. The open loop response is the ratio of B to A.
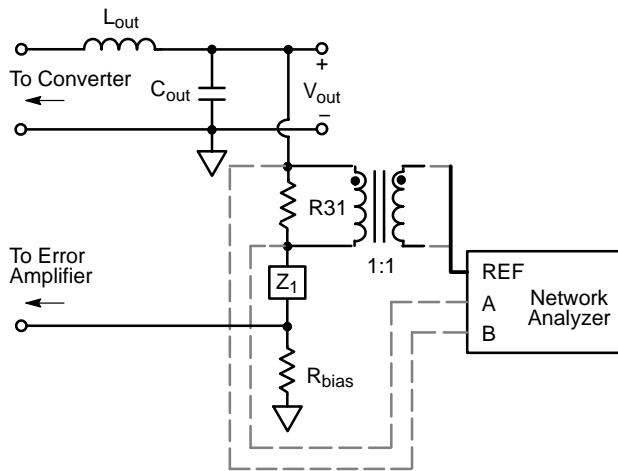
Figure 15. Open Loop Frequency Response Measurement Setup

The measured open loop response is shown in Figure 16. The measured phase margin is 57° and the crossover frequency is 11 kHz. The ringing observed in Figure 9 at $f_{p(LC)}$ is significantly reduced. The ringing is damped by the loop gain because the crossover frequency is beyond the L–C filter corner frequency.
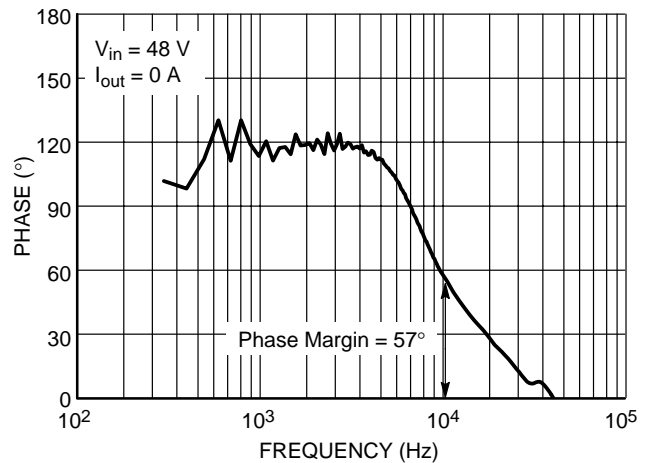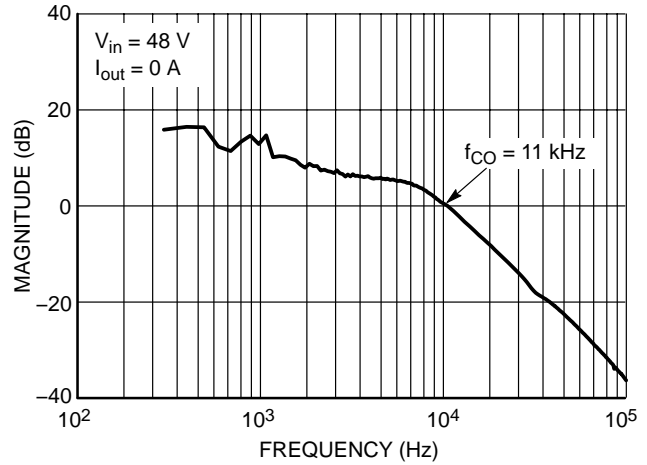
Figure 16. Open Loop Frequency Response

The peak efficiency is typically measured at 90%. Figure 17 shows the efficiency vs output current under several operating conditions.
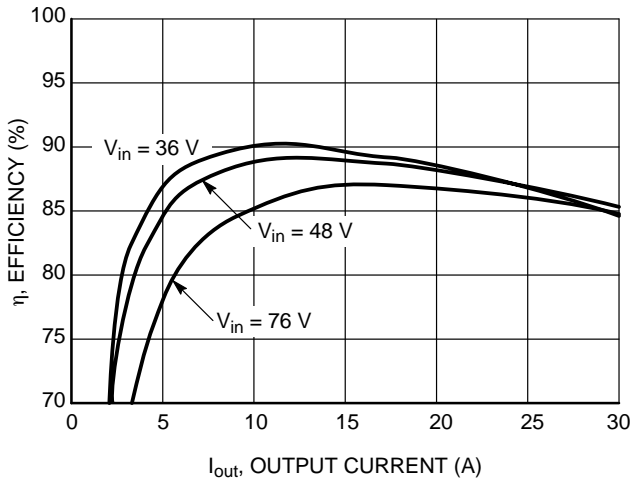
Figure 17. Efficiency vs. Output Current

Line and load regulation are calculated using (38) and (39), respectively. Line regulation is measured below 0.003% and load regulation is measured below 0.8%.

$$\text{Reg}_{\text{LINE}} = \frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{IN}}} \qquad (38)$$

$$\text{Reg}_{\text{LINE}} = \frac{V_{\text{OUT (No load)}} - V_{\text{OUT (Full load)}}}{V_{\text{OUT (No load)}}} \qquad (39)$$

The dynamic response of the converter is evaluated stepping the load current from 50% to 75% and from 75% to 50% of $I_{\text{out(max)}}$. The output voltage responses are shown in Figures 18 and 19.
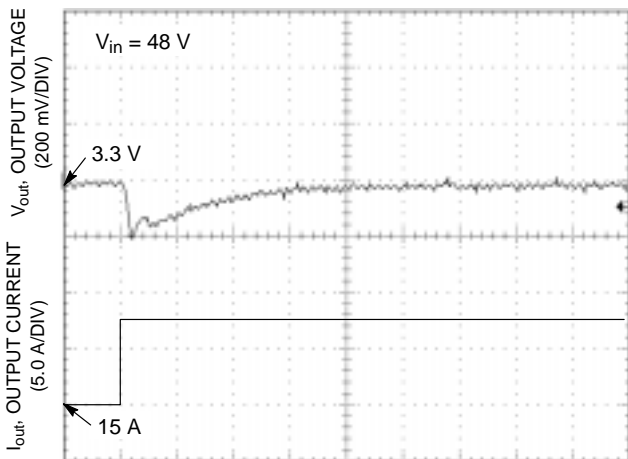
Figure 18. Output Voltage Response to a Step Load from 15 A to 22.5 A
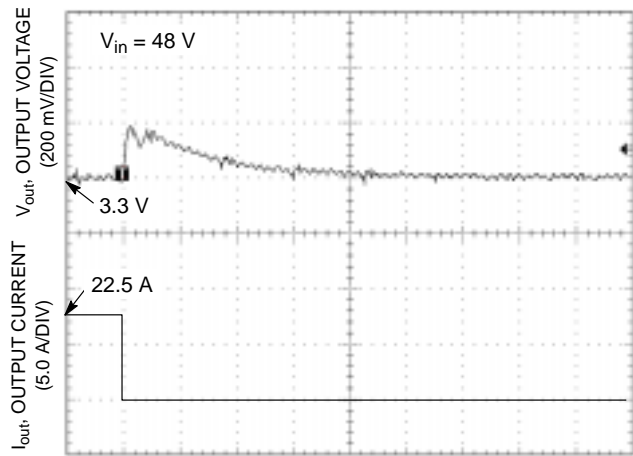
Figure 19. Output Voltage Response to a Step Load from 22.5 A to 15 A

The output voltage ripple is measured at 16 mV for an output current of 15 A. It is significantly below the 50 mV target. The output voltage ripple waveform is shown in Figure 20.
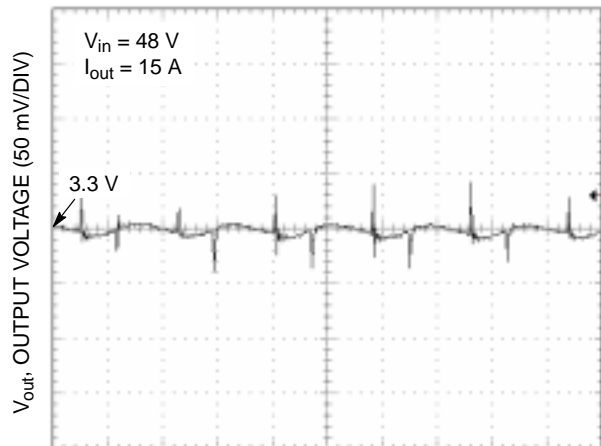
Figure 20. Output Voltage Ripple

SUMMARY

A 100 W converter is designed and built using the NCP1560. The converter provides excellent transient response. Output voltage ripple is measured at 16 mV. Phase margin and crossover frequency are measured at 57° and 11 kHz, respectively.

REFERENCES

1. Pressman, Abraham I. Switching Power Supply Design. 2nd ed. New York, NY: MacGraw Hill.
2. Ridley, Ray. "The Evolution of Power Electronics." Switching Power Magazine Fall 2001:16−30.
3. Tuttle, Wayne H. 1986. "The Relationship of Output Impedance to Feedback Loop Parameters."PCIM November: 90−97.
4. Ridley, Ray. 2002. Power Supply Design Workshop. Alpharetta, GA: Ridley Engineering.