# FS98O11
# Data Sheet

8-bit MCU with 14-bit ADC and GPIOs

*Rev. 0.1*
*Oct., 2005*

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# 1. General Description

The FS98O11 is a 8-bit high performance and cost-efficient microcontroller, 7-channel 14-bit sigma-delta ADC, and 16-bit general purpose I/O port. The device is suited for use in low power measurement and control applications such as: NiMH charger…etc.

# 2. Features

## 2.1 High Performance RISC CPU

- 8-bit single chip microcontroller(MCU).
- Embedded 2k x 16 bits program memory with one-time programmable (OTP) ROM.
- 128-byte data memory (SRAM).
- Only 37 single word instructions to learn
- 6-level memory stacks.

## 2.2 Peripheral Features

- 16-bit bi-directional I/O port.
- Charger current control.
- I2C serial I/O port (slave mode only).
- 7-channel 14-bit fully differential input analog to digital converter(ADC)

## 2.3 Analog Features

- 7-channel Sigma-Delta ADC with programmable output rate and resolution.

## 2.4 Special Microcontroller Features

- Embedded Low Voltage Reset (LVR).
- Embedded voltage regulator (3.6V regulated output).
- 3 Interrupt sources.
- Watchdog timer (WDT).
- Embedded 4.0 MHz oscillator.

## 2.5 CMOS Technology

- Voltage operation ranges from 3.6V to 6.0V.

# 3. Applications

- **ADC measure and I/O controls.**
- **NiMH/NiCd charger.**

# 4. Ordering Information

➢ Table 4-1: Ordering Information

| Product Number | Description | Package Type |
|---|---|---|
| FS98O11 | MCU with OTP ROM; The customer has to program the compiled hex code into OTP ROM. | 24-pin Dice form |
| FS98M11-nnnV | MCU with program type; FSC programs the customer's compiled hex code into EPROM at factory before shipping. | 24-pin Dice form |

Note1: Code number (nnnV) is assigned for customer.

Note2: Code number (nnn = 001~999); Version (V = A~Z).

## 5. Functional Block Diagram

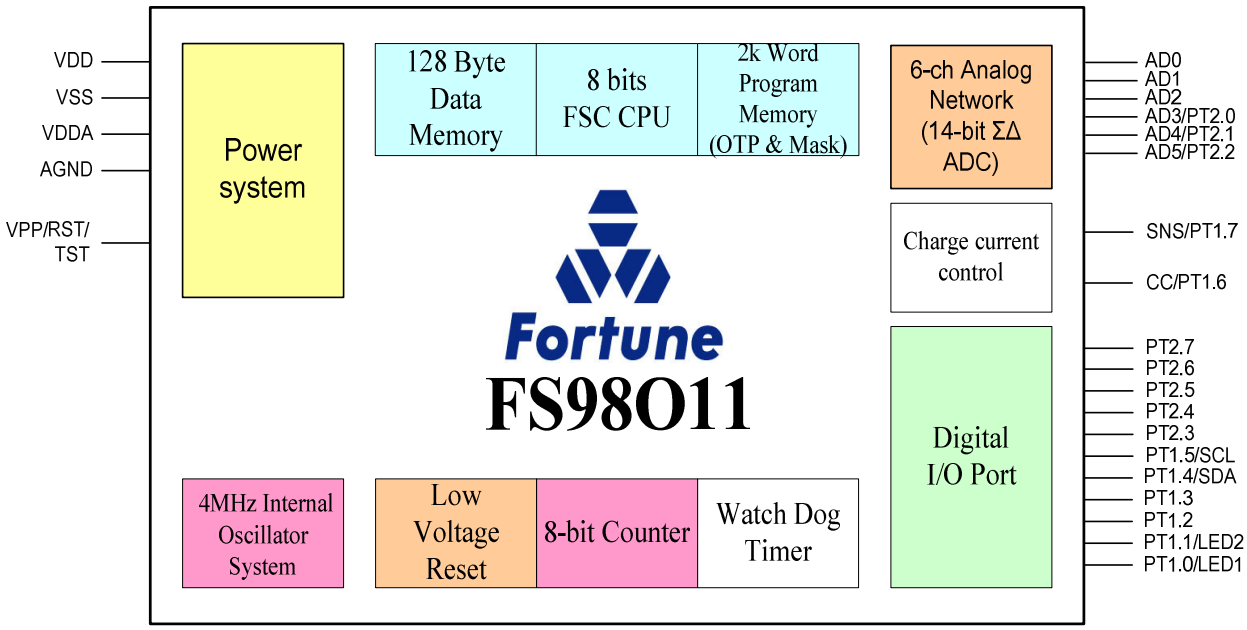
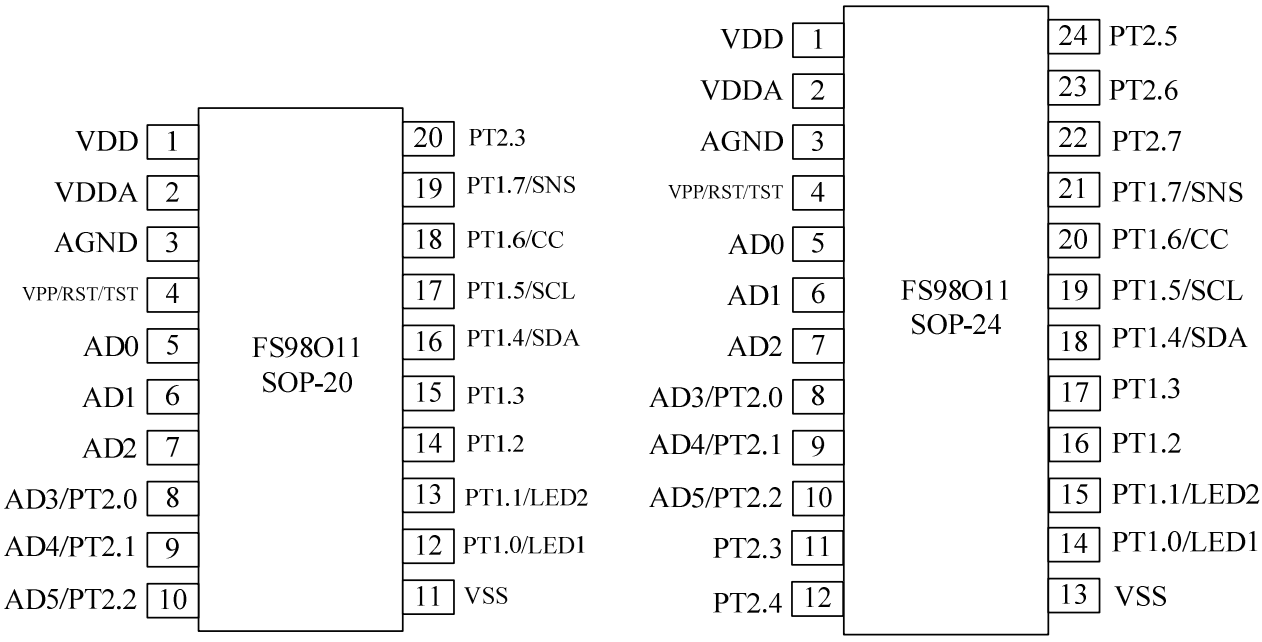



Figure 5-1: FS98O11 functional block

## 6. Pin Assignment



# 7. Pin Description

| Name | Function | Input type | Description |
|---|---|---|---|
| VDD | VDD | PWR | Positive power supply for logic and I/O pins |
| VSS | VSS | PWR | Ground reference for logic and I/O pins |
| VDDA | VDD | PWR | Positive power supply for analog |
| AGND | AGND | PWR | Ground reference for analog |
| VPP/RST/TST | VPP | PWR | The OTP ROM programming power |
| | RST | | Reset pin. |
| | TST | | Test pin |
| PT1.0/LED1 | PT1.0 | TTL | General I/O pin. |
| | LED1 | | Source or sink LED1 display. |
| PT1.1/LED2 | PT1.1 | TTL | General I/O pin. |
| | LED1 | | Source or sink LED2 display. |
| PT1.2 & PT1.3 | | TTL | General I/O pin. |
| PT1.4/SDA | PT1.4 | | General I/O pin. |
| | SDA | ST | Serial data I/O for I2C. |
| PT1.5/SCL | PT1.5 | | General I/O pin. |
| | SCL | ST | Serial clock I/O for I2C. |
| PT1.6/CC | PT1.6 | OD | General I/O pin. |
| | CC | ST | Charge current control output |
| PT1.7/SNS | PT1.7 | TTL | General I/O pin. |
| | SNS | AN | Current sensing using an external sensing resistor $R_{SNS}$ |
| AD0 | AD0 | AN | Analog channel 0 input. |
| AD1 | AD1 | AN | Analog channel 1 input. |
| AD2 | AD2 | AN | Analog channel 2 input. |
| AD3/PT2.0 | AD3 | AN | Analog channel 3 input. |
| | PT2.0 | TTL | General I/O pin. |
| AD4/PT2.1 | AD4 | AN | Analog channel 4 input. |
| | PT2.1 | TTL | General I/O pin. |
| AD5/PT2.2 | AD5 | AN | Analog channel 5 input. |
| | PT2.2 | TTL | General I/O pin. |
| PT2.3~PT2.7 | | TTL | General I/O pin. |

**Legend:** TTL= TTL input buffer, ST= Schmitt trigger input buffer, AN= Analog channel, OD= Open drain output, PWR= Power pin.

# 8. Typical Application Circuit

## 8.1 NI-MH Batteries Parallel Charging Application Circuit

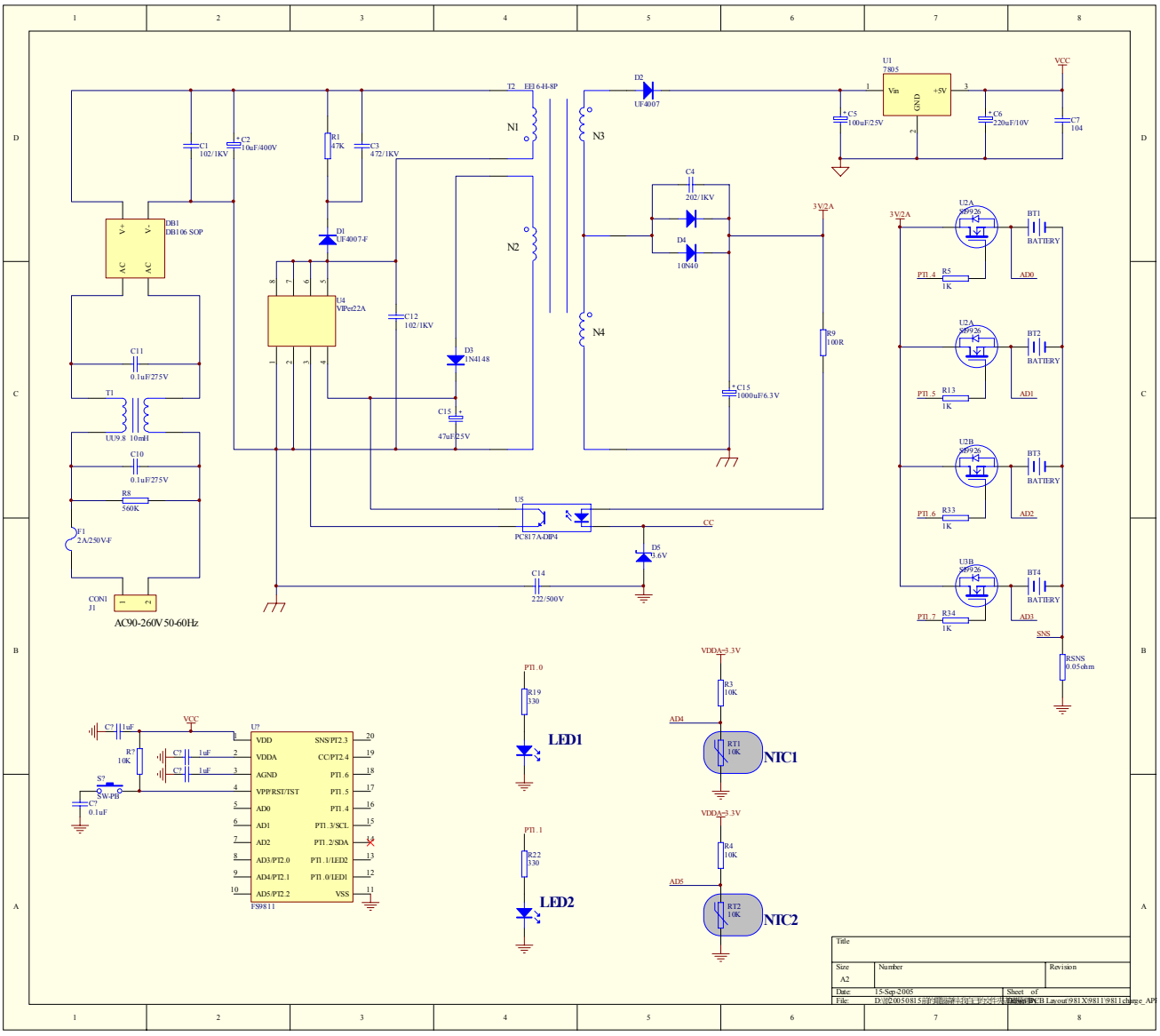



Figure 8-1: FS98O11 application circuit Ⅰ

## 8.2 NI-MH Batteries Serial Charging Application Circuit

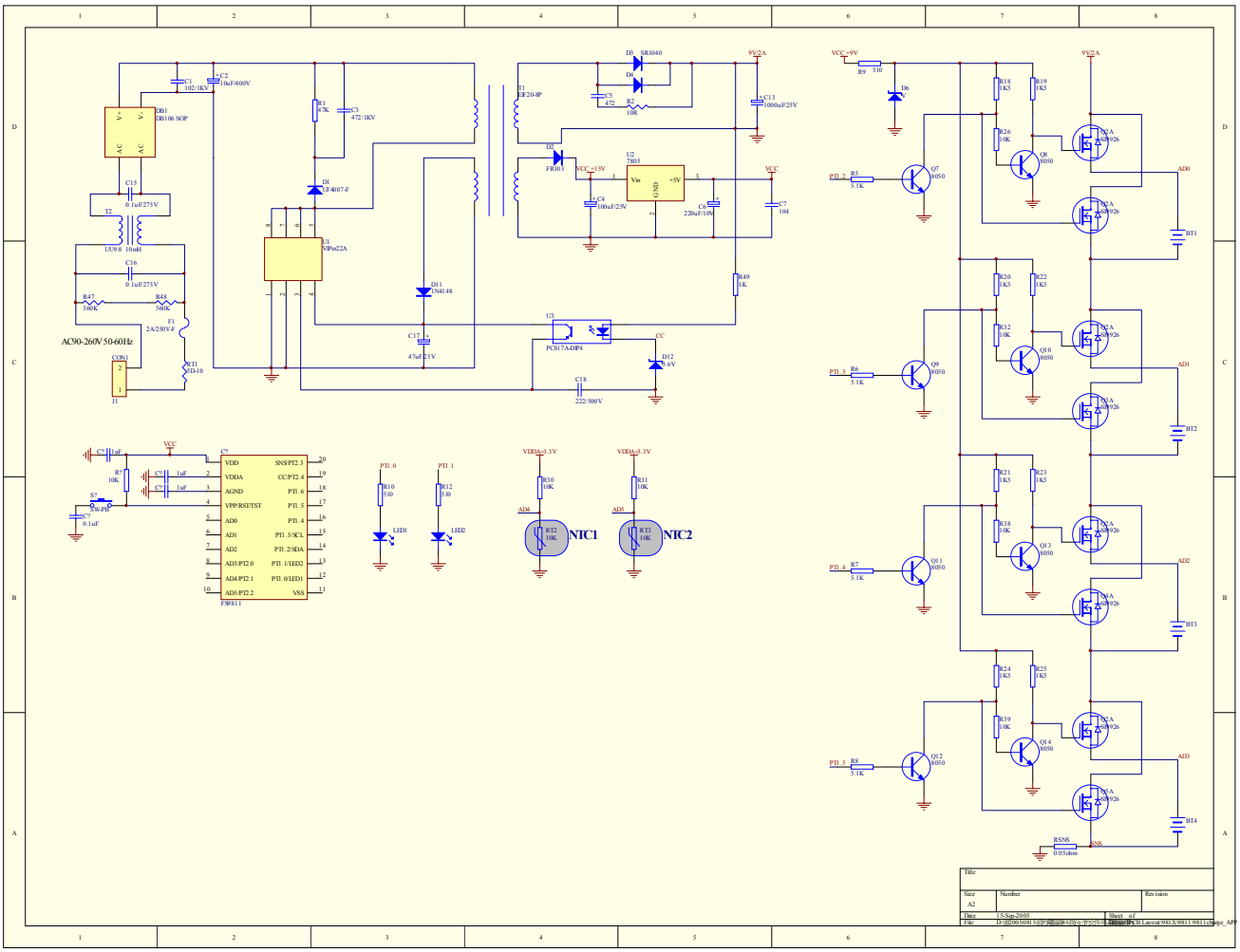



Figure 8-2: FS98O11 application circuit Ⅱ

# 9. Electrical Characteristics

## 9.1 Absolute Maximum Ratings

| Parameter | Rating | Unit |
|---|---|---|
| Supply Voltage to Ground Potential | -0.3 to 6.0 | V |
| Applied Input/Output Voltage | VSS-0.3 to VDD+0.3 | V |
| Ambient Operating Temperature | 0 to +70 | °C |
| Storage Temperature | -55 to +150 | °C |
| Soldering Temperature, Time | 260°C, 10 Sec | |

# 10. Electrical Characteristics

## 10.1 DC Characteristics (VDD=3.3V, $T_A$=25℃, unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VDD | Recommend Operation Power Voltage | For MCU only | 2.2 | | 6.0 | V |
| | | For Reference Voltage | 3.6 | | 6.0 | |
| IDD1 | Supply Current 1 | | | 1.5 | | mA |
| IDD2 | Supply Current 2 | Internal Oscillator Off, | | 1.5 | | μA |
| IPO | Sleep Mode Supply Current | Sleep Instruction | | 1.5 | | μA |
| VIH | Digital Input High Voltage | PT1, Reset | 0.7 | | | VDD |
| VIL | Digital Input Low Voltage | PT1, Reset | | | 0.3 | VDD |
| VIHSH | Input Hys. High Voltage | Schmitt-trigger port | | 0.45 | | VDD |
| VIHSL | Input Hys. Low Voltage | Schmitt-trigger port | | 0.20 | | VDD |
| IPU | Pull up Current | Vin=0 | | | | μA |
| IOH | High Level Output Current | VOH=VDD-0.3 V | | | | mA |
| IOL | Low Level Output Current | VOL=0.3 V | | | | mA |
| VDDA | Analog Power | | 3.27 | 3.3 | 3.33 | V |
| VDROP | Dropout Voltate | Output Current=30mA | | 0.15 | | V |
| AGND | Analog Ground Voltage | 1/2VDDA | 1.617 | 1.65 | 1.683 | V |
| TCVDDA | Build in Reference Voltage Temperature Coefficient | Ta=0~50℃ | | 100 | | ppm/℃ |
| FRC | Internal RC oscillator | | | 4.0 | | MHz |
| FWDT | Internal WDT Clock | | | | | kHz |

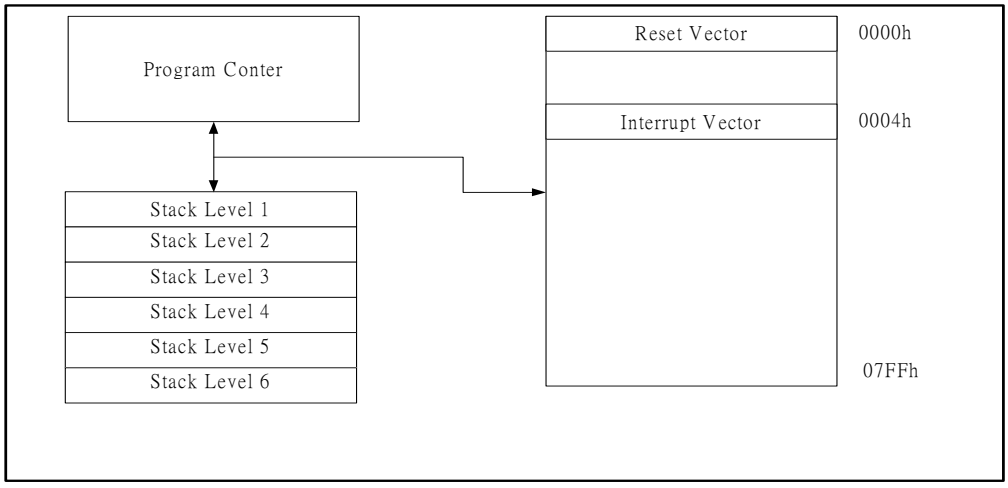
## 10.2 ADC Characteristics (VDD=3.3V, $T_A$=25℃, unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VACIN | ADC Common Mode Input Range | INH,INL,VRH,VRL to VSS | 0.6 | 0 | 2.3 | V |
| VADIN | ADC Differential Mode Input Range | (INH,INL), (VRH,VRL) | | | 0.6 | V |
| | Resolution | | | ±15625 | | Counts |
| | ADC Linearity Error | VRFIN=0.44V | -0.1 | 0 | +0.1 | mV |
| | ADC Input Offset Voltage With Zero Cancellation | VRFIN=0.44V VAIN=0 | | 0 | | V |

# 11. Memory Organization

## 11.1 Program Memory Structure

FS98O11 has an 2k x 16bits program memory space and a 6 level depth 11bits Stack Register. The Start up/Reset Vector is at 0x0000H. When FS98O11 is started or its program is reset, the Program Counter will point to Reset Vector. The Interrupt Vector is at 0x0004H. No matter what ISR is processed, the Program Counter will point to Interrupt Vector.




## 11.2 Data Memory Structure

FS98O11 has a 128 byte SRAM for Data Memory. The data memory is partitioned into three parts. The area with address 00h~07h is reserved for system special registers, such as indirect address, indirect address pointer, status register, working register, interrupt flag, interrupt control register. The address 08h~7Fh areas are peripheral special registers, such as I/O ports, timer, ADC, signal conditional network control register, LCD driver. The address 80h~FFh areas are general data memory.

| Start Address | End Address | Data Memory |
|---|---|---|
| **0X00H** | **0X07H** | ***System Special Registers*** |
| **0X08H** | **0X7FH** | ***Peripheral Special Registers*** |
| **0X80H** | **0XFFH** | ***General Data Memory*** |

## 11.3 System Special Registers

The System Special Registers are designed to complete CPU Core functions, and consists of indirect address, indirect address pointer, status register, work register, interrupt flag, and interrupt control register.

| Address | Name | Content ( u mean unknown or unchanged) | | | | | | | | Reset State |
|---|---|---|---|---|---|---|---|---|---|---|
| 00H | IND0 | Use contents of FSR0 to address data memory | | | | | | | | uuuuuuuu |
| 01H | IND1 | Use contents of FSR1 to address data memory | | | | | | | | uuuuuuuu |
| 02H | FSR0 | Indirect data memory, address point 0 | | | | | | | | uuuuuuuu |
| 03H | FSR1 | Indirect data memory, address point 1 | | | | | | | | uuuuuuuu |
| 04H | STATUS | | | | PD | TO | DC | C | Z | 00u00uuu |
| 05H | WORK | WORK register | | | | | | | | uuuuuuuu |
| 06H | INTF | | | | TMIF | I2CIF | ADIF | | | 00000000 |
| 07H | INTE | GIE | | | TMIE | I2CIE | ADIE | | | 00000000 |
| 08h~7Fh | | Peripheral special registers | | | | | | | | - |
| 80h~FFh | | General data Memory 0 page | | | | | | | | uuuuuuuu |

- IND0, IND1: indirect addressing mode address
- FSR0, FSR1: indirect addressing mode point
- IRP0: Indirect address 0 page select.
- IRP1: Indirect address 1 page select.
- PD: Power down Flag. Cleared by writing 0 or power-on reset. Set by sleep instruction
- TO: Watch Dog Time Out Flag. Cleared by writing 0 or power-on reset. Set by Watch Dog Time Out
- DC: Digit Carry Flag, for ADDWF(C) and SUBWF(C), this bit is set if there is a carry out from the 4th order bit of resultant.
- C: Carry Flag (~Borrow)
- Z: Zero Flag
- ADIF, ADIE: Analog to digital converter Interrupt flag and enable.
- TMIF, TMIE: 8-bit Timer Interrupt flag and enable.
- I2CIF, I2CIE: I2C Interface Interrupt flag and enable.
- GIE: Global interrupt enable.

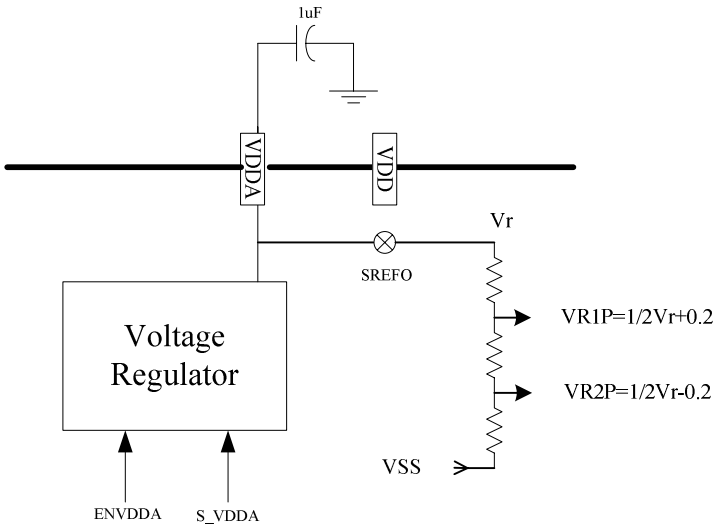
## 11.4 Peripheral Special Registers

| Address | Name | Content ( u mean unknown or unchanged) | | | | | | | | Reset State |
|---|---|---|---|---|---|---|---|---|---|---|
| 0AH | CCCTL | ENCCref | ENCC | SCHAN[1:0] | | CURSEL[3] | CURSEL[2] | CURSEL[1] | CURSEL[0] | 0uuuu000 |
| 0DH | WDTCON | WTDTEN | | | | | WTS [2:0] | | | 0uuuu000 |
| 0EH | TMOUT | TMOUT [7:0] | | | | | | | | 00000000 |
| 0FH | TMCON | TRST | | | | TMEN | INS [2:0] | | | 1uuu0000 |
| 10H | ADOH | ADO [15:8] | | | | | | | | 00000000 |
| 11H | ADOL | ADO [7:0] | | | | | | | | 00000000 |
| 13H | ADCON | | | | | ADRST | ADM [2:0] | | | uuuu0000 |
| 14H | MCK | | | M5_CK | | | M2_CK | M1_CK | | 00000000 |
| 18H | NETA | SINL[1:0] | | SINH[2:0] | | | | | | 00000000 |
| 19H | NETB | | | | | SVRL[1:0] | | SVRH[1:0] | | 00000000 |
| 1AH | NETC | SREFO | | | | ADG[1:0] | | ADEN | AZ | 00000000 |
| 1DH | NETF | | | ENVDDA | | S_AGND[1:0] | | ENAGND | | 00000000 |
| 20H | PT1 | PT1 [7:0] | | | | | | | | uuuuuuuu |
| 21H | PT1EN | PT1EN [7:0] | | | | | | | | 00000000 |
| 22H | PT1PU | PT1PU [7:0] | | | | | | | | 00000000 |
| 24H | PT2 | PT2 [7:0] | | | | | | | | uuuuuuuu |
| 25H | PT2EN | PT2EN [7:0] | | | | | | | | 00000000 |
| 26H | PT2PU | PT2PU [7:0] | | | | | | | | 00000000 |
| 27H | PT2MR | | | | PM1EN | | | | | 00000000 |
| 28H | AIENB2 | | | | AIENB[4:0] | | | | | 00000000 |
| 30H | PMD1H | PMD1[15:8] | | | | | | | | 00000000 |
| 31H | PMD1L | PMD1[7:0] | | | | | | | | 00000000 |
| 37H | PT1OCB | | | | | PT1OC[3:2] | | | | uuu11uuu |
| 57H | I2CCON | WCOL | I2COV | I2CEN | CKP | | | | | 0001uuuu |
| 58H | I2CSTA | | | DA | P | S | RW | | BF | uu0000u0 |
| 59H | I2CADD | I2CADD [7:0] | | | | | | | | 00000000 |
| 5AH | I2CBUF | I2CBUF [7:0] | | | | | | | | 00000000 |

## 11.5 Power System

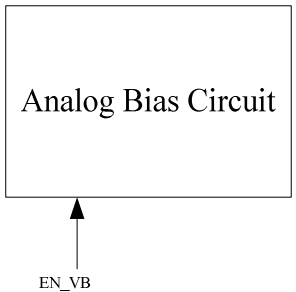
| Address | Name | Content ( u mean unknown or unchanged) | | | | | | | Reset State |
|---|---|---|---|---|---|---|---|---|---|
| 1DH | NETF | | | ENVDDA | S_VDDA | S_AGND [1:0] | | ENAGND | EN_VB | 00000000 |

### 11.5.1 Voltage Regulator




- Before enabling the VDDA, S_VDDA must be set 10mS.
- VDDA is the power supply voltage for analog circuit and LCD driver. When ENVDDA is set, the voltage regulator will active, and VDDA=3.3V. Otherwise VDDA can be as external regulated power supply input.

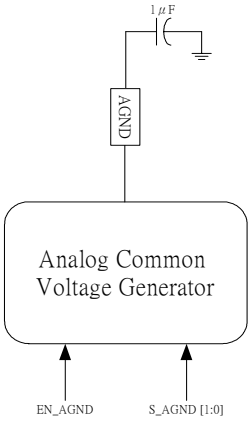
### 11.5.2 Analog Bias Circuit




- Before enabling the analog block, EN_VB must be set.

### 11.5.3 Analog Common Voltage Generator

Analog common voltage generator is used to generate the analog common voltage, AGND.



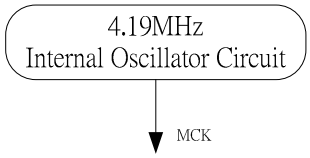

- When EN_AGND = 1, analog common voltage generator is enabled. S_AGND is used to select the AGND voltage level.

| S_AGND [1:0] | AGND voltage |
|---|---|
| 00 | 1/4 VDDA |
| 01 | 1/2 VDDA |
| 10 | 1/3 VDDA |
| 11 | 2/3 VDDA |

## 11.6 Clock System

The clock system offers several clocks to some important blocks in FS98O11, such as CPU clock, ADC sample frequency, beeper clock, voltage doubler operating frequency, etc. Only with the clock signals from the clock system, the FS98O11 can work normally.

| Address | Name | Content ( u mean unknown or unchanged) | | | | | | | | Reset State |
|---|---|---|---|---|---|---|---|---|---|---|
| 14H | MCK | | | | | | M2_CK | M1_CK | | 00000000 |




### 11.6.1 Oscillator State

MCK is the heart of the clock system. Almost all clock signals are derived from the MCK. If we stop MCK, many clock signals will be stopped.

| **Sleep** | **MCK** |
|---|---|
| 1 | Disable |
| 0 | Enable |

- MCK and CLK

| M1_CK | CLK |
|---|---|
| 0 | MCK |
| 1 | MCK/4 |

### 11.6.2 CPU Instruction Cycle

- When M2_CK=0, CPU has a different operation clock cycle from ADC in order to maintain a stable ADC output. In applications where a resolution of more than 13-bits is necessary, M2_CK should be set to zero.
- CPU's operation clock cycle may change as M1_CK,M2_CK change. Users must make sure that switching can be made only after the oscillator's output is stabilized. An NOP command should be added after the switching.

  BSF MCK, 2

  NOP

  ….

| M2_CK | M1_CK | Instruction Cycle (IF ADEN=1) | Instruction Cycle (IF ADEN=0) |
|---|---|---|---|
| 0 | 0 | MCK/7.14 | MCK/2 |
| 0 | 1 | MCK/14.28 | MCK/4 |
| 1 | 0 | MCK/2 | MCK/2 |
| 1 | 1 | MCK/4 | MCK/4 |

### 11.6.3 ADC Sample Frequency

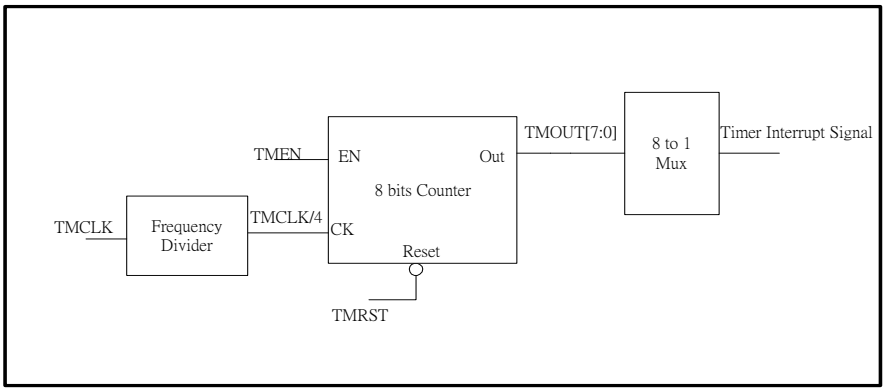
| M1_CK | ADC sample Frequency (ADCF) |
|---|---|
| 0 | MCK/100 |
| 1 | MCK/200 |

### 11.6.4 Timer Module Input Clock

| Timer Module input Clock TMCLK |
|---|
| CLK/4096 |

## 11.7 8-bits Timer

| Address | Name | Content ( u mean unknown or unchanged) | | | | | | | | Reset State |
|---|---|---|---|---|---|---|---|---|---|---|
| 06H | INTF | | | | TMIF | - | - | - | - | 00000000 |
| 07H | INTE | GIE | | | TMIE | - | - | - | - | 00000000 |
| 0EH | TMOUT | TMOUT [7:0] | | | | | | | | 00000000 |
| 0FH | TMCON | TRST | | | | TMEN | INS [2:0] | | | 1uuu0000 |

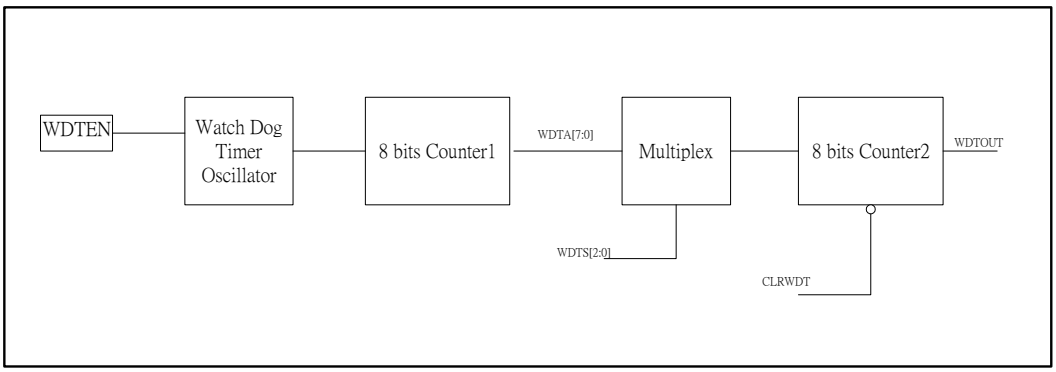



- Write a “0” to bit 7 of address 0Fh; the CPU will send a low pulse to TRST and reset the 8-bit counter. Then read bit 7 of TMCON to get “1”.
- TMEN=1, the 8-bit counter will be enabled. TMEN=0, the 8-bit counter will stop.
- TMOUT [7:0] is the output of the 8-bit counter. It is read-only.
- INS [2:0] selects timer interrupt source. The selection codes are as follows:

| INS | interrupt source | Time at TMCLK=4096Hz |
|---|---|---|
| 0 | TMOUT[0] | (TMCLK/4)/8 |
| 1 | TMOUT[1] | (TMCLK/4)/16 |
| 10 | TMOUT[2] | (TMCLK/4)/32 |
| 11 | TMOUT[3] | (TMCLK/4)/64 |
| 100 | TMOUT[4] | (TMCLK/4)/128 |
| 101 | TMOUT[5] | (TMCLK/4)/256 |
| 110 | TMOUT[6] | (TMCLK/4)/512 |
| 111 | TMOUT[7] | (TMCLK/4)/1024 |

## 11.8 Watch Dog Timer

| Address | Name | Content ( u mean unknown or unchanged) | | | | | | | | Reset State |
|---|---|---|---|---|---|---|---|---|---|---|
| 04H | STATUS | - | - | | - | TO | - | - | - | 00u00uuu |
| 0DH | WDTCON | WDTEN | | | | | WTS [2:0] | | | 0uuuu000 |




- WDTEN = “1” : enable watchdog timer oscillator. “0” : watchdog timer function will be disabled. WDTEN write “1” only.
- When WDT Counter 2 overflows, it will send WDTOUT to reset the CPU and set TO flag.
- CLRWDT instruction will reset WDT Counter 2
- WTS [2:0] selects WDT Counter 2 and the code

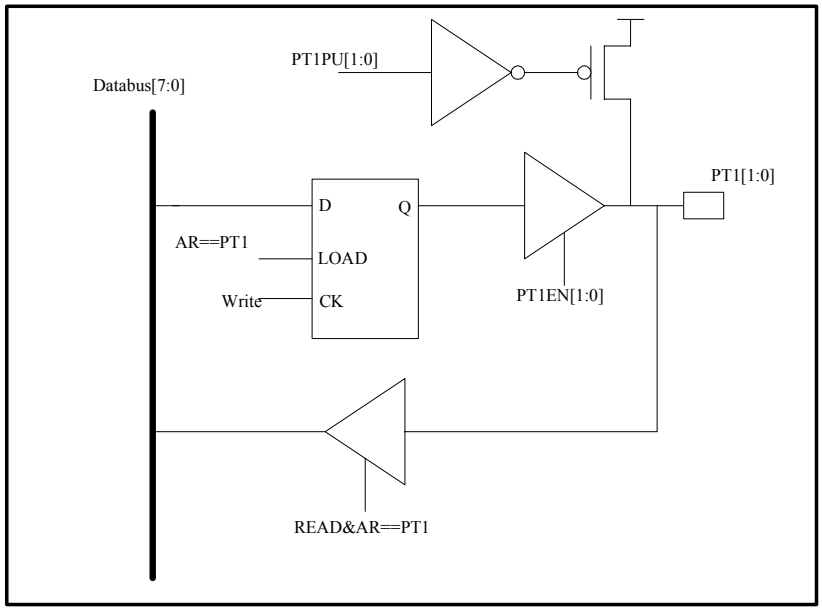
| WTS[2:0] | Interrupt source | WDTOUT Time |
|---|---|---|
| 000 | WDTA[0] | 32 sec. |
| 001 | WDTA [1] | 16 sec. |
| 010 | WDTA [2] | 8 sec. |
| 011 | WDTA [3] | 4 sec. |
| 100 | WDTA [4] | 2 sec. |
| 101 | WDTA [5] | 1 sec. |
| 110 | WDTA [6] | 1/2 sec. |
| 111 | WDTA [7] | 1/4 sec. |

## 11.9 I/O Port

| Address | Name | Content ( u mean unknown or unchanged) | | | | | | | | Reset State |
|---|---|---|---|---|---|---|---|---|---|---|
| 06H | INTF | | | | - | I2CIF | - | | | 00000000 |
| 07H | INTE | GIE | | | - | I2CIE | - | | | 00000000 |
| 20H | PT1 | PT1 [7:0] | | | | | | | | uuuuuuuu |
| 21H | PT1EN | PT1EN [7:0] | | | | | | | | 00000000 |
| 22H | PT1PU | PT1PU [7:0] | | | | | | | | 00000000 |
| 24H | PT2 | PT2 [7:0] | | | | | | | | uuuuuuuu |
| 25H | PT2EN | PT2EN [7:0] | | | | | | | | 00000000 |
| 26H | PT2PU | PT2PU [7:0] | | | | | | | | 00000000 |
| 27H | PT2OCB | | | | | | PT2OCB[2:0] | | | 00000000 |
| 37H | PT1OCB | PT1OCB[7:4] | | | | | | | | 10000000 |

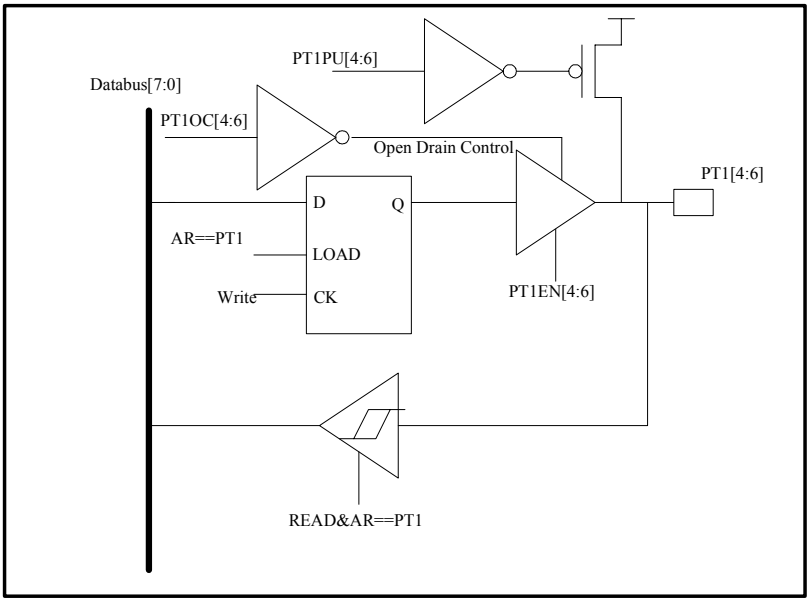
- I/O ports with pull-up resistor enable control. PT1PU [N]=”0”: PT1 [N] without pull-up resistor, “1”: PT1 [N] with pull-up resistor.
- I/O ports with pull-up resistor enable control. PT2PU [N]=”0”: PT2 [N] without pull-up resistor, “1”: PT2 [N] with pull-up resistor.
- PT1EN [N] =”0”: PT1 [N] is as input port, “1”: PT1 [N] is as output port.
- PT2EN [N] =”0”: PT2 [N] is as input port, “1”: PT2 [N] is as output port.
- PT1 is the data register of I/O port.
- PT2 is the data register of I/O port.

### 11.9.1 Digital I/O Port and LED Display : PT1<0:1>



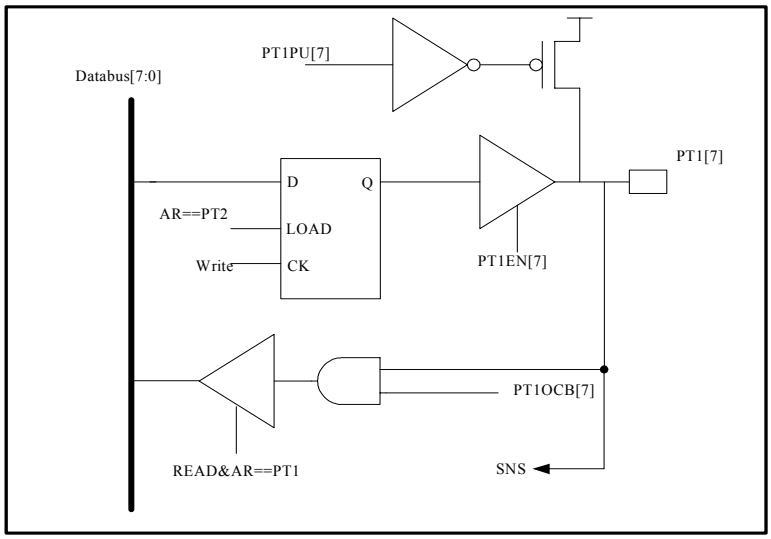

- PT1<0>/LED1 ~ PT1<1>/LED2 can be as Source or sink LED0 display.(10mA)

### 11.9.2 Digital I/O Port or I2C Serial Port and CC output: PT1<4:5>/SDA:SCL, PT1<6>/CC



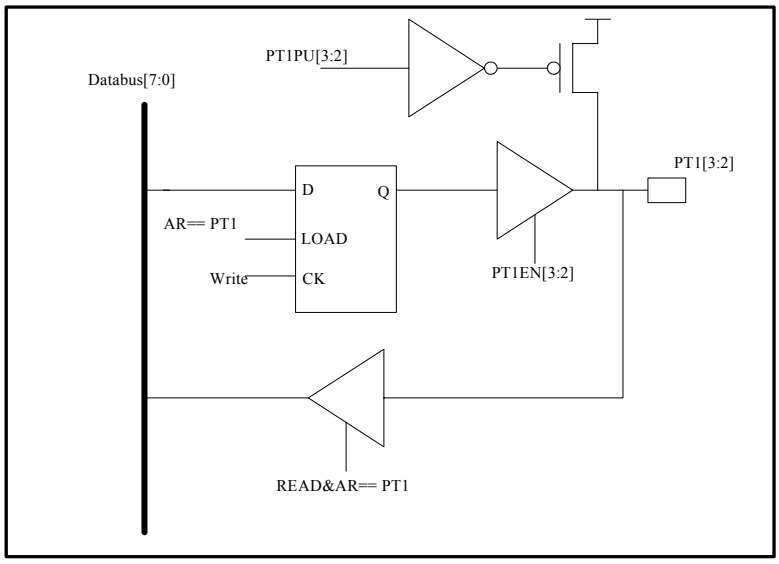

- When PT1OCB [4] =”1”: PT1[4] is open-drain;”0”: PT1 [4] is normal digital I/O port.
- When PT1OCB [5] =”1”: PT1[5] is open-drain;”0”: PT1 [5] is normal digital I/O port.
- When PT1OCB [6] =”1”: PT1[6] is open-drain;”0”: PT1 [6] is normal digital I/O port.
- CC is Charge control to Drive the pass Transistor.
- There has Schmitt-trigger input.
- I2C details see section I2C module.

### 11.9.3 Digital I/O Port with Analog Input Channel Shared : PT1<7>

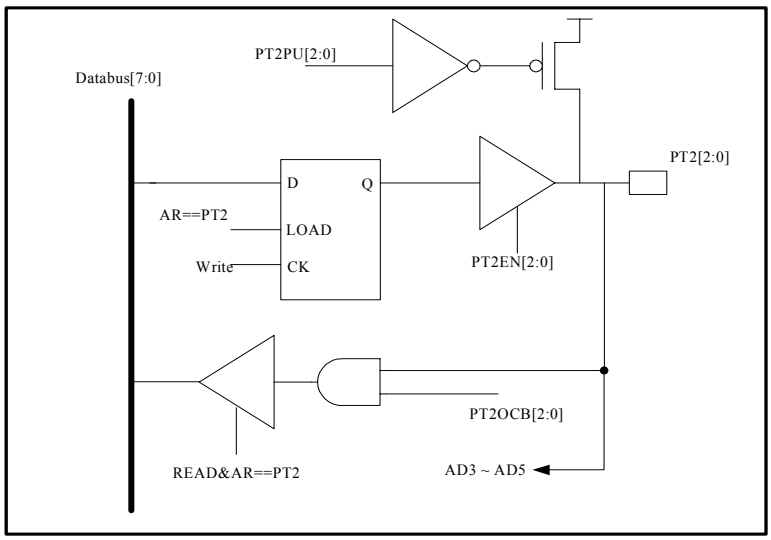



- SNS is Charge current sensing input.
- PT1OCB [7] =”1”, this port is Analog input channel (SNS), “0”: This port is Digital I/O port (PT1.7).

### 11.9.4 Digital I/O Port : PT1<2 > & PT1<3>

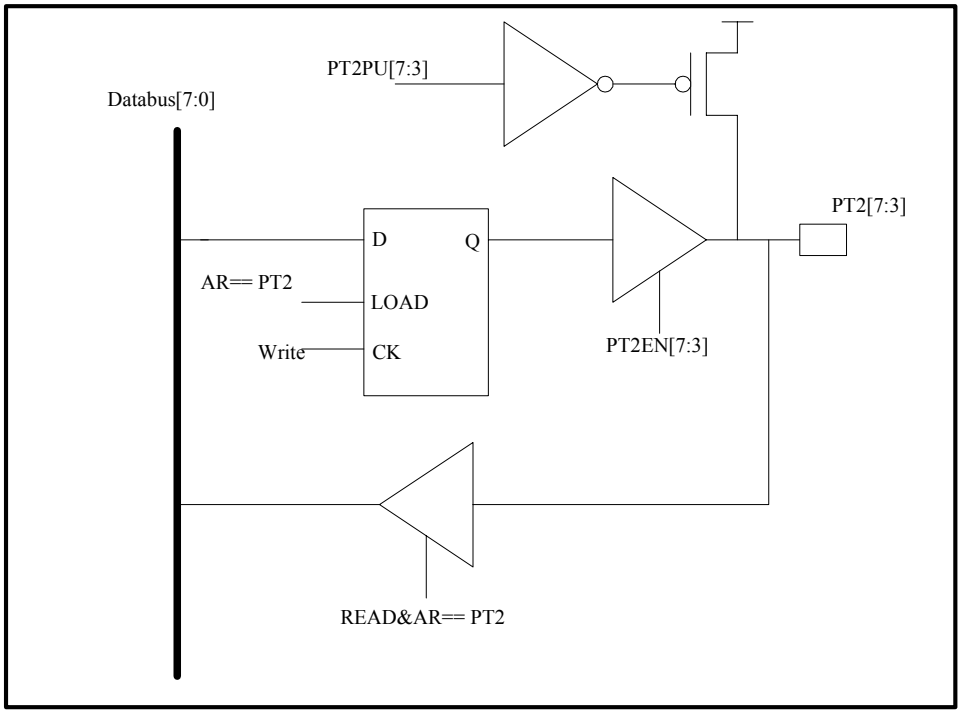



### 11.9.5 Digital I/O Port with Analog Input Channel Shared : PT2<0> ~ PT2<2>



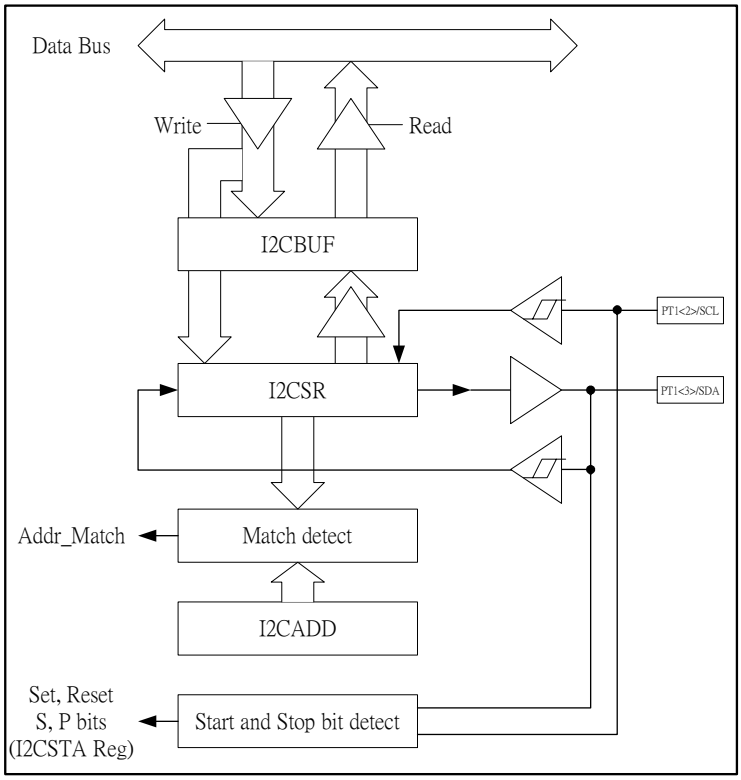

- PT2OCB [0] =”1”, this port is Analog input channel (AD3), “0”: This port is Digital I/O port (PT2.0).
- PT2OCB [1] =”1”, this port is Analog input channel (AD4), “0”: This port is Digital I/O port (PT2.1).
- PT2OCB [2] =”1”, this port is Analog input channel (AD5), “0”: This port is Digital I/O port (PT2.2).

### 11.9.6 Digital I/O Port : PT2<3 > ~ PT2<7>



## 11.10 I2C (slave mode only)

| Address | Name | Content ( u mean unknown or unchanged) | | | | | | | | Reset State |
|---|---|---|---|---|---|---|---|---|---|---|
| 06H | INTF | | | | - | I2CIF | - | - | - | 00000000 |
| 07H | INTE | GIE | | | - | I2CIE | - | - | - | 00000000 |
| 57H | I2CCON | WCOL | I2COV | I2CEN | CKP | | | | | 0001uuuu |
| 58H | I2CSTA | | | DA | P | S | RW | | BF | uu0000u0 |
| 59H | I2CADD | I2CADD [7:0] | | | | | | | | 00000000 |
| 5AH | I2CBUF | I2CBUF [7:0] | | | | | | | | 00000000 |




- The I2C module implements the standard specifications as well as 7-bit addressing. Two pins are used for data transfer. There are the PT1<2>/SCL pin, which is the clock, and the PT1<3>/SDA pin, which is the data. The user must configure these pins as open-drain through the PTOCB[3:2]. I2CSR: Shift Register is not directly accessible.

- I2CCON is the CONTROL REGISTER of I2C module.

  WCOL : Write collision detect.

  1 = the I2CBUF register is written while it is still transmitting the previous word.

  Must be cleared in software.

  0 = No collision.

  I2COV : Receive overflow flag.

  1 = A byte is received while the I2CBUF is still holding the previous byte.

  I2COV is a don't care in transmit mode.

  I2COV must be cleared in software in either mode.

  I2CEN : I2C functional enable.

  1 = Enables the serial port and configures SDA and SCL pins as serial port pins.

  0 = Disable serial port and configures these pins as I/O port pins.

  In both modes, when enabled, these pins must be properly configured as input or output.

  CKP : SCK release control.

  1 = Enable clock.

  0 = Holds clock low (clock stretch)

  Note : Used to ensure data setup time.

- I2CSTA is the STATUS REGISTER of I2C module

  DA : Data/Address bit

  1 = indicates that the last byte received was data

  0 = indicates that the last byte received was address

  P : Stop bit. This bit is cleared when the I2C module is disabled (I2CEN is cleared).

  1 = Indicates that a stop bit has been detected last.

  0 = Stop bit was not detected last.

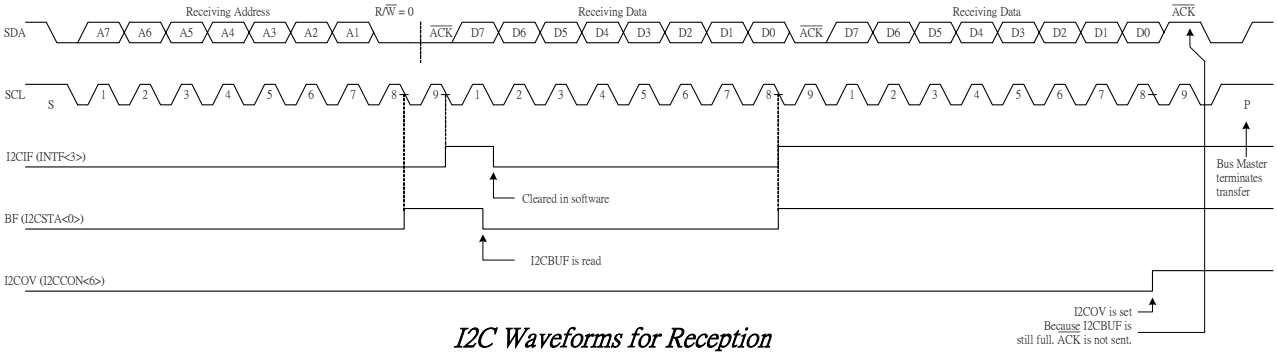
  S : Start bit. This bit is cleared when the I2C module is disabled (I2CEN is cleared).

  1 = Indicates that a start bit has been detected last.

  0 = Start bit was not detected last.

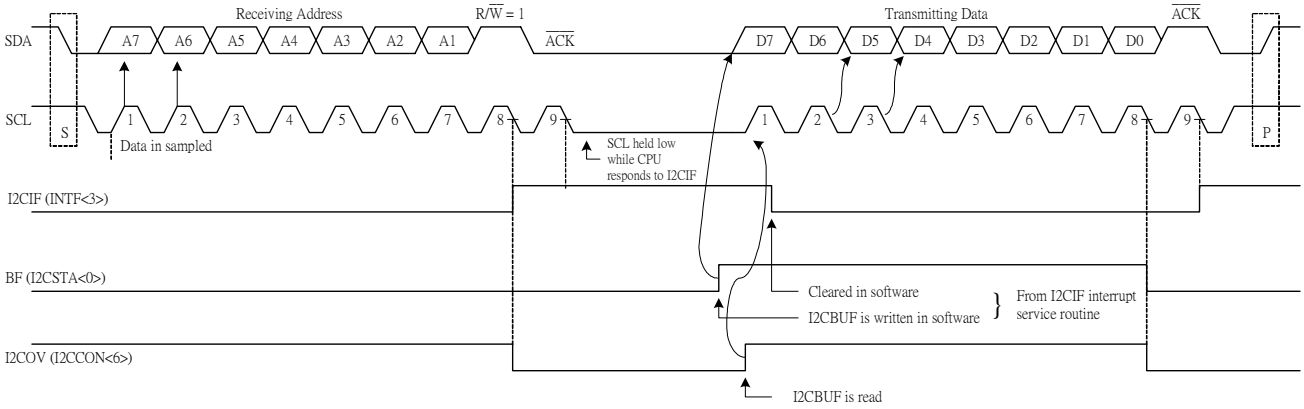
  RW : Read/Write bit information. This bit holds the RW bit information received following the last address match. This bit is only valid during the transmission. The users may use this bit in software to determine whether transmission or reception is in progress. 1 = Read, 0 = Write

- I2CBUF is the BUFFER REGISTER of I2C module
- I2CADD is the ADDRESS REGISTER of I2C module
- Reception: When the R/W bit of the address byte is clear and an address match occurs, the R/W bit of the I2CSTA register is cleared. The received address is loaded into the I2CBUF. When the address byte overflow conditions exist then no acknowledge (ACK) pulse is given. An overflow condition is defined as either the BF bit (I2CSTA<0>) is set or the I2COV bit (I2CCON<6>) is set. An I2CIF interrupt is generated for each data transfer byte. The I2CIF bit must be cleared in software, and the I2CSTA register is used to determine the status of the byte.




*I2C Waveforms for Reception*

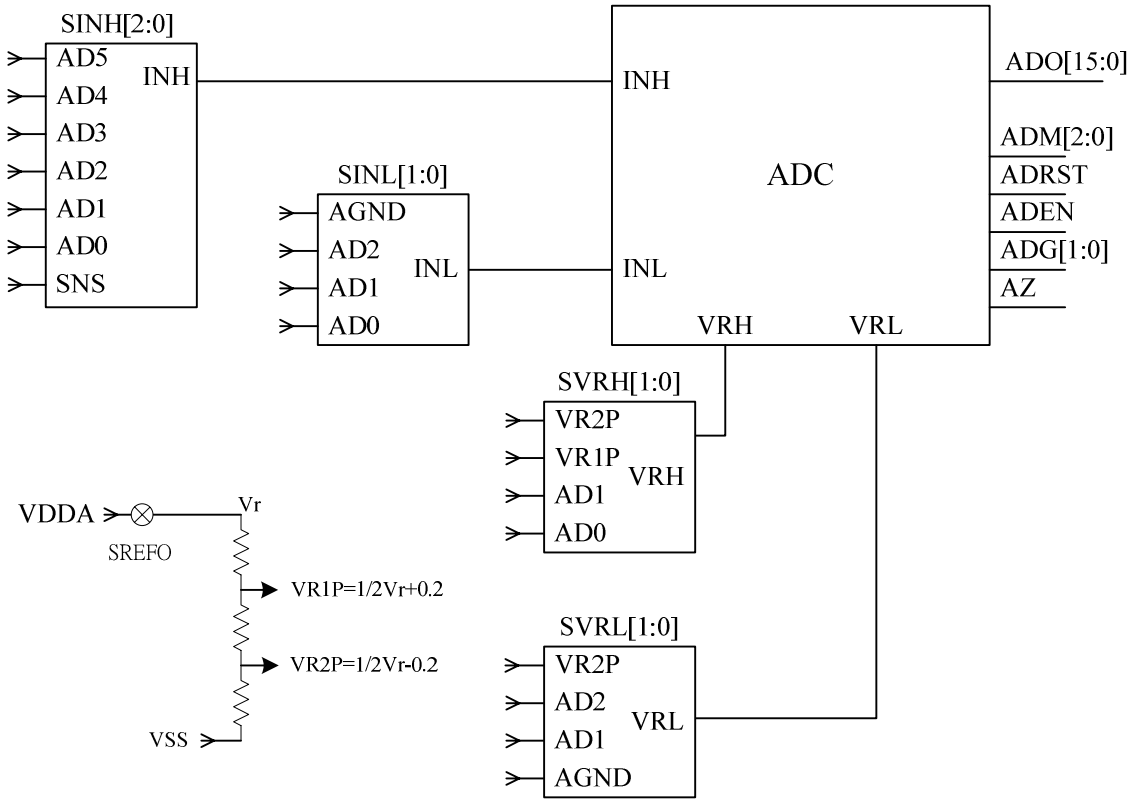
- Transmission: When the R/W bit of the address byte is set and an address match occurs, the R/W bit of the I2CSTA register is set. The received address is loaded into the I2CBUF. The ACK pulse will be sent on the ninth bit, and the SCL pin is held low. The transmit data must be loaded into the I2CBUF register, which also loads the I2CSR register. Then the SCL pin should be enabled by setting the CKP bit (I2CCON<4>). The right data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time. A I2CIF interrupt is generated for each data transfer byte. The I2CIF bit must be cleared in software, and the I2CSTA register is used to determine the status of the byte. The I2CIF bit is set on the falling edge of the ninth clock pulse. As a slave-transmitter, the ACK pulse from the master-receiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line was high (not ACK), then the data transfer is complete. The slave then monitors for another occurrence of the I2CSTA bit. If the SDA line was low (ACK), the transmit data must be loaded into the I2CBUF register, which also loads the I2CSR register. Then the SCL pin should be enabled by setting the CKP bit (I2CCON<4>).




*I2C Waveforms for Transmission*

## 11.11 Analog Function Network

| Address | Name | Content ( u mean unknown or unchanged) | | | | | | | | Reset State |
|---|---|---|---|---|---|---|---|---|---|---|
| 06H | INTF | | | | - | - | ADIF | - | - | 00000000 |
| 07H | INTE | GIE | | | - | - | ADIE | - | - | 00000000 |
| 15H | PCK | | - | | | S_CH1CK [1:0] | | - | - | 00000000 |
| 10H | ADOH | ADO [15:8] | | | | | | | | 00000000 |
| 11H | ADOL | ADO [7:0] | | | | | | | | 00000000 |
| 13H | ADCON | | | | | ADRST | ADM [2:0] | | | uuuu0000 |
| 18H | NETA | SINL[1:0] | | SINH[2:0] | | | | | | 00000000 |
| 19H | NETB | | | SOP1N[1:0] | | SVRL[1:0] | | SVRH[1:0] | | 00000000 |
| 1AH | NETC | SREFO | | | | ADG[1:0] | | ADEN | AZ | 00000000 |
| 1BH | NETD | | | | | OP1EN | SOP1P[2:0] | | | 00000000 |



### 11.11.1 Analog to Digital Converter (ADC) :

- The ADC contains Σ-Δ modulator and digital comb filter. When ADRST=1, comb filter will be enabled. When ADRST=0, the comb filter will be reset. ADEN=1 starts the Σ-Δ modulator.
- The output rate is selected by ADM (N).

| ADM (N) | ADC Output Rate |
|---|---|
| 000 | ADCF/125 |
| 001 | ADCF/250 |
| 010 | ADCF/500 |
| 011 | ADCF/1000 |
| 100 | ADCF/2000 |
| 101 | ADCF/4000 |
| 110 | ADCF/8000 |
| 111 | ADCF/8000 |

- AZ=0 means that the ADC differential inputs are (INH, INL); AZ= 1 means that the ADC differential inputs are (INL, INL). We can use this mode to measure the ADC offset.
- ADG [1:0] will set ADC input gain as follows, 00: 2/3, 01: 1, 10: 2, 11: 2 1/3.

### 11.11.2 Analog Multiplex :

- Analog Input:

| SINH[2:0] | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
|---|---|---|---|---|---|---|---|---|
| Select | AD0 | AD1 | AD2 | AD3 | AD4 | AD5 | AD5 | AD5 |

- ADC Negative Input:

| SINL[1:0] | 00 | 01 | 10 | 11 |
|---|---|---|---|---|
| Select | AIN0 | AIN1 | AIN2 | AGND |

- Internal Reference Voltage Control: SREFO=1, to CDDA short; SREFO=0, to VDD short.
- ADC Reference Voltage Negative Input:

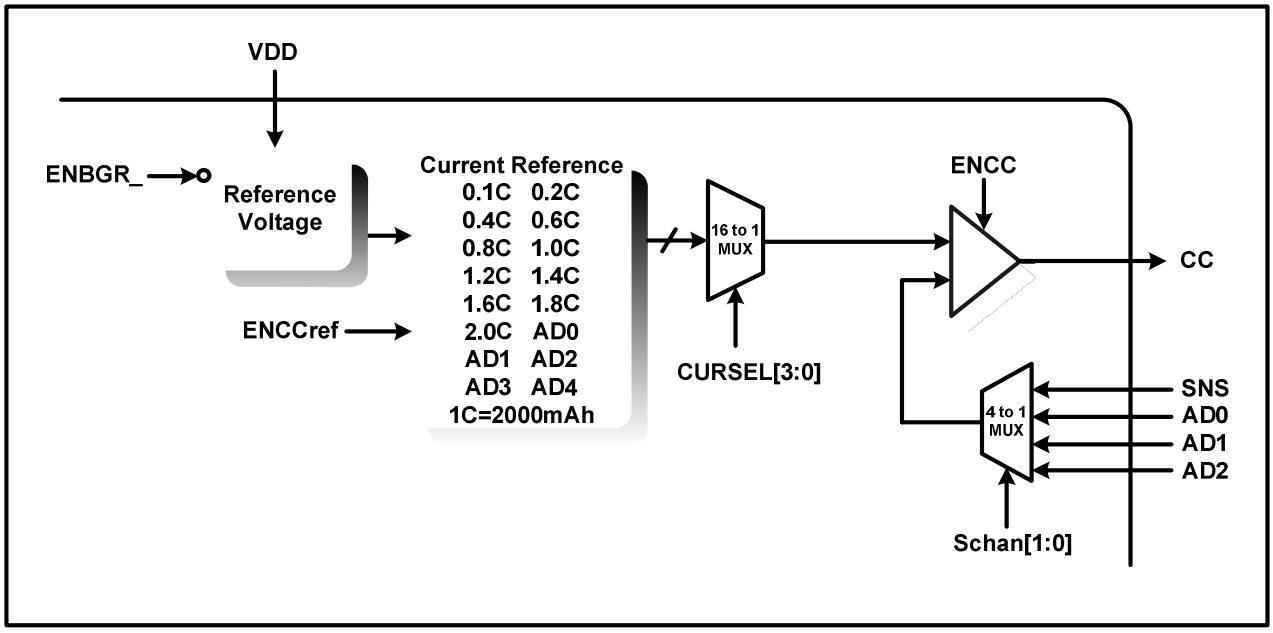
| SVRL[1:0] | 00 | 01 | 10 | 11 |
|---|---|---|---|---|
| Select | AGND | AIN1 | AIN2 | VR2P |

- ADC Reference Voltage Positive Input:

| SVRH[1:0] | 00 | 01 | 10 | 11 |
|---|---|---|---|---|
| Select | AD0 | AD1 | VR1P | VR2P |

## 11.12 Charge Current Control

| Address | Name | Content ( u means unknown or unchanged ) | | | | | | | | Reset State |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| 0AH | CCCTL | ENCCref | ENCC | SCHAN[1] | SCHAN[0] | CURSEL[3] | CURSEL[2] | CURSEL[1] | CURSEL[0] | 00uu0000 |




- Current sensing using an external sensing resistor $R_{SNS}$=0.05ohm
- **ENCCref**: Enable constant current regulation reference current.
- **ENCC**: Enables the constant current regulation for constant current charge.
- The 3-bits select **CURSEL[3:0]** selects constant current regulation reference current. 1C=2000mAh

| CURSEL[3:0] | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 |
|---|---|---|---|---|---|---|---|---|
| Select | **200mA** | **400mA** | **800mA** | **1200mA** | **1600mA** | **2000mA** | **2400mA** | **2800mA** |
| voltage | **10mV** | **20mV** | **40mV** | **60mV** | **80mV** | **100mV** | **120mV** | **140mV** |
| CURSEL[3:0] | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
| Select | **3200mA** | **3600mA** | **4000mA** | **AD0** | **AD1** | **AD2** | **AD3** | **AD4** |
| voltage | **160mV** | **180mV** | **200mV** | | | | | |

- Current sensing Input select **SCHAN[1:0]**

| Schan[1:0] | 00 | 01 | 10 | 11 |
|---|---|---|---|---|
| Select | SNS | AD0 | AD0 | AD0 |

## 11.13 External Reset

The CPU has a “RST_” pin for external reset usage. When “RST_” is in logic “low” state, the CPU will go into external reset status. The external R/C circuit for reset is shown as following. When VDD changes from “low” to “high”, the CPU external reset status will be released, and the CPU will be in normal operating condition.

The signal from the “RST_” pin to CPU should remain in logic “low” state for more than 2μs to reset the CPU. If the signal from the “RST_” pin to CPU is in “low” state less than 2μs, the CPU will not be reset.

Figure 11-1: the Reset Circuit and the Reset Timing

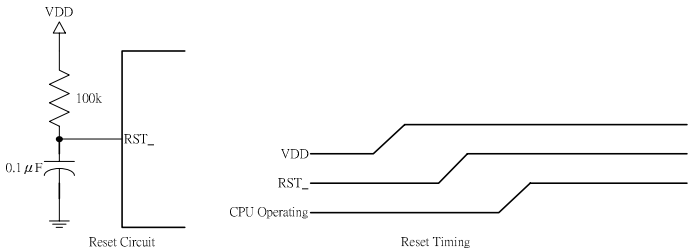
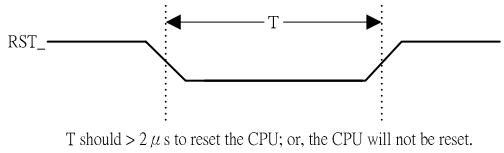



Figure 11-2: the Minimum Reset Period to Reset the CPU




## 11.14 Low Voltage Reset

To avoiding the CPU in an abnormal power status that makes the CPU unable to reset and causes the CPU operating abnormally, there’s a low voltage reset circuit embedded in FS98O11. When the voltage of VDD is less than LVR threshold low voltage, the CPU enters reset state; and when the voltage of VDD comes back above the LVR threshold high voltage, the CPU will be in normal operating condition.

# 12. Revision history

| Ver. | Date | Page | Description |
|---|---|---|---|
| 0.1 | 2005/10 | - | Preliminary version. |
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