

Change Summary

CHANGES

No.	Applicable Section	Description	Page(s)
1.	Features	Modify the last feature to read 'Toggle ENA pin...'	1
2	Ordering Information	Add GN, SN, IS, ISN, D & DN packages	1
3	Pin Description	Modify Pin 7 ADJ description	3
4	Absolute Maximum Ratings	a. Change ' VIN ' to 32V; b. Change ' Logic Inputs ' to '-0.3V to VREF+0.3V '	3
5	Recommended Operating Range	a. Change ' VIN ' to '6V~27V'; b. Add ' 16-pin DIP ' Thermal Impedance	3
6	Electrical Characteristics	a. Change 1 st line Test Conditions ' C_{CT}=131pF to 220pF '; b. Change High Frequency Oscillator, Normal Operating Frequency Typ value fm 56 to 62 ; c. Change High Frequency Oscillator, Ramp Valley Typ value fm 7 to 100 ; d. Change Low Frequency Oscillator, Operating Frequency Typ value fm 200 to 187 ; e. Change Low Frequency Oscillator, Ramp Valley fm 84.9 to 110 ; f. Add ' Analog Dimming Range ' parameter; g. Add ' ISEN Reference Voltage ' & ' VSEN Reference Voltage ' symbols; h. Change Supply, HSB voltage Typ value fm 7 to Vin-5 ; i. Change Max./Min. Overlap, Max Overlap between diagonal switches Typ value fm 94.5 to 95 ; j. Change Threshold, Vin Under Voltage Lock Out Threshold Min. Value fm 5.8 to 5.95 , Max fm 5.4 to 4.95 ; k. Change Timer, Over Voltage Protection Timer Typ value fm 50 to 15 .	4
7	Functional Information	Modify the value in last line of NO. 2. Enable fm '6.0V' to '5.8V'	7
8	Same as above	Modify the formula in NO. 4. Ignition fm '3300' to '3700'	8
9	Reference Application Circuit- Figure 2	Add over current protection circuit (D6, R6, R9 & R10)	10
10	Reference Application Circuit- Figure 3	Correct the connection of rectifier	11
11	OZ9910 Waveforms	Delete Figure 4a. and rename Figure 4b as Figure 4.	12
12	Package Information	Add OZ9910D 16-pin DIP package drawings	15
13	Throughout data sheet	Miscellaneous corrections.	---

REVISION HISTORY

Revision No.	Description of change	Release Date
0.96	1. Ordering Information: Add OZ9910S 16 pin-SSOP package; 2. Recommended Operating Range: Add OZ9910S 16 pin-SSOP thermal impedance; 3. Electrical Characteristics: a) Add general test conditions before "High Frequency Oscillator" ; b) Normal operating frequency: delete test conditions; correct Typ limit to 56 ; c) Striking frequency: delete test conditions; correct Typ limit to 72 ; d) Operating frequency: delete test conditions; e) Supply current: correct test conditions; f) REF voltage: add Symbol; correct test conditions; g) Min. overlap between diagonal switches & Max. overlap between diagonal switches: correct test conditions; h) PDRV3/ NDRV2 & PDRV1/ NDRV4: correct test conditions i) Over time protection timer: correct test conditions; 4. Function Information: a) Section 4 Ignition: correct striking frequency equation denominator from C_{lct}[pF] to C_{ct}[pF] & R_{rt} to R_{ct} ; b) Section 5 Normal Operation: correct fop equation numerator fm 18.7 to 9.35 ; c) Section 6 Proection: correct 2 nd paragraph to read "If the lamp fails to ignite after approximately 1.5 seconds, the IC will shut down."; 5. Package Information: Add OZ9910S 16 pin-SSOP package drawings	7/26/2004
0.95	Initial release	6/15/2004

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Dual Forward PWM Controller

FEATURES

- Controller for high-voltage DC/DC and DC/AC converters
- High-efficiency, zero voltage switching dual forward controller
- Feed forward compensation
- Combined analog and/or PWM control modes for wide-range load regulation
- Supports wide input voltage range
- Constant operating frequency
- Soft start function
- Built-in open-load protection, over-voltage protection and over-current protection
- Built-in under-voltage lockout function
- Low stand-by power
- Toggle ENA pin to reset IC

efficiency resulting in lower power dissipation and higher system reliability that are critical for radar transmitters and display systems

OZ9910 supports a wide input voltage range and provides a constant, user-defined, operating frequency, ensuring that the load operates at a fixed frequency. In display systems, a single operating frequency eliminates interference among the lamps and the display panel. In radar systems, a single operating frequency avoids any influence by alias signals.

The OZ9910 provides a wide-range load regulation through low-frequency LPWM and/or analog-adjust dimming controls. It also provides an option for selecting a different turn-on frequency from the operation frequency that is suitable for loads such as CCFL and TWT.

ORDERING INFORMATION

Part Number	Temp Range	Package
OZ9910G	0°C to 70°C	16-pin SOP
OZ9910GN	0°C to 70°C	16-pin SOP, Lead-Free
OZ9910S	0°C to 70°C	16-pin SSOP
OZ9910SN	0°C to 70°C	16-pin SSOP, Lead-Free
OZ9910IS	-40°C to 85°C	16-pin SSOP
OZ9910ISN	-40°C to 85°C	16-pin SSOP, Lead-Free
OZ9910D	0°C to 70°C	16-PIN DIP
OZ9910DN	0°C to 70°C	16-PIN DIP, Lead-Free

The OZ9910 provides a built-in feed-forward compensation function for applications requiring a wider, dynamic input voltage range. The feed-forward compensation feature optimizes line and load regulation.

To avoid over-shoot and in-rush current to both input and output loads during start up, a soft start function is provided to improve system reliability.

The controller provides open-load protection, over-voltage protection and over-current protection. The striking time (turn-on) for open-load protection is user-defined.

OZ9910 provides under-voltage lockout protection and will disable the IC if VIN falls below a threshold. OZ9910 resumes normal operation when VIN exceeds the threshold.

To reset the IC, toggle the ENA pin. OZ9910 operates with a standby current of approximately 74uA.

GENERAL DESCRIPTION

The OZ9910 is a high-efficiency pulse-width modulation (PWM) controller designed for both DC/DC and DC/AC high voltage applications. Devices such as magnetrons and traveling wave tubes (TWT) require a bias voltage up to several thousand Volts DC and Cold Cathode Fluorescent Lamp (CCFL) requires several hundred to thousand Volts AC to operate. The OZ9910, dual forward PWM controller, is optimized for such applications

OZ9910 operates in a zero-voltage switch mode through the dual forward topology utilizing free-wheeling diodes. The IC operates in a constant frequency mode that minimizes electromagnetic interference (EMI). In addition, OZ9910 achieves a high power-conversion

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FUNCTIONAL BLOCK DIAGRAM

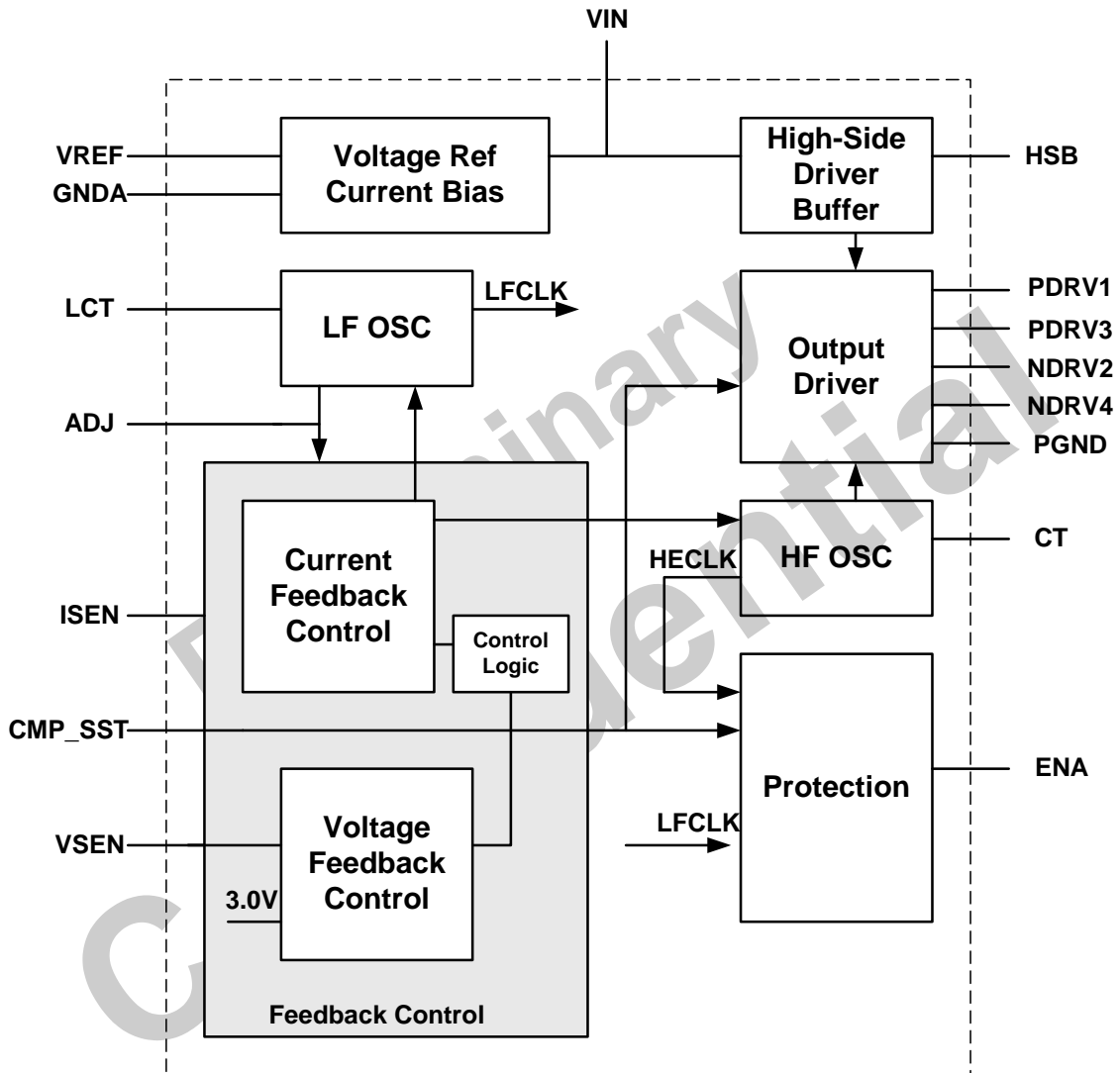


Figure 1. Functional Block Diagram

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PIN DESCRIPTION

Pin No.	Names	Description
1	NDRV4	Bottom MOSFET gate drive output in dual forward converter
2	PGND	High-current power ground
3	NDRV2	Bottom MOSFET gate drive output in dual forward converter
4	GND A	Low-current signal ground
5	CT	Timing capacitor of high frequency oscillator
6	LCT	Timing capacitor to set LPWM frequency
7	ADJ	Analog/PWM Dimming Control
8	ENA	Enable input
9	VSEN	Voltage sense feedback
10	CMP_SST	Soft start and loop compensation capacitor
11	ISEN	Current sense feedback
12	VREF	Reference voltage output
13	VIN	Supply voltage for IC
14	HSB	High side driver buffer output
15	PDRV3	Top MOSFET gate drive output in dual forward converter
16	PDRV1	Top MOSFET gate drive output in dual forward converter

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

VIN	32V
GND A, PGND	+/-0.3V
Logic Inputs	-0.3V to VREF +0.3V

Operating temp.	0°C to 70°C
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Operating Junction Temp.	150°C
Storage Temp.	-55°C to 150°C

RECOMMENDED OPERATING RANGE

VIN	6V ~ 27V
Operating Frequency	30 KHz to 150 KHz
Thermal Impedance (θ_{J-A})	
16-pin SOP	TBD °C/W
16-pin SSOP	TBD °C/W
16-pin DIP	TBD °C/W

Note ⁽¹⁾: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The "Functional Specifications" table will define the conditions for actual device operation. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
		C _{CT} = 220pF, R _{CT} = 68.1kΩ ⁽¹⁾ C _{LCT} = 4700pF, R _{LCT} = 3.3MΩ Unless Specified				
High Frequency Oscillator						
Normal operating frequency	f _{op}		-	62	-	KHz
Striking frequency	F _{striking}		-	72	-	KHz
Ramp peak ⁽⁴⁾		Normal operation	-	2.04	-	V
Ramp valley ⁽⁴⁾		Normal operation	-	100	-	mV
Temp. stability		T _a = 0 °C to 70°C	-	TBD	-	ppm/°C
Low Frequency Oscillator						
Operating frequency	f _{LF}		-	187	-	Hz
Ramp peak ⁽⁴⁾		Normal operation	-	1.50	-	V
Ramp valley ⁽⁴⁾		Normal operation	-	110	-	mV
Low Frequency PWM						
Duty Cycle Range			0	-	100	%
Error Amplifier						
Analog Dimming Range	ADJ	Normal operation	1.5	-	3.5	V
ISEN Reference Voltage	ISEN	ADJ=1.0V	-	1.5	-	V
VSEN Reference Voltage	VSEN	ADJ=1.0V	-	3.0	-	V
Supply						
Supply current	I _{OFF}	ENA = low	-	74	-	μA
Supply current	I _{ON}	ENA = high; ADJ = 2.0V; Ca=Cb=Cc=Cd=2nF ⁽³⁾	-	3.89	-	mA
REF voltage	VREF	V _{in} = 12v I _{LOAD} ≤ 10mA	-	5	-	V
HSB voltage		V _{in} =12v I _{LOAD} ≤ 5mA	-	V _{in} -5	-	V
NDR-PDR Output						
NDRV2/4 sourcing resistance	R _{nso}	Current source	-	17	-	Ω
NDRV2/4 sinking resistance	R _{nsi}	Current sink	-	11	-	
PDRV 1/3 sourcing resistance	R _{pso}	Current source	-	12	-	Ω
PDRV1/3 sinking resistance	R _{psi}	Current sink	-	16	-	

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ELECTRICAL CHARACTERISTICS (Continued)

Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Max. / Min. Overlap						
Min. Overlap between diagonal switches		Ca=Cb=Cc=Cd=2nF ⁽³⁾	-	2.38	-	%
Max. Overlap between diagonal switches		Ca=Cb=Cc=Cd=2nF ⁽³⁾	-	95	-	%
Brake Before Make						
PDRV3 / NDRV2		Ca=Cb=Cc=Cd=2nF ⁽³⁾	-	162	-	ns
PDRV1 / NDRV4		Ca=Cb=Cc=Cd=2nF ⁽³⁾	-	198	-	ns
Threshold						
Vin Under Voltage Lock Out (UVLO) Threshold		Vin rising (leaving lockout)	5.95	-	-	V
		Vin falling (entering lockout)	-	-	4.95	V
Enable Threshold		Ena rising (enable)	2.0	-	-	V
		Ena falling (disable)	-	-	1.0	V
Timer						
Over Time Protection Timer			-	1.5	-	sec
Over Voltage Protection Timer			-	15	-	msec

Note⁽¹⁾

Cct : capacitor from CT (Pin 5) to ground
Rcr: resistor from CT (Pin 5) to VREF

Note⁽²⁾

CLct : capacitor from LCT (Pin 6) to ground
RLct: resistor from LCT (Pin 6) to VREF

Note⁽³⁾

Ca: capacitor from NDRV2 (Pin 3) to ground
Cb: capacitor from NDRV4 (Pin 1) to ground
Cc: capacitor from PDRV3 (Pin 15) to Vin
Cd: capacitor from PDRV1 (Pin 16) to Vin

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FUNCTIONAL BLOCK DIAGRAM DESCRIPTION

Refer to the Functional Block Diagram in Figure 1, page 2, and the Pin Description Table on page 3.

Voltage REF/Current Bias Block generates a bias current reference for internal use and precision 5V reference for both internal and external use. In addition, it provides a feed-forward compensated current to the Feedback Control Block.

LFOSC block supplies a low frequency ramp signal to Feedback Control block. The ramp signal is compared with the external ADJ signal to yield a low-frequency, pulse-width-modulation (LPWM) signal to regulate the power delivered to the load. LFOSC also provides the striking time (turn-on) for open-load protection.

The Feedback Control block consists of Current Feedback Control, Voltage Feedback Control and Control Logic. This block receives the command signal from ADJ, feedback for output voltage (VSEN) and load current (ISEN), Compensation (CMP) and LPWM. When the voltage at ADJ is greater than 1.5V, LPWM will not affect either the current feedback or voltage feedback controls. When the voltage at ADJ is less than 1.5V, the LPWM signal is activated to modulate the current feedback control loop. At this point, the analog signal applied to the error amplifier is fixed at 1.5V. The Control Logic selects either voltage feedback or current feedback as the control command to the output drives.

Depending on the system design, the Feedback Control block selects either the voltage feedback control or the current feedback control command to provide suitable load regulation. In TWT applications, the initial turn-on may rely on regulating the current. In CCFL applications, the initial turn-on is to regulate the ignition voltage. The Feedback Control block provides a high-degree of flexibility for various applications. The error amplifiers for Current Feedback Control and Voltage Feedback Control are configured as a trans-impedance amplifier to work with either voltage control or current control.

HFOSC block generates a high frequency ramp signal. This signal is compared with the control command from the Feedback Control block to determine the appropriate drive outputs.

Protection block protects the IC and external devices from over-voltage, open-load and over-current conditions.

The High-side driver buffer provides a buffered voltage of $V_{in} - 5V$ to the high-side switches in the dual forward converter.

FUNCTIONAL INFORMATION

1. Steady-State Operation

Referring to the schematics shown in Figures 2 and 3 on pages 10 and 11 the OZ9910 drives a zero-voltage switching (ZVS), dual forward power stage where the transformer couples the energy from the power source to the secondary load. In both applications, the voltage and the current can be used as the feedback control signals to regulate the outputs. In CCFL applications, Figure 2, the current flowing through the CCFL is sensed and regulated, through sense resistor R8, then compared with a reference voltage via a current amplifier, resulting in PWM drive outputs to the dual forward converter switches. Switches M1, M2, M3, M4 are configured such that the switch in each pair, M1/M4 and M2/M3, are turned-on complementarily. The amount of time where switches M1/M2 and M3/M4 conduct, determine the amount of energy delivered to the load. A voltage loop is established to monitor the output voltage such that a required turn-on voltage is achieved. A soft-start circuit ensures a gradual increase in the output power to minimize stress to the other components. The capacitor at CMP_SST (pin 10), determines the rate of rise of the voltage on CMP_SST pin, where the voltage at this pin determines the on-time duration of switches M1/M2 and M3/M4.

Circuit operation is initiated by applying the bias voltage to VIN (pin13) and subsequently providing the enable signal to ENA (pin 8) of the IC. The output drives, include NDRV4, NDRV2, PDRV3 and PDRV1 (pins 1,3,15,16 respectively) output square pulses. The frequency is determined by resistor R4 and capacitor C2 connected to CT (pin 5). Initially, the energy converted from the power source to the load is low due to the soft-start function. The energy increases as the soft-start capacitor voltage increases linearly with time. The voltage at the secondary side of the transformer T1 increases correspondingly. This process continues until the load current is detected and reaches a regulated value. The output of the error amplifier, CMP_SST (pin 10), commands proper switching among the four output drives to maintain current regulation. The operations of the four switches are implemented with zero-voltage switching to provide a high-efficiency power conversion.

In the TWT application, Figure 3, either the current or the voltage can be used as a feedback control parameter. The operation theory is similar to the above discussion.

Referring to Figure 2, in the case of an open-lamp condition emulating an aged lamp, the OZ9910 provides an optional, user-defined, turn-on frequency. The turn-on frequency is implemented through capacitor C2 connected to CT pin. The striking (turn-on) time is determined by capacitor C9 connected to LCT (pin 6). The ignition voltage (open-lamp voltage) is regulated through the voltage feedback loop. This highly integrated circuit (IC) provides a cost effective yet high-degree of design flexibility.

An open-load protection feature is provided for safe operation when removing a lamp during normal operation under either one of the two following conditions. For condition one, when the IC senses the missing current signal through ISEN (pin 11) and the voltage at CMP_SST (pin 10) reaches an ~2.5V threshold, the output drives are shut off. Under condition two, when the voltage at VSEN (pin 9) reaches an ~ 3.0V threshold, the output drives are shut off. The output drives will remain in the latched mode. Toggling ENA (pin 8) is necessary to resume normal operation.

Dimming control of OZ9910 is implemented by combining LPWM and analog-adjust for regulating the current in the CCFL. This provides a very wide range of dimming control to a CCFL. When ADJ (pin 7) input voltage is less than 1.5V, the LPWM control is activated while the amplitude of the lamp current is maintained. This mode provides a wide dimming control while maintaining the operational life-time of a CCFL. The LPWM frequency is determined by capacitor C9 and resistor R1 connected to LCT (pin 6). When ADJ (pin 7) input voltage is greater than 1.5V, the CCFL current amplitude will be increased.

OZ9910 operates in a constant frequency mode. This eliminates any undesired interference between inverter and LCD panels where interference is usually associated with variable-frequency designs.

2. Enable

OZ9910 is enabled when the voltage on ENA (pin 8) is greater than 2V. A voltage of less than 1V disables the IC. When the IC is disabled, it draws approximately 74uA. An under-voltage lockout protection feature is provided that will disable the IC if VIN voltage drops below a threshold of approximately 5.6V. The IC will resume normal operation once VIN reaches a threshold voltage of greater than approximately 5.8V.

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3. Soft Start

To avoid component stresses and in-rush current to the load during turn-on, a soft-function is implemented to provide reliable load operation. The soft-start function is initiated when the voltage at ENA (pin 8) is greater than 2V. The soft-start time is determined by capacitor C22 connected to CMP_SST (pin 10). The Feedback Control circuitry provides a current to charge capacitor C22.

4. Ignition

During striking (turn-on), OZ9910 generates a higher frequency for CCFL ignition. This frequency is approximately 30% higher than the normal operating frequency. The ignition (turn-on) time is determined by capacitor C9 connected to LCT (pin 6) and is approximated by the following equation:

$$T[\text{second}] = C_{LCT}[\text{nF}] \times 0.33$$

The striking frequency is approximated by the following equation:

$$f_{\text{striking}}[\text{kHz}] = \frac{3700 / R_{ct} [\text{k}\Omega] + 15}{4 \times C_{ct} [\text{pF}]} \times 1000$$

5. Normal Operation

Once the IC is enabled, the voltage at CMP_SST (pin 10) controls the rate of power delivered to the load. The voltage increases to a level such that the CCFLs are ignited. The voltage feedback loop takes control to regulate lamp voltage during the striking period. Once the current is sense at a threshold of ~0.6V, when ADJ ≤ 1.5V or 0.4 * DIM, when ADJ > 1.5V, the IC will switch to normal operating frequency. The operating frequency is determined by resistor R4 and capacitor C2 connected to CT (pin 5). The operating frequency is approximated by the following equation:

$$f_{op}[\text{kHz}] = \frac{9.35 \times 10^5}{C_{ct}[\text{pF}] \times R_{ct}[\text{k}\Omega]}$$

6. Protection

The IC provides time-out protection, open-load protection and over-voltage protection features.

Time-out protection for striking (turn-on): An internal counter is started when the IC is enabled. If the lamp fails to ignite after approximately 1.5 seconds, the IC will shut down

Open-load protection: If the lamp is removed during normal operation, the voltage of CMP_SST will increase rapidly. Once the voltage at CMP_SST (pin 10) reaches a threshold of approximately 2.5V, the IC will shut down.

Over-voltage protection: During normal operation, if the voltage at VSEN (pin 9) reaches a threshold of approximately 3.0V, the output of the error amplifier will maintain a constant voltage level. Meanwhile, an internal clock triggers a timer. When the timer expires (approximately 50ms), the IC shuts down.

7. Error Amplifier

OZ9910 implements two error amplifiers, one for current feedback and the other for voltage feedback. For a CCFL working in the ignition period, the voltage feedback loop controls the ignition voltage. The non-inverting input is fixed at 3V. Once the lamp is ignited, the current feedback loop controls the amount of power delivered to the lamp. The non-inverting input is either ADJ when ADJ pin is greater than 1.5V or fixed at 1.5V when ADJ pin is less than 1.5V.

8. Combined Analog and Digital Dimming Control

A built-in function combines the low-frequency PWM (LPWM) and analog adjustment dimming functions to perform wide dimming control for the CCFL. The LPWM frequency is determined by capacitor C9 and resistor R1 connected to LCT (pin 6). The frequency is approximated by the following equation:

$$f_{LF}[\text{Hz}] = \frac{2.9 \times 10^6}{C_{LCT} [\text{pF}] \times R_{LCT} [\text{Meg}\Omega]}$$

When the ADJ pin input voltage is less than 1.5V, the ADJ pin is compared with the triangle LCT waveform and yields a proper low frequency pulse width to modulate the CCFL brightness. The peak and valley of the LCT signal are 1.5V and 0V respectively. When the ADJ pin input voltage is increased above 1.5V, the low frequency pulse width achieves 100% duty cycle and ADJ pin input voltage serves as the command signal to regulate the CCFL current.

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9. Feed-forward Compensation

Input voltage to the IC is intelligently processed to yield a constant/symmetrical waveform at CMP_SST (pin 10) to achieve a feed-forward-compensation function during dimming control.

10. Output Drives

The four output drives are designed to turn-on and turn-off four switches M1, M2, M3 and M4 with intelligent phase-shift control technique. The design allows the free-wheeling diode to reset transformer in each half cycle. The body diodes associated with four switches can be served as the free-wheeling diodes. For example, the diode D3 and diode D4 are used as free-wheeling diodes for M1 and M2 switches during the first half cycle. The diodes D1 and D2 are used as the free-wheeling diodes for M3 and M4 switches during the next half cycle. The switches in the bridge are configured such that M1/M4 and M2/M3 are turned-on complementarily. This brake before make (BBM) is implemented to prevent the power source shorted to the ground. Adjusting the overlapped conduction between switches M1/M2 and M3/M4 senses the current flowing in the CCFL, thus the power delivered to the CCFL is regulated.

The waveforms associated with a typical two-transistor forward converter are shown in Figures 4, pages 12.

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REFERENCE APPLICATION CIRCUIT

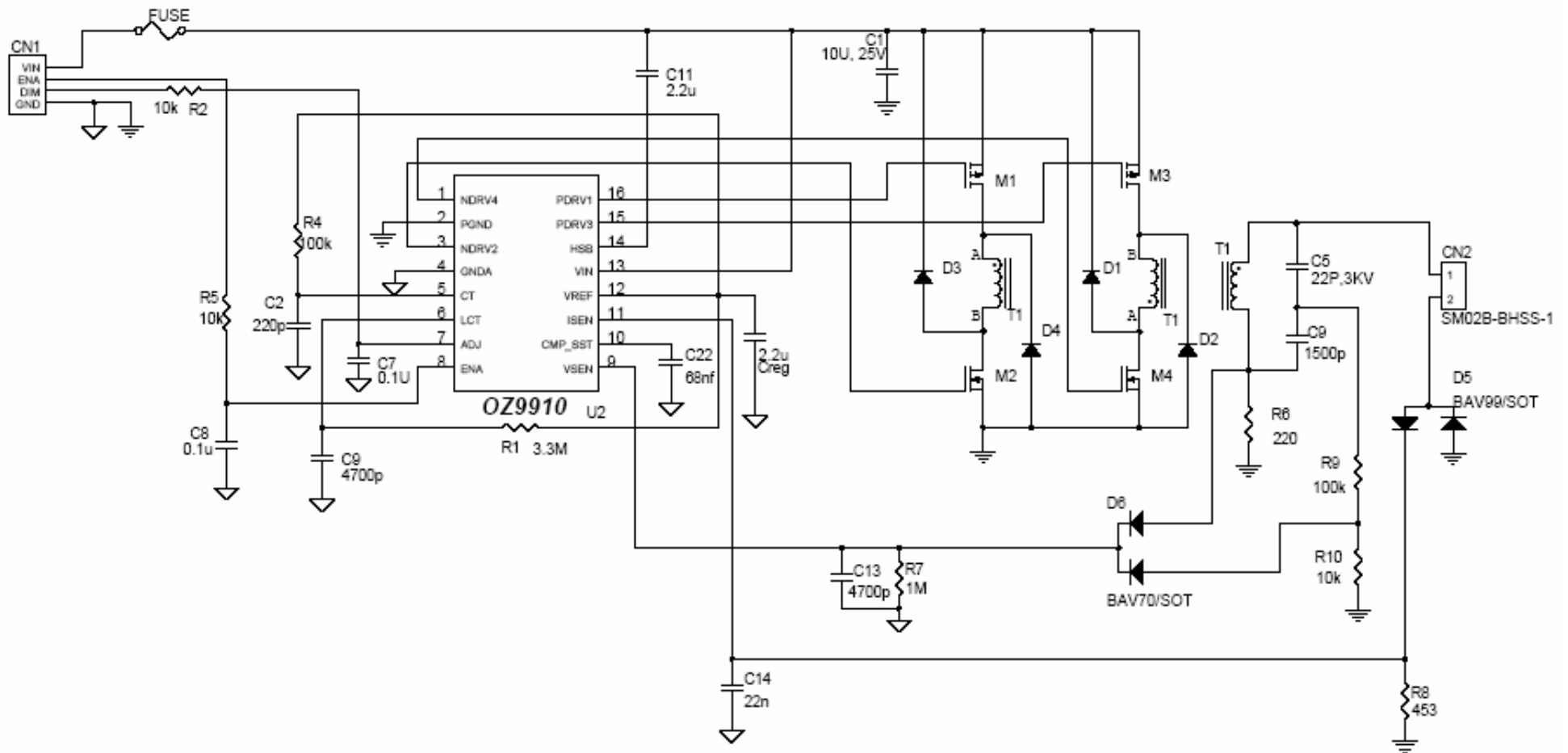


Figure 2. Application Circuit for CCFL

REFERENCE APPLICATION CIRCUIT

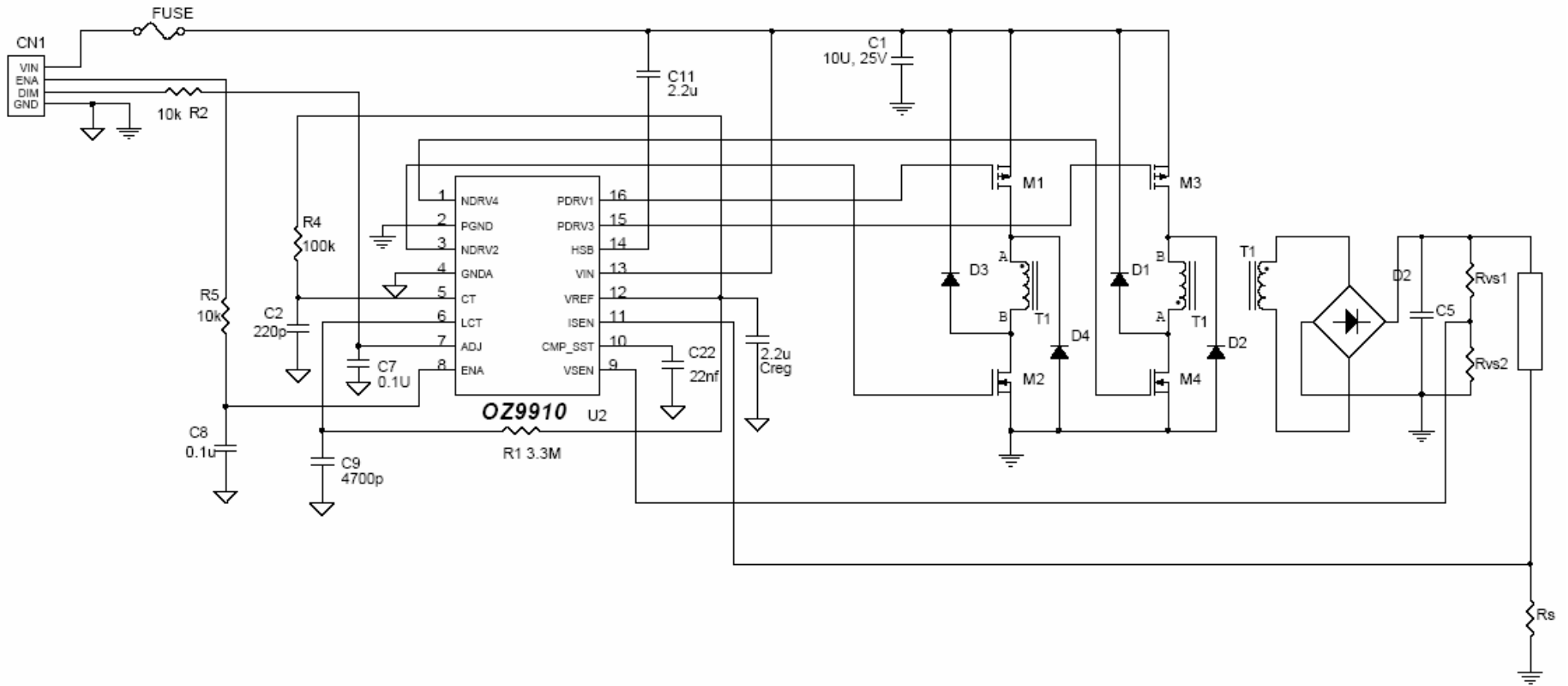
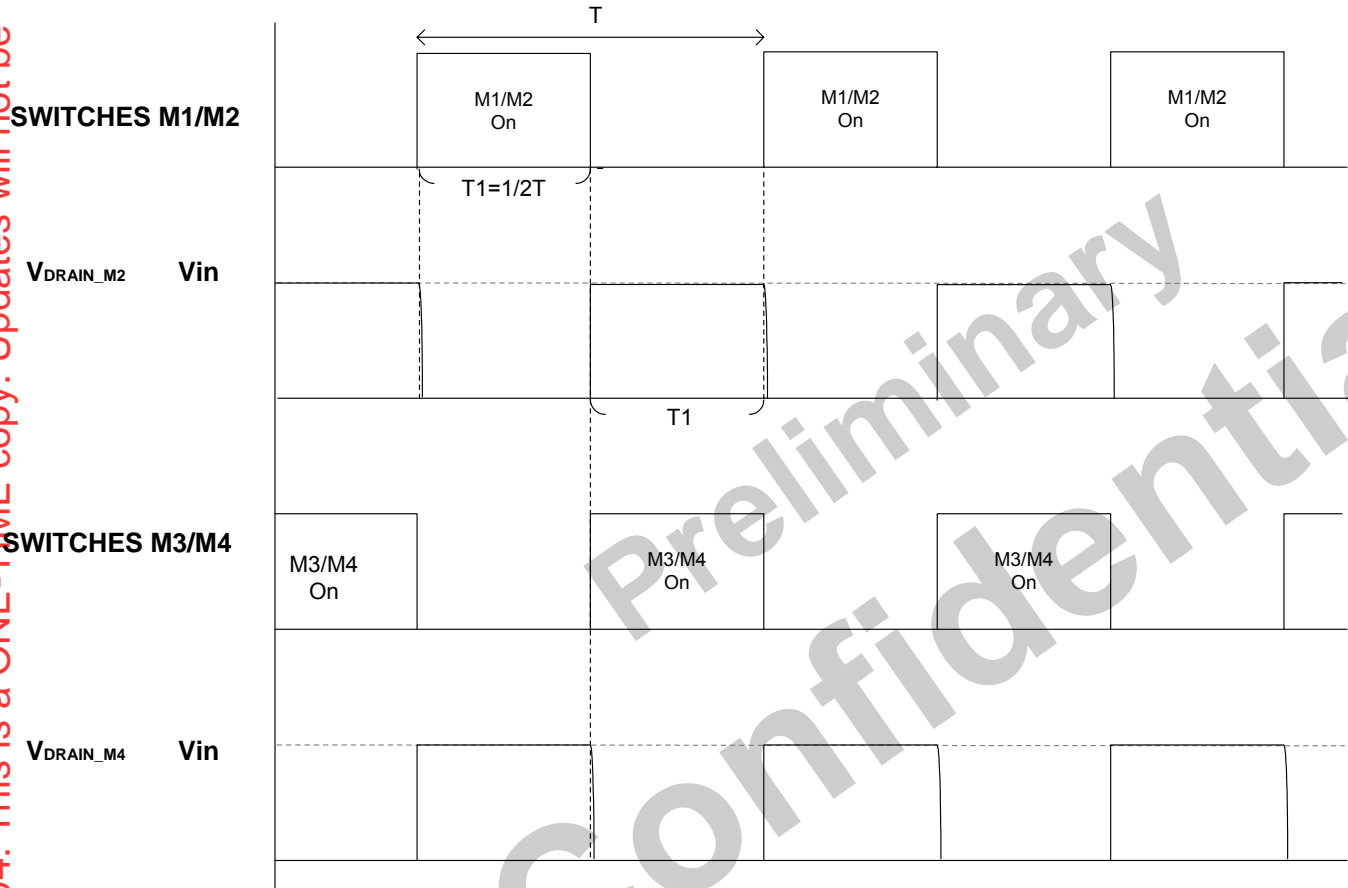


Figure 3. Application Circuit for TWT

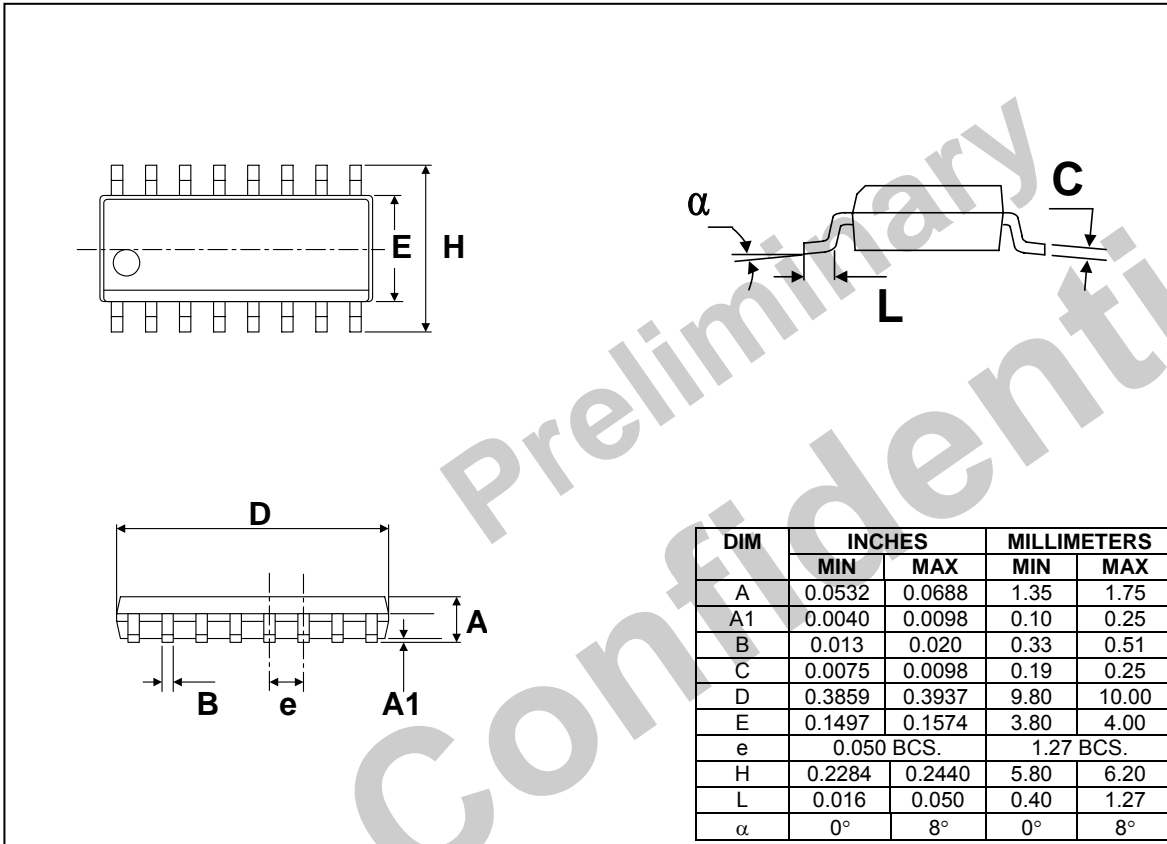
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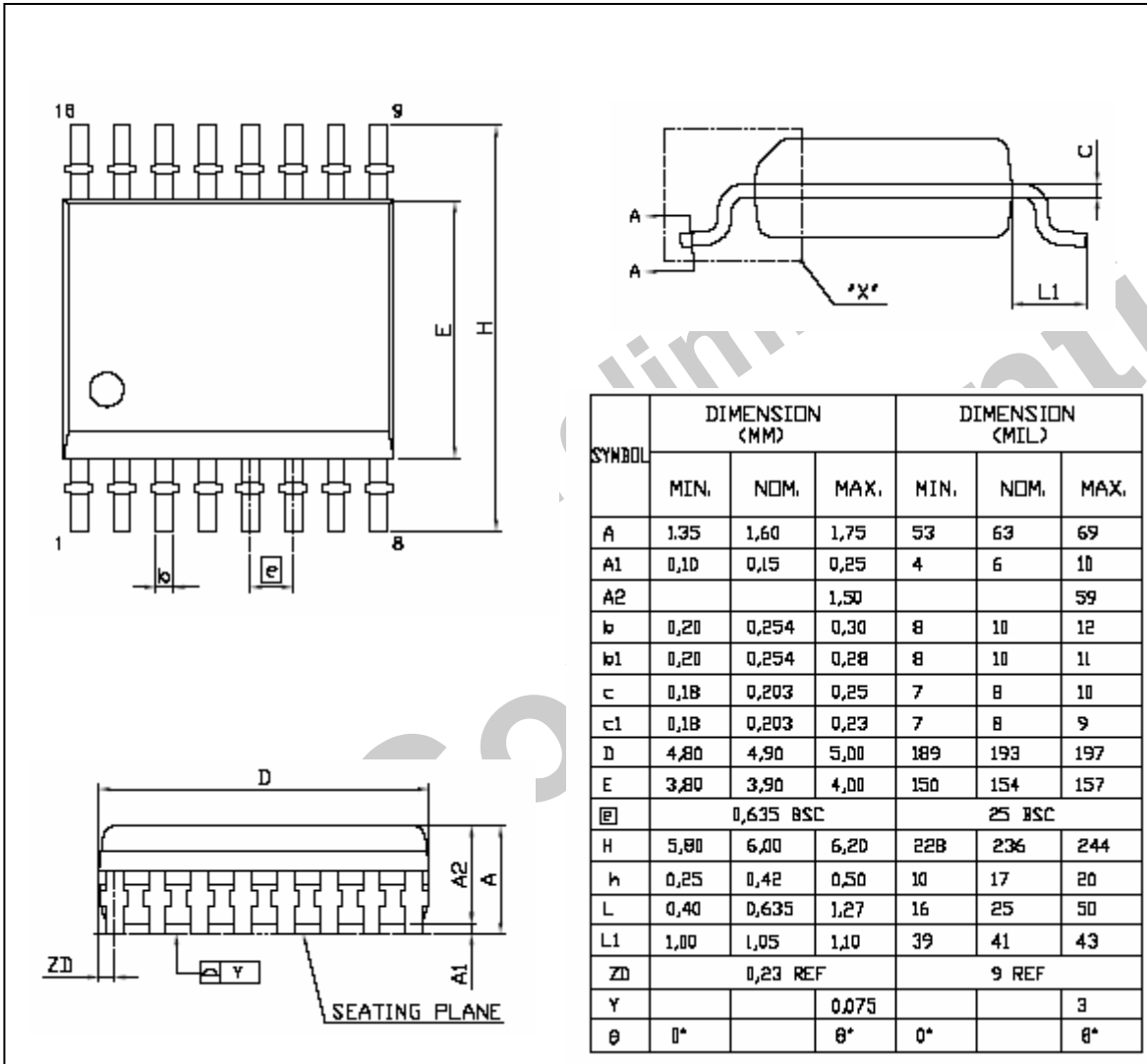
**Figure 4. OZ9910 Waveforms:
50% Duty Cycle of a 2 Transistor Forward Converter**

PACKAGE INFORMATION – 16-PIN SOP 150mil: OZ9910G

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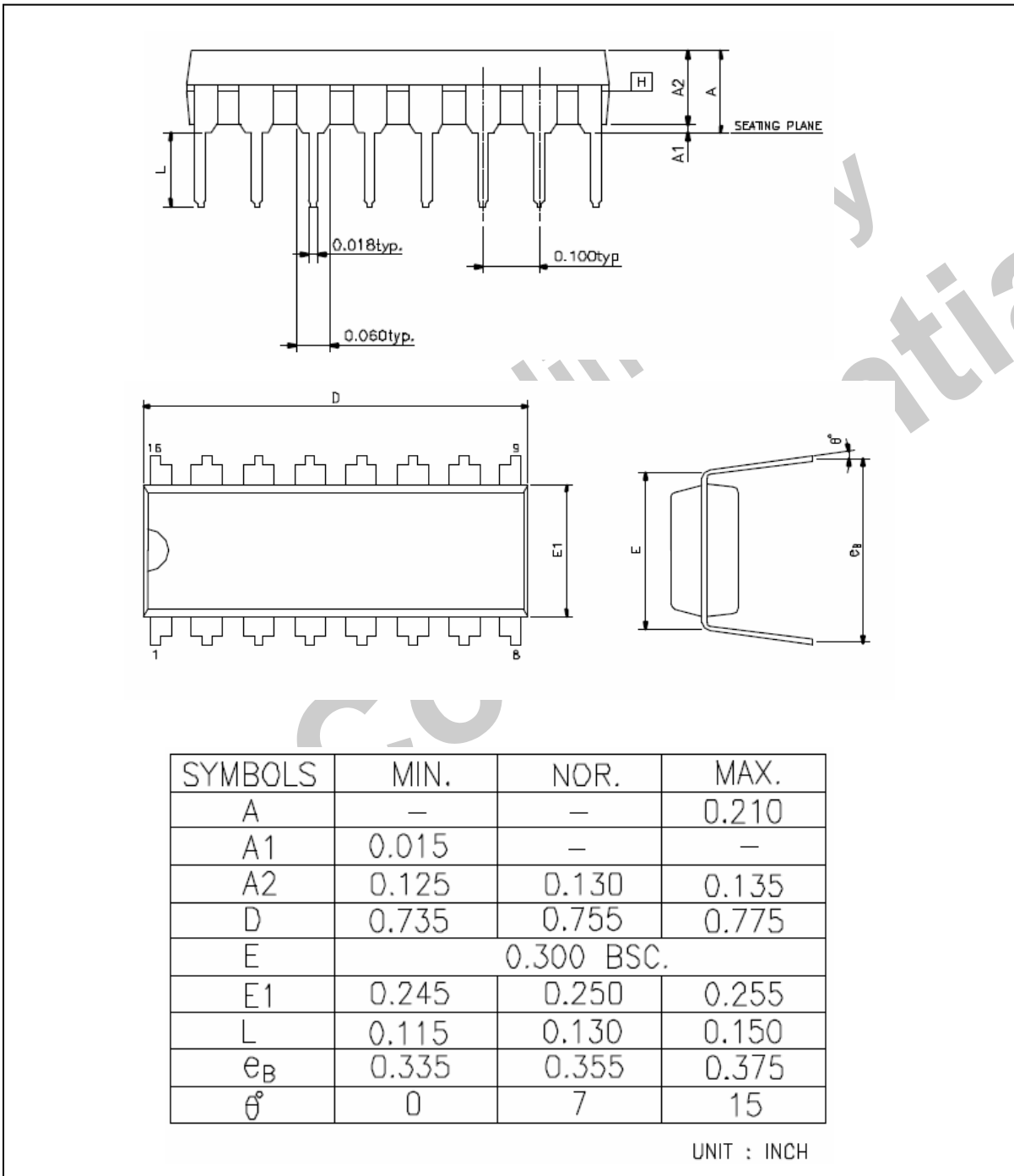
PACKAGE INFORMATION – 16-PIN SSOP 150mil: OZ9910S



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PACKAGE INFORMATION – 16-PIN DIP 300mil: OZ9910D

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