Prediction Technology to Control Synchronous Rectifiers

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INTRODUCTION

There are many discrete solutions to control and drive synchronous rectifiers (SR) in isolated switch mode power converters. Some complex discrete self-driven solutions attempt to provide full width gate drive to synchronous rectifiers in order to minimize synchronous rectifier body diode conduction and obtaining maximum converter efficiency.

This paper focuses and limits our subject area to providing full width gate drive to synchronous rectifiers in the freewheel position of a forward converter for better converter efficiency, and its associated problems. More specifically, we will review the principles of the full width gate self-driven synchronous rectifier techniques and describe the predictive technology used in the new Synchronous Rectifier Controller IC (SR-CIC) from SYNC POWER CORP.

FULL WIDTH SELF-DRIVEN SYNCHRONOUS RECTIFIERS

There are two well known techniques using discrete solution to achieve Full Width Self-Driven Synchronous Rectifiers (FW-SD-SR) in forward converters: active clamped and output inductor voltage-based.

Active Clamp Based

Active clamped forward converters have been widely discussed in other publications and its operation is well understood, but its use has been limited mostly due to patent issues. In general, active clamped forward converters provide a good almost full gate width drive to the freewheel synchronous rectifier, where the body diode conduction is minimized. However, active clamped synchronous rectifier forward converters have the following problems:

1) **Light load reverse conduction**

   In light load condition, because the transformer is actively clamped, the freewheel synchronous rectifier reverse conducts and forces the converter into Forced-Continuous Current Mode (F-CCM) operation, where the output inductor current reverses. This affects the light load efficiency, but improves converter load response time. Excluding the Japanese market, some N+1 systems and portable applications, the synchronous rectifier reverse conduction in light load or the F-CCM may not be a major issue in most applications.

2) **Negative converter output voltage when input voltage is being shut-off**

   The actively clamped transformer reset voltage keeps the freewheel synchronous rectifier in the bi-directional ON conduction state when the converter PWM controller locks OFF the primary switch in a UVL state -- this occurs when the converter input source is being removed or shut-off.

After the output inductor energy has been dissipated though the reverse conducting freewheel synchronous rectifier, the output capacitor and inductor goes into oscillation through the bi-directional freewheel synchronous rectifier, resulting in a negative converter output voltage (as shown in Figure 1). This negative output voltage can result in the destruction of the load (typically VLSI IC, such as micro-processors, DSP or other logic IC). Often other measures must be taken with the standard active clamped converters to avoid this serious problem; however, circuit complexity also increases substantially.

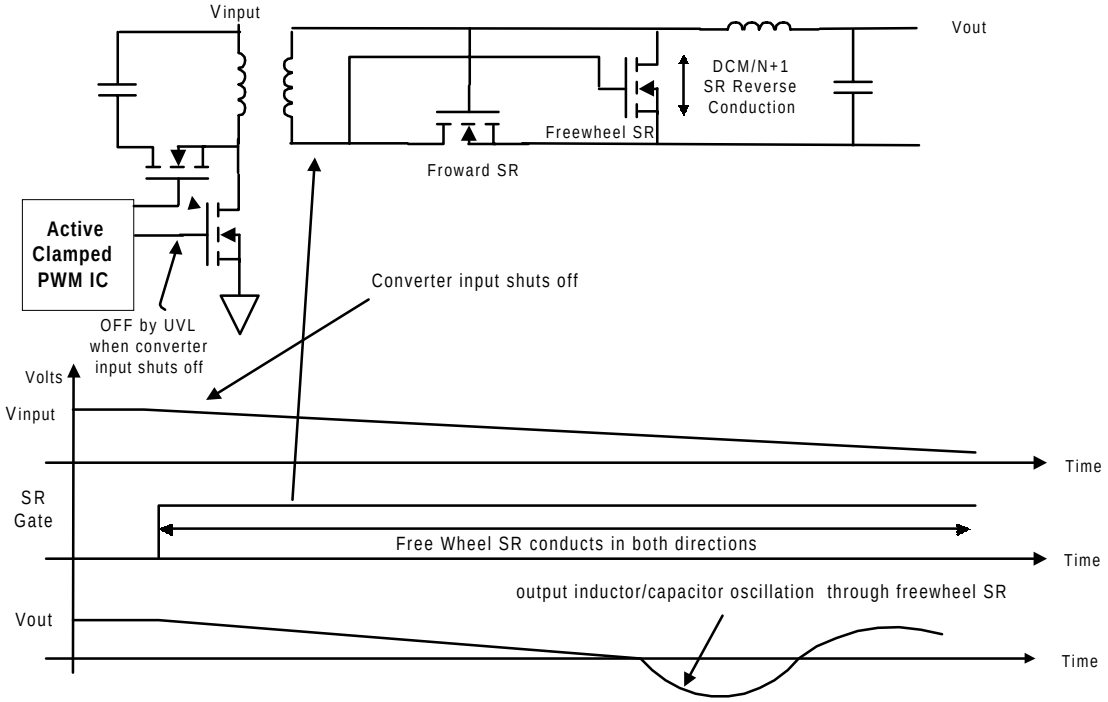

Figure 1. Active clamped synchronous rectifier forward converter may produce a negative output voltage when input shuts off.

Output Inductor Voltage Based

The voltage across the output inductor in a forward converter can also be used to obtain the gate drive signal for the freewheel synchronous rectifier. Because of the patent issue with the active clamped converter, many companies have chosen to use one form or another of the output inductor voltage-based synchronous rectifier control schemes. While it can potentially offer higher converter efficiency, the control scheme itself is inherently dangerous, operating with possible significant cross conduction between the primary switch and the secondary freewheel synchronous rectifier (as will be discussed in the following section).

Shown in Figure 2, while the converter is in the freewheel state (primary switch OFF, the output inductor discharging through the output capacitors), the voltage across the output inductor (VL) is approximately the converter output voltage (Vout). This VL can be used to drive the freewheel synchronous rectifier.

The concept is that since VL is equal to Vout until the primary switch is turned ON, the freewheel synchronous rectifier receives the full width gate drive during the entire period that the inductor is in freewheel state, and obtaining the maximum possible efficiency (as shown in Figure 2). There are various different forms of this type of synchronous rectifier drivers, but all are based on the same principles.

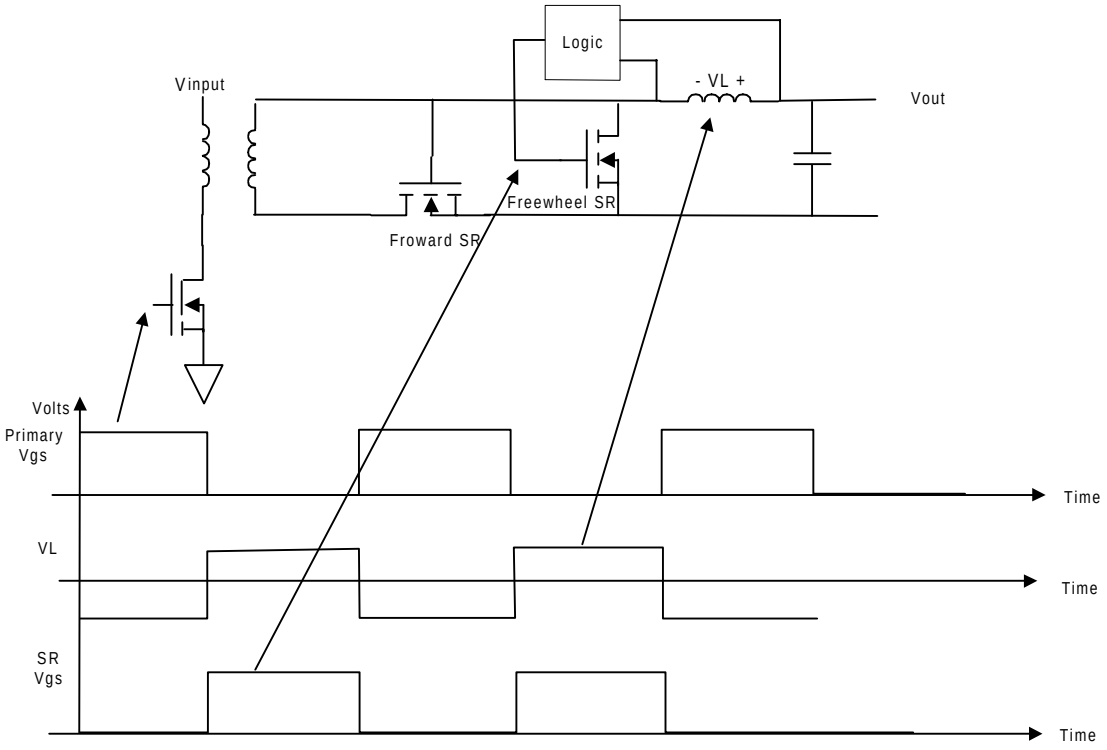

Figure 2. Output inductor voltage-based (VL) freewheel synchronous rectifier driving circuit

There are, however, two major problems with VL based synchronous rectifier drive schemes. They are discussed below:

1) Turn off synchronous rectifier cross conduction

The ideal operation requires the freewheel synchronous rectifier to turn off before the primary switch turns on. Otherwise, large reverse conduction (cross conduction with primary switch) in the freewheel synchronous rectifier occurs. This reverse conduction negates synchronous rectifier efficiency, causes conduction and EMI noises and at worst, may even cause destruction of the converter.

In the VL based synchronous rectifier driving schemes, the freewheel synchronous rectifier is on as long as inductor voltage (VL) is negative and the inductor is discharging. But the inductor voltage remains negative and remains in the discharging state as long the freewheel synchronous rectifier is on. This interlocking relationship can only be reversed when the primary switch and the freewheel synchronous rectifier goes through a substantial cross conduction as shown in Figure 3. This substantial cross conduction is required at every cycle to turn OFF the freewheel synchronous rectifier.

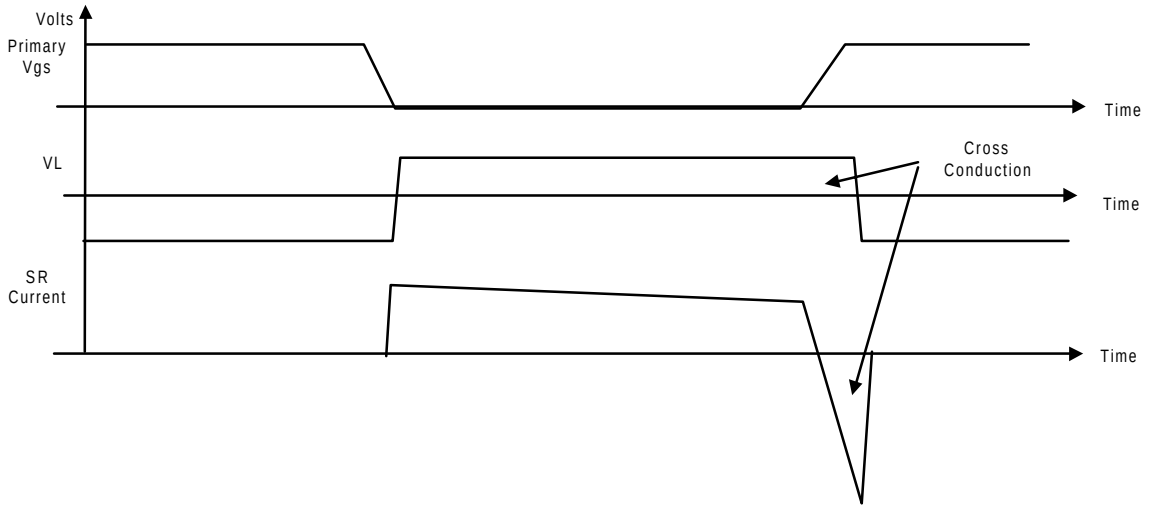

Figure 3. The interlocking relationship of synchronous rectifier Vgs and VL makes synchronous rectifier cross conduction unavoidable at every cycle

2) Light load synchronous rectifier reverse conduction

Similar to the active clamped forward converters, the output inductor voltage (VL) based controlled freewheel synchronous rectifier reverse conduct in light load, thus the converter goes into the forced continuous current mode (F-CCM) as shown in Figure 4. Except for the Japanese market and some N+1 systems, forced continuous current mode may not be an issue.

SYNCHRONOUS RECTIFIER CONTROLLER IC (SR-CIC)

The recently introduced Synchronous Rectifier Controller IC (SR-CIC) uses prediction technology to control the operation of synchronous rectifiers.

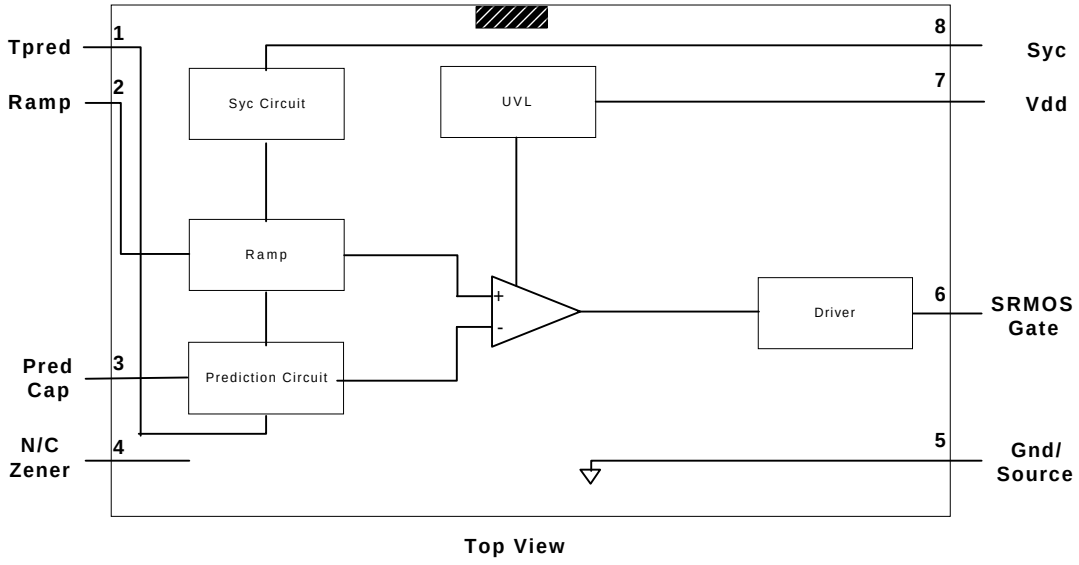

Figure 4. Block diagram of the Synchronous Rectifier Controller IC (SR-CIC)

In the SR-CIC, this prediction intelligence is achieved by using previous primary switch timing information to predict the present timing, and synchronous rectifier cross conduction and reverse conduction are avoided. The previous cycle timing information is sensed at the drain of the freewheel synchronous rectifier MOS. The SR-CIC synchronizes this node (or other nodes with similar timing information), but allows the synchronous rectifier body diode to conduct for a small (adjustable at about 50ns) amount of time, so as to avoid reverse current through the channel of synchronous rectifiers. This is achieved by keeping a timing gap between the falling edge of the synchronous rectifier Vgs and the rising edge of the freewheel synchronous rectifier drain voltage (for the forward position, the timing gap is between the rising edge of forward the synchronous rectifier Vgs and rising edge of the freewheel synchronous rectifier drain voltage). This timing gap is referred to as the prediction time. During this timing gap, the body diode carries the current.

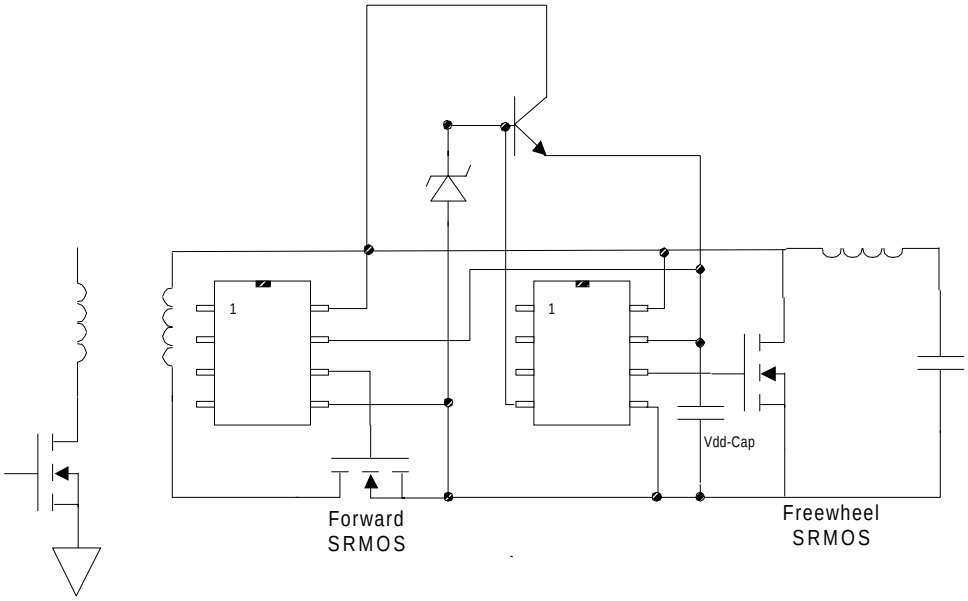

Figure 5. Forward converter schematic utilizing SR-CIC for both positions

The block diagram of the SR-CIC is shown in Figure 4, and schematic for a forward converter implemented by using SR-CIC is shown in Figure 5. The complete prediction-timing diagram is shown in Figure 6. In the same figure, comparison was also made with the output inductor based (VL) self-driven synchronous rectifier timing.

By using this SR-CIC, synchronous rectifier reverse conduction is avoided while achieving very high converter efficiency. We are able to obtain over efficiency over 92 percent in a 3.3V, 10A and 250Khz forward converter using the SR-CIC in both the forward and freewheel position.

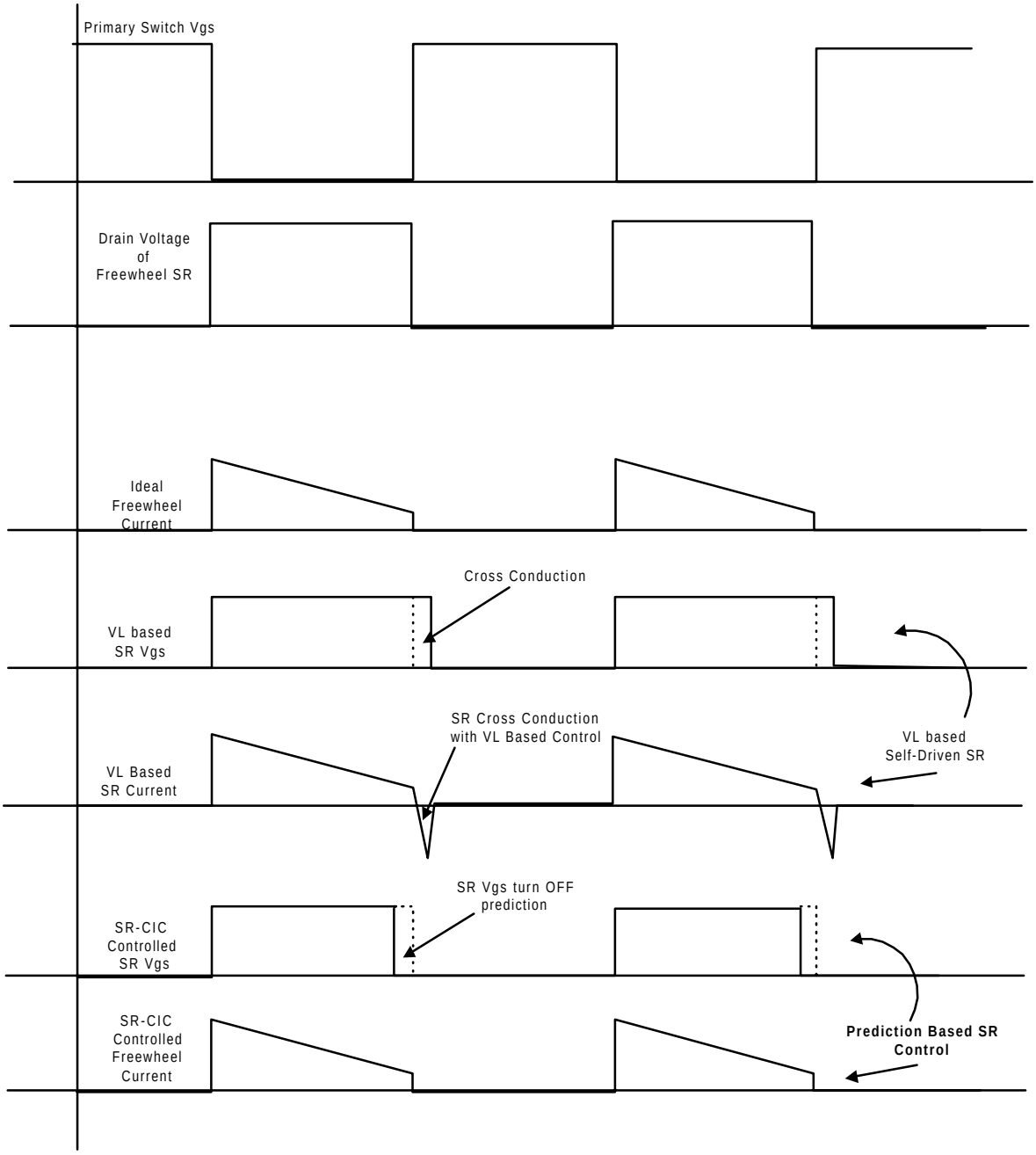

Figure 6. Comparison of timing diagram between SR-CIC (prediction) controlled and VL based Self-Driven synchronous rectifier

CONCLUSION

Most self-driven synchronous rectifier control methods are messy to use and require significant design effort. Still, many problems (mostly related to synchronous rectifier reverse conduction) cannot be easily resolved. With today's time to market pressure, the cumbersome self-driven method desperately needs alternatives.

The easy-to-use SR-CIC offers significant savings in effort, while providing high-converter efficiency as shown in the table below. Because the SR-CIC does not allow reverse synchronous rectifier conduction, the converter operates much like a traditional diode was in place, but at higher efficiency.

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250KHz Forward	Typical Efficiency
Schottky	Low 80%
Self-Driven Synchronous Rectifier	Mid to High 80%
SR-CIC	**Low 90%**