

EVALPFC2-ICE2PCS01

300W PFC Evaluation Board with CCM PFC controller ICE2PCS01

Power Management & Supply



Never stop thinking.

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EVALPFC2-ICE2PCS01**Revision History: 2006-12****V1.0**

Previous Version:

Page	Subjects (major changes since last revision)

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Table of Content

1	Content.....	5
2	Evaluation Board.....	5
3	Technical Specifications	6
4	Circuit Description	6
5	Circuit Operation.....	6
6	Circuit Diagram	8
7	PCB Layout Top Layer.....	9
8	PCB layout Bottom Layer	10
9	Component List.....	11
10	Boost Choke Layout	122
11	Test report	12
11.1	Load test (table and figure)	12
11.2	Harmonic test according to EN61000-3-2 Class D requirement.....	14
11.3	Test Waveforms	15
12	References:.....	16



3 Technical specifications:

Input voltage	85VAC~265VAC
Input frequency	50Hz
Output voltage and current	393VDC, 0.75A
Output power	~ 300W
Efficiency	>90% at full load
Switching frequency	62.5kHz (with R8=76K)

4 Circuit Description

Line Input

The AC line input side comprises the input fuse F1 as over-current protection. The high frequency current ripple is filtered by R1, L1 and CX1. The choke L2, X2-capacitors CX1 and CX2 and Y1-capacitor CY1 and CY2 are used as radio interference suppressors. RT1 is placed in series to limit inrush current during each power on.

Power Stage – Boost Type PFC Converter

After the bridge rectifier BR1, there is a boost type PFC converter consisting of L3, Q1, D1 and C2. The third generation **CoolMOS™** is used as the power switch Q1. Due to its low $R_{ds(on)}$, the small heat sink can fulfill the dissipation requirement. SiC Schottky diode **thinQ!™** is used for D1. As SiC Schottky diode does not show a reverse recovery behavior, the stress on the MOSFET will be reduced due to very low current spike during turn on transient. Simultaneously higher reliability of the entire system can be achieved. However, due to the poor pulse current capability of SiC Schottky diode, a standard diode D2 is necessary to bypass the high inrush current during each power on transient. Output capacitor C2 provides energy buffering to reduce the output voltage ripple (100Hz) to the acceptable level.

PWM control of Boost Converter

The PWM control is realized by 8-Pin CCM PFC IC **ICE2PCS01**. Unlike the conventional PFC controller, **ICE2PCS01** does not need direct sine wave reference signal. The switching frequency is fixed and programmed by R8. There are two control loops in the circuit, voltage loop and current loop. The output voltage is sensed by the voltage divider of R5A, R5B, R6A and R6B and sent to internal error amplifier. The output of error amplifier is used to control current in the inner current loop. The compensation network C4, C5, R7 constitutes the external circuitry of the error amplifier. This circuitry allows the feedback to be matched to various load conditions, thereby providing stable control. In order not to make the response for 100Hz ripple, the voltage loop compensation is implemented with low bandwidth. The inner loop, current control loop, is implemented with average current mode strategy. The instant current is adjusted to be proportional to both of MOSFET off duty D_{OFF} and the error amplifier output voltage of voltage loop. The current is sensed by shunt resistors R2, R2A and R2B and fed into IC through R9. The current sense signal is averaged by an internal operating amplifier and then processed in the PWM generator which drives the gate drive. The averaging is realized by charging and discharging an external capacitor C7.

The IC supply is provided by external voltage source and filtered and buffered by C8 and C9. The IC output gate driver is a fast totem pole gate drive. It has an in-built cross conduction current protection and a Zener diode to protect the external transistor switch against undesirable over voltages. The gate drive resistor R4 is selected to limit and gate pulse current and drive MOSFET for fast switching.

5 Circuit Operation

Soft Start

When Vcc pin is higher than turn-on threshold, typical 11V, PFC is going to start. The unique soft start is integrated. Input current keeps sinusoidal and is increasing gradually until output voltage reaches



75% of rating. Because the peak current limit is not activated, the boost diode is not stressed with large diode duty cycle under high current.

Enhanced Dynamic Response

Due to inherent low bandwidth of PFC dynamic, in case of load jump, regulation circuit can not response fast enough and it will lead to large output voltage overshoot or drop. To solve this problem in PFC application, enhance dynamic response is implemented in the IC. Whenever output voltage exceeds by $\pm 5\%$, it will bypass the slow compensation operating amplifier and act on the nonlinear gain block to affect the duty cycle directly. The output voltage can be recovered in a short time.

Protection Features

a. Open loop protection (OLP) / Mains under voltage protection

The open loop protection is available for this IC to safe-guard the output. Whenever V_{SENSE} voltage falls below 0.6V, or equivalently V_{OUT} falls below 20% of its rated value, it indicates an open loop condition (i.e. VSENSE pin not connected). In this case, most of the blocks within the IC will be shutdown. It is implemented using a comparator with a threshold of 0.6V. Insufficient input voltage V_{IN} will also trigger this protection.

b. Output over-voltage protection

Output over-voltage protection is also available by the same integrated blocks of enhanced dynamic response. Whenever V_{OUT} exceeds the rated value by 5%, the over-voltage protection OVP is active. This is implemented by sensing the voltage at pin V_{SENSE} with respect to a reference voltage of 3.15V. A V_{SENSE} voltage higher than 3.15V will immediately reduce the output duty cycle even down to zero, bypassing the normal voltage loop control. This results in a lower input power and the output voltage V_{OUT} is reduced.

c. Soft over current control (SOC) and peak current limit

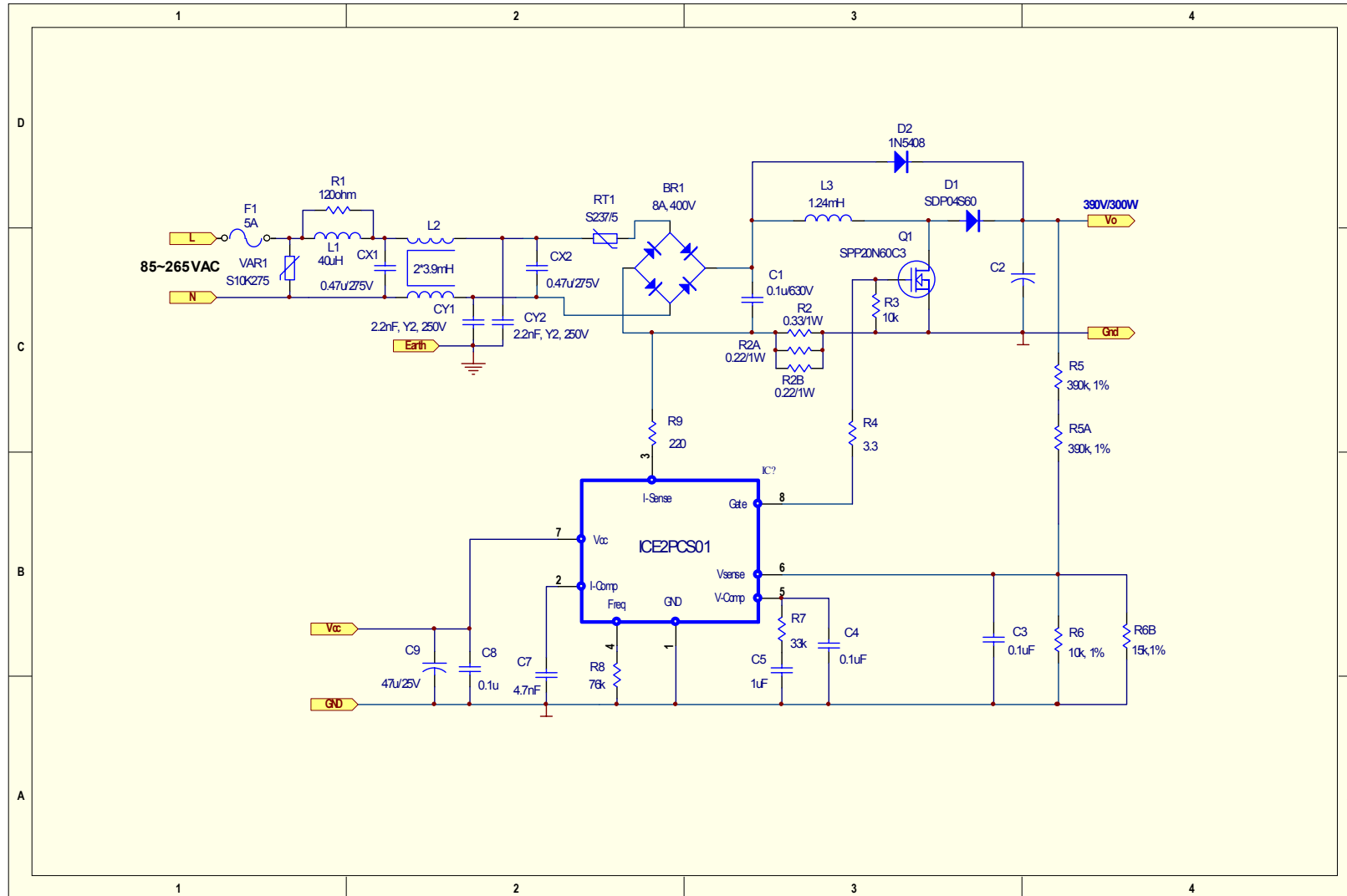
When the amplitude of current sense voltage reaches 0.68V, Soft Over Current Control (SOC) is activated. This is a soft control does not directly switch off the gate drive but acts on the internal blocks to result in a reduced PWM duty cycle.

The IC also provides a cycle by cycle peak current limitation (PCL). It is active when the voltage at current sense voltage reaches -1.04V. The gate output is immediately off after 300ns blanking time.

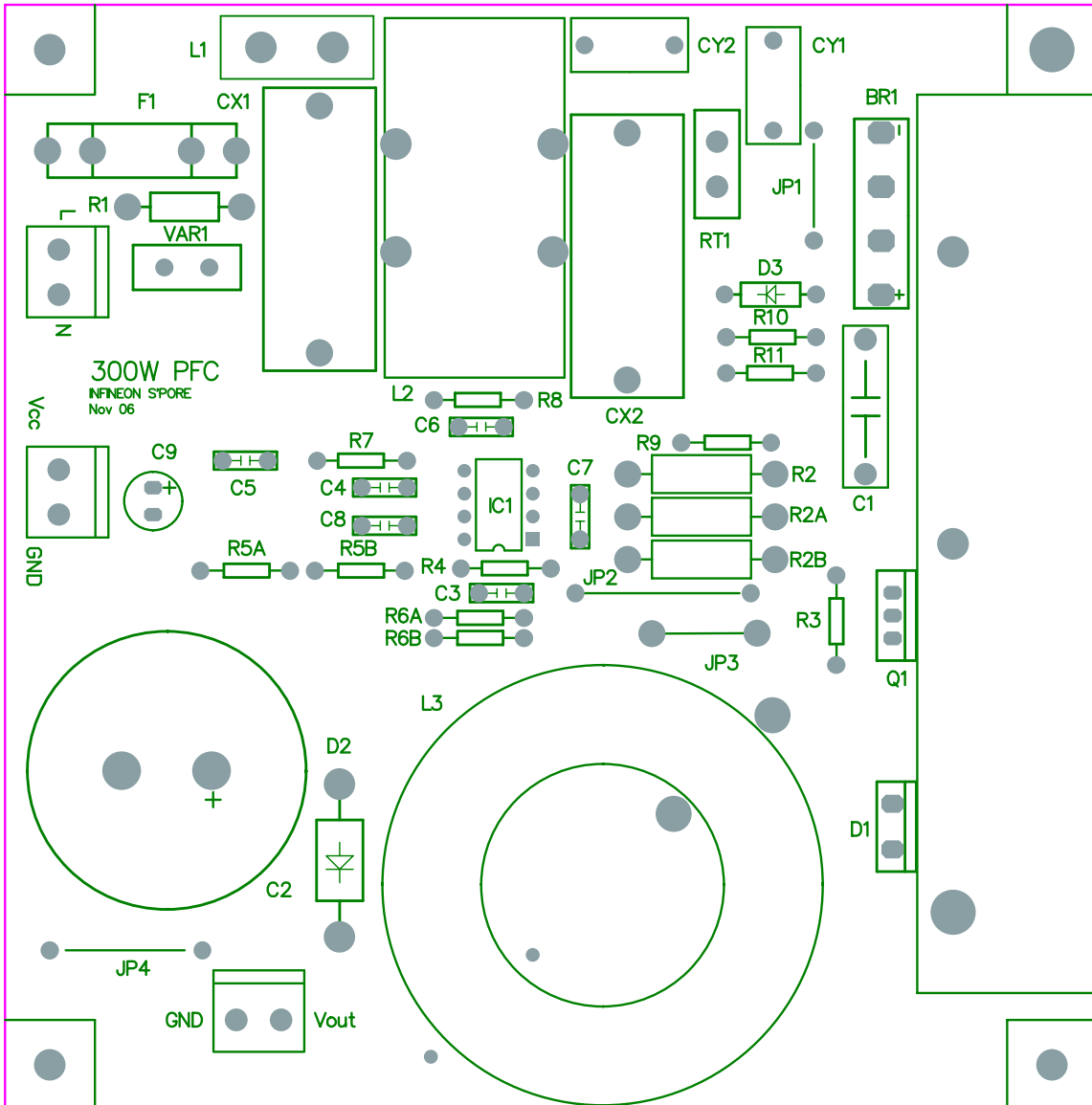
d. IC supply under voltage lock out

When VCC voltage is below the under voltage lockout threshold V_{CCUVLO} , typical 11V, IC is off the gate drive is internally pull low to maintain the off state. The current consumption is down to 200uA only.

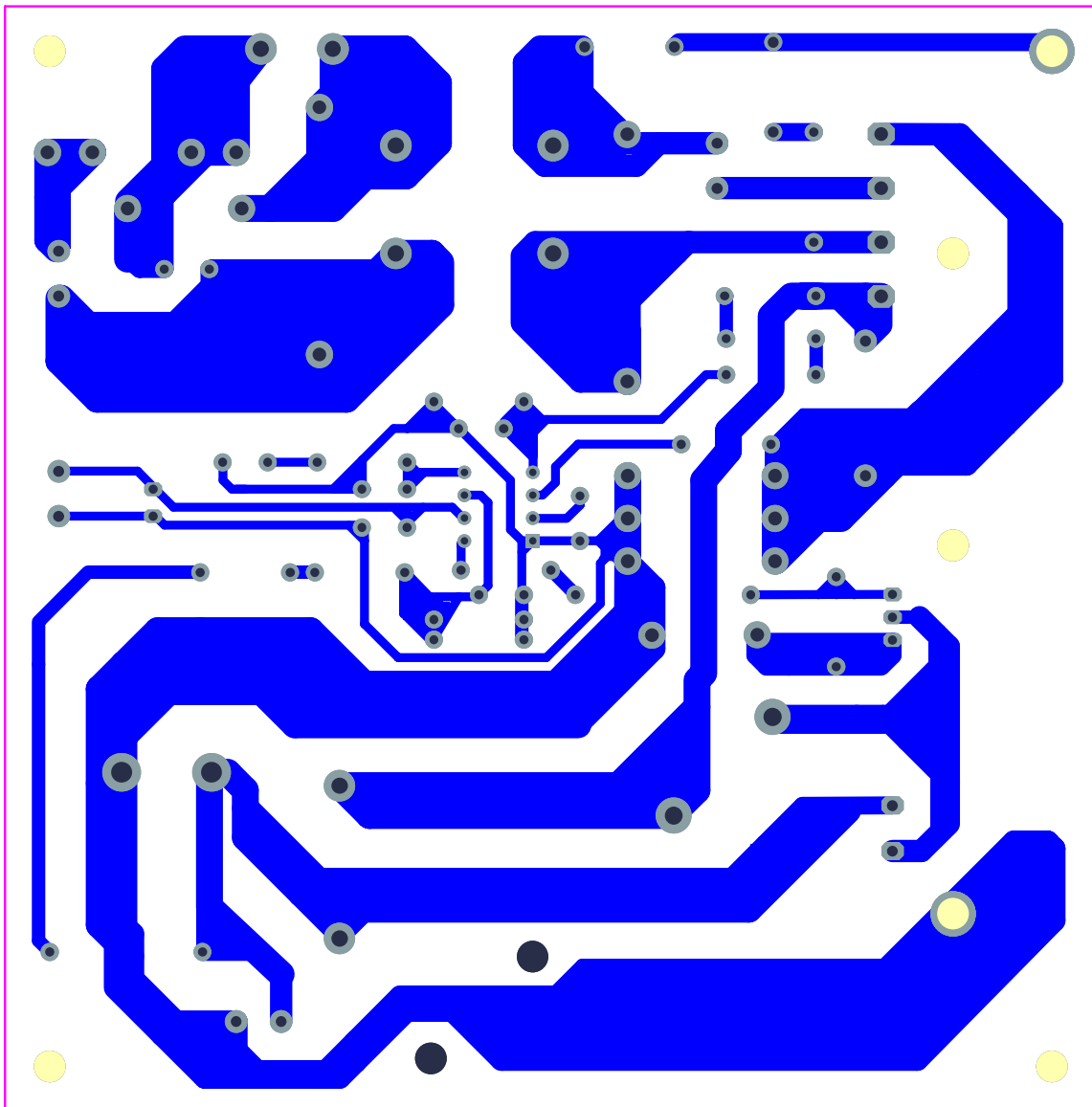
6 Circuit Diagram



7 PCB layout top layer



8 PCB layout Bottom:



9 Component List:

Designator	Part Type	Description	Quantity
BR1	8A, 400V	Bridge Rectifier	1
C1	0.1uF/630V	Ceramic Cap	1
C2	220uF/450V	Electrolytic Cap	1
C3	0.1uF/50V	Ceramic Cap	1
C4	0.1uF/50V	Ceramic Cap	1
C5	1uF/50V	Ceramic Cap	1
C7	4.7nF/50V	Ceramic Cap	1
C8	0.1uF/50V	Ceramic Cap	1
C9	47uF/25V	Electrolytic Cap	1
CX1	0.47uF, X1, 275V	Ceramic Cap	1
CX2	0.47uF, X1, 275V	Ceramic Cap	1
CY1	2.2nF, Y2, 250V	Ceramic Cap	1
CY2	2.2nF, Y2, 250V	Ceramic Cap	1
		Connector	3
D1	SDT04S60	Diode	1
D2	1N5408	Diode	1
F1	5A	Fuse	1
		Fuse Holder	2
IC1	ICE2PCS01		1
JP1	12.5mm, Φ 0.7mm	Jumper	1
JP2	20mm, Φ 0.7mm	Jumper	1
JP3	12mm, Φ 1.2mm	Jumper	1
JP4	17.5mm, Φ 0.7mm	Jumper	1
L1*	Shorted		0
L2	2*3.9mH	CM Choke	1
L3	1.24mH	Choke	1
Q1	SPP20N60C3	Power MOSFET	1
		Heat Sink	1
		TO220 Clip	2
		TO247 Clip	1
		TO220 Isolation Pad	2
		3mm Screw	3
R2	0.33/1W, 5%	Metal Film Resistor	1
R2A	0.22/1W, 5%	Metal Film Resistor	1
R2B	0.22/1W, 5%	Metal Film Resistor	1
R3	10k/0.25W, 5%	Carbon Film Resistor	1
R4	3.3/0.25W, 5%	Carbon Film Resistor	1
R5A	390k/0.25W, 1%	Carbon Film Resistor	1
R5B	390k/0.25W, 1%	Carbon Film Resistor	1
R6A	10k/0.25W, 1%	Carbon Film Resistor	1
R6B	15k/0.25W, 1%	Carbon Film Resistor	1
R7	33k/0.25W, 5%	Carbon Film Resistor	1
R8	76k/0.25W, 1%	Carbon Film Resistor	1
R9	220/0.25W, 5%	Carbon Film Resistor	1
RT1	S237/5	NTC Thermistor	1
VAR1	S10K275	Varistor	1

10 Boost Choke Layout

Core: CS468125 toriod

Turns: 83

Wire: 1 x Φ 1.0mm, AWG19

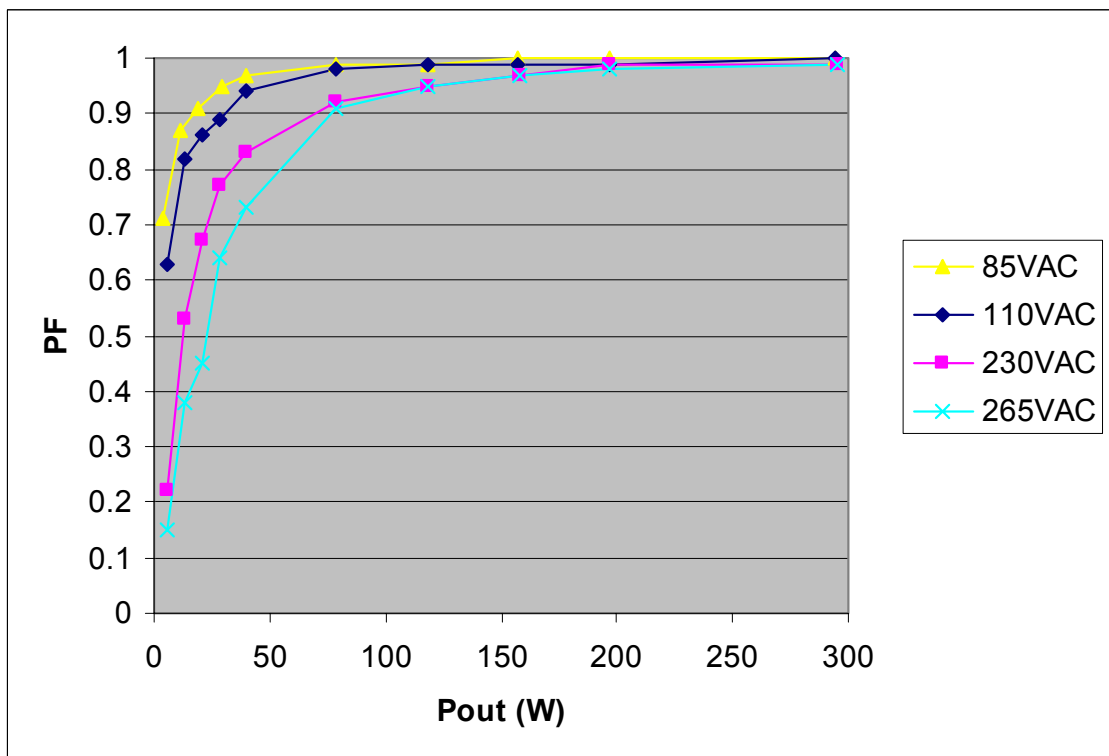
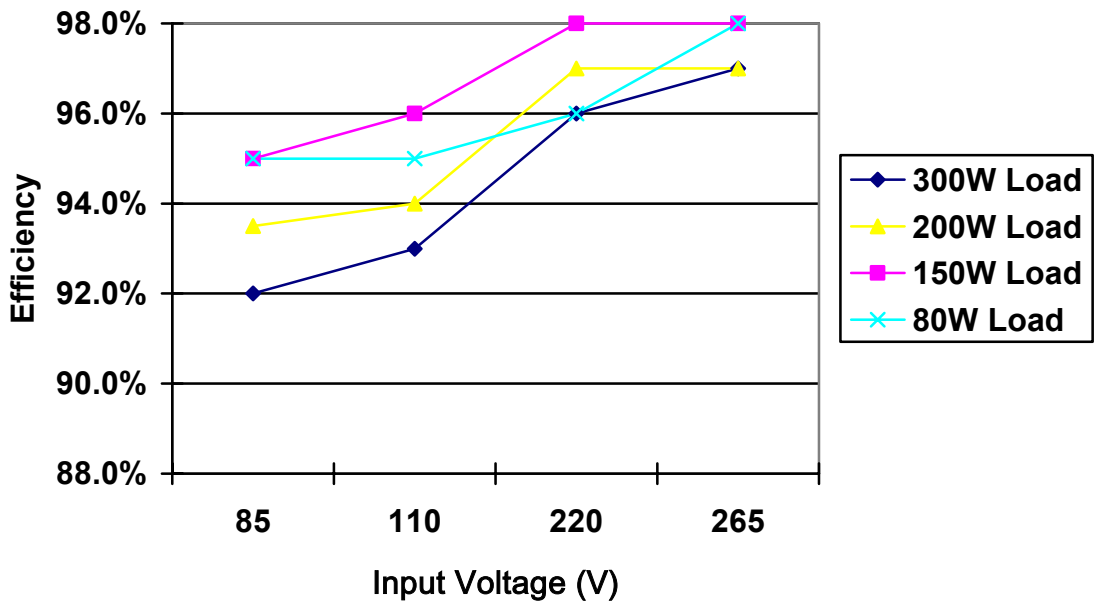
Inductance: L=1.24mH

11 Test report

11.1 Load test (table and figure):

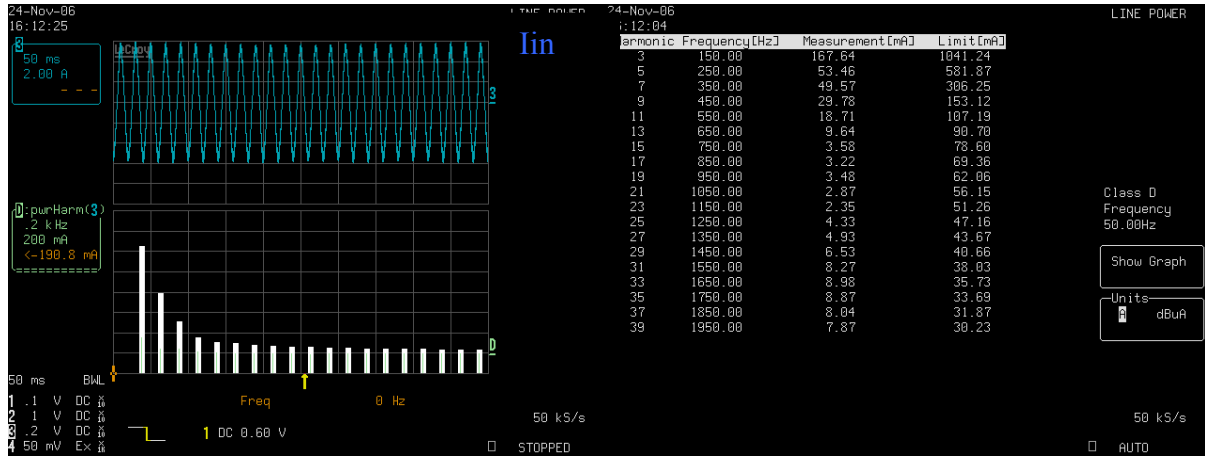
Vin (VAC)	Pin (W)	Iin (A)	Vout (V)	Iout (A)	Pout (W)	efficiency	PF
85	320	3.8	393	0.75	294.75	92%	1
	211	2.51	393	0.5	196.5	93%	1
	165	1.96	393	0.4	157.2	95%	1
	124	1.47	393	0.3	117.9	95%	0.99
	83	0.99	393	0.2	78.6	95%	0.99
	43	0.52	394	0.1	39.4	92%	0.97
	31	0.39	394	0.075	29.55	95%	0.95
	20.3	0.26	395	0.049	19.355	95%	0.91
	12.2	0.17	396	0.029	11.484	94%	0.87
	4.2	0.07	396	0.01	3.96	94%	0.71
110	316	2.9	393	0.75	294.75	93%	1
	208	1.91	393	0.5	196.5	94%	0.99
	163	1.5	393	0.4	157.2	96%	0.99
	123	1.13	393	0.3	117.9	96%	0.99
	83	0.77	393	0.2	78.6	95%	0.98
	42.3	0.4	393	0.1	39.3	93%	0.94
	30	0.29	394	0.0718	28.2892	94%	0.89
	22	0.22	394	0.0525	20.685	94%	0.86
	14.2	0.15	394	0.034	13.396	94%	0.82
	6.2	0.076	394	0.014	5.516	89%	0.63
220	307	1.4	394	0.75	295.5	96%	0.99
	204	1	394	0.5	197	97%	0.99
	161	0.8	394	0.4	157.6	98%	0.97
	120	0.63	394	0.3	118.2	99%	0.95
	82	0.45	394	0.2	78.8	96%	0.92
	41	0.29	394	0.1	39.4	96%	0.83
	29.5	0.16	395	0.072	28.44	96%	0.77
	21.7	0.133	395	0.053	20.935	96%	0.67
	14	0.1	395	0.033	13.035	93%	0.53
	6	0.093	395	0.014	5.53	92%	0.22
265	305	1.2	394	0.75	295.5	97%	0.99
	203	0.79	394	0.5	197	97%	0.98
	161	0.63	394	0.4	157.6	98%	0.97
	120	0.48	395	0.3	118.5	99%	0.95
	81	0.34	395	0.2	79	98%	0.91
	41	0.21	395	0.1	39.5	96%	0.73

29.5	0.17	395	0.072	28.44	96%	0.64
21.7	0.16	395	0.053	20.935	96%	0.45
13.8	0.15	395	0.033	13.035	94%	0.38
5.83	0.1	395	0.014	5.53	95%	0.15

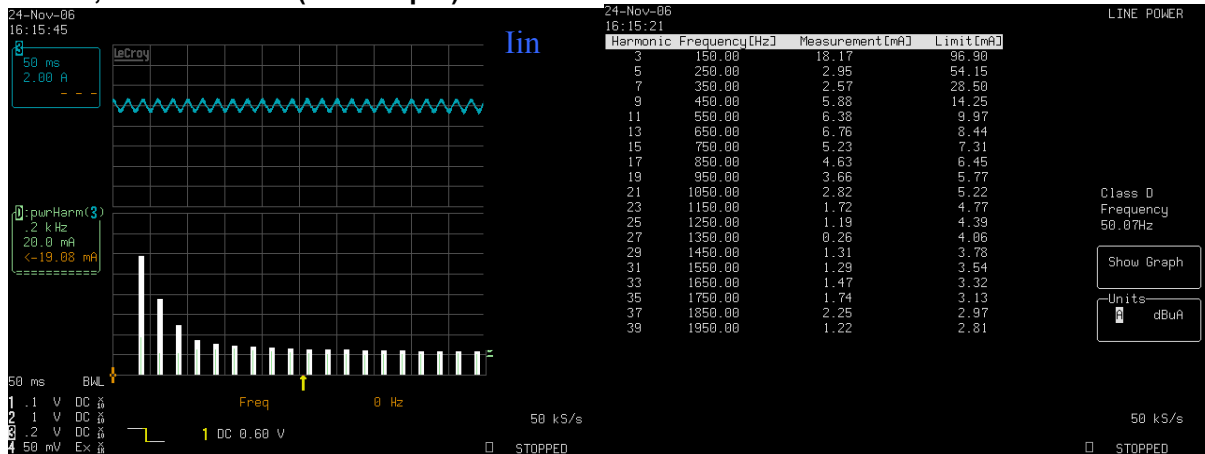


11.2 Harmonic test according to EN61000-3-2 Class D requirement

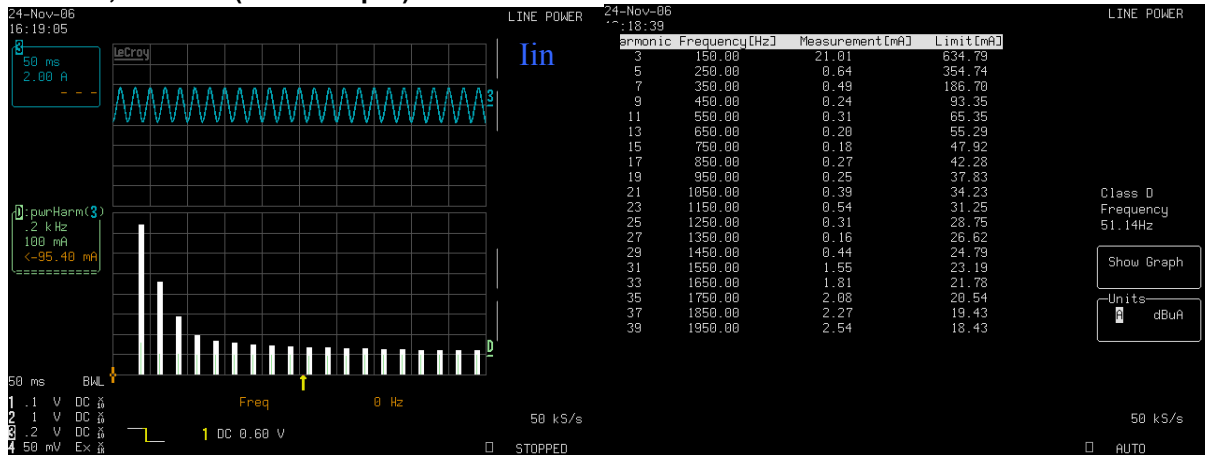
85VAC, full load (300W output)



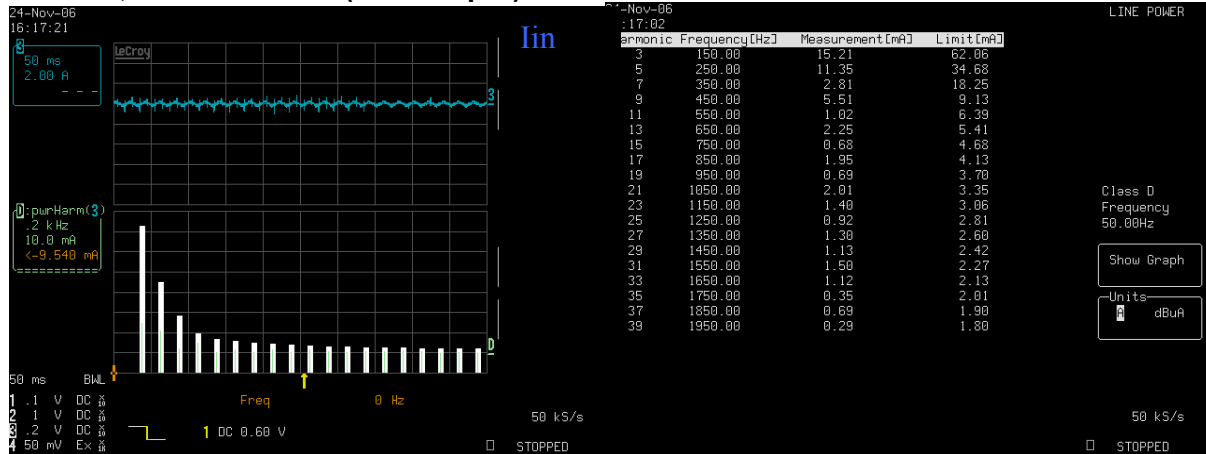
85VAC, 9% of full load (28W output)



265VAC, full load (300W output)

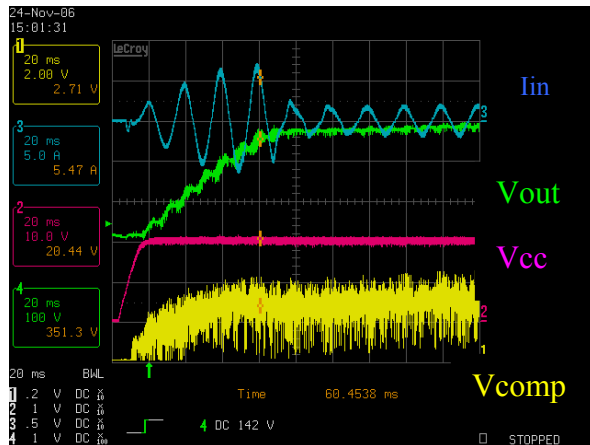


265VAC, 9% of full load (28W output)



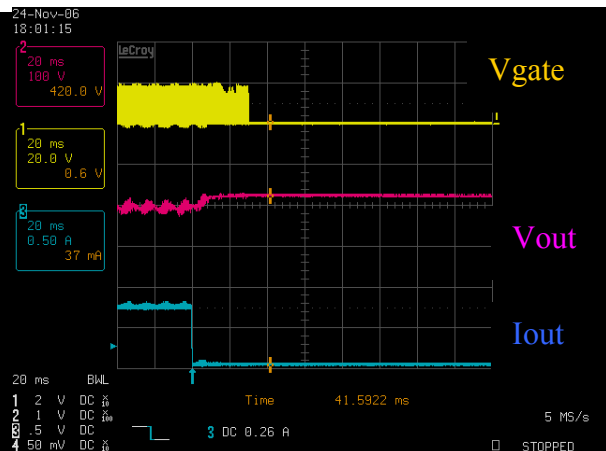
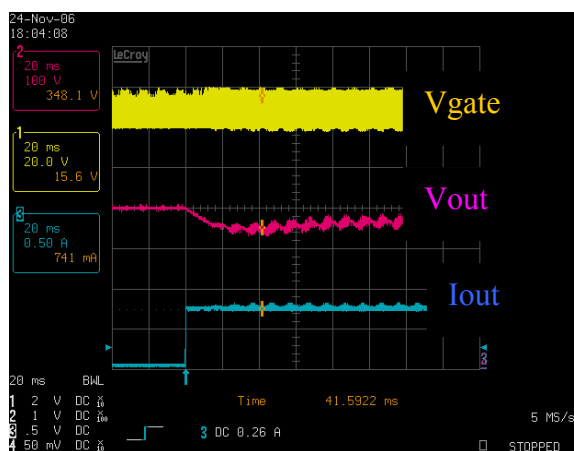
11.3 Waveforms (soft start, load jump, open loop)

Soft start, test at 85VAC, Iout=0.2A

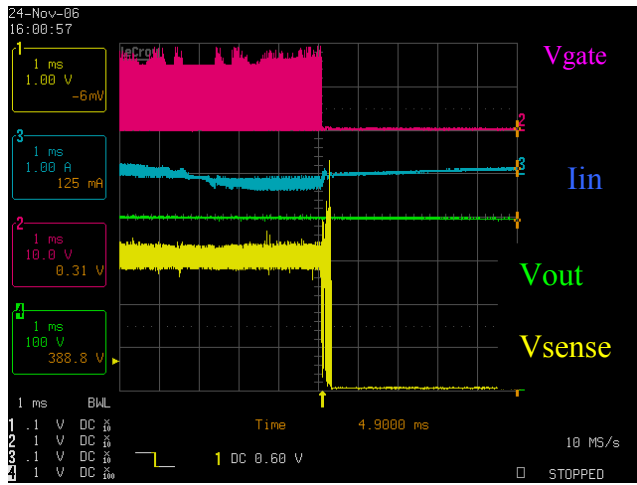


Load jump test at 85VAC, Iout from 0A to 0.75A

Load jump test at 85VAC, Iout from 0.75A to 0A



Open loop test at 265VAC, Iout=0.1A



12 References: