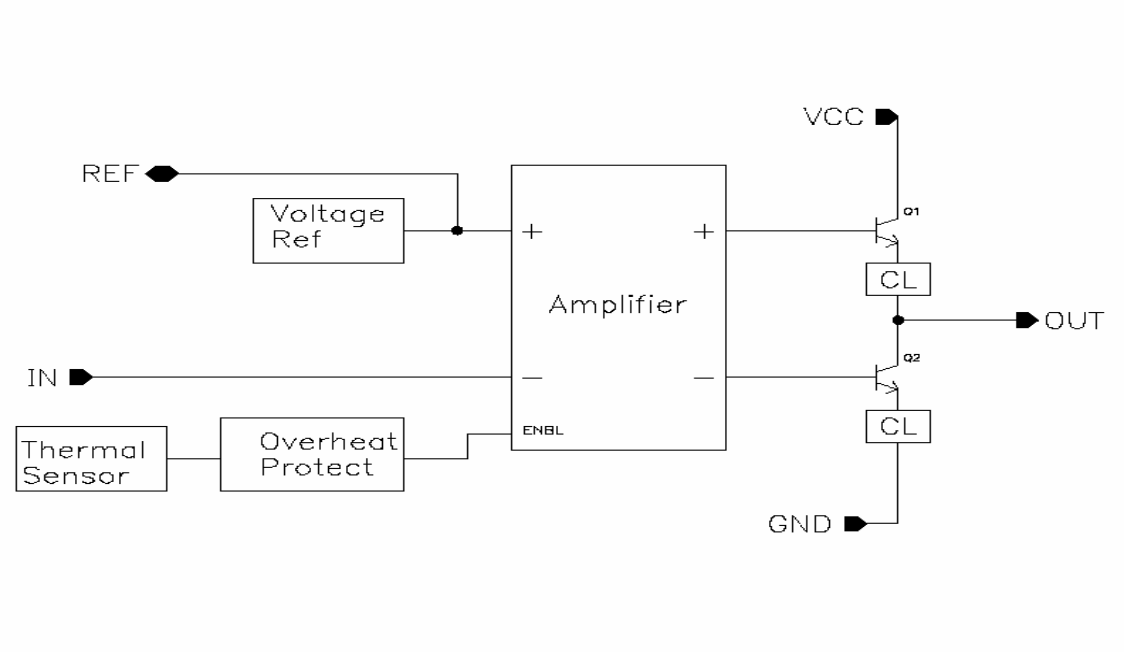
Features

- Provide active common mode current cancellation
- Operating bandwidth covers most of the international conducted EMI limits
- Single supply voltage easily obtained from generic auxiliary supply
- High output driving capability
- Low power consumption meets no load standby requirements
- Simple configurations for isolated switching power supplies
- Reduces input EMI filters in switching power supplies and effectively increase power density
- Cancellation operation is independent of power converter power level
- Available in 8-pin SOIC.

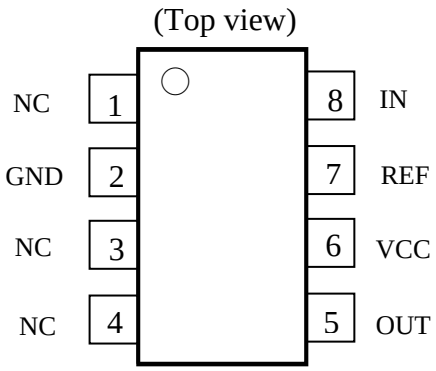
Description

This active EMI cancellation IC provides an effective solution to common mode EMI problems. It can be easily understood as a Y-cap booster circuit that provides very low impedance path to bypass noise current without violating leakage current specifications. Different circuit configurations suggested here effectively bypass noise current between any two nodes in a circuit within the conducted EMI spectrum. Effectively this IC produces a cancellation signal to reduce common mode current. As it deals with low power noise current only its application is not limited by converter power level. Built-in protection circuits allow operation against hi-pot test and high voltage application. It is intended to reduce conventional passive filter requirement which introduce considerable losses and size to switching power converters. Significant reduction in size, cost and loss of EMI components makes the applications more compact and highly efficient to meet nowadays tight requirements.

Block Diagram



Pin descriptions



Pin 2 GND :

This pin is the supply reference for the noise cancellation IC. It is also the first node of the two nodes that active bypass wants to be applied.

Pin 5 OUT :

Connect this pin to the second node that active bypass applies. It is connected to an external safety capacitor which provides sufficient isolation. Use safety approved capacitor if isolation between this pin and the pin 8 is required.

Pin 6 VCC :

Power supply to the IC. The maximum supply voltage of the low and high voltage version is +15V.

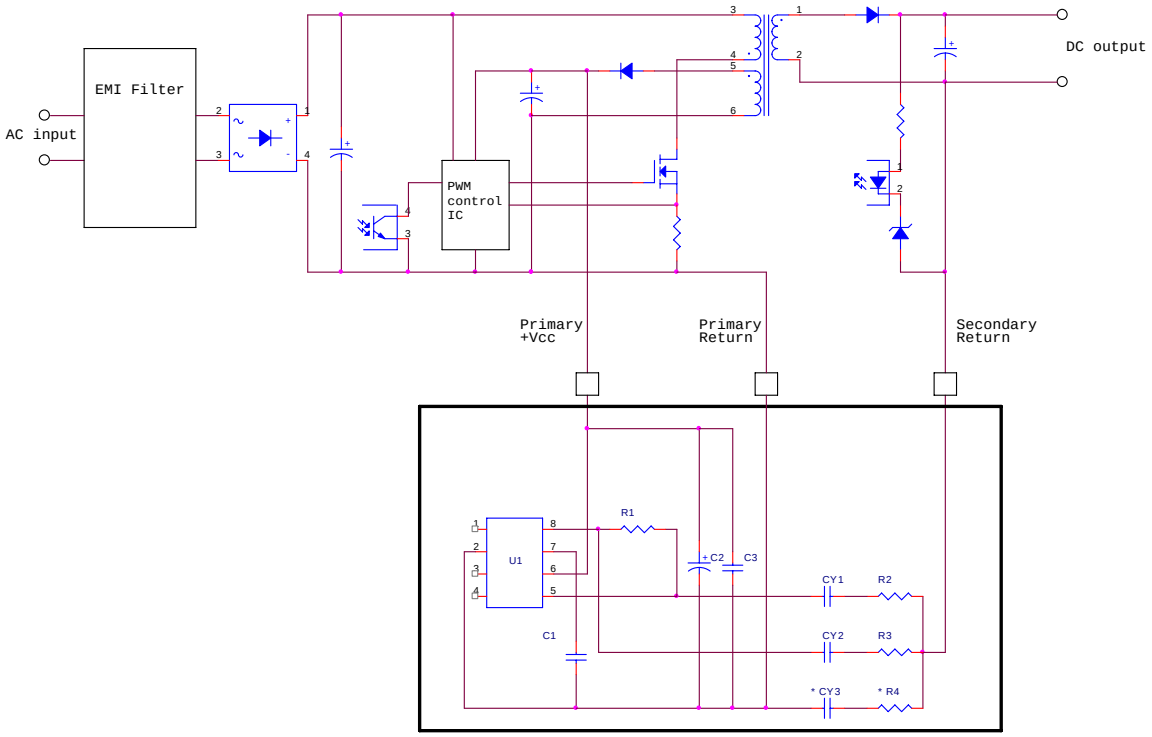
Pin 7 REF :

This pin provides the internal bias voltage to IC. Internal reference sets the bias level to ensure maximum noise cancellation dynamic range. This bias point may be connected to an external capacitor for optimum operation.

Pin 8 IN :

This pin receives the noise signal and compares it with pin5. The second note can be maintained at the same potential (AC only) as the first node connected to pin 5 through this feedback control. Also use safety approved capacitor if isolation between this pin and the pin 5 is required.

Typical Application



◆ Patent Pending

C1	50V 100nF ceramic capacitor
C3	50V 100nF ceramic capacitor
CY1	1nF Y1 safety capacitor
CY2	220pF Y1 safety capacitor
CY3*	470pF Y1 safety capacitor (optional)
R1	470K resistor
R2	2R2 resistor
R3	10R resistor
R4*	2R2 resistor (optional)
U1	EMI cancellation IC

Example 1

Example 1 shows a practical application. Noise current generated by the switching circuits in the primary side flows to the secondary parts including the load through the inter-winding capacitance of the isolation transformer T1. Common noise current will then flow back to the primary noise source in terms of common mode current through the parasitic impedance between the secondary parts and the ground. Conventional design use a Y-capacitor (C_{Y3}) and common mode filters at the input in order to bypass and block the common mode noise. As the maximum capacitance of C_{Y3} is limited by the leakage current standards, it cannot

effectively bypass the noise current back to the noise source and hence a large common mode filter is usually required at the input to block the common mode current. The EMI cancellation circuit in this example provides much lower impedance between the primary and the secondary side to bypass the noise current that a Y-cap can do without exceeding the leakage current specifications.

The supply voltage of the noise cancellation circuit is obtained from the primary PWM controller supply. The capacitor $C_1$and C_3 is a bypassing capacitor for the supply voltage and the internal bias voltage and their values should be at lease 100nF to provide low impedance at high frequency. As isolation is required in example 1, C_{Y1} and C_{Y2} should be safety approved Y-capacitors (Y1 in this case). The capacitor C_{Y3} now is for very high frequency bypass only. It can be very small or even be removed, depending on the real situation.

EMI cancellation circuit design steps (Example 1 application):

1. **Determine the required supply voltage for the EMI cancellation IC**

   First check applicability of this IC to a particular power converter. Disconnect the EMI cancellation circuit components. Starting from the lowest value, choose C_{Y3} from the range of 220pF to a value without breaking the leakage current specifications. Operate the converter at different input and output conditions and check the peak to peak noise voltage across C_{Y3}. This noise voltage is caused by the noise current flowing between the primary and secondary side through the inter-winding capacitance of T1B. The peak to peak noise voltage increases with the winding capacitance of T_{1B} and decreases with the increase of C_{Y3}. The supply voltage to the EMI cancellation IC must be at least equal to the peak to peak noise voltage. So designers can select their desirable supply by varying the value of C_{Y3}.

2. **Determine the value of C_{Y1}**

   Use the value of C_{Y3} obtained in Step 1 for $\boldsymbol{C_{Y1}}$. Now, you can remove C_{Y3}. Note that the higher the value of C_{Y1}, the lower the supply voltage *Vcc* can be used.

3. **Determine the value of C_{Y2}**

   The EMI cancellation circuit in example 1 provides low impedance between primary and secondary circuit.

   The actual low impedance Z_v provided by the EMI cancellation circuit depends on $\boldsymbol{C_{Y1}}$, $\boldsymbol{C_{Y2}}$, the concerned noise frequency f_n and an external resistor R1. It can be approximately calculated by the following equations.

$$|Zv| = \frac{1}{6 f_n C_{Y1}(6 f_n C_{Y2} R_3)} \qquad for\ f_n < 1MHz \qquad Eqn(1)$$

$$|Zv| = \frac{1}{6 f_n C_{Y1} \cdot \left| \frac{1}{\frac{10^4 + i \cdot f_n}{10^8} - \frac{1}{i \cdot 6 f_n R_3 C_{Y2}}} \right|} \qquad for\ f_n > 1MHz \qquad Eqn(2)$$

From *Eqn(1)* show that the impedance Z_v can be viewed as a large capacitance = $\boldsymbol{C_{Y1}}$ times a amplification factor $6f_nC_{Y2}R_1$*(boosting factor)*. To avoid the Y-cap boosting effect that affects the leakage current test concerned frequency range (usually 50 – 800Hz), C_{Y2} should be chosen such that the boosting factor is less than one at this range but high enough in the conducted EMI frequency range. A suggested range of C_{Y2} is from 50pF to 220pF.

For C_{Y2} = 220pF, C_{Y1} = 1nF, the boosting factor is less than 1 at 800Hz and will increase to ~93 (an effective Y-cap of 93nF) at 150KHz.

After the three design steps described above, an oscilloscope can be used to check the noise voltage across the primary and the secondary side to see whether the cancellation circuit functions normally. The noise level between the primary and the secondary circuit (the two nodes which C_{Y3} is connected as shown in the circuit of Example 1) should be much lower than simply using a Y-capacitor. A typical measured noise voltage waveforms before and after using the cancellation circuit are shown in figure 1A and 1B respectively.

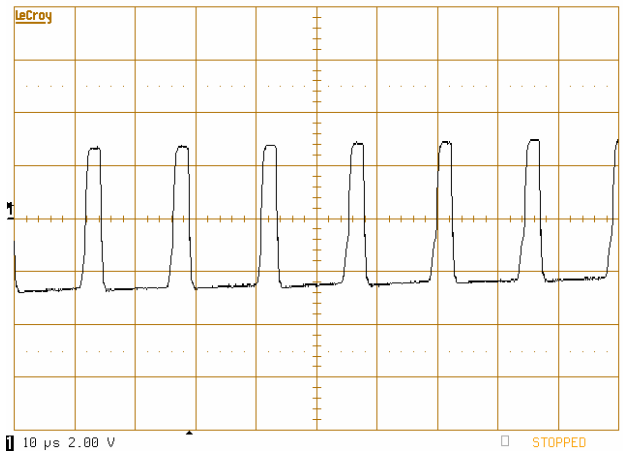


Figure 1A: C_{Y3} = 1nF

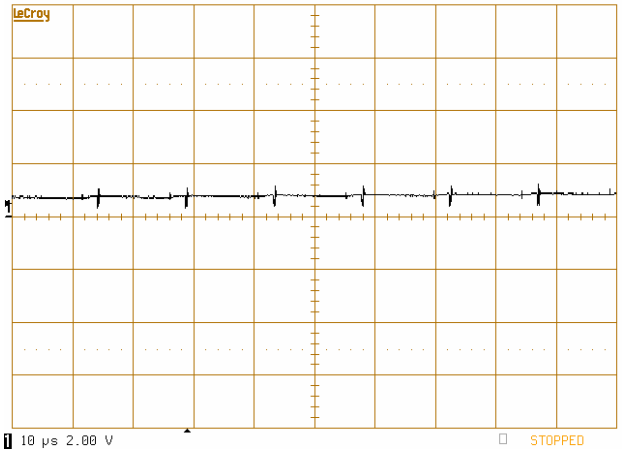


Figure 1B: C_{Y3} replaced by cancellation IC

4. Determine the value of C_{Y3}

The remaining step is to see whether C_{Y3} is required for very high frequency filter (usually in the radiated EMI range above 30MHz) in the real application.

Similar to example 1, an output common mode filter can be added to limit the slew rate of the noise current flowing in to the EMI cancellation circuit and make the cancellation operation more effective.

EMI cancellation application example 2

This application example applies the EMI cancellation IC to a switching converter system with safety ground connection to the output load. Figure 2 shows the cancellation circuit installed between primary return and safety ground. It should be noted that when the cancellation circuit is connected to safety ground, it may interact with the input EMI filter and cause stability problem. In addition to the design steps described in example 1, the following procedures and actions are required to determine the values of R1 and R5 in order to guarantee stable and effective EMI cancellation.

Stability check

Conduct the design steps 1-3 described in example 1. Check the waveform across primary return and the safety ground by an oscilloscope.

Case I:

Ignore the high frequency noise like voltage spike, if the observed noise voltage level is much lower than the result from design step 1, keep the value of *R1* and remove *R5*.

Case II:

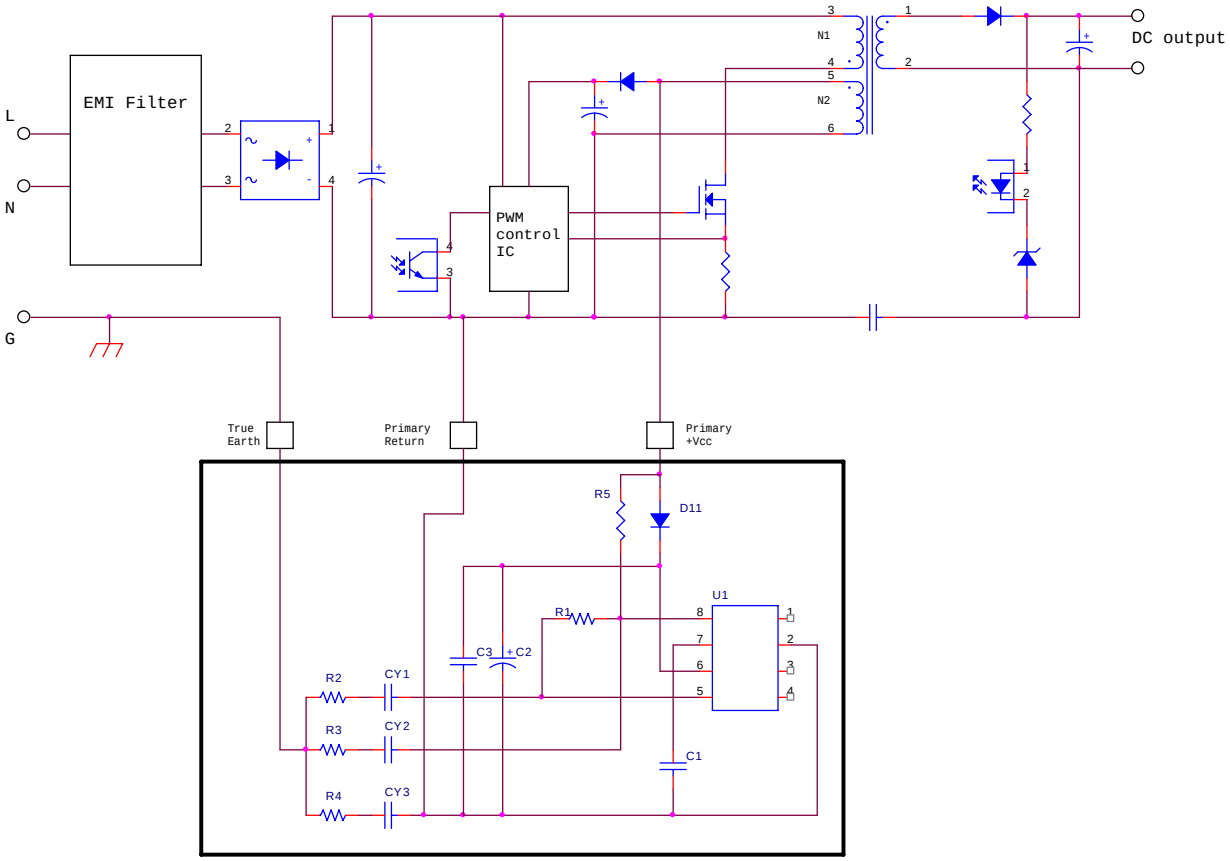
Ignore the high frequency noise like voltage spike, if noise voltage level is high (usually worst than the results obtained in design step 1) and the noise frequency is different from switching frequency, it means the cancellation circuit is unstable and interacting with the input EMI filter.

Reduce *R1* until only the switching frequency noise is observed.

Set R5 by the following equation, where *N1* and *N2* are the no. of turns of the main and the auxiliary windings as shown in the schematic.

$$R5 = \frac{N2}{N1} \cdot \frac{R1}{R5} \cdot CY3 \cdot 10^{10}$$

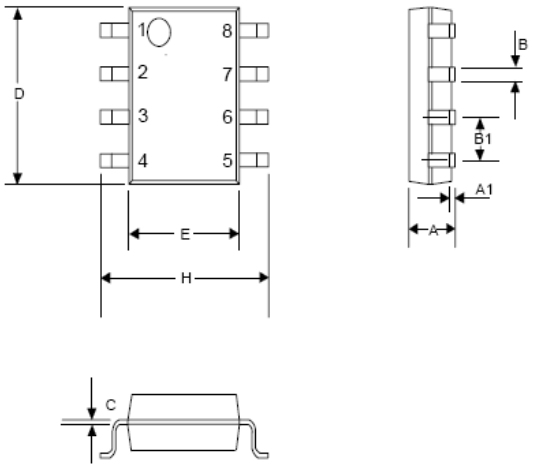
Based on the calculated *R5*, adjust its value around until the observed noise voltage is minimum.



C1	50V 100nF ceramic capacitor
C3	50V 100nF ceramic capacitor
CY1	1nF Y2 safety capacitor
CY2	220pF Y2 safety capacitor
CY3*	470pF Y2 safety capacitor (optional)
R1	Default value = 470K (Trim for stability)
R2	2R2 resistor
R3	10R resistor
R4*	2R2 resistor (optional)
R5	Trim for effective noise cancellation
U1	EMI cancellation IC

Figure 2 (Application example 2)

Outline Drawing SOP-8



DIMENSIONS				
DIM^N	INCHES		MM	
	MIN	MAX	MIN	MAX
A	0.0578	0.0681	1.47	1.73
A1	0.0040	0.0087	0.10	0.22
B	0.0138	0.0197	0.35	0.50
B1	0.050 BSC		1.27 BSC	
C	0.0071	0.0098	0.18	0.25
D	0.1897	0.1940	4.82	4.93
H	0.2299	0.2417	5.84	6.14
E	0.1500	0.1559	3.81	3.96