

## Wide Input 3A Step Down Converter

### FEATURES

- 3A Output Current
- Up to 95% Efficiency
- 4.5V to 30V Input Range
- 6 $\mu$ A Shutdown Supply Current
- 400kHz Switching Frequency
- Adjustable Output Voltage
- Cycle-by-Cycle Current Limit Protection
- Thermal Shutdown Protection
- Internal Soft Start Function
- Frequency Fold Back at Short Circuit
- Stability with Wide Range of Capacitors, Including Low ESR Ceramic Capacitors
- SOP-8/EP (Exposed Pad) Package

### GENERAL DESCRIPTION

The ACT4070 is a current-mode step-down DC/DC converter that generates up to 3A output current at 400kHz switching frequency. The device utilizes Active-Semi's proprietary ISOBCD30 process for operation with input voltage up to 30V.

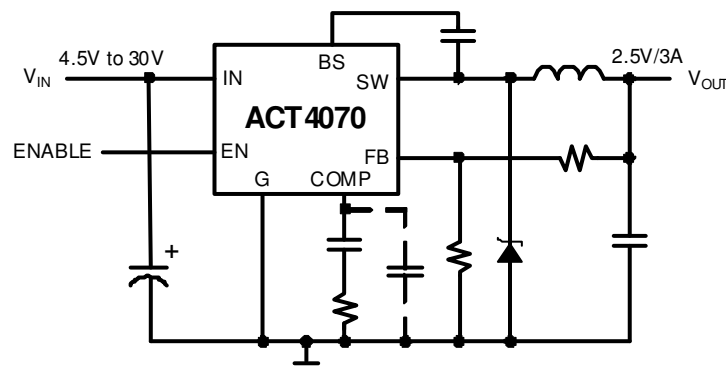
Consuming only 6 $\mu$ A in shutdown mode, the ACT4070 is highly efficient with peak efficiency at 95% when in operation. Protection features include cycle-by-cycle current limit, thermal shutdown, and frequency fold back at short circuit. The device also includes an internal soft start function to prevent overshoot.

The ACT4070 is available in SOP-8/EP exposed pad package and requires very few external devices for operation.

### APPLICATIONS

- TFT LCD Monitors or Televisions and HDTV
- Portable DVD Players
- Car-Powered or Battery-Powered Equipment
- Set-Top Boxes
- Telecom Power Supplies
- DSL and Cable Modems and Routers

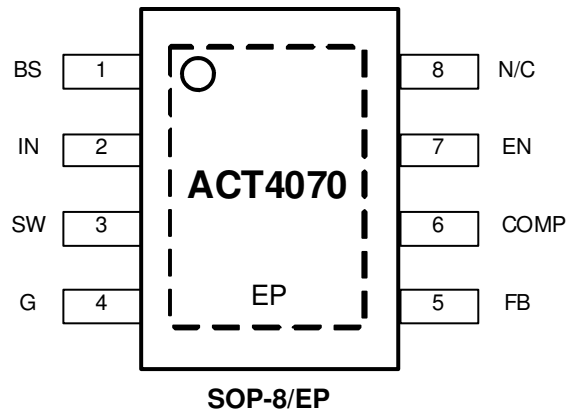
### TYPICAL APPLICATION CIRCUIT



## ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PINS	PACKING
ACT4070YH	-40°C to 85°C	SOP-8/EP	8	TUBE
ACT4070YH-T	-40°C to 85°C	SOP-8/EP	8	TAPE & REEL

## PIN CONFIGURATION



## PIN DESCRIPTION

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	BS	Bootstrap. This pin acts as the positive rail for the high-side switch's gate driver. Connect a 10nF between this pin and SW.
2	IN	Input Supply. Bypass this pin to G with a low ESR capacitor. See <i>Input Capacitor</i> in <i>Application Information</i> section.
3	SW	Switch Output. Connect this pin to the switching end of the inductor.
4	G	Ground.
5	FB	Feedback Input. The voltage at this pin is regulated to 1.222V. Connect to the resistor divider between output and ground to set output voltage.
6	COMP	Compensation Pin. See <i>Compensation Technique</i> in <i>Application Information</i> section.
7	EN	Enable Input. When higher than 1.3V, this pin turns the IC on. When lower than 0.7V, this pin turns the IC off. Output voltage is discharged when the IC is off. This pin has a small internal pull up current to a high level voltage when pin is not connected.
8	N/C	Not Connected.
EP	EP	Exposed Pad shown as dashed box. The exposed thermal pad should be connected to board ground plane and pin 4. The ground plane should include a large exposed copper pad under the package for thermal dissipation (see package outline). The leads and exposed pad should be flush with the board, without offset from the board surface.

## ABSOLUTE MAXIMUM RATINGS<sup>Ⓞ</sup>

PARAMETER	VALUE	UNIT
IN to G	-0.3 to +34	V
EN to G	-0.3 to $V_{IN} + 0.3$	V
SW to G	-1 to $V_{IN} + 1$	V
BS to SW	-0.3 to +8	V
FB, COMP to G	-0.3 to 6	V
Continuous SW Current	Internally limited	A
Junction to Ambient Thermal Resistance ( $\theta_{JA}$ )	46	°C/W
Maximum Power Dissipation	1.8	W
Operating Junction Temperature	-40 to 150	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

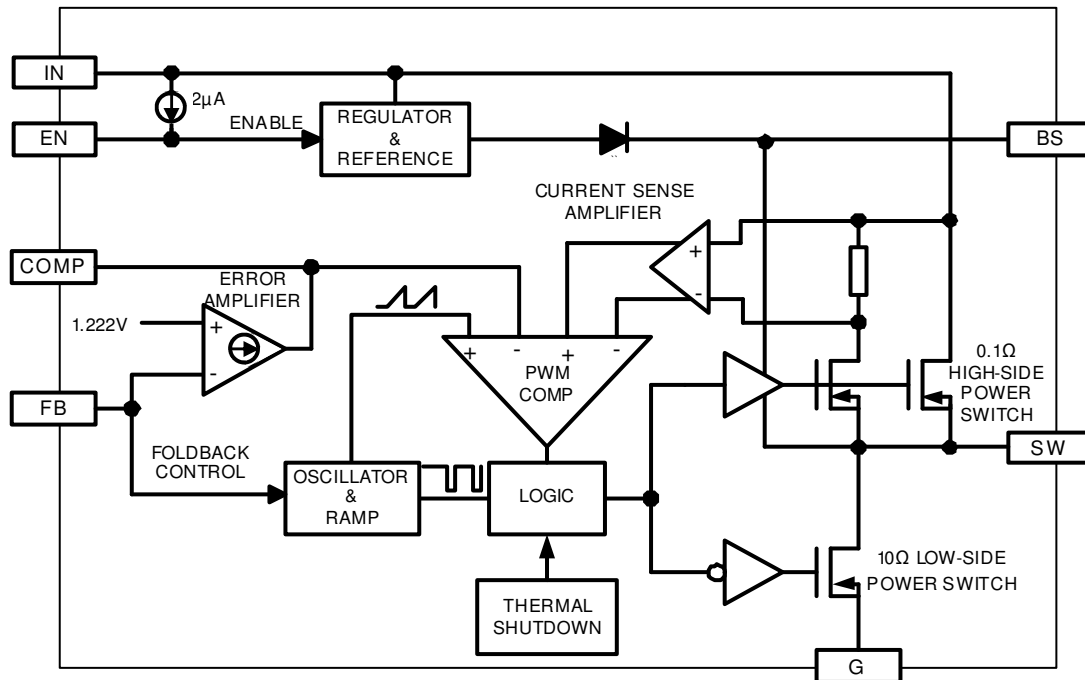
Ⓞ: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

( $V_{IN} = 12V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	$V_{IN}$	$V_{OUT} = 2.5V$ , $I_{LOAD} = 0A$ to $3A$	4.5		30	V
Feedback Voltage	$V_{FB}$		1.198	1.222	1.246	V
High-Side Switch On Resistance	$R_{ONH}$			100		m $\Omega$
Low-Side Switch On Resistance	$R_{ONL}$			10		$\Omega$
SW Leakage		$V_{EN} = 0$ , $V_{IN} = 12V$ , $V_{SW} = 0V$		0	10	$\mu A$
Current Limit	$I_{LIM}$		3.5	5		A
COMP to Current Limit Transconductance	$G_{COMP}$	$\Delta I_{LOAD} / \Delta I_{COMP}$		3		A/V
Error Amplifier Transconductance	$G_{EA}$	$\Delta I_{COMP} = \pm 10\mu A$		550		$\mu A/V$
Error Amplifier DC Gain	$A_{VEA}$			4000		V/V
Switching Frequency	$f_{SW}$		340	400	460	kHz
Short Circuit Switching Frequency		$V_{FB} = 0V$		40		kHz
Maximum Duty Cycle	$D_{MAX}$	$V_{FB} = 1.1V$ , PWM mode		90		%
Minimum Duty Cycle		$V_{FB} = 1.4V$ , PFM mode		0		%
Enable Threshold Voltage		Hysteresis = 0.1V	0.7	1	1.3	V
Enable Pull Up Current		Pin pulled up to $V_{IN}$ when left unconnected		2		$\mu A$
Supply Current in Shutdown		$V_{EN} = 0$		6	20	$\mu A$
IC Supply Current in Operation		$V_{EN} = 3V$ , not switching		0.85	2	mA
Thermal Shutdown Temperature		Hysteresis = 10°C		160		°C

## FUNCTIONAL BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

As seen in the *Functional Block Diagram*, the ACT4070 is a current mode pulse width modulation (PWM) converter. The converter operates as follows:

A switching cycle starts when the rising edge of the Oscillator clock output causes the High-Side Power Switch to turn on and the Low-Side Power Switch to turn off. With the SW side of the inductor now connected to IN, the inductor current ramps up to store energy in its magnetic field. The inductor current level is measured by the Current Sense Amplifier and added to the Oscillator ramp signal. If the resulting summation is higher than the COMP voltage, the output of the PWM Comparator goes high. When this happens or when Oscillator clock output goes low, the High-Side Power Switch turns off and the Low-Side Power Switch turns on. At this point, the SW side of the inductor swings to a diode voltage below ground, causing the inductor current to decrease and magnetic energy to be transferred to output. This state continues until the cycle starts again.

The High-Side Power Switch is driven by logic using BS bootstrap pin as the positive rail. This pin is charged to  $V_{SW} + 6V$  when the Low-Side Power Switch turns on.

The COMP voltage is the integration of the error between FB input and the internal 1.222V reference. If FB is lower than the reference voltage, COMP tends to go higher to increase current to the output. Current limit happens when COMP reaches its maximum clamp value of 2.65V.

The Oscillator normally switches at 400kHz. However, if FB voltage is less than 0.7V, then the switching frequency decreases until it reaches a typical value of 40kHz at  $V_{FB} = 0V$ .

### Shutdown Control

The ACT4070 has an enable input EN for turning the IC on or off. When EN is less than 0.7V, the IC is in 6µA low current shutdown mode and output is discharged through the Low-Side Power Switch. When EN is higher than 1.3V, the IC is in normal operation mode. EN is internally pulled up with a 2µA current source and can be left unconnected for always-on operation.

### Thermal Shutdown

The ACT4070 automatically turns off when its junction temperature exceeds 160°C and then restarts once the temperature falls to 150°C.

## APPLICATIONS INFORMATION

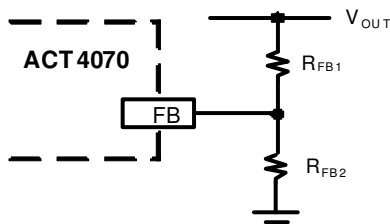
### Output Voltage Setting

Figure 1 shows the connections for setting the output voltage. Select the proper ratio of the two feedback resistors  $R_{FB1}$  and  $R_{FB2}$  based on the output voltage. Typically, use  $R_{FB2} \approx 10k\Omega$  and determine  $R_{FB1}$  from the output voltage:

$$R_{FB1} = R_{FB2} \left( \frac{V_{OUT}}{1.222V} - 1 \right) \quad (1)$$

Figure 1:

#### Output Voltage Setting



### Inductor Selection

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value: higher inductance reduces the peak-to-peak ripple current. The trade off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value  $L$  based on ripple current requirement:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} f_{SW} I_{OUTMAX} K_{RIPPLE}} \quad (2)$$

where  $V_{IN}$  is the input voltage,  $V_{OUT}$  is the output voltage,  $f_{SW}$  is the switching frequency,  $I_{OUTMAX}$  is the maximum output current, and  $K_{RIPPLE}$  is the ripple factor. Typically, choose  $K_{RIPPLE}$  = between 20% and 30% to correspond to the peak-to-peak ripple current being a percentage of the maximum output current.

With this inductor value (Table 1), the peak inductor current is  $I_{OUT} (1 + K_{RIPPLE} / 2)$ . Make sure that this peak inductor current is less than the 5A current limit. Finally, select the inductor core size so that it does not saturate at 5A.

Table 1:

#### Typical Inductor Values

$V_{OUT}$	1.5V	1.8V	2.5V	3.3V	5V
L	6.8 $\mu$ H	6.8 $\mu$ H	6.8 $\mu$ H	8.5 $\mu$ H	15 $\mu$ H

### Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.

The input capacitance needs to be higher than 10 $\mu$ F. The best choice is the ceramic type; however, low ESR tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. The input capacitor should be placed close to the IN and G pins of the IC, with shortest traces possible. In the case of tantalum or electrolytic types, they can be further away if a small parallel 0.1 $\mu$ F ceramic capacitor is placed right next to the IC.

### Output Capacitor

The output capacitor also needs to have low ESR to keep low output voltage ripple. The output ripple voltage is:

$$V_{RIPPLE} = I_{OUTMAX} K_{RIPPLE} R_{RIPPLE} + \frac{V_{IN}}{28 \cdot f_{SW}^2 LC_{OUT}} \quad (3)$$

where  $I_{OUTMAX}$  is the maximum output current,  $K_{RIPPLE}$  is the ripple factor,  $R_{ESR}$  is the ESR resistance of the output capacitor,  $f_{SW}$  is the switching frequency,  $L$  is the inductor value,  $C_{OUT}$  is the output capacitance. In the case of ceramic output capacitors,  $R_{ESR}$  is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic type. In the case of tantalum or electrolytic type, the ripple is dominated by  $R_{ESR}$  multiplied by the ripple current. In that case, the output capacitor is chosen to have sufficiently low ESR.

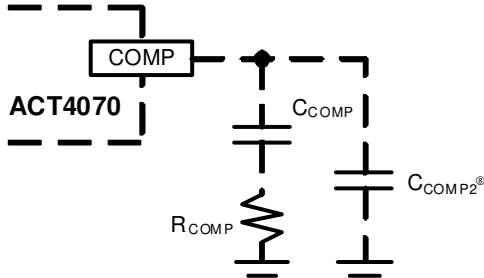
For ceramic output type, typically choose a capacitance of about 22 $\mu$ F. For tantalum or electrolytic type, choose a capacitor with less than 50m $\Omega$  ESR.

### Rectifier Diode

Use a Schottky diode as the rectifier to conduct current when the High-Side Power Switch is off. The Schottky diode must have current rating higher than the maximum output current and the reverse voltage rating higher than the maximum input voltage.

## Stability compensation

**Figure 2:**  
**Stability Compensation**



①: C<sub>COMP2</sub> is needed only for high ESR output capacitor

The feedback system of the IC is stabilized by the components at COMP pin, as shown in Figure 2. The DC loop gain of the system is determined by the following equation:

$$A_{VDC} = \frac{1.222V}{I_{OUT}} A_{VEA} G_{COMP} \quad (4)$$

The dominant pole P1 is due to C<sub>COMP</sub>:

$$f_{P1} = \frac{G_{EA}}{2\pi A_{VEA} C_{COMP}} \quad (5)$$

The second pole P2 is the output pole:

$$f_{P2} = \frac{I_{OUT}}{2\pi V_{OUT} C_{OUT}} \quad (6)$$

The first zero Z1 is due to R<sub>COMP</sub> and C<sub>COMP</sub>:

$$f_{Z1} = \frac{1}{2\pi R_{COMP} C_{COMP}} \quad (7)$$

And finally, the third pole is due to R<sub>COMP</sub> and C<sub>COMP2</sub> (if C<sub>COMP2</sub> is used):

$$f_{P3} = \frac{1}{2\pi R_{COMP} C_{COMP2}} \quad (8)$$

Follow the following steps to compensate the IC:

**STEP 1.** Set the cross over frequency at 1/10 of the switching frequency via R<sub>COMP</sub>:

$$R_{COMP} = \frac{2\pi V_{OUT} C_{OUT} f_{SW}}{10 G_{EA} G_{COMP} 1.222V} = 1.25 \times 10^8 V_{OUT} C_{OUT} \quad (\Omega) \quad (9)$$

but limit R<sub>COMP</sub> to 15kΩ maximum.

**STEP 2.** Set the zero f<sub>Z1</sub> at 1/4 of the cross over frequency. If R<sub>COMP</sub> is less than 15kΩ, the equation for C<sub>COMP</sub> is:

$$C_{COMP} = \frac{1.6 \times 10^{-5}}{R_{COMP}} \quad (F) \quad (10)$$

If R<sub>COMP</sub> is limited to 15kΩ, then the actual cross over frequency is 4.8/(V<sub>OUT</sub>C<sub>OUT</sub>). Therefore:

$$C_{COMP} = 8.8 \times 10^{-6} V_{OUT} C_{OUT} \quad (F) \quad (11)$$

**STEP 3.** If the output capacitor's ESR is high enough to cause a zero at lower than 4 times the cross over frequency, an additional compensation capacitor C<sub>COMP2</sub> is required. The condition for using C<sub>COMP2</sub> is:

$$R_{ESROUT} \geq \text{Min} \left( \frac{1.1 \times 10^{-6}}{C_{OUT}}, 0.012 V_{OUT} \right) \quad (\Omega) \quad (12)$$

And the proper value for C<sub>COMP2</sub> is:

$$C_{COMP2} = \frac{C_{OUT} R_{ESROUT}}{R_{COMP}} \quad (13)$$

Though C<sub>COMP2</sub> is unnecessary when the output capacitor has sufficiently low ESR, a small value C<sub>COMP2</sub> such as 220pF may improve stability against PCB layout parasitic effects.

Table 2 shows some calculated results based on the compensation method above.

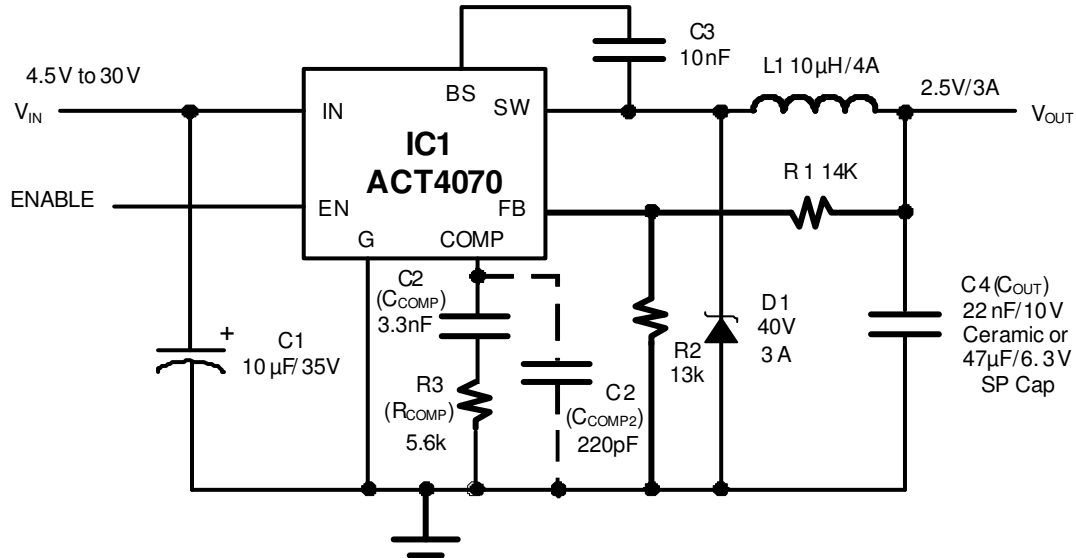
**Table 2:**  
**Typical Compensation for Different Output Voltages and Output Capacitors**

V <sub>OUT</sub>	C <sub>OUT</sub>	R <sub>COMP</sub>	C <sub>COMP</sub>	C <sub>COMP2</sub> ①
1.8V	22μF Ceramic	4kΩ	3.3nF	220pF
2.5V	22μF Ceramic	5.6kΩ	3.3nF	220pF
5V	22μF Ceramic	12kΩ	1.5nF	220pF
1.8V	100μF SP CAP	15kΩ	1.5nF	220pF
2.5V	100μF SP CAP	15kΩ	2.2nF	220pF
5V	100μF SP CAP	15kΩ	4.7nF	220pF

①: C<sub>COMP2</sub> is needed for board parasitic and high ESR output capacitor.

Figure 3 shows a sample ACT4070 application circuit generating a 2.5V/3A output.

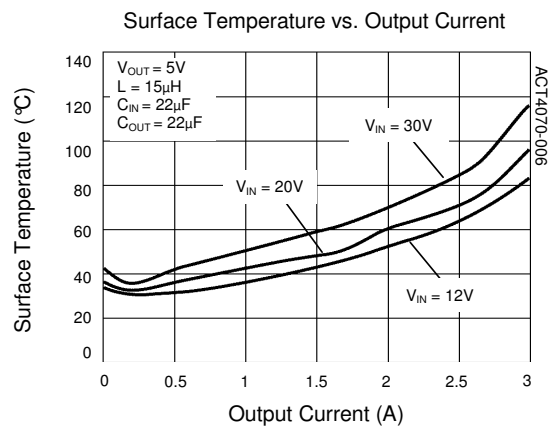
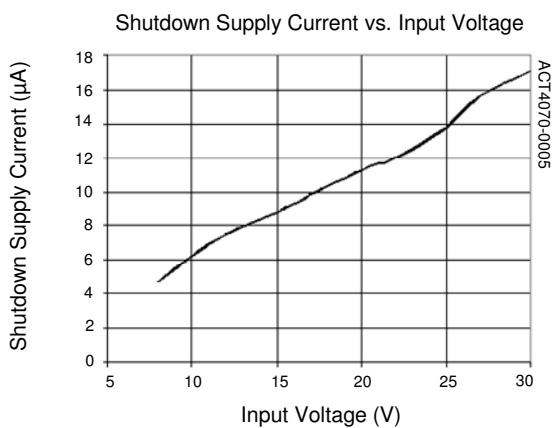
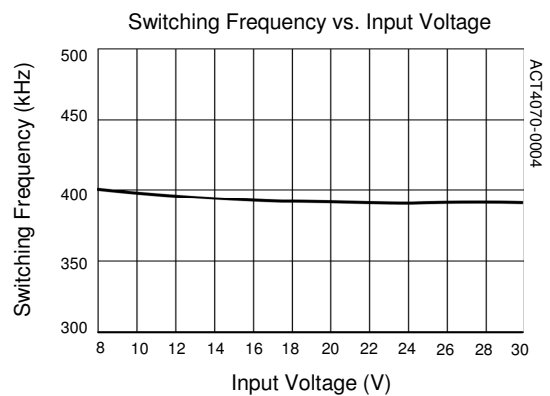
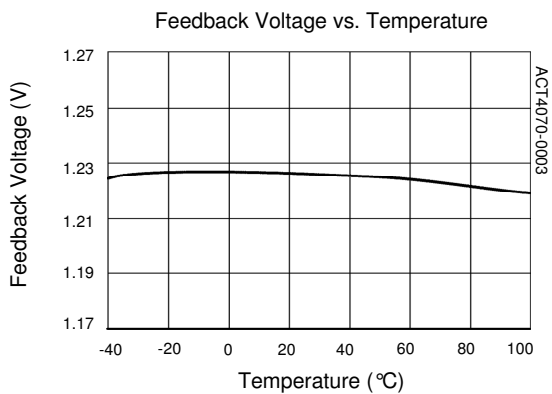
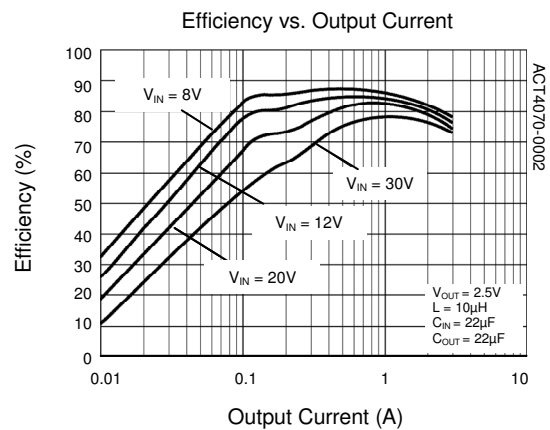
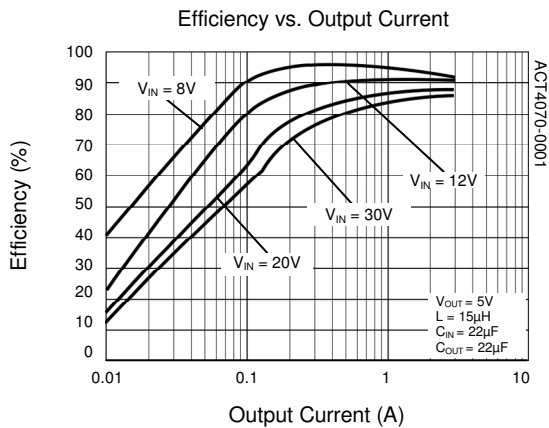
**Figure 3:**  
**ACT4070 2.5V/3A Output Application<sup>Ⓞ</sup>**



Ⓞ: D1 is a 40V, 3A Schottky diode with low forward voltage, an IR 30BQ040 or SK34 equivalent. C4 can be either a ceramic capacitor (Panasonic ECJ-3YB1C226M) or SP-CAP (Specialty Polymer) Aluminum Electrolytic Capacitor such as Panasonic EEFC0J470XR. The SP-Cap is based on aluminum electrolytic capacitor technology, but uses a solid polymer electrolyte and has very stable capacitance characteristics in both operating temperature and frequency compared to ceramic, polymer, and low ESR tantalum capacitors.

## TYPICAL PERFORMANCE CHARACTERISTICS

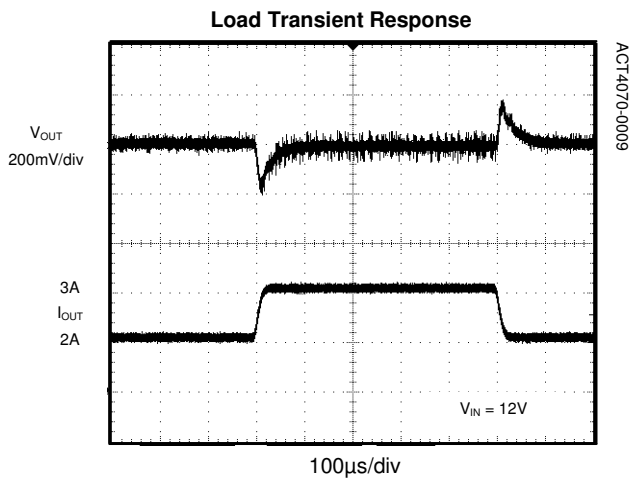
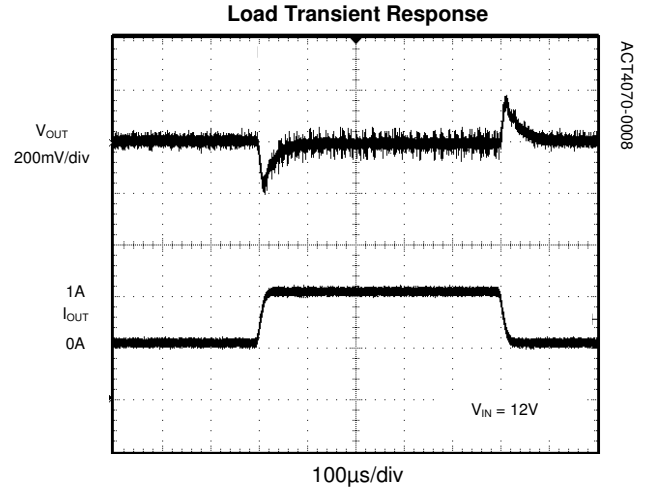
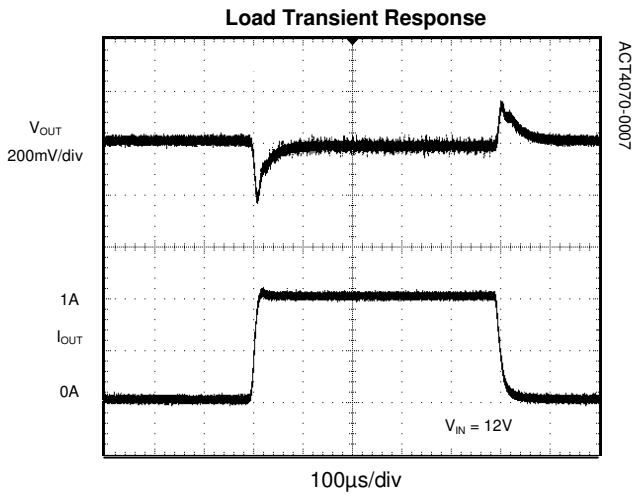
(Circuit of Figure 3, unless otherwise specified.)





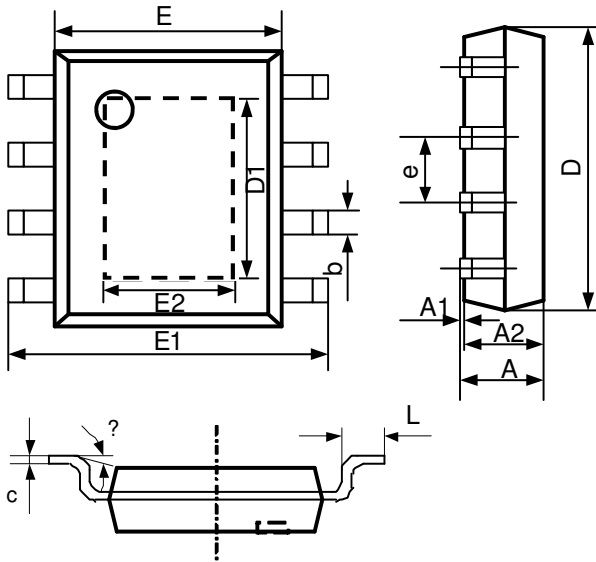
TYPICAL PERFORMANCE CHARACTERISTICS

(Circuit of Figure 3, unless otherwise specified.)



## PACKAGE OUTLINE

### SOP-8/EP PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.150	0.002	0.006
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270 TYP		0.050 TYP	
L	0.400	1.270	0.016	0.050
$\theta$	0°	8°	0°	8°