TEA1761T

GreenChip synchronous rectifier for flyback

Rev. 01 — 31 March 2006 Objective data sheet

1. General description

The TEA1761T is a member of the new generation of Synchronous Rectifier (SR) controller ICs for switched mode power supplies. Its high level of integration allows the design of a cost-effective power supply with a very low number of external components.

The TEA1761T is a controller IC dedicated for synchronous rectification on the secondary side of discontinuous conduction mode and quasi resonant flyback converters. Besides electronics for synchronous rectification, it also has integrated circuitry for output voltage and output current regulation.

The TEA1761T is fabricated in a Silicon On Insulator (SOI) process. This Philips SOI process makes possible a wide range of operation.

2. Features

2.1 Distinctive features

- Combined synchronous rectification and primary feedback control functionality
- Wide supply voltage range (8.5 V to 38 V)
- High level of integration, resulting in a very low external component count
- Wide opto output voltage range (3.5 V to 38 V)
- Accurate internal voltage reference for voltage control (within 1 %)
- High driver output voltage of 10 V to drive all MOSFET brands to the lowest R_{DSon}

2.2 Green features

- Low current consumption
- High system efficiency from no load to full load

2.3 Protection features

- Undervoltage protection
- Internal over-temperature protection

3. Applications

The TEA1761T is intended for adapters. The device can also be used in all other discontinuous conduction mode and quasi resonant flyback systems that demand a highly efficient and cost-effective solution.

PHILIPS

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA1761T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

5. Block diagram

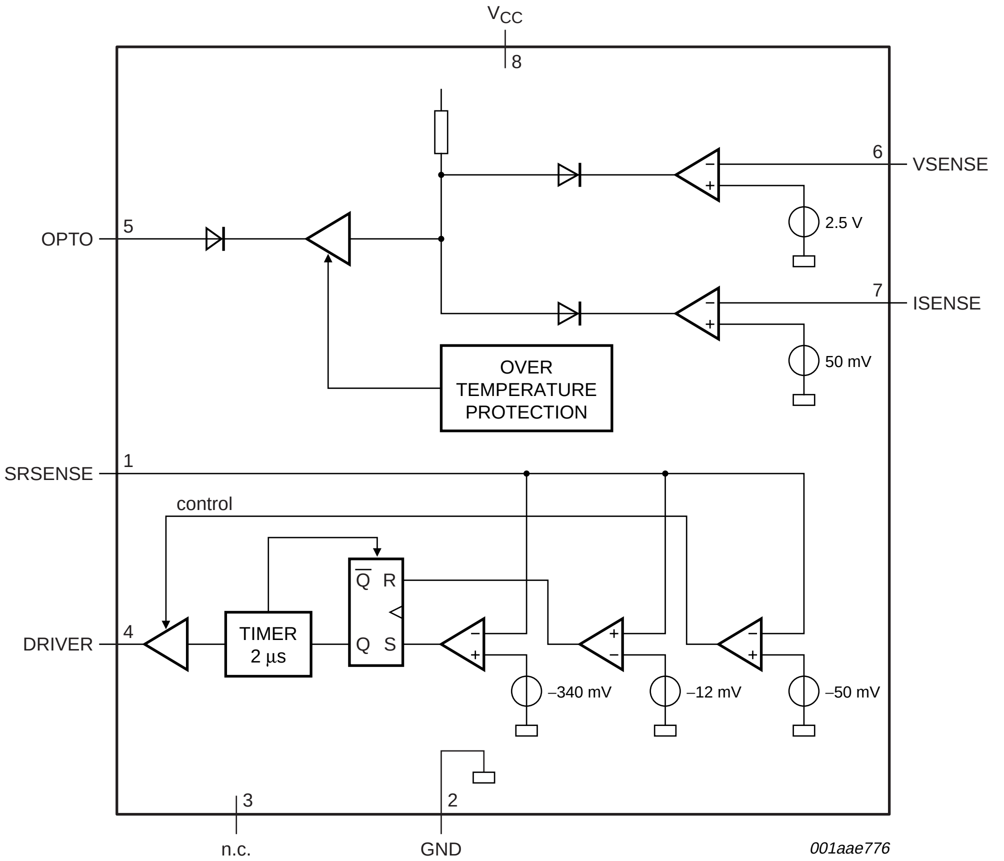


Fig 1. TEA1761T block diagram

6. Pinning information

6.1 Pinning

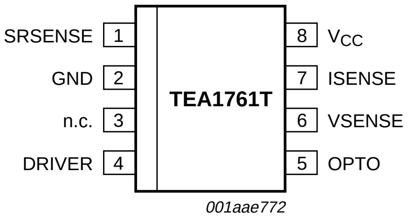


Fig 2. Pin configuration for SOT96-1

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
SRSENSE	1	synchronous timing input
GND	2	ground
n.c.	3	not connected
DRIVER	4	driver output for SR MOSFET
OPTO	5	opto coupler driver output
VSENSE	6	sense input for voltage control
ISENSE	7	sense input for current control
V_{CC}	8	supply voltage

7. Functional description

The TEA1761T is the controller for synchronous rectification to be used in discontinuous conduction mode and quasi resonant flyback converters. Besides controlling the SR MOSFET, the TEA1761T contains the voltage reference and amplifiers to regulate and control the output voltage and current of the power supply.

7.1 Start-up and undervoltage lock out

The IC will activate the synchronous rectifier circuitry and the voltage/current sense circuitry as soon as the voltage on the V_{CC} pin is above 8.6 V (typical). As soon as the voltage drops below 8.1 V (typical), the SR driver output is actively kept low and the opto driver output is disabled.

7.2 Synchronous rectification

After a negative voltage (–340 mV typical) is sensed on the SRSENSE pin, the driver output voltage is made high and the external MOSFET is switched on. As soon as the SRSENSE voltage rises to –50 mV, the driver output voltage is regulated to maintain the –50 mV on the SRSENSE pin. As soon as the SRSENSE voltage is above –12 mV, the driver output is pulled to ground. After switch-on of the SR MOSFET, the input signal on the SRSENSE pin is blanked for 2 µs (typical). This will eliminate false switch-off due to high frequency ringing at the start of the secondary stroke.

Because the driver output voltage is reduced as soon as the voltage on the SRSENSE pin is –50 mV, the external power switch can be switched off fast when the current through the switch reaches zero. With this zero-current switch off, no separate standby mode is needed to maintain high efficiency during no-load operation. The zero current is detected by sensing a –12 mV level on the SRSENSE pin. See Figure 3.

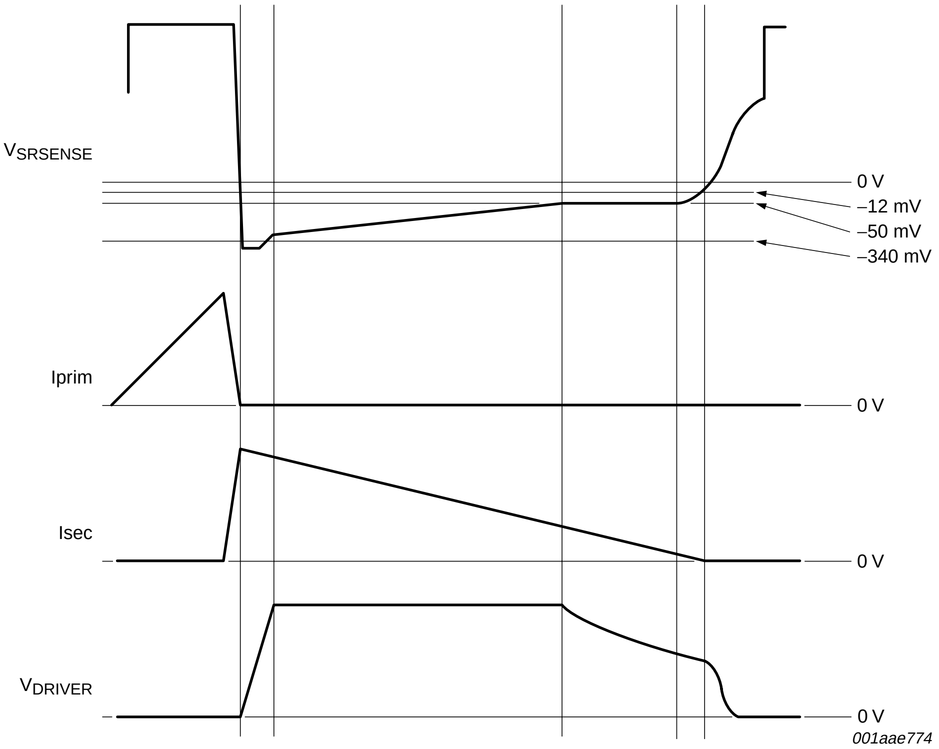


Fig 3. Synchronous rectification signals

If the secondary stroke of the flyback converter is shorter than 2 µs (typical), the driver output is disabled. This will guarantee stable operation for very low duty cycles.

7.3 SMPS output voltage and current regulation

The output voltage of the flyback Switched Mode Power Supply (SMPS) can be controlled by sensing the output voltage via the VSENSE pin. The feedback loop via the primary controller can regulate the output voltage of the switched mode power supply by regulating the voltage on the VSENSE pin to 2.5 V.

Also the output current of the flyback SMPS can be controlled or limited. The voltage on the ISENSE pin is regulated or limited to 50 mV above the voltage on pin GND.

7.4 Opto output

The opto output is intended to drive an opto coupler (see Figure 5). The opto output has an open-drain output configuration. The maximum sink current is internally limited to 5 mA (typical). The output is linearly controlled via the VSENSE and ISENSE input pins. An over-temperature situation will switch the opto output to its maximum sink current.

During start-up ($V_{CC} < V_{startup}$) and undervoltage lock-out the output is disabled.

7.5 Supply management

All (internal) reference voltages are derived from a temperature compensated, on-chip band gap circuit. The reference voltage is trimmed to an accuracy within 1 %.

7.6 Over-Temperature Protection (OTP)

The IC provides an accurate internal over-temperature protection of 150 °C (typical). The IC will maximize the current of pin OPTO as soon as the internal temperature limit is reached. The opto signal can be used on the primary side of the flyback controller to activate the SMPS protection or limit the output power. As soon as the over-temperature condition is solved, normal operation will resume.

7.7 Driver

The driver circuit to the gate of the external power MOSFET has a source capability of typically 300 mA and a sink capability of typically 2.2 A. This permits fast turn-on and turn-off of the power MOSFET for efficient operation. The output voltage of the driver is limited to 10 V (typical). This high output voltage will drive all MOSFET brands to the minimum on-state resistance.

During start-up conditions ($V_{CC} < V_{startup}$) and undervoltage lock-out the driver output voltage is actively pulled low.

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground (pin 2); positive currents flow into the chip. The voltage ratings are valid provided other ratings are not violated; current ratings are valid provided the other ratings are not violated.

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{CC}	supply voltage	continuous	–0.4	+38	V
V_{OPTO}	voltage on pin OPTO	continuous	–0.4	+38	V
$V_{SRSENSE}$	voltage on pin SRSENSE	continuous	-	+120	V
V_{VSENSE}	voltage on pin VSENSE	continuous	–0.4	+5	V
V_{ISENSE}	voltage on pin ISENSE		–0.4	+5	V
Currents					
I_{OPTO}	current on pin OPTO		-	+12	mA
I_{DRIVER}	current on pin DRIVER	duty cycle < 10 %	–0.8	+3	A
$I_{SRSENSE}$	current on pin SRSENSE		–3		mA
General					
P_{tot}	total power dissipation	T_{amb} < 80 °C	-	0.45	W
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–20	+150	°C
ESD					
V_{ESD}	electrostatic discharge voltage	class 1			
	human body model	pins 2 to 8 [1]	-	2000	V
		pin 1 [1]	-	1500	V
	machine model	[2]	-	200	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] Equivalent to discharging a 200 pF capacitor through a 0.75 µH coil and a 10 Ω resistor.

9. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	150	K/W

The graph in Figure 4 shows the relationship between junction temperature and VSENSE voltage.

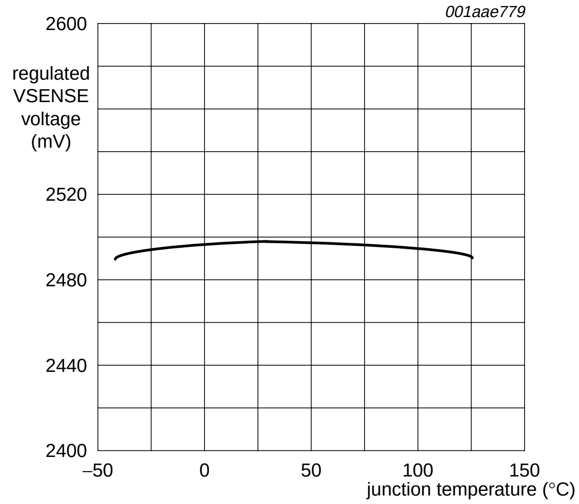


Fig 4. Typical regulated VSENSE voltage versus junction temperature

10. Characteristics

Table 5. Characteristics

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage management (pin V_{CC})						
$V_{startup}$	start-up voltage		8.35	8.6	8.85	V
V_{hys}	hysteresis voltage			0.5		V
$I_{CC(oper)}$	operating supply current	$V_{CC} < V_{startup}$; V_{CC} = 8 V	-	1	-	mA
$I_{CC(oper)}$	operating supply current	under normal operation; no load on pin DRIVER	-	1.4	-	mA
Synchronous rectification sense input (pin SRSENSE)						
$V_{act(drv)}$	driver activation voltage		–370	–340	–310	mV
$V_{reg(drv)}$	driver regulation voltage		–60	–50	–40	mV
$V_{deact(drv)}$	driver deactivation voltage			–12		mV
$t_{d(act)(drv)}$	driver activation delay time		-	350	-	ns
$t_{act(sr)(min)}$	minimum synchronous rectification active time		1.5	2	2.5	µs
Driver (pin DRIVER)						
I_{source}	source current	V_{CC} = 15 V; voltage on pin DRIVER = 2 V	-	–0.3	-	A
I_{sink}	sink current	V_{CC} = 15 V;				
		voltage on pin DRIVER = 2 V	-	1	-	A
		voltage on pin DRIVER = 9.5 V	-	2.2	-	A
$V_{o(max)}$	maximum output voltage	V_{CC} = 15 V	-	10	12	V

Table 5. Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Opto output (pin OPTO)						
$I_{O(max)}$	maximum output current	V_{OPTO} > 5 V	4	5	12	mA
$V_{O(min)}$	minimum output voltage	I_{OPTO} = 4 mA	-	-	3.5	V
Voltage sense (pin VSENSE)						
$V_{reg(VSENSE)}$	regulation voltage on pin VSENSE	See Figure 4	2.475	2.5	2.525	V
$I_{I(VSENSE)}$	input current on pin VSENSE	V_{VSENSE} = 2.5 V	–100	0	100	nA
g_m	transconductance	V_{VSENSE} to I_{OPTO}	-	40	-	A/V
GB	gain bandwidth product	R_L = 1 kΩ	1			MHz
Current sense (pin ISENSE)						
$V_{reg(ISENSE)}$	regulation voltage on pin ISENSE		46	50	54	mV
$I_{I(reg)(ISENSE)}$	regulation input current on pin ISENSE	V_{ISENSE} = 50 mV	–200	–100	0	nA
g_m	transconductance	V_{ISENSE} to I_{OPTO}	-	15	-	A/V
GB	gain bandwidth product	R_L = 1 kΩ	1	-	-	MHz
Temperature protection						
$T_{pl(max)}$	maximum protection level temperature		140	150	-	°C
$T_{pl(hys)}$	protection level hysteresis temperature		-	12	-	°C

11. Application information

A switched mode power supply with the TEA1761T consists of a primary side discontinuous conduction mode flyback controller, a transformer, and an output stage with a feedback circuit. In the output stage a MOSFET (Qsec) is used for low conduction losses. The MOSFET is controlled by the TEA1761T. The output voltage and/or current is also controlled by the TEA1761T via the opto coupler connection to the primary side. See Figure 5.

The output voltage is set by resistors Rfb1 and Rfb2. The output current is controlled by the resistor Risense. The timing for the synchronous rectifier switch is derived from the voltage sensed on the SRSENSE pin. The resistor in the SRSENSE connection is needed to protect the TEA1761T from excessive voltages. The SRSENSE resistor should typically be 1 kΩ. Higher values might impair correct timing, lower values may not provide sufficient protection.

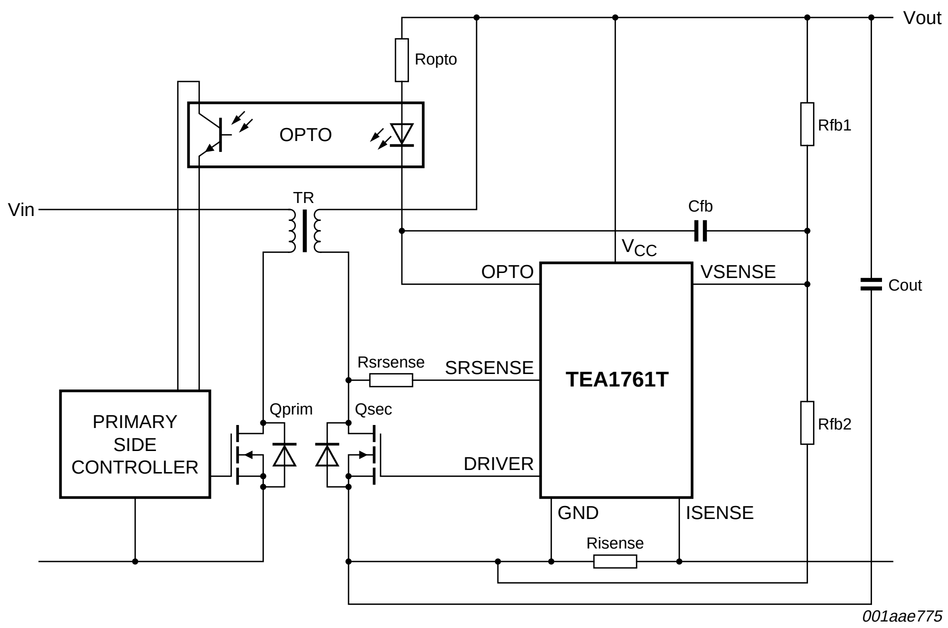


Fig 5. Application example TEA1761T

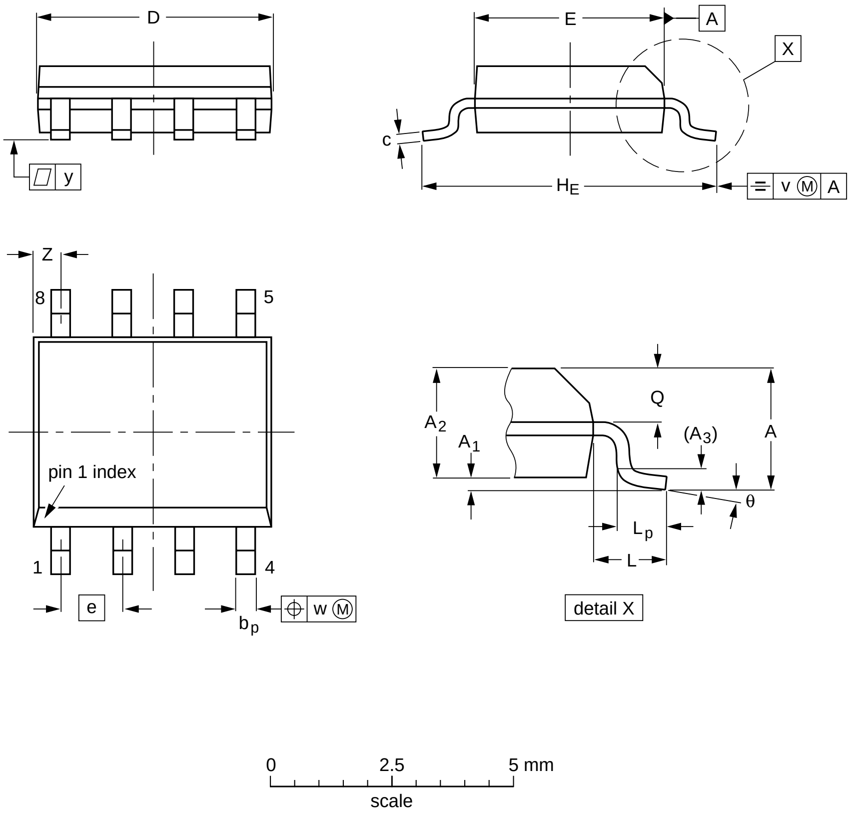
12. Test information

12.1 Quality information

The *General Quality Specification for Integrated Circuits, SNW-FQ-611* is applicable.

13. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 6. Package outline SOT96-1 (SO8)

14. Soldering

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness $\geq$ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume $\geq$ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

14.5 Package related soldering information

Table 6. Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	**Soldering method**	
	Wave	**Reflow**[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

15. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1761T_1	20060331	Objective data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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18. Contents

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