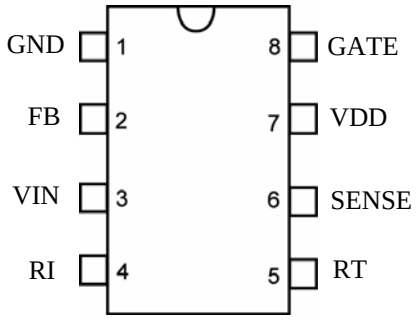
Applying SG5841 to Control a Flyback Power Supply **AN5841**

ABSTRACT

The present application note describes a detailed design strategy for a high efficiency and compact flyback converter. Design considerations and mathematical equations are presented. Finally, the guidelines for a printed circuit board layout are also given.

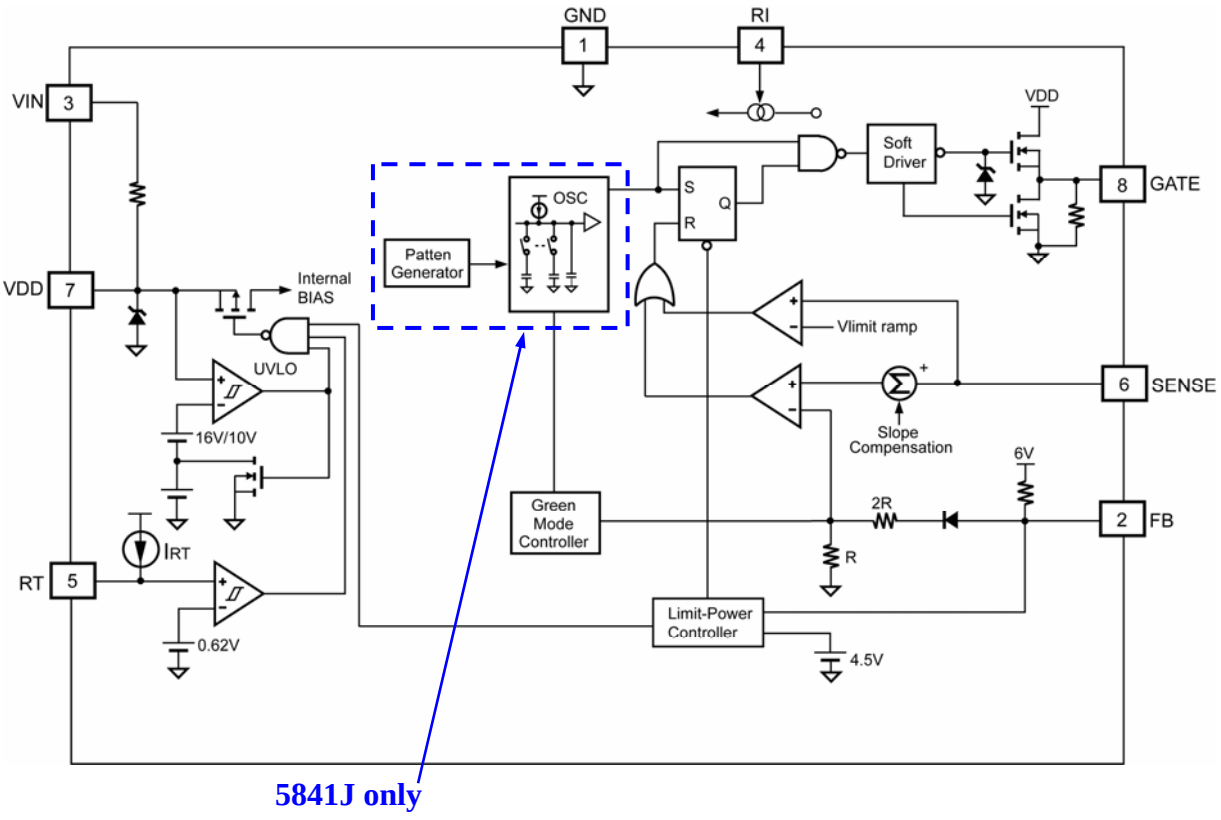
PIN CONFIGURATION



FEATURES OVERVIEW

- Green-mode PWM Controller
- Low Start-Up Current (14uA)
- Low Operating Current (4mA)
- Programmable PWM frequency with Hopping
- Peak-current-mode Control
- Cycle-by-Cycle Current Limiting
- Synchronized Slope Compensation
- Leading-Edge Blanking
- Constant Output Power Limit
- Totem Pole Output with Soft Driving
- VDD Over Voltage Clamping
- Programmable Over Temperature Protection (OTP)
- Internal Open-loop Protection
- V_{DD} Under-voltage Lockout (UVLO)
- GATE Output Maximum Voltage Clamp (18V)

BLOCK DIAGRAM



DESCRIPTION

The SG5841 is a highly integrated PWM controller IC. It provides special features satisfying the needs for low standby power consumption. It also incorporates manifold protection functions. With low start-up current and low operating current, high-efficiency power conversion is achieved. Typical start-up current is only 14uA and operating current is around 4mA. In nominal loading conditions, the SG5841 operates at fixed PWM frequency. As the load decreases, its patented green-mode circuit gradually reduces the PWM frequency. This green-mode function dramatically cuts the power loss in no-load and light-load conditions, enabling the power supply to meet power conservation requirements. Additionally, the controller incorporates many protection functions. Once the power supply is overloaded, the controller forces the power supply into hiccup mode to limit output power. The built-in line-voltage compensation circuit maintains constant maximum output power for a wide input line voltage range. An external negative-temperature-coefficient (NTC) thermistor can be connected to the RT pin for over-temperature protection.

Start-up Circuitry

When the power is turned on, the input rectified voltage Vdc charges the hold-up capacitor C_1 via a start-up resistor R_{IN}. R_{IN} can be connected to pin VIN or VDD directly. As the voltage of VDD pin reaches the start threshold voltage V_{DD-ON}, the SG5841 activates and drives the entire power supply to work.

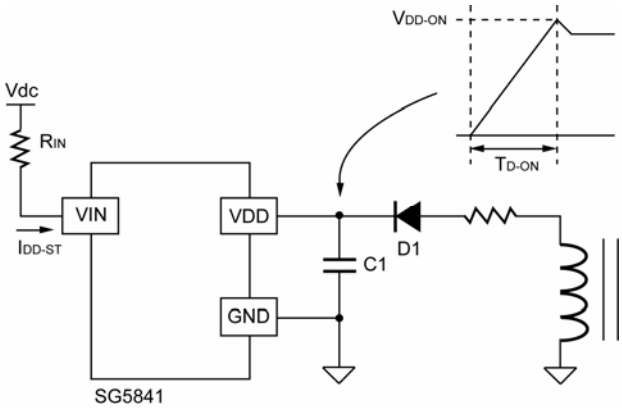


Figure 1. Single step circuit of providing power to the SG5841

The maximum power-on delay time is determined as follows:

$$V_{DD-ON} = (V_{dc} - I_{DD-ST} \cdot R_{IN}) \left[1 - e^{-\frac{T_{D-ON}}{R_{IN} \cdot C1}} \right] \quad (1)$$

where

I_{DD-ST} is the start-up current of the SG5841;

T_{D-ON} is the power-on delay time of the power supply.

Due to the low start-up current, a large R_{IN} such as 1.5Mohm can be used. Also with a hold-up capacitor of 4.7uF, the power-on delay T_{D_ON} is less than 3.3s for 90Vac input.

If a shorter start-up time is required, a two steps start-up circuit as shown in Figure 2 is recommended. In this circuit, a smaller C1 capacitor can be used to speed up the start-up time without using smaller start-up resistor R_{IN} and increasing the power dissipation on R_{IN} resistor. The energy supporting the SG5841 after start-up is mainly from a bigger capacitor C2.

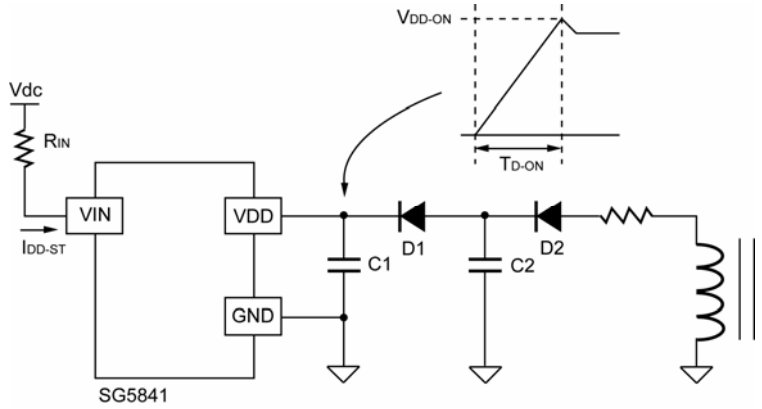


Figure 2. Two steps circuit of providing power to the SG5841

The maximum power dissipation of R_{IN} is

$$P_{RIN,\max} = \frac{(V_{dc,\max} - V_{DD})^2}{R_{IN}} \cong \frac{V_{dc,\max}^2}{R_{IN}} \quad (2)$$

where

$V_{dc,max}$ is the maximum rectified input voltage.

Take a wide-range input (90Vac-264Vac) as an example,

V_{dc} =100V ~ 380V

$$P_{RIN,\max} = \frac{380^2}{1.5 \times 10^6} \cong 96mW \quad (3)$$

In addition to the low start-up current, the SG5841 consumes less normal operating current than traditional UC384x.

To achieve a successful start up and keep a no load input power low enough to meet the power saving requirement, the voltage level of VDD is recommended to design at above 12V at no load.

Or, the voltage of VDD may fall below UVLO during “Adaptive off-time modulation” condition and the unit will enter hiccup operation.

Oscillator & Green Mode Operation

Resistor R_I programs the frequency of the internal oscillator of the SG5841. A 26Kohm resistor R_I generates PWM frequency as 65KHz,

$$f_{PWM}(KHz) = \frac{1690}{R_I(K\Omega)} \quad (4)$$

The range of the PWM frequency is recommended between 47KHz ~ 109KHz.

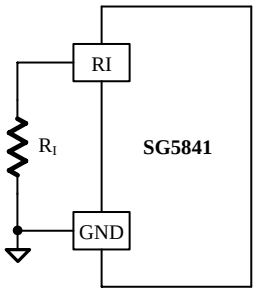


Figure 3. Setting PWM frequency

The patented green-mode function provides off-time modulation to reduce the PWM frequency at light-load and in no-load conditions. The feedback voltage of the FB pin is taken as a reference. When the feedback voltage is lower than about 2.1V, the PWM frequency decreases. Because most losses in a switching mode power supply are proportional to the PWM frequency, the off-time modulation of the SG5841 reduces the power consumption of the power supply at light-load and no-load conditions. For a typical case of RI = 26Kohm, the PWM frequency is 65KHz at nominal load, and decreases to 22KHz at light load, about 1/3 of the nominal PWM frequency. The power supply will enter "Adaptive off-time modulation" in zero-load conditions.

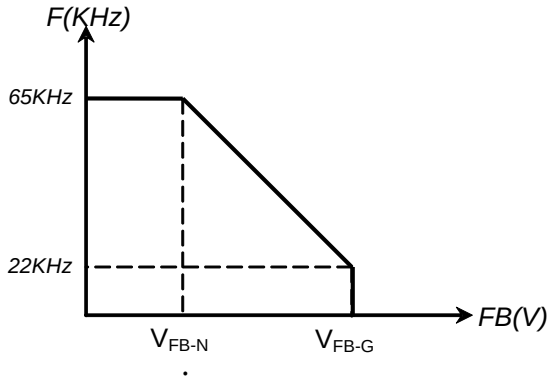


Figure 4-1. PWM frequency versus FB voltage (RI=26Kohm)

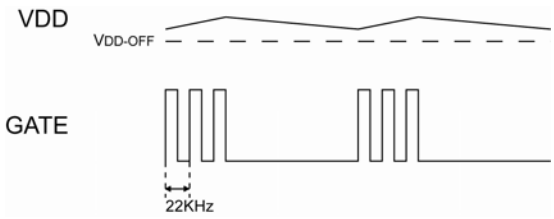


Figure 4-2. Adaptive off-time modulation

A frequency hopping function is built to improve the system level of EMI performance. The PWM switching frequency will hop between 65KHz +/- 4.2KHz. The hopping period is around 4.4msec. (5841J only)

The FB input

The SG5841 is designed for peak-current-mode control. A current-to-voltage conversion is done externally with a current-sense resistor R_S. Under normal operation, the peak inductor current is controlled by FB level,

$$I_{pk} = \frac{V_{FB} - 1.2}{3 \cdot R_S} \quad (5)$$

where

V_{FB} is the voltage of FB pin.

When V_{FB} is less than 1.2V, the SG5841 terminates the output pulses.

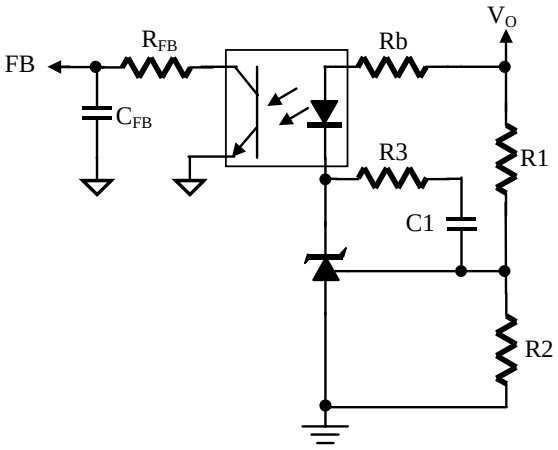


Figure 5. Feedback circuit.

Figure 5 is a typical feedback circuit mainly consisting of a shunt regulator and an opto-coupler. R_1 and R2 form a voltage divider for the output voltage regulation. R3 and C1 are adjusted for control-loop compensation. A small-value RC filter (e.g. R_{FB}= 47ohm, C_{FB}= 1nF) placing from FB pin to GND can increase stability. The maximum sourcing current of FB pin is 2mA. The phototransistor must be capable of sinking this current to pull FB level down at no load. Thus, the value of biasing resistor Rb is determined as follows,

$$\frac{V_o - V_D - V_Z}{R_b} \cdot K \geq 2mA \quad (6)$$

where

V_D is the drop voltage of photodiode, about 1.2V;

V_Z is the minimum operating voltage, 2.5V of the shunt regulator;

K is the current transfer rate (CTR) of the opto-coupler.

For an output voltage Vo=5V, with CTR=100%, the maximum value of Rb is 650ohm.

Built-in Slope Compensation

A flyback converter can be operated in either discontinuous current mode (DCM) or continuous current mode (CCM). There are many advantages when operating the converter in CCM. With the same output power, a converter in CCM exhibits smaller peak inductor current than the one in DCM. Therefore, a small sized transformer and a low-rating MOSFET can be applied. On the secondary side of the transformer, the rms output current of DCM can be up to twice of CCM. Larger wire gauge and output capacitors with larger ripple current rating are required. DCM operation also results in higher output voltage spikes. A large LC filter has also to be added. Therefore, a flyback converter in CCM achieves better performance with lower component cost.

Despite the above advantages of CCM operation, there is one concern – stability issue. In CCM operation, the output power is proportional to the average inductor current, while the peak current is controlled. This causes the well-known sub-harmonic oscillation when the PWM duty cycle exceeds 50%. Adding slope compensation (reducing the current-loop gain) is an effective way to prevent oscillation. The SG5841 introduces a synchronized positive-going ramp (V_{SLOPE}) in every switching cycle to stabilize the current loop. Therefore, users can use the SG5841 to design a cost effective, highly efficient and compact sized flyback power supply operating in CCM without adding any external component.

The positive ramp added is,

$$V_{SLOPE} = V_{SL} \cdot D \quad (7)$$

where

V_{SL} = 0.33V;

D: Duty cycle

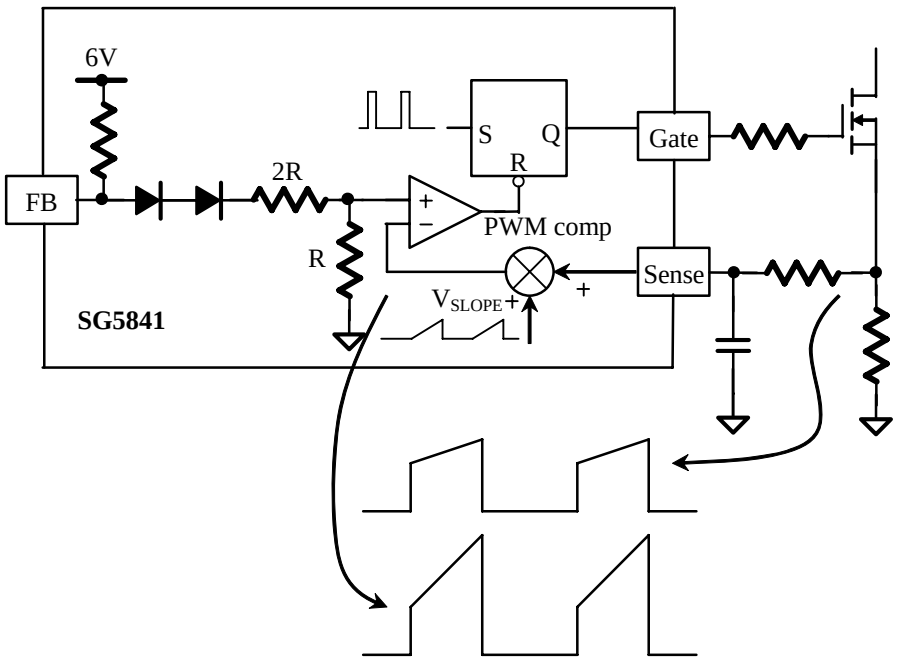


Figure 6. Synchronized slope compensation

Leading Edge Blanking

A voltage signal proportional to the MOSFET current develops on the current-sense resistor Rs. Each time the MOSFET is turned on, a spike, which is induced by the diode reverse recovery and by the output capacitances of the MOSFET and diode, inevitably appears on the sensed signal. Inside the SG5841, a leading edge blanking time about 270nsec is introduced to avoid premature termination of MOSFET by the spike. Therefore, only a small-value RC filter (e.g. 100ohm + 470pF) is required between the SENSE pin and Rs. Still, a non-inductive resistor for the R_S is recommended.

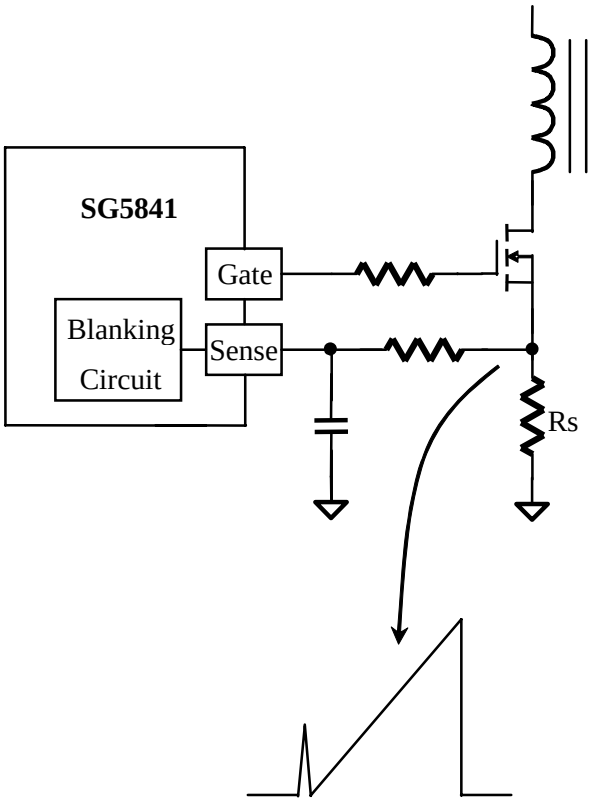


Figure 7. Turn on spike

Output driver / Soft driving

The SG5841's output stage is a fast totem-pole gate driver capable of directly driving external MOSFET's. An internal zener diode clamps the driver voltage under 18V to protect MOSFET's against over voltage. The maximum duty cycle is around 65%. By integrating special circuits to control the slew rate of switch-on rising time, the external resistor R_G may not be necessary to reduce switching noise, improving EMI performance.

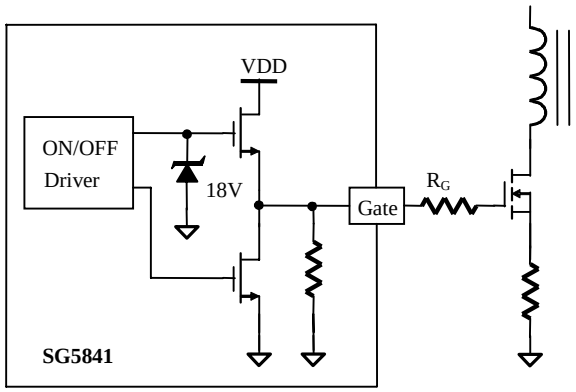


Figure 8. Gate drive

Constant Output Power Limit

The maximum output power of a flyback converter can generally be determined from the current-sense resistor R_S. When the load increases, the peak inductor current increases accordingly. Once the output current arrives at the protection value, the OCP comparator dominates the current control loop. OCP occurs when the current-sense voltage reaches the threshold value. The output GATE driver is turned off after a small propagation delay, t_{PD}. The delay time results in unequal power-limit level under universal input. In SG5841, a saw-tooth power-limiter (saw limiter) is designed to solve the unequal power-limit problem. As shown in Figure 9, the saw limiter is designed as a positive ramp signal (Vlimit ramp) and is fed to the inverting input of the OCP comparator. This results in a lower current limit at high-line inputs than at low-line inputs. However, with fixed propagation delay, t_{PD}, the peak primary current would be the same for various line input voltages. Therefore the maximum output power can practically be limited to a constant value within a wide input voltage range without adding any external circuitry.

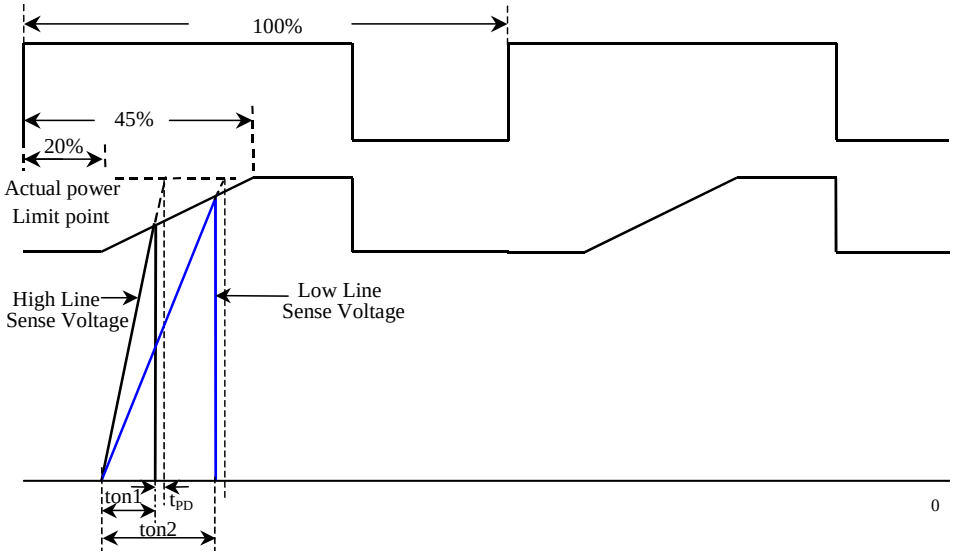


Figure 9. Constant power limit compensation

VDD Over-voltage Clamping

VDD over-voltage Clamping has been built in to prevent damage due to abnormal conditions. Once the VDD voltage is over than the VDD over voltage clamping voltage($V_{DD-CLAMP}$), and lasts for $t_{D-VDDCLAMP}$, the PWM pulses will be disable until the VDD voltage drops below the VDD over voltage clamping voltage.

Thermal Protection

A constant current I_{RT} is provided from pin RT. The resistor connected to pin RI decides its magnitude,

I_{RT} = 100uA * (26 KΩ / RI) (8)

For example,

I_{RT} = 100uA if RI = 26KΩ.

For over-temperature protection, an NTC thermistor RT in series with a resistor Ra can be connected between pin RT and ground. When, V_{RT}, the voltage level of RT pin is less than 0.62V, PWM output will be turned off.

If the thermal protection is not used, please connect a small capacitor (around 1nF is recommended) from RT pin to GND pin to prevent interfere by noises. This RT capacitor can not larger than 4.7nF or the thermal protection will be triggered before a successful start up of output voltage.

Lab Note

Before rework or solder/desolder on the power supply, it is suggested to discharge primary capacitors by external bleeding resistor. Otherwise the PWM IC may be destroyed by external high voltage during solder/desolder.

This device is sensitive to ESD discharge. To improve production yield, production line should be ESD protected according to ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1.

Printed Circuit Board Layout

High frequency switching current/voltage makes printed circuit board layout a very important design issue. Good PCB layout minimizes excessive EMI and helps the power supply survive during surge/ESD tests. Here, we give some common guidelines:

- In order to get better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitor C1 first, and then to the switching circuits.
- The high frequency current loop is in **C1 – Transformer – MOSFET – R_S – C1**. The area enclosed by this current loop should be as small as possible. Keep the traces (especially 4→1) short, direct, and wide. High voltage traces related the drain of MOSFET and RCD snubber should be kept far way from control circuits to prevent unnecessary interference. If a heatsink is used for MOSFET, it's better to connect this heatsink to ground.
- As indicated by 3, the ground of control circuits should be connected first and then to other circuitry.
- As indicated by 2, the area enclosed by **transformer aux winding, D1, and C2** should also be kept small. Place C2 close to the SG5841 for good decoupling.
- Two suggestions with different pros and cons for ground connections are recommended.
- GND3→2→4→1: This could avoid common impedance interference for sense signals.
- GND3→2→1→4: This could be better for ESD testing where the earth ground is not available on the power supply. Regarding the ESD discharge path, the charges go from secondary through the transformer stray capacitance to GND2 first. And then the charges go from GND2 to GND1 and go back to mains. It should be noted that control circuits should not be placed on the discharge path. Point discharge for common choke can decrease high frequency impedance and help to increase ESD immunity.
- Should a Y-cap between primary and secondary be required, it is suggested to connect this Y-cap to the **positive terminal of C1 (Vdc)**. If this Y-cap is connected to the primary GND, it should be connected to the **negative terminal of C1 (GND1)** directly. Point discharge of this Y-cap also helps ESD. However, the creepage between these two pointed ends should be at least 5 mm according to safety requirements.

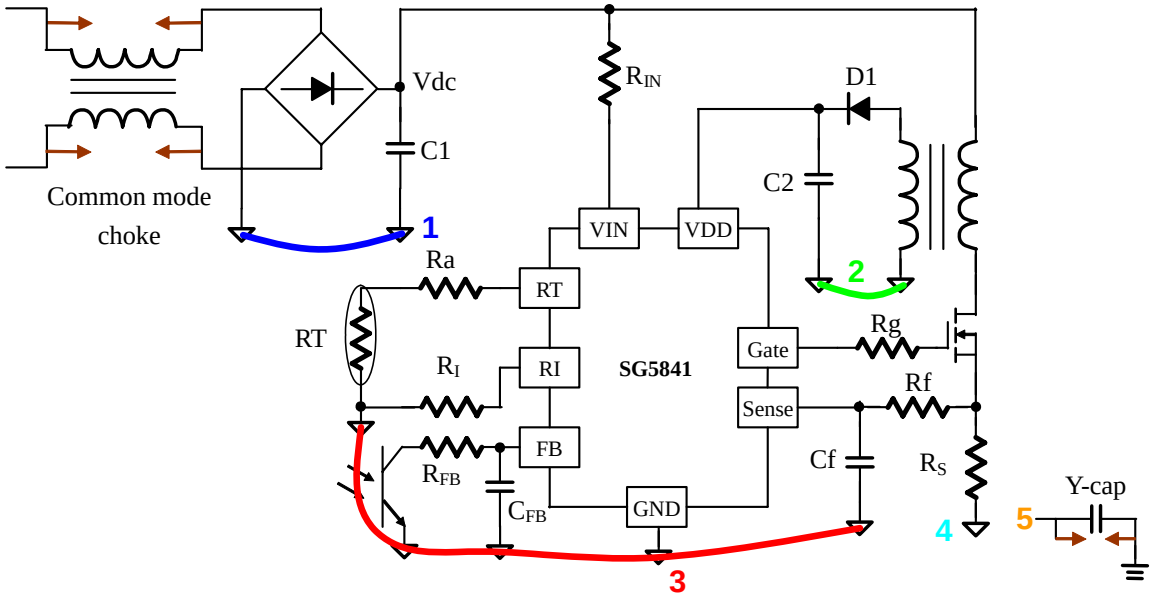


Figure 10. Layout considerations

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