Spice model eases feedback loop designs

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Within the wide family of Switch Mode Power Supplies (SMPS), the Flyback converters represent the preferred structure for use in small and medium power applications (50-100W) such as wall adapters, off-line battery chargers, fax machines etc. Thanks to the recent introduction of MOTOROLA Very High Voltage Integrated Circuits (VHVICs), the design phase of a Flyback converter has almost turned into a child's play: a bunch of passive components around the MC33370 and you are all set! However, the impact of the environment upon the system can be much longer to iterate in order to cover the numerous situations the converter will encounter in its future life: ESRs variations due to temperature cycles, aging of the capacitors, various types of load, load and line transients, effect of the filter stage etc.

In this article, we will show how a Spice simulator can help the designer to quickly implement his concept and show how it reacts to the outside world constraints. This brings several benefits such as an immediate understanding of how the circuit operates and naturally, an improved time-to-market cycle.

Defining the chain

Figure 1 depicts the complete chain implemented in a standard Flyback converter. In order to draw a Bode plot and thus place appropriate pole/zeroes combinations, we need to individually assess every gain block.

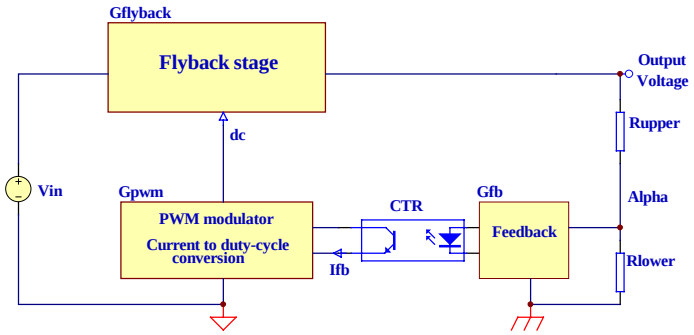

Figure 1
A Flyback chain implementing current feedback

In a shunt regulator, such as the new VHVIC series, the duty-cycle is adjusted by injecting a current into the feedback pin. The approach differs from the classical voltage feedback devices and requires a detailed explanation to help you comfortably deal with this concept.

The duty-cycle conversion

The members of the MC3337X series implements a duty-cycle control through a shunt regulator. That is to say, the duty-cycle (*dc*) is adjusted by injecting a current into a feedback pin (FB). When the current is low

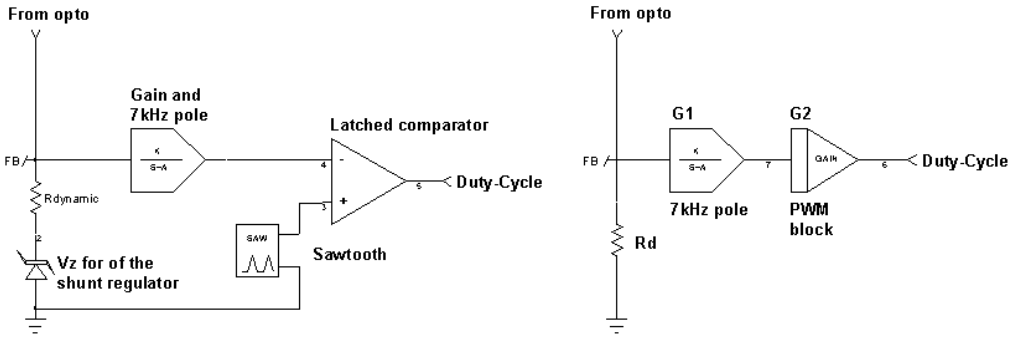

Figure 2a
The PWM chain in a shunt regulator

or zero, the duty-cycle is pushed to the max (74% typical for the MC33370). If more current is pushed into the pin, the duty-cycle goes toward a few percents (0.9% typical). The amount of current needed to go from full *dc* to null *dc* determines the PWM gain. **Figure 2a** details how the duty-cycle conversion takes place :

To remove any spurious noises due to the high peak currents flowing around the IC, the designers have installed an internal 7kHz low-pass filter. This pole shall be included in the final AC study.

As previously said, the FB corresponds to the input of a shunt regulator. To better understand the way it works, you can replace the shunt regulator by a power zener: when the voltage you apply on the FB pin is below the shunt breakdown level, no current flows into the pin and *dc* is maximum. When the FB level reaches the zener threshold, a current circulates in the pin and is converted into a lowering duty-cycle. First remark, in steady-state operation, the FB pin is at the shunt level as given in the data-sheet: 8.6V for the MC3337X. You shall then provide the feedback current through a source whose value is, at least, two or three volts above the shunt value. Otherwise you will not reach the appropriate level to regulate and you will force the optocoupler to operate in a low V_{CE} region where the conductance d_{IC}/dV_{CE} is rather poor.

For AC analysis, the FB pin can be replaced by the dynamic resistor of the power zener, dVzener/dIdiode or 18Ω for the MC3337X series. This value gives you the AC impedance seen from the FB pin. It will dictates the locations of the poles and zeroes you create by adding capacitors around this pin. This is NOT the PWM gain, but rather an intermediate current/voltage conversion gain. The complete gain, as highlighted by figure 1, depends on the internal sawtooth amplitude (1.4Vpp for the MC3337X) and the maximum duty-cycle. In these ICs, the presence of the latched comparator makes the error signal reach the sawtooth peak value when the duty-cycle is at the maximum (74%). The total gain calculation is done following the steps:

ΔI_{FB} of 6mA→Δdc of 74% or a slope of 12.3%/mA typical.

6mA . 18Ω = 108mV

$$G1 = 20 \cdot Log\left(\frac{1.4}{108m}\right) = 22.25dB$$

$$G2 = 20 \cdot Log\left(\frac{0.74}{1.4}\right) = -5.53dB$$

Finally since the internal FB dynamic impedance also participates to the gain, the complete PWM chain exhibits the following values:

MC3337X: 22.25dB + 25.1dB$_{18\Omega}$ - 5.53dB = 41.82dB

Figure 2b gives the data-sheet information on the duty-cycle conversion ratio while **figure 2c** gives simulation results of the PWM stage only as it is offered in the MC3337X Spice model.

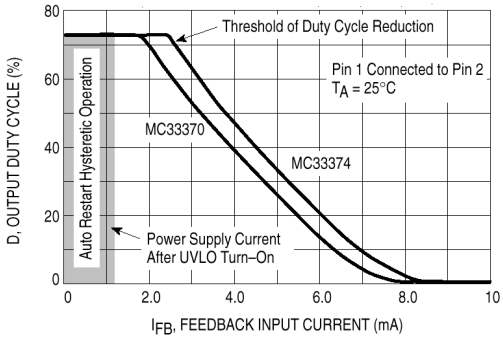

Figure 2b
MC3337X duty-cycle versus injected current

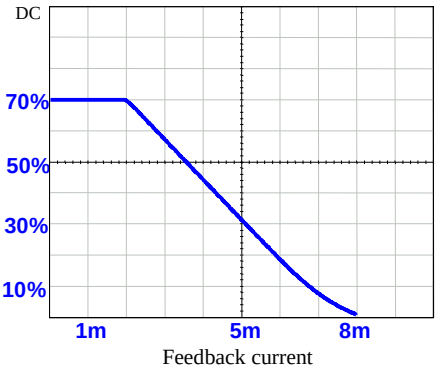

Figure 2c
Simulated PWM section of the MC3337X

As we will see later on, the calculation of the whole chain (Flyback stage, feedback etc.) *static* gain does NOT involve the knowledge of the input impedance of the FB pin, but rather the current/*dc* conversion ratio, S_{PWM}.

First case: the optocoupler is alone

This is the most economic case where the output voltage does not require a tight regulation. The optocoupler Light Emitting Diode (LED) is simply inserted in series with a zener diode. The output level is then close to Vz + Vf, with Vz the zener voltage and Vf the forward level of the LED. **Figure 3a** depicts this situation when a compensation network made of Rs and C1 is added (Z1 impedance). In the calculation, we are evaluating the voltage present on the FB pin to isolate the feedback network contribution.

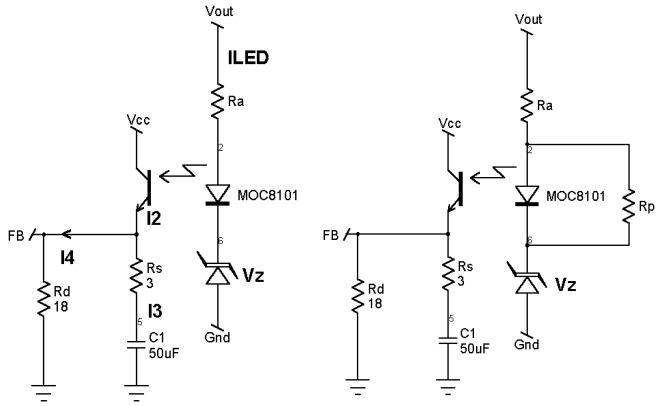

Figure 3a and 3b

On the right side, a resistor Rp is added to refine the stabilization but it also ***slightly*** decreases the loop gain

The calculation steps are rather easy and will be reproduced all along this document. It consists in a) evaluating the LED current b) finding its relationship with I_{FB} or V_{PWM} c) derive the result to obtain the small-signal gain. However, in a so simple schematic, we can highlight the parasitic element the LED and the zener are made of (**figure 4a**). Taking into account that the perfect sources Vf and Vz do not move with Vout, the final equation for the LED current reduces to: $I_{LED} = \frac{Vout}{R_A + Rd_{LED} + Rd_Z}$.

$$I_2 = I_{LED} \cdot C\mathrm{TR}$$

$$V_{FB} = I_4 \cdot Rd = I_2 \cdot \frac{Z1 \cdot Rd}{Z1 + Rd} = I_{LED} \cdot C\mathrm{TR} \cdot \frac{Z1 \cdot Rd}{Z1 + Rd}$$

$$V_{FB} = \frac{Vout}{Ra + Rd_{LED} + Rd_Z} \cdot C\mathrm{TR} \cdot Rd \cdot \frac{1 + \frac{1}{Rs \cdot C1 \cdot p}}{1 + \frac{1}{(Rs + Rd) \cdot C1 \cdot p}}$$

$$\frac{dV_{FB}}{dVout} = [Rd \,//\, Rs] \cdot \frac{C\mathrm{TR}}{Ra + Rd_{LED} + Rd_Z} \cdot \frac{1 + \frac{1}{Rs \cdot C1 \cdot p}}{1 + \frac{1}{(Rs + Rd) \cdot C1 \cdot p}}$$

we then define a zero f_Z and a pole f_P: $f_Z = \frac{1}{2 \cdot \pi \cdot Rs \cdot C1} and, f_P = \frac{1}{2 \cdot \pi \cdot (Rd + Rs) \cdot C1}$

In DC, the gain simplifies to: $DCgain = \frac{d_{dc}}{dVout} = -\frac{Rd \cdot CTR}{Ra + Rd_{LED} + Rd_Z}$ while in high-frequency, when C1 is a complete short: $HFgain = \frac{d_{dc}}{dVout} = -\frac{[Rd \,//\, Rs] \cdot CTR}{Ra + Rd_{LED} + Rd_Z}$. To obtain the final chain Vout to the PWM's output, you need to add G1 and G2 as defined above.

However, if you only account for the I_{FB}/dc conversion slope (S_{PWM}) of –12.3%/mA (or -123/A), the *complete* DC gain from Vout to the PWM stage's output is simply:

$$DCgain = \frac{d_{dc}}{dVout} = -\frac{C\,\mathrm{TR}\cdot S_{PWM}}{Ra + Rd_{LED} + Rd_Z}$$

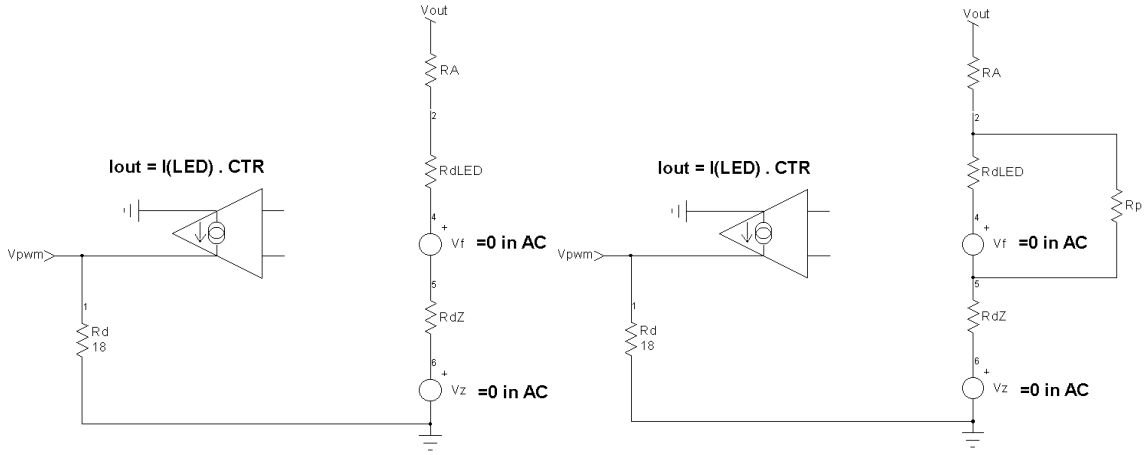

Figure 4a and 4b
Since Vf and Vz do not vary in AC, we can put them to zero for the analysis

In some applications, it is interesting to increase the current flowing into the zener to gain in precision: the zener operates away from its knee where dVz/dIzener is rather high. To implement this option, simply wire a resistor in parallel with the LED as **figure 3b** and **figure 4b** show. In AC, Rp now comes in parallel with Rd and affects the total DCgain (from Vout to the PWM's output) by: $DC_{gain} = -\frac{1}{RA + Rd_{LED} // Rp + Rd_Z} \cdot \frac{Rp}{Rp + Rd_{LED}} \cdot C\,\mathrm{TR}\cdot S_{PWM}$. When Rp becomes infinite, this formula simplifies to the previous one. As we can imagine, with rather low values of Rd_{LED}, the gain is *slightly* degraded by the presence of Rp.

Numerical application for figure 3a example:

Rd = 18Ω CTR = 1.8 (180%) S_{PWM} = 12.3%/mA
Cs = 50µF R_A = 270Ω
Rs = 3Ω Rd_{LED} and Rd_Z are neglected.

DC_{gain} = -18.41dB + G1 + G2 = -1.723dB
HF_{gain} = -35.32dB + G1 + G2 = -18.6dB
1st pole = 151Hz
1st zero = 1.061kHz

The very low static-gain engendered by this configuration is not compatible with a good audiosusceptibility (input line rejection). The TL431 will help us to raise this poor value.

An integrator with the TL431 to boost the DC gain

By wiring a TL431 as depicted by **figure 5a**, we will offer better ripple rejection by raising the DC gain. For the sake of clarity we have removed the previous passive RC network, but its action is similar as the one already calculated. Please note that Vout is split in two values: Vout and k x Vout. In Flyback converters operating in Discontinuous Conduction Mode (DCM), the high secondary peak current generates a thin output spike when combined with the output capacitor's ESR. To fight against this problem, you can add a small series inductor of a few µH. Unfortunately, it also adds a second order high-frequency pole that you do not want to include into the final feedback path. You then split the feedback in two ways: a fast one with low gain through the LED anode (k x Vout) and a low-frequency with high gain on the resistive divider (Vout). As a first remark, we can see that when either the TL431's gain or the network across it roll its gain to zero, we come back to

figure 3a configuration. Therefore we cannot really roll the whole loop gain to zero! That is a typical pain of the TL431 but we can also turn it into an advantage as we will see later on.

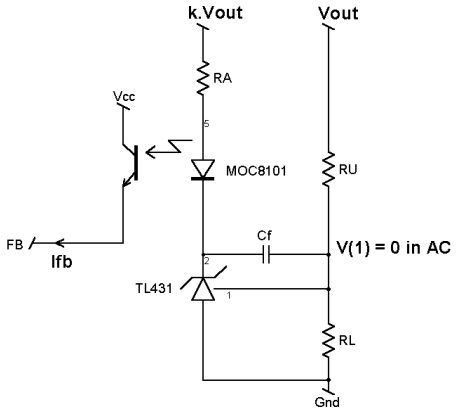

Figure 5a
A TL431 helps to rise the gain in DC

Let us start by the DC analysis where Cf is open and in lack of feedback on the TL431, the node 1 is NOT a virtual ground (or at internal Vref):

$I_{LED} = \dfrac{k \cdot Vout - (Vf + Vz)}{R_A}$ with Vz = TL431'Anode-Cathode voltage.

$Vz = -Vout \cdot \dfrac{RL}{RU + RL} \cdot Av_{TL431}$ and $I_{FB} = I_{LED} \cdot C\,\mathrm{TR}$. The final equation for I_{FB} is then:

$$I_{FB} = \frac{k \cdot Vout - \left(Vf - \dfrac{Vout \cdot RL}{RL + RU} \right) \cdot Av_{TL431}}{R_A} \cdot C\,\mathrm{TR}$$

$$\frac{d_{dc}}{dVout} = -\frac{k \cdot (RL + RU) + RL \cdot Av_{TL431}}{R_A \cdot (RL + RU)} \cdot C\,\mathrm{TR} \cdot S_{PWM} \rightarrow \text{DCgain.}$$

In AC, the first I_{LED} equation still holds. But this time Cf closes the TL431 feedback path and maintains a true virtual ground on node 1: V(1) = 0 in AC. Cf creates an integrator with RU (RL does not play in AC because of the virtual ground) and the Vz parameter is expressed by:

$$Vz = -Vo \cdot \frac{1}{RU \cdot Cf \cdot p}$$

$$I_{LED} = \frac{k \cdot Vout - \left(Vf - Vout \cdot \dfrac{1}{RU \cdot Cf \cdot p} \right)}{R_A}$$

$$\frac{d_{dc}}{dVout} = -\frac{(k \cdot RU \cdot Cf + 1)}{RU \cdot Cf \cdot p} \cdot \frac{C\,\mathrm{TR} \cdot S_{PWM}}{R_A} \rightarrow$$ ACgain with a pole $fp = \dfrac{1}{2 \cdot \pi \cdot RU \cdot Cf}$ and a zero located at $fz = \dfrac{1}{2 \cdot \pi \cdot k \cdot RU \cdot Cf \cdot p}$.

To verify our calculations, a Spice engine is a very good tool. **Figure 5b** depicts an INTUSOFT's IsSpice4 (San-Pedro, CA) simulation schematic of the TL431 architecture.

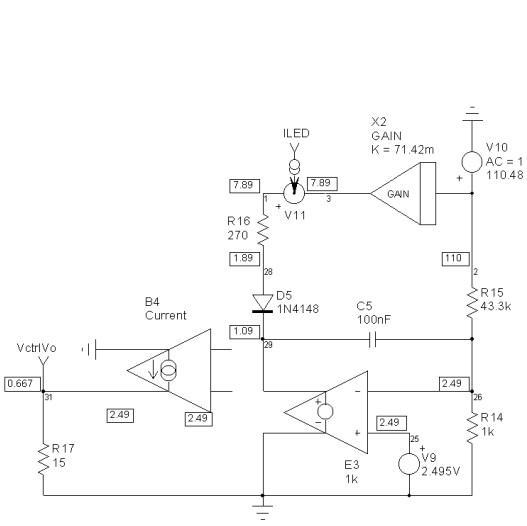

Figure 5b
A IsSpice4 simulation schematic of the TL431 structure

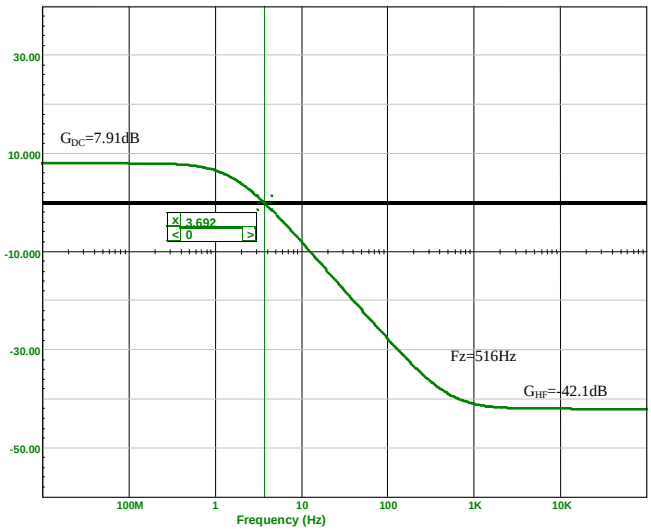

Figure 5c
The Bode plot revealed after simulation

This example simulates a Flyback converter delivering a 112V level (e.g. in a TV application) while the LED is biased through an auxiliary 8V winding. Therefore k = 8/112 = 71.42m. The optocoupler is replaced by a current-controlled current source with a gain of 2 (CTR = 200%) for simpler calculations. V10 is adjusted to keep a correct DC point (as the schematic values testify) and is AC modulated to draw the output Bode plot. Again, we purposely isolate this feedback system and the output is taken *upon R17* and NOT, as before, at the PWM's output.

Numerical application for figure 4b example:

Rd = 15Ω	CTR = 2 (200%)
R_A = 270Ω	TL431 gain = 1000
RU = 43.3kΩ	RL = 1kΩ
Cf = 100nF	k = 71.42m

DC_{gain} = 8dB
HF_{gain} = -42dB
1st pole x $\frac{C\,\mathrm{TR}\cdot Rd}{R_A}$ = fc @ 0dB = 4.08Hz (the small mismatch is due to the natural low Av_{TL431} of 55dB)
1st zero = 514.6Hz

The TL431 with a DC feedback

We now add a simple feedback resistor between the TL431's cathode and its reference pin (**figure 5b**).

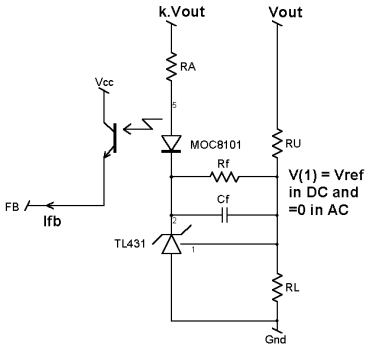

Figure 5b
The DC is no longer in open-loop for the TL431 thanks to Rf

This time, we have a virtual ground in DC ($Vnode1_{DC}$=Vref) and AC. The expression of the LED current changes a bit as RL no longer acts:

$$I_{LED} = \frac{k \cdot Vout - \left(Vf - Vout \cdot \frac{Rf}{RU} \right)}{RA} \text{ and } I_{FB} = I_{LED} \cdot C\,\text{TR}$$

$$\frac{d_{dc}}{Vout} = -\frac{k \cdot RU + Rf}{RU \cdot R_A} \cdot CTR \cdot S_{PWM} \rightarrow \text{DCgain}$$

In AC, $Vz = -Vout \cdot \frac{Rf}{RU \cdot (1 + Rf \cdot Cf \cdot p)}$ and the final gain becomes:

$$\frac{d_{dc}}{dVout} = -\frac{(k \cdot RU + Rf) \cdot \left(1 + \frac{k \cdot RU \cdot Rf}{k \cdot RU + Rf} \cdot Cf \cdot p \right)}{RU \cdot RA \cdot (1 + Rf \cdot Cf \cdot p)} \cdot C\,\text{TR} \cdot S_{PWM} \rightarrow \text{ACgain expression}$$

Spice eases the Bode plot generation

As we have seen, many parameters affect the feedback path and greatly complicate the manual drawing of the Bode plot. Therefore, an automated solution calculating automatically the operating DC point while plotting the AC response of the whole system would be welcome. A Spice simulator is the ideal tool for this purpose. **Figure 6a** shows a simple secondary regulated SMPS made with the new member of the MC3337X family Spice model [2]. Please note that a Spice model is also available for TRANsient simulations.

The usual method consists in opening the loop at a place where ALL the feedback paths are gathered. It is obviously the PWM's output fortunately made available in the AC model. The most difficult thing in a high-gain closed-loop system is to open the loop without disturbing the operating point (e.g. at given conditions). Various methods including injection transformers have been extensively described and relevant information can be found on Venable's Web site [1]. With Spice, L1 opens the loop in AC (huge inductor value) but nicely closes it in DC, thus always keeping the good operating point.

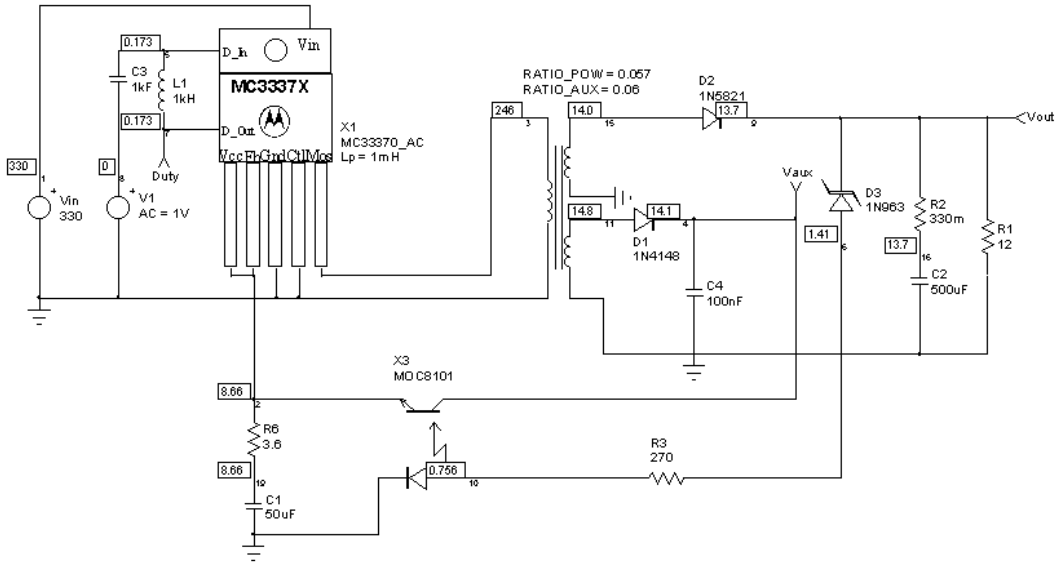

Figure 6a
A simple 12W SMPS made with an MC3337X

Node 5 will receive the AC stimulus via C3, the injection capacitor. To check the transient response, simply reduce *both* values to 1p. The Bode plot is easily generated and the DC point moves in function of the external conditions (line level, load variations etc.). Figure 6a numerical values are transferred to the schematic once the simulation has completed. Their values let you check the validity of the selected DC point. It also delivers the static duty-cycle corresponding to the operarting conditions (with AC models, 1V gives 100% *dc*, so 173mV corresponds to 17.3%). As you can see, Spice offers a tremendous help since it naturally includes the optocoupler pole but also the internal PWM 7kHz pole. The bode plot is given below (**figure 6b**).

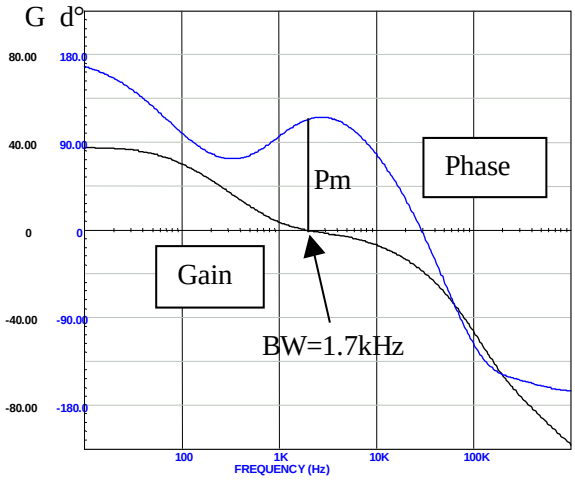

Figure 6b
The bode plot is drawn in a snap-shot

By adjusting the values of the load, mains input etc. you can immediately verify if the SMPS stays stable for instance on universal mains. If not, simply moves the location of the pole/zeroes with R6-C1 until you obtain a sufficient phase margin (Pm). Cannot be so easy, isn't it? The Spice model of the MC3337X operates in both Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM). Please note that this simulation example netlist is available to download on the MOTOROLA Web site [2] in both INTUSOFT's IsSpice4 and MICROSIM's PSpice syntax. The other goods news is that it works on the demonstration versions!

Checking the model's validity

Figure 7a depicts a multi-output SMPS using another member of the VHVICs, the new MC44608. This IC is dedicated to monitor applications where standby power is premium. It also uses a PWM shunt regulator but its FB pin is kept at 5V rather than 8.6V. The PWM modulator and the Flyback stage are identical to that of the MC3337X. Figure 7a strengthens the help of the model because Spice naturally reduces the multi-output system to a single output (the regulated one) loaded by $Rload_{eq}$ and filtered by $Cout_{eq}$. These elements simply represent the actual components you should have reflected back to the regulated winding accordingly with their squared turn ratios. You easily imagine the pain when covering load or ESR variations! In the below example we have completely opened the loop and the injection point is the FB pin via a 100Ω resistor.

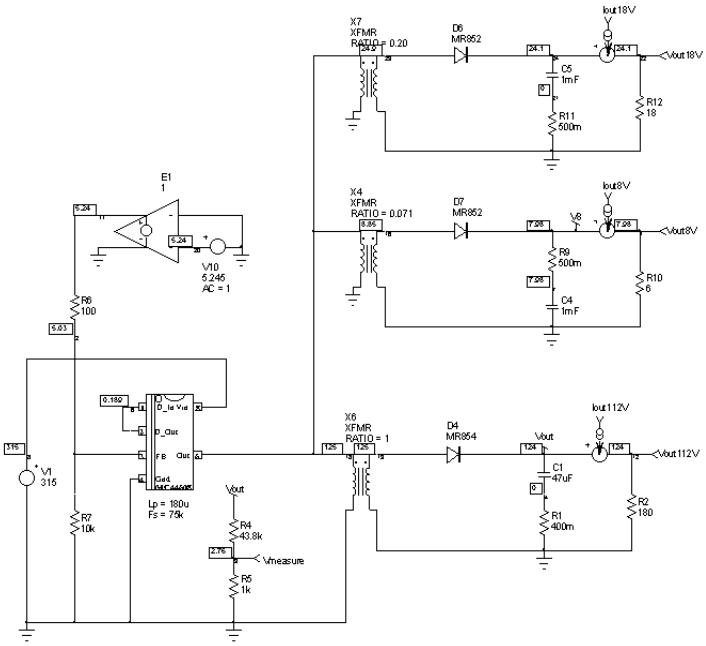

Figure 7a
The multi-output Flyback converter for TVs applications

To verify the validity of our approach, a real Bode plot has been drawn from the regulated point Vout 112V using a network analyzer. As you can see on **figures 7b** and **7c**, the results are in very good agreements with an IsSpice4 plot.

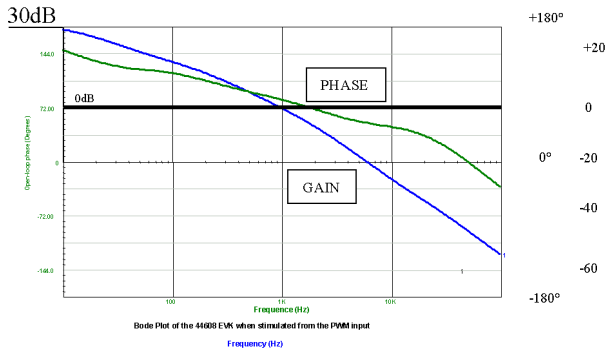

Figure 7b
IsSpice4 simulation results

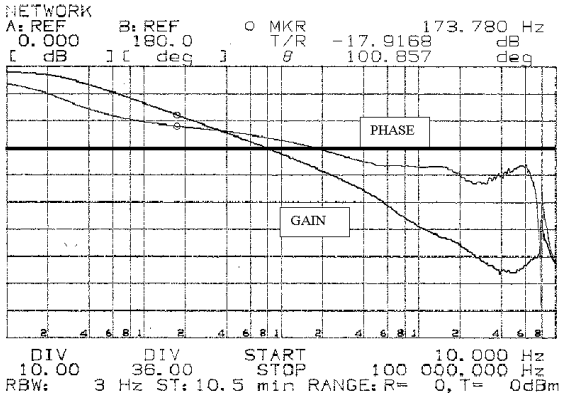

Figure 7c
A real Bode plot measurement

Conclusion

This paper shows the benefits of using a Spice model when designing Switch-Mode Power Supplies. It also details the way to introduce various poles/zeroes combinations when implementing a shunt regulator. Finally, it confirms the power of a simulation engine to help adapting the system performance to the application needs in a minimum of time and without tears!

1. http://www.venableind.com/
2. MOTOROLA's Spice models and example netlists: http://sps-mot.com/scg then click on "Device models"