FSF2100
Fairchild Power Switch (FPS™) for Zero-Voltage-Switching (ZVS) Half-Bridge Converter

Features

- According to the feedback circuit configuration, it can be used for PWM (Pulse-Width-Modulation) control or PFM (Pulse-Frequency-Modulation) control.
- Can be applied to various topologies : Asymmetric PWM half bridge converter, LLC resonant Half-bridge converter, Asymmetric PWM flyback converter, Active clamp flyback converter
- High efficiency through zero voltage switching (ZVS)
- Internal soft-start (Duty cycle controlled soft-start for PWM operation and Frequency controlled soft-start for PFM operation
- Internal SuperFET with Fast Recovery Type Body Diode (trr=120ns)
- Pulse-by-Pulse Current Limit
- Various Protection functions: Over Load Protection (OLP), Over Voltage Protection (OVP), Over Current Protection (OCP), Abnormal Over Current Protection (AOCP), Internal Thermal Shutdown (TSD)

Applications

- Power Supply for PDP TV and PDP TV
- Adapter
- PC Power

Description

The growing demand for higher power density and low profile in power converter designs has forced designers to increase switching frequencies. Operation at higher frequencies considerably reduces the size of passive components such as transformers and filters. However, switching losses have been an obstacle to high frequency operation. In order to reduce switching losses, allowing high frequency operation, resonant switching and PWM soft-switching techniques have been developed. These techniques allow the switching devices to be softly commutated. Therefore, the switching losses and noise can be dramatically reduced. FSF2100 is an integrated Pulse Width Modulation (PWM)/Pulse Frequency Modulation (PFM) controller and Super FETs specifically designed for Zero Voltage Switching (ZVS) half-bridge converters with minimal external components. The internal controller includes an oscillator, under voltage lockout, leading edge blanking (LEB), optimized high side / low side gate driver, internal soft start, temperature-compensated precise current sources for a loop compensation and self protection circuitry. Compared with discrete MOSFET and PWM controller solution, FSF2100 can reduce total cost, component count, size and weight, while simultaneously increasing efficiency, productivity, and system reliability.

Ordering Information

Part Number	Package	Operating Ambient Temperature Ranges	$R_{DS(ON)}$ (MAX)	Maximum Output Power without heat sink (Vin=350~400V) (1) (2)	Maximum Output Power with heat sink (Vin=350~400V) (1) (2)
FSF2100	9-SIP	-25 to +85	0.38Ω	200W	450W
FSF2000	9-SIP	-25 to +85	0.6Ω	160W	350W
FSF1900	9-SIP	-25 to +85	0.8Ω	140W	300W

Notes:
1. The junction temperature can limit the maximum output power.
2. Maximum practical continuous power in an open frame design at 50°C ambient.

Application Circuit Diagram

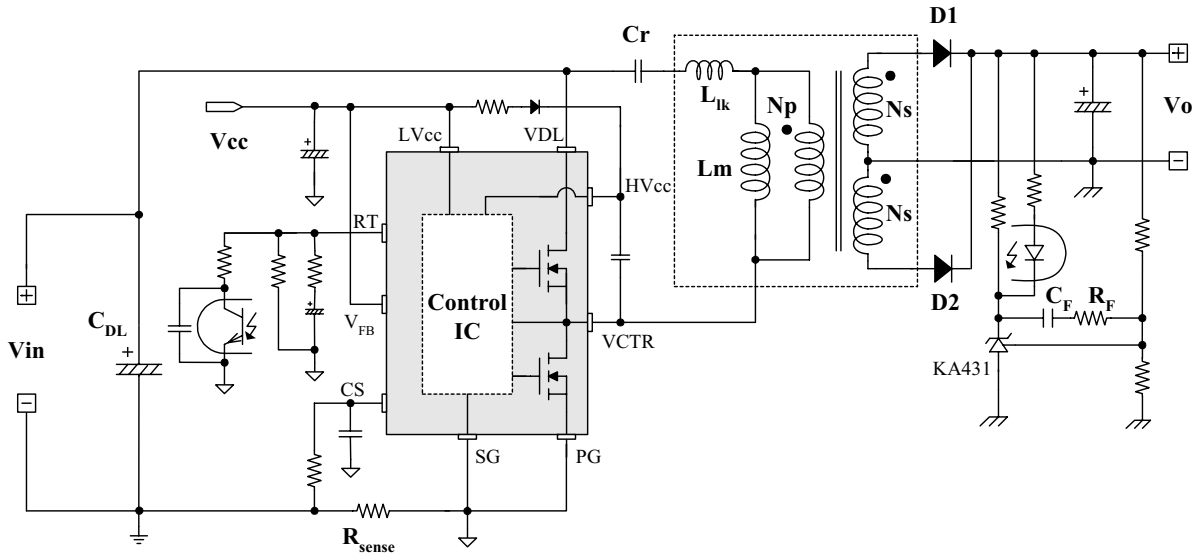


Figure 1. Typical Application Circuit (LLC Resonant Half-bridge Converter configuration)

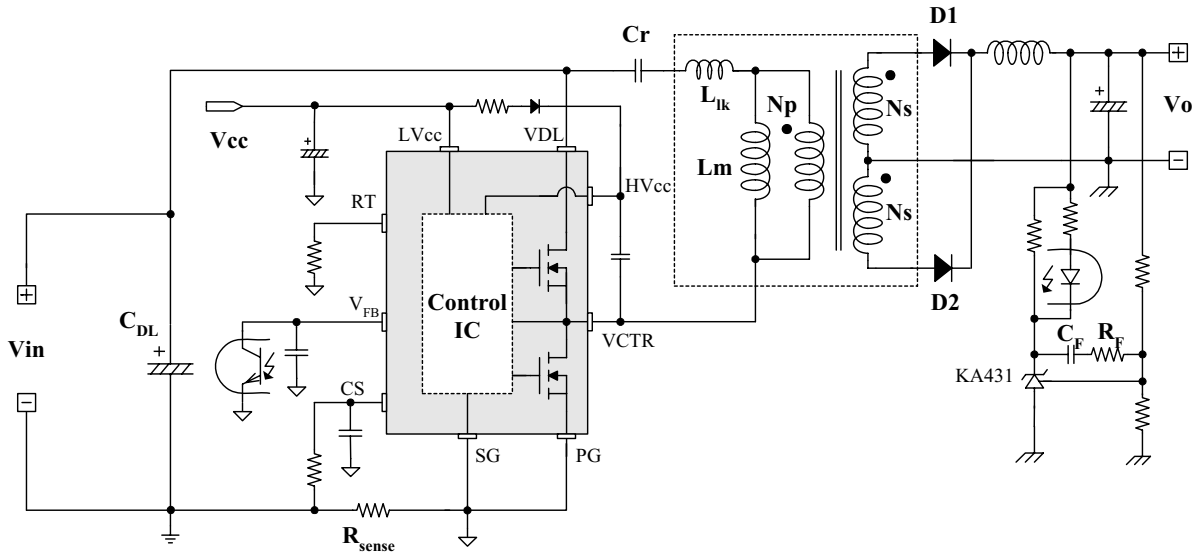


Figure 2. Typical Application Circuit (Asymmetric PWM Half-bridge converter configuration)

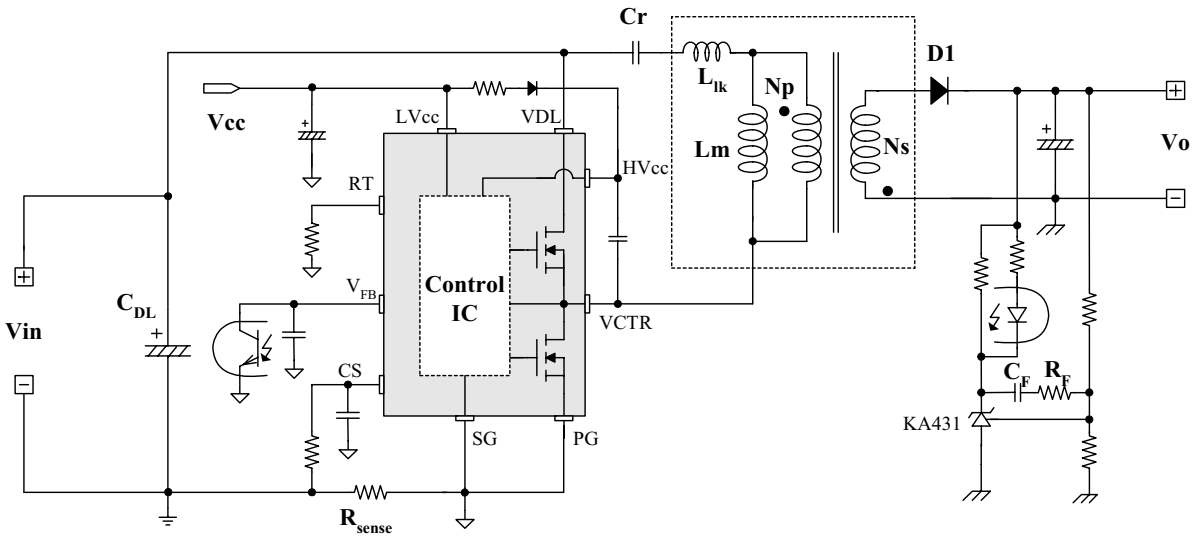


Figure 3. Typical Application Circuit (Asymmetric PWM Flyback converter configuration)

Block Diagram

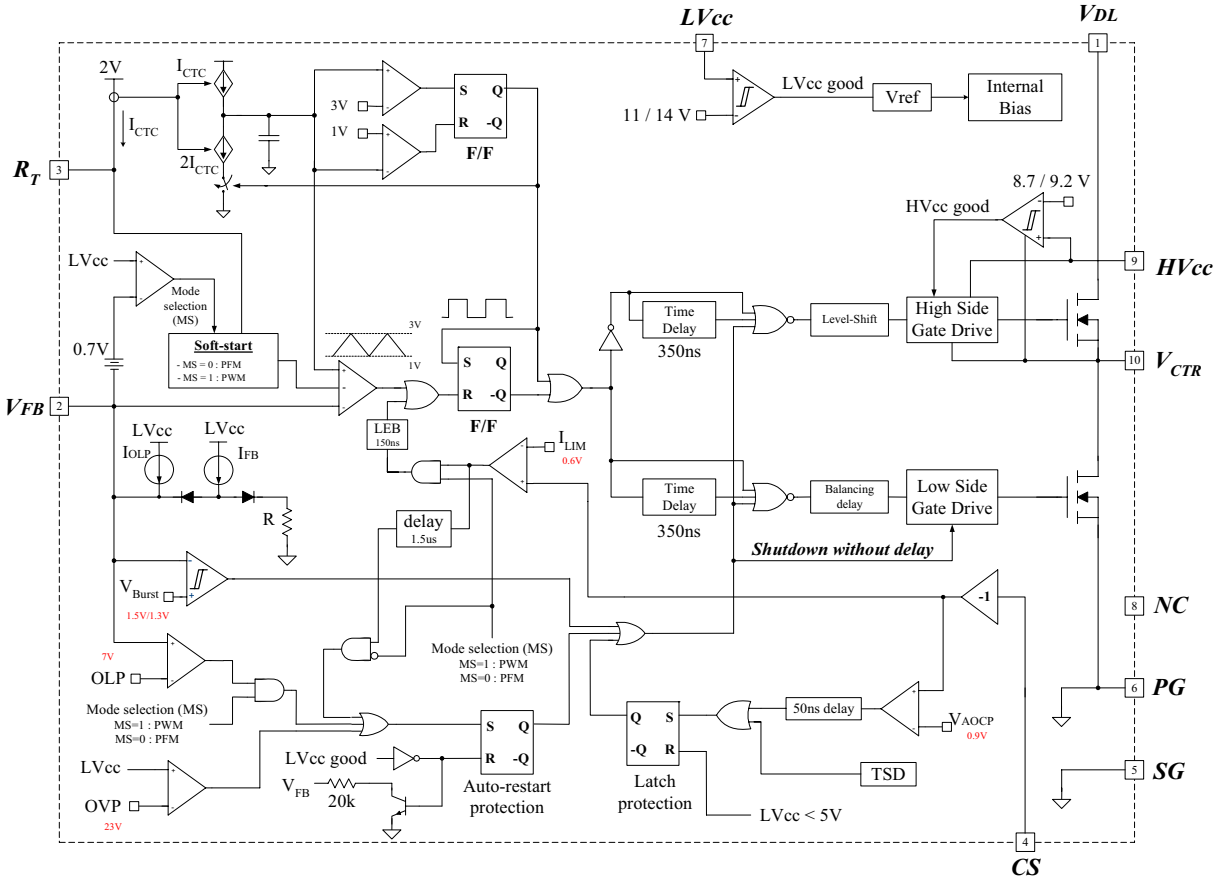


Figure 4. Internal Block Diagram

Pin Assignments

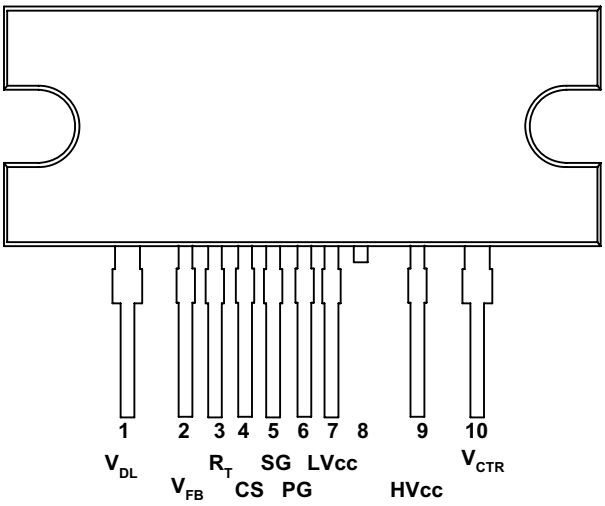


Figure 5. Package diagram

Pin Definitions

Pin No.	Pin Name	Pin Function Description
1	V_{DL}	This pin is the drain of the high side MOSFET. It is typically connected to the input DC link voltage.
2	V_{FB}	This pin is internally connected to the inverting input of the PWM comparator. The duty cycle ratio is determined by the voltage on this pin. Typically, opto-coupler is connected to this pin in PWM mode configuration. For PFM operation, this pin should be connected to the L-Vcc pin to fix the duty cycle as 50%.
3	R_T	This pin is to program the switching frequency. Typically, only a resistor is connected to this pin when used for constant frequency PWM mode. Meanwhile, opto-coupler is connected to this pin when used for frequency controlled resonant mode configuration.
4	CS	This pin is to sense the current flowing through the low side MOSFET. Typically negative voltage is applied on this pin.
5	SG	This pin is the control ground.
6	PG	This pin is the Power ground. This pin is connected to the source of the low side MOSFET
7	LVcc	This pin is the supply voltage of the control IC
8	NC	
9	HVcc	This pin is the supply voltage of the high side drive circuit IC.
10	V_{CTR}	This pin is the drain of the low side MOSFET. Typically transformer is connected to this pin.

Absolute Maximum Ratings

The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{DS}	Maximum Drain to source Voltage (V_{DL}-Vctr and Vctr-PG)	600		V
LVcc	Low Side Supply Voltage	-0.3	25	V
HVcc to Vctr	High side Vcc pin to Low side drain voltage	-0.3	25	V
HVcc	High Side Floating Supply Voltage	-0.3	625	V
V_{FB}	Feedback pin Input Voltage	-0.3	L-Vcc	V
V_{CS}	Current sense (CS) pin input voltage	-5.0	1.0	V
V_{RT}	RT pin input voltage	-0.3	5.0	V
dVctr/dt	Allowable Low side MOSFET dtain Voltage Slew Rate		50	V/ns
Pd	Total Power Dissipation			W
Tj	Operating Junction Temperature.		150	°C
Ta	Operating Ambient Temperature.	-25	85	°C
T_{STG}	Storage Temperature Range.	-55	150	°C
MOSFET section				
V_{DGR}	Drain-Gate Voltage(R_{GS}=1㏁)	600		V
V_{GS}	Gate-Source (GND) Voltage	±30		V
I_{DM}	Drain Current Pulsed	33		A
I_D	Continuous Drain Current (TC = 25℃) (TC = 100℃)	 11 7		 A A

Notes:

Electrical Characteristics

Symbol	Parameter	Test Condition	Specifications			Unit
			Min	Typ	Max	
MOSFET Section						
BVdss	Drain to Source Breakdown voltage	I_D = 250uA, Ta=25°C	600	-	-	V
		I_D = 250uA, Ta=125°C	-	650	-	V
Idss	Zero Gate Voltage Drain Current	V_{DS} = 480V, Ta=125°C	-	-	10	μA
RDS(ON)	On-State Resistance	V_{GS}=10, ID=5.5A	-	0.32	0.38	Ohm
Trr	Body diode reverse recovery time			120		ns
Supply Section						
I_{LK}	Offset Supply Leakage Current	H-Vcc = VC = 600V	-	-	50	μA
I_QHV_{CC}	Quiescent H-Vcc supply Current	(H-VCCUV+) - 0.1V	-	50	120	μA
I_QLV_{CC}	Quiescent L-Vcc supply Current	(L-VCCUV+) - 0.1V	-	100	200	μA
I_OHV_{CC}	Operating H-Vcc supply Current	F_{osc} = 100KHz, rms value	-	-	2.0	mA
I_OLV_{CC}	Operating L-Vcc supply Current	F_{osc} = 100KHz, rms value		4.0	6.0	mA
UVLO Section						
$LV_{CC}UV+$	L-Vcc supply under-voltage positive going threshold (L-Vcc start)		12.5	14	15.5	V
$LV_{CC}UV-$	L-Vcc supply under-voltage negative going threshold (L-Vcc stop)		10	11	12	V
$LV_{CC}UVH$	L-Vcc supply undervoltage Hysteresis		-	3	-	V
$HV_{CC}UV+$	H-Vcc supply under-voltage positive going threshold (H-Vcc start)		8.2	9.2	10.0	V
$HV_{CC}UV-$	H-Vcc supply under-voltage negative going threshold (H-Vcc stop)		7.6	8.7	9.6	V
$HV_{CC}UVH$	H-Vcc supply under-voltage Hysteresis		-	0.5	-	V
Current Sense Section						
V_{LIM}	Maximum Current Limit Voltage	$\Delta V/\Delta t$ = -0.1V/us	-0.66	-0.60	-0.54	V
T_{BL}	Current Limit Blanking Time (*)	$V_{CS} < V_{LIM}$, $\Delta V/\Delta t$ = 0.1V/us	-	150	-	ns
T_{DL}	Delay time from V_{LIM} to Switch off	$\Delta V/\Delta t$ = 0.1V/us	-	450	-	ns

Electrical Characteristics (Continued)

Symbol	Parameter	Test Condition	Specifications			Unit
			Min	Typ	Max	
Oscillator & Feedback Section (PWM Control)						
V_{RT}	V-I Converter Threshold	RT=30Kohm, CT=330pF	1.8	2.0	2.2	V
F_{OSC}	Output Oscillation Frequency		97	100	103	KHz
D_{MAX}	Maximum Duty Cycle	VFB = 4V,	48	50	52	%
D_{MIN}	Minimum Duty Cycle	VFB = 0V	-	-	0	%
V_{FB}^{MAX}	Maximum Duty FB Voltage	DMAX >= 48%	2.7	3.0	3.3	V
V_{FB}^{MIN}	Minimum Duty FB Voltage(*)	DMAX = 0%	0.9	1.0	1.1	V
I_{FB}	FB Source Current	VFB = 0V	400	500	600	uA
V_{BH}	Burst mode FB High Threshold Voltage		1.34	1.5	1.66	V
V_{BL}	Burst mode FB Low Threshold Voltage		1.16	1.3	1.44	V
V_{BHY}	Burst mode FB Hysteresis Voltage		0.1	0.2	0.3	V
$\mathbf{T_{SS1}}$	Soft-start time for PWM operation	Fs=100kHz	10	15	20	ms
Oscillator & Feedback Section (Variable frequency Control , RT=30KΩ , V_{FB}=LV_{CC})						
V_{RT}	V-I Converter Threshold Voltage		1.8	2.0	2.2	V
F_{OSC}	Output Oscillation Frequency		97	100	103	KHz
DC	Output Duty Cycle		48	50	52	%
F_{SS}	Soft-Start Initial Frequency	F_{SS} = 1.4 * F_{OSC}	-	140	-	KHz
T_{SS2}	Soft-Start Time for PFM operation		8	12	16	ms
I_{SC}	Initial skip cycle at startup			8		Cycles

Electrical Characteristics (Continued)

Parameter	Symbol	Test Conditions	Specifications			Unit
			Min	Typ	Max	
Protection Section						
I_{OLP}	OLP Delay Current (ASH Control Only)	V_{FB} = 5V	4	5	6	uA
V_{OLP}	OLP FB Voltage(ASH Control Only)	V_{FB} > 6.5V	6	7	8	V
V_{OVP}	L-Vcc Over Voltage Protection	L-Vcc > 21V	21	23	25	V
V_{AOCP}	AOCP Threshold Voltage	$\Delta V/\Delta t$ = -1V/us	-1.0	-0.9	-0.8	V
T_{BAO}	AOCP Blanking Time (*)	$V_{CS} < V_{OCP}$ $\Delta V/\Delta t$ = -1V/us	-	50	-	ns
V_{OCP}	OCP Threshold Voltage	$\Delta V/\Delta t$ = -1V/us V_{FB} = L_V_{CC}	-0.66	-0.60	-0.54	V
T_{BO}	OCP Blanking Time (*)	$V_{CS} < V_{OCP}$ $\Delta V/\Delta t$ = -1V/us V_{FB} = L_V_{CC}	1	1.5	2	us
T_{DA}	Delay time (Low Side) Detecting from VAOCP to Switch off	$\Delta V/\Delta t$ = -1V/us	-	250	400	ns
T_{SD}	Thermal Shutdown Temperature(*)	-	110	130	150	℃
I_{SU}	Protection Latch sustain L-Vcc Supply Current	L-Vcc = 7.5V	-	100	150	uA
V_{PRSET}	Protection Latch Reset L-Vcc Supply Voltage	-	5	-	-	V
Dead Time Control Section						
D_T	Dead Time		-	350	-	ns

Functional Description

1. Internal Oscillator: FSF-series employs current controlled oscillator as shown in Figure 6. Internally, the voltage of R_T pin is regulated at 2V and the charging/discharging current for the oscillator capacitor, C_T is determined by the current flowing out of R_T pin (I_{CTC}). When a resistor, R_{SET} is connected to this pin, the switching frequency is fixed as

$$f_s = \frac{30k\Omega}{R_{SET}} \times 100(kHz) \quad (1)$$

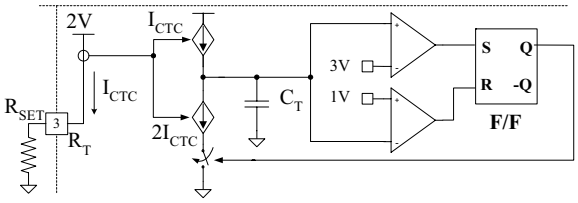


Figure 6. Current controlled oscillator

2. Operation mode selection: FSF-series is designed to operate in PWM (Pulse-Width-Modulation) mode or PFM (Pulse-Frequency-Modulation) mode according to the circuit configuration. Figure 7 shows the internal mode selection block. The operation modes are determined by the voltage difference between LV_{cc} and V_{FB}. In actual application circuit, PFM mode is selected by directly connecting the Vcc pin to the V_{FB} pin as shown in Figure 8.

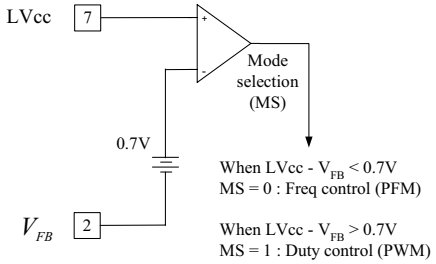


Figure 7. Mode Selection Block

2.1 PFM control: Figure 8 shows the typical circuit configuration for PFM mode, where the opto-coupler transistor is typically connected to the RT pin to control the switching frequency with a fixed duty cycle of 50%. The minimum switching frequency is determined as

$$f_{min} = \frac{30k\Omega}{R_{min}} \times 100(kHz) \quad (2)$$

Assuming the saturation voltage of opto-coupler transistor is 0.2V, the maximum switching frequency is determined as

$$f_{max} = \left(\frac{30k\Omega}{R_{min}} + \frac{27k\Omega}{R_{max}}\right) \times 100(kHz) \quad (3)$$

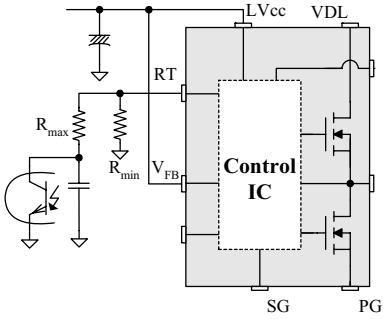


Figure 8. PFM configuration

2.2. PWM control: Figure 9 shows the typical circuit configuration for PWM mode. The opto-coupler transistor should be connected to the V_{FB} pin to control the duty cycle while a resistor is connected to the RT pin to fix the switching frequency.

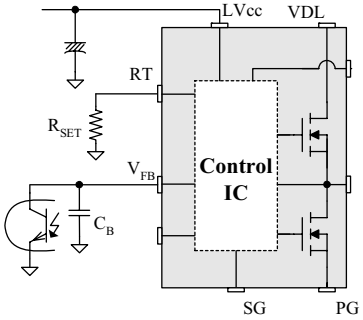


Figure 9. PWM Configuration

Figure 10 shows internal block for PWM operation. Comparing the feedback voltage with the triangular signal makes it possible to control the switching duty cycle.

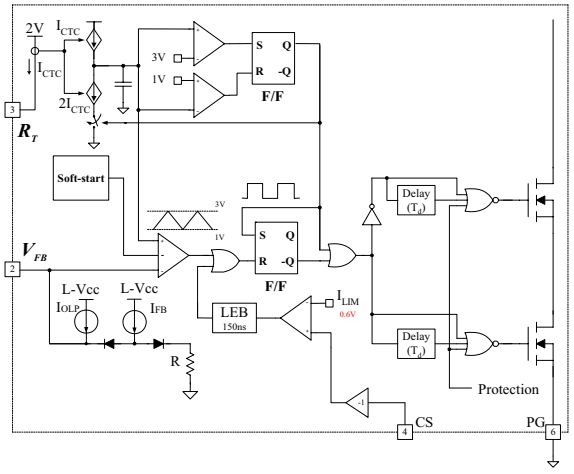


Figure 10. Internal PWM block

3. Protection Circuits: The FSF-Series has several self-protective functions such as Over Load Protection (OLP), Over Current Protection (OCP), Abnormal Over Current Protection (AOCP), Over Voltage Protection (OVP) and Thermal Shutdown (TSD). According to the selected control mode (PWM/PFM), different protections are applied as summarized in table I. Over Load Protection (OLP), Over Current Protection (OCP) and Over Voltage Protection (OVP) are auto-restart mode protection while Abnormal Over Current Protection (AOCP) and Thermal Shutdown (TSD) are latch mode protection as shown in Figure 11.

Table I Protections according to the operation mode

	PWM	PFM
Pulse-by-pulse current limit	O	X
Over Current Protection	X	O
Abnormal Over Current Protection	O	O
Over Load Protection	O	X
Over Voltage Protection	O	O
Thermal Shutdown	O	O

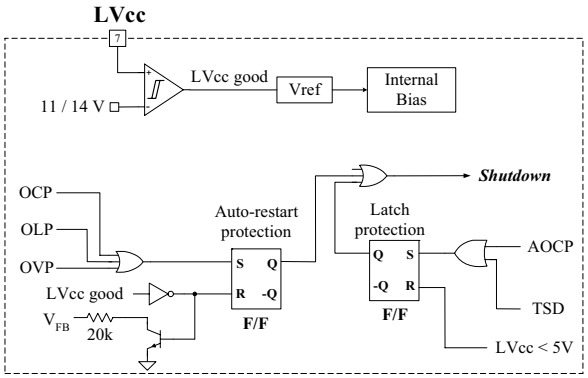


Figure 11. Protection blocks

-Auto-restart mode protection: Once the fault condition is detected, switching is terminated and the MOSFETs remain off. This causes LVcc to fall. When LVcc falls down to the under voltage lockout (UVLO) stop voltage of 11V, the protection is reset and FSF-Series consumes only startup current. Then, the LVcc capacitor is charged up, since the current supplied through the startup resistor is larger than the current that FPS consumes. When LVcc reaches the start voltage of 14V, the FSF-Series resumes its normal operation. If the fault condition is not removed, the MOSFETs remain off and LVcc drops to stop voltage again. In this manner, the auto-restart can alternately enable and disable the switching of the power MOSFETs until the fault condition is eliminated (see Figure 12).

-Latch mode protection: Once this protection is triggered, switching is terminated and the MOSFETs remain off. Then, LVcc continues charging and discharging between 11V and 14V until the AC power line is un-plugged. The latch is reset only when LVcc is discharged to 5V by un-plugging the AC power line.

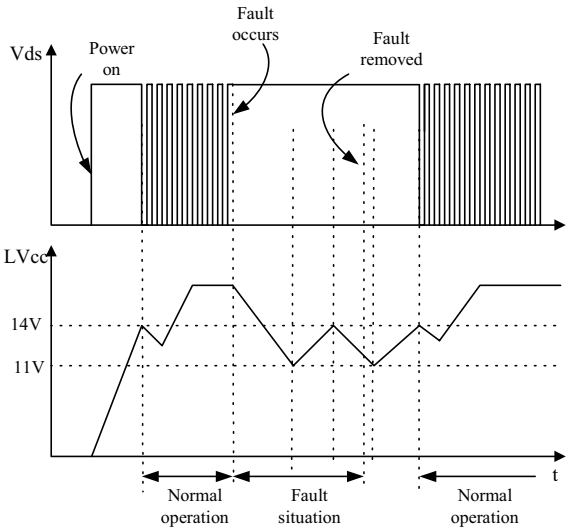


Figure 12. Auto Restart Protection Waveforms

Low side MOSFET current should be sensed for Pulse-by-pulse current limit, over current protection and abnormal over current protection. FSF-series senses drain current as a negative voltage as shown in Figure 13 and 14. Half-wave sensing allows low power dissipation in the sensing resistor while full-wave sensing has less noise in the sensing signal.

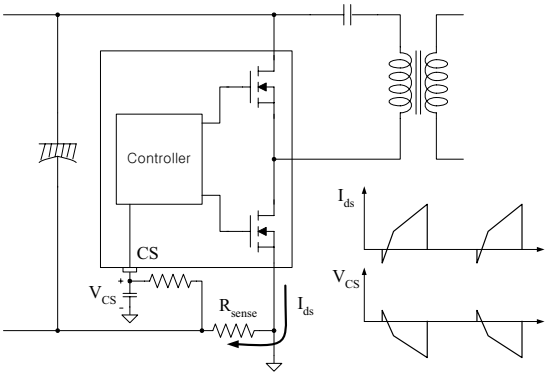


Figure 13. Half-wave sensing

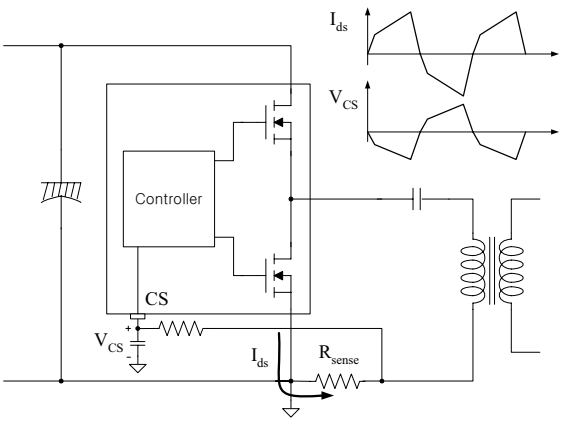


Figure 14. Full-wave sensing

3.1 Pulse-by-pulse current limit: In normal operation, the low side MOSFET is controlled to turn off when the internal triangular signal exceeds the feedback voltage. However, the low side MOSFET is forced to turn off when the current sense pin voltage drops below -0.6V. Pulse-by-pulse current limit is enabled only for PWM operation while disabled for PFM operation.

3.2 Over Current Protection (OCP): This protection is auto-restart mode and applied only for PFM operation. When the sensing pin voltage drops below -0.6V, OCP is triggered and MOSFETs remain off. This protection has a shutdown time delay of 1.5us to prevent premature shutdown during startup.

3.3 Abnormal Over Current Protection (AOCP): This protection is applied for both PFM and PWM. If the secondary rectifier diodes are shorted, large current with extremely high di/dt can flow through the MOSFET before OCP or OLP is triggered. AOCP is triggered when the sensing pin voltage drops below -0.9V without shutdown delay. This protection is lath mode and reset when LVcc is pulled down below 6V.

3.4 Overload Protection (OLP): This protection is applied only for PWM operation. Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in the normal operation, the overload protection circuit can be triggered during the load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the MOSFET is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (V_O) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 3V, D1 is blocked and the OLP current source starts to charge C_B slowly. In this condition, V_{FB} continues increasing until it reaches 7V, when the switching operation is terminated, as shown in Figure 16. The delay time for shutdown is the time required to charge C_B from 3V to 7V with 5μA as

$$T_{delay} = \frac{(7V - 3V) \times C_B}{5\mu A} \qquad (2)$$

A 30 ~ 50ms delay time is typical for most applications.

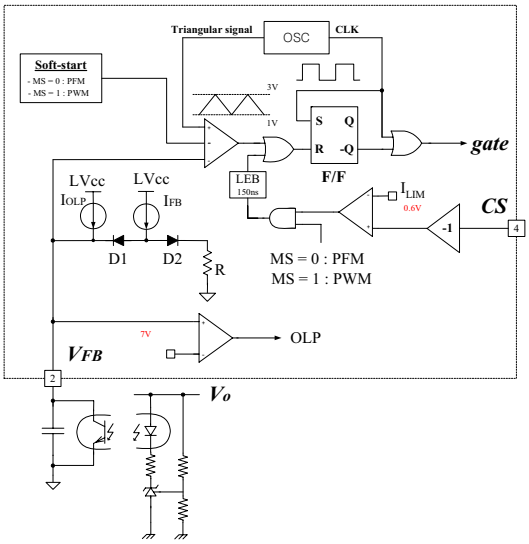


Figure 15. External Soft-start

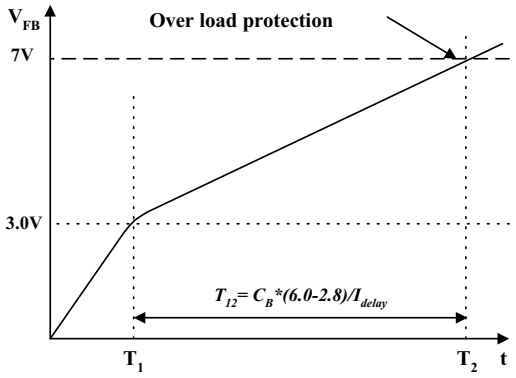


Figure 16. Overload Protection

3.5 Over-Voltage Protection (OVP): This protection is applied for both PFM and PWM. When the LVcc reaches 23V, OVP is triggered.

3.6 Thermal Shutdown (TSD): The MOSFETs and the control IC are built in one package. This makes it easy for the control IC to detect the abnormal over temperature of the MOSFET. If the temperature exceeds approximately 140°C, the thermal shutdown triggers.

4. Soft Start: The FSF-series employs two different soft-start schemes for PFM and PWM operations. For PWM operation, the duty cycle increases slowly after it starts up to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. Meanwhile, for PFM operation, the switching frequency decreases slowly after it starts up. The typical soft-start time is 15ms. When longer soft-start time is

required, external soft-start circuit for PFM operation is used as shown in Figure 16.

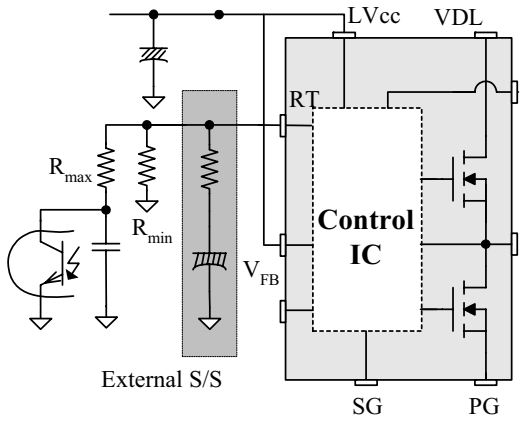


Figure 17. External Soft-start

5. Burst Operation: To minimize power dissipation in standby mode, the FSF-series enters burst-mode operation in PWM operation. As the load decreases, the feedback voltage decreases. As shown in Figure 18, the device automatically enters burst mode when the feedback voltage drops below V_{BURL} (1.3V). At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (1.5V), switching resumes. The feedback voltage then falls and the process repeats. Burst-mode operation alternately enables and disables switching of the MOSFETs thereby reducing switching loss in standby mode.

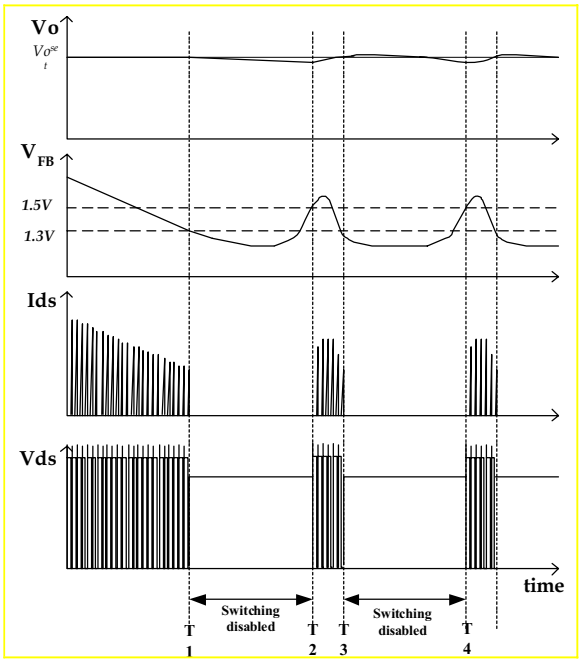


Figure 18. Burst-Mode Operation

Typical Application Circuit (LLC Resonant Half-bridge converter)

Application	FPS device	Input voltage range	Rated output power	Output voltage (Rated current)
LCD TV	FSF2100	220-280Vac	168W	24V-7A

Features

High efficiency (>94% at 400Vdc input)

Reduced EMI noise throgh zero-voltage-switching (ZVS)

Enhanced system reliability thru various protection functions

Internal soft start (12ms)

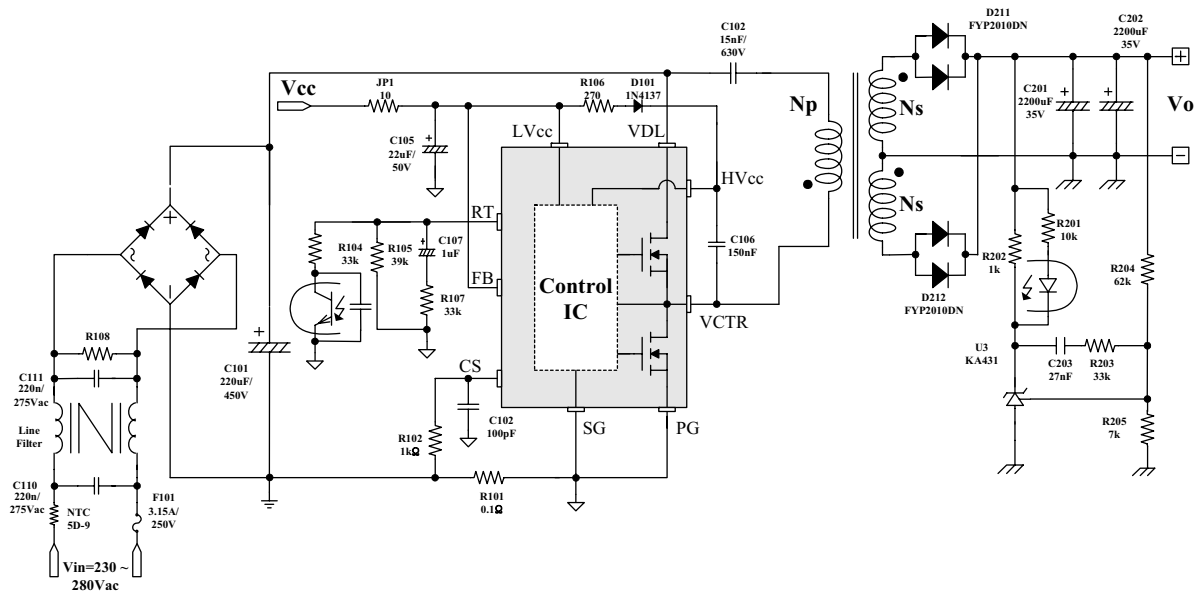
Key Design Notes

The operating frequency is determined by the current out of the RT pin. Thus, the feedback control circuit should be connected to the RT pin for LLC resonant converter operation.

To select the variable frequency soft-start for resonant operation, Vcc pin should be connected to the feedback pin.

The resonant frequency (fo) of the resonant network is designed at 100kHz.

1. Schematic

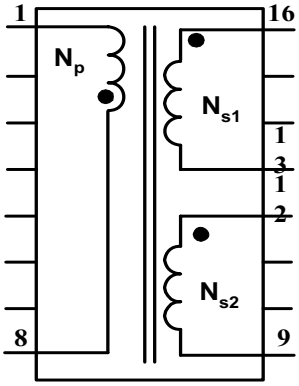


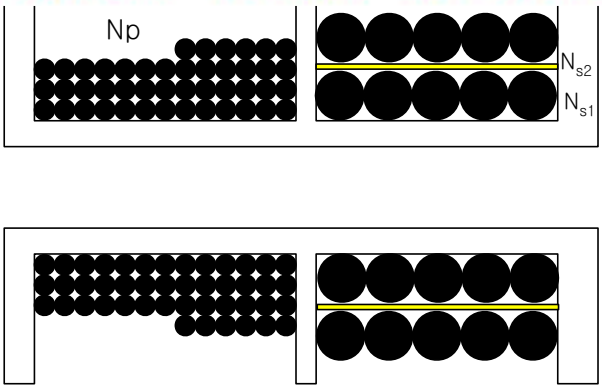
2. Transformer Schematic Diagram

Usually, LLC resonant converter requires large leakage inductance value. To obtain a large leakage inductance, sectional winding method i

- Core: EER3542 (Ae=96 mm^2)
- Bobbin: EER3542 (Horizontal)

EER3542





Winding specification

	Pin(S → F)	Wire	Turns	Winding Method
N_p	1 → 8	0.12φ×30 (Litz wire)	45	Section winding
N_{s1}	16 → 13	0.1φ×100 (Litz wire)	5	Section winding
N_{s2}	12 → 9	0.1φ×100 (Litz wire)	5	Section winding

Electrical Characteristics

	Pin	Spec.	Remark
Inductance	1 – 8	630μH ± 5%	100kHz, 1V
Leakage	1 – 8	135μH Max.	Short one of the secondary windings

Typical Application Circuit (Asymmetric PWM Half-bridge converter)

Application	FPS device	Input voltage range	Rated output power	Output voltage (Rated current)
Adaptor	FSF2100	370~410Vdc	140W	20V-7A

Features

High efficiency (>93% at 410Vdc input)

Reduced EMI noise throgh zero-voltage-switching (ZVS)

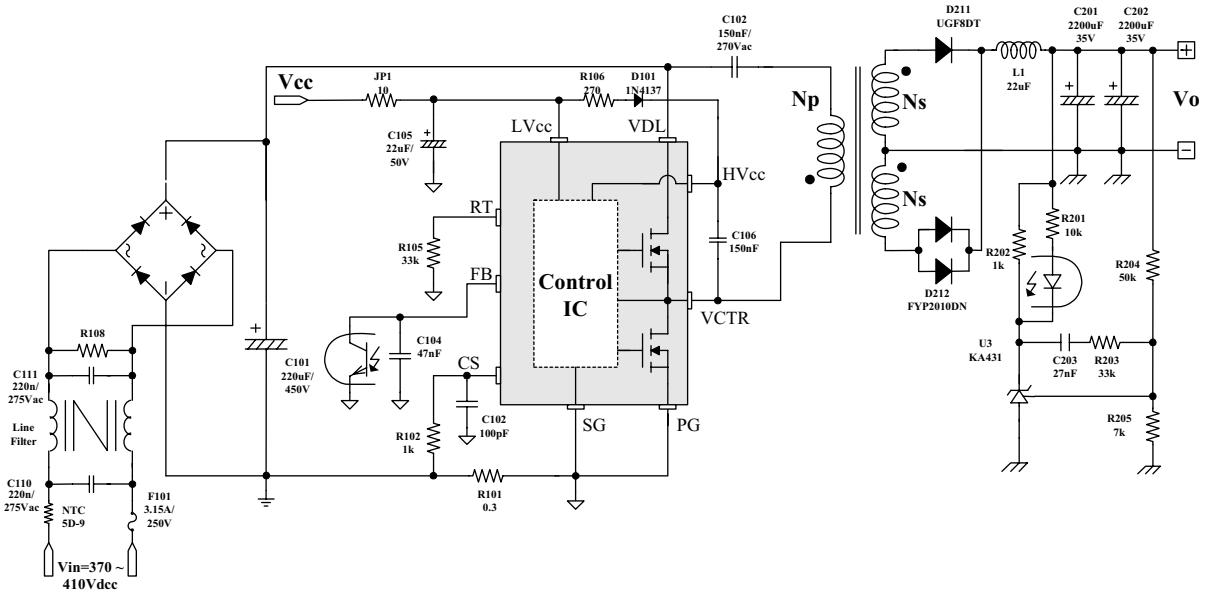
Enhanced system reliability thru various protection functions

Internal soft start (15ms)

Key Design Notes

For asymmetric PWM converter configuration, feedback control circuit is connected to the feedback pin, while only a resistor is connected to RT pin. The switching frequency is selected as 90kHz

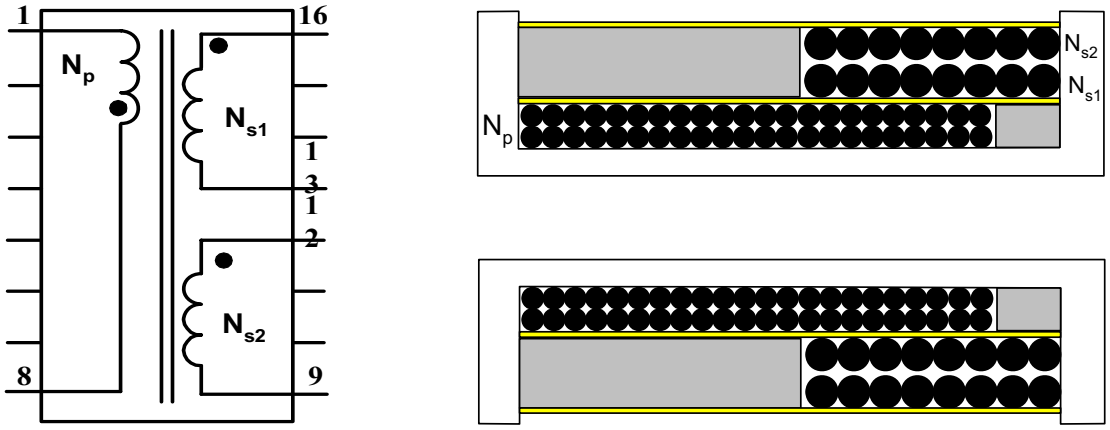
1. Schematic



2. Transformer Schematic Diagram

- Core: EER3542 (Ae=96 mm^2)
- Bobbin: EER3542 (Horizontal)

EER3542



Winding specification

	Pin(S → F)	Wire	Turns	Winding Method
N_p	1 → 8	0.12φ×30 (Litz wire)	44	Solenoid winding
N_{s1}	16 → 13	0.1φ×100 (Litz wire)	8	Solenoid winding
N_{s2}	12 → 9	0.1φ×100 (Litz wire)	8	Solenoid winding

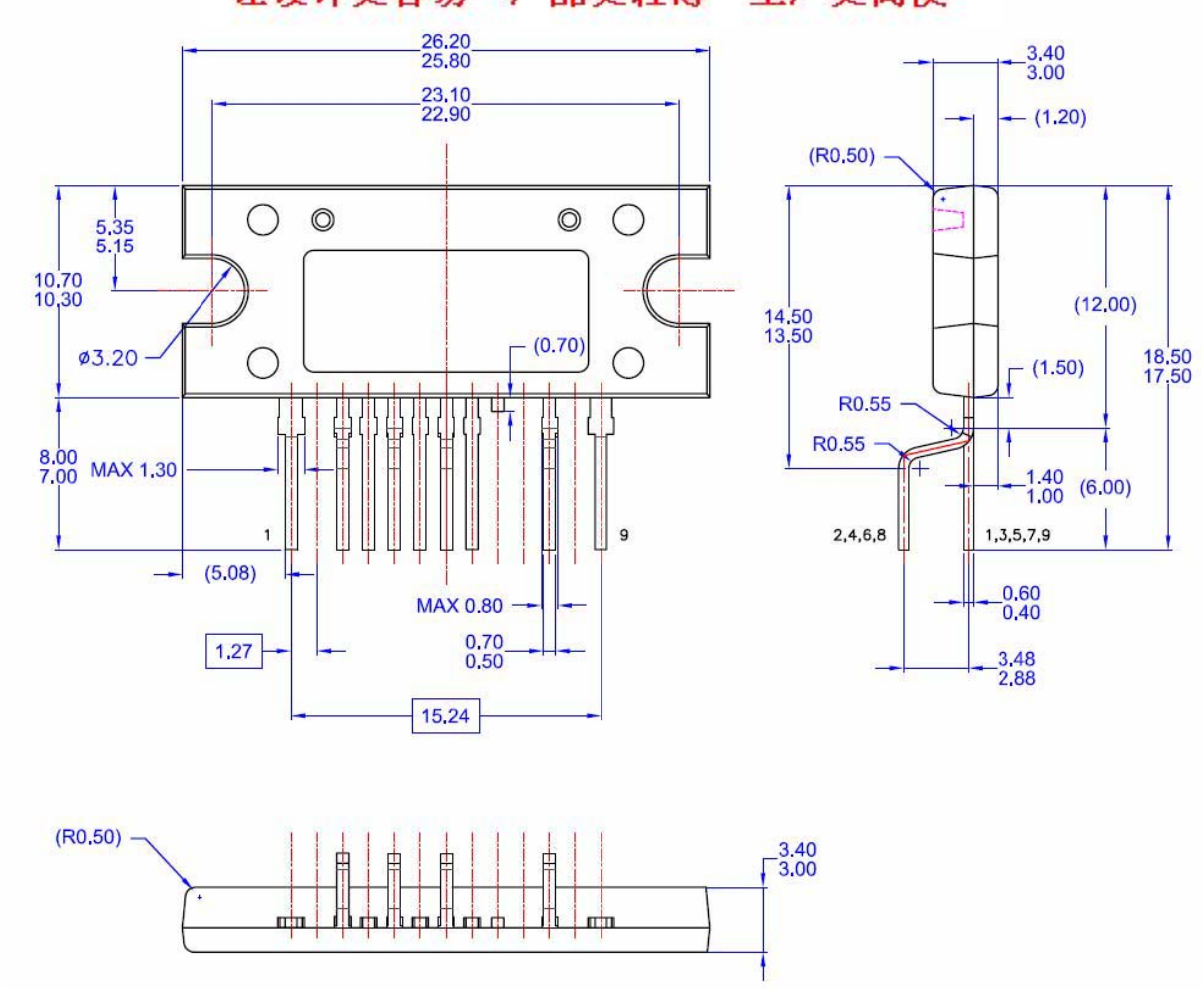
Electrical Characteristics

	Pin	Spec.	Remark
Inductance	1 – 8	580μH ± 5%	100kHz, 1V
Leakage	1 – 8	110μH Max.	Short all other pins

Physical Dimensions

Dimensions are in m

9-SIP



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