SS-11X Application Notes

Sony corporation
Semiconductor Business Unit

CONTENTS

1. System Outline

1.1. SS-11X System Outline

Table 1.1-1 SS-11X System Outline

Features	Description of functions	Detailed description
Supported CCDs	Type 1/3, Type 1/4 510H, 760H NTSC, PAL	-
System Configuration	3-chip configuration	3-chip configuration (DSP, AFE, V-Dr)
Mirror function	Video right/left inversion	Right/left inversion of the video signal output
Color-rollingless mode	Color rolling suppression	In addition to high accuracy and high-speed pull-in control, a dedicated color rolling pull-in window can be set.
Flickerless	Flicker suppress function	This function suppresses flicker by shutter fixing and AGC modulation.
MODESEL control	Automatic control of system related parameters	This function automatically changes parameters that are set differently for each clock system.
Port driver function	Easy changing of parameter setting values by external switches	This function directly operates the internal parameters from the outside using switches assigned to the DSP ports. (16 ports)
Private masking	Masking function	This function hides optional locations in the video screen. (Up to 8 masks can be output.)
Automatic blemish detection and compensation function	Pixel blemish detection and compensation	Automatically detects and corrects spot blemishes which are CCD pixel blemishes. (up to 8 points max.) (Static detection, Dynamic detection)
Internal A/D converter	10bit A/D converter	10-bit ADC realizes high performance image reproductivity.
Analog output	Composite video and Y/C component video both supported	-
Digital output	Conforms to ITU-Rec.656	-
Built-in LPF	Elimination of excess modulation components	Improved built-in LPF performance eliminates need for external LPF.

2. System Configuration

2.1. Internal System

The internal system (hereafter "INT system") is the system to which external synchronization is not applied.

The output configuration supports YCMIX analog output, YC separated analog output, and digital output.

* When using a Type 1/3 CCD, an external H-Dr voltage step-up circuit is required for H1, H2 and RG clock voltage step-up (3.3 V -> 5.0 V).

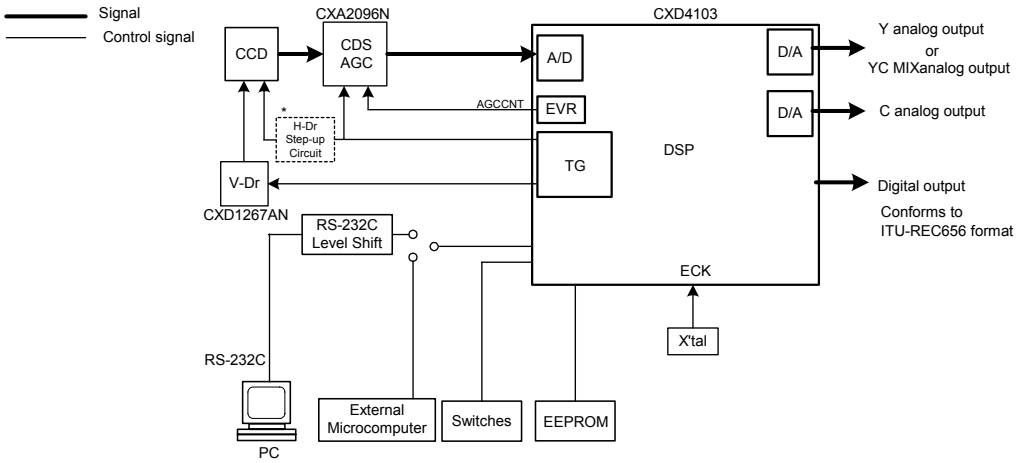


Fig 2.1-1 Internal System Block Diagram

2.2. Line Lock System

The line lock system synchronizes the camera's vertical phase to the AC power supply. The power supply frequency is 60 Hz for NTSC and 50 Hz for PAL. The line lock system can also be used to synchronize multiple cameras and as a countermeasure against color rolling.

The output configuration supports YCMIX analog output and YC separated analog output.

* When using a Type 1/3 CCD, an external H-Dr voltage step-up circuit is required for H1, H2 and RG clock voltage step-up (3.3 V -> 5.0 V).

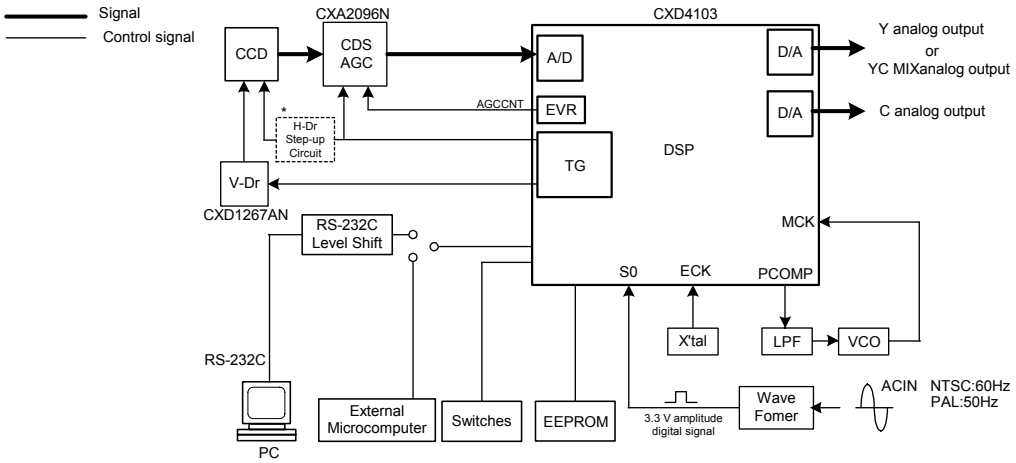


Fig 2.2-1 Line Lock System Block Diagram

The specification changed.
Please refer to "INT/LL Combined System" in "Technical Document" of the homepage for details.

2.3. Internal / Line Lock Switching System

The internal/line lock switching system (hereafter "INT/LL system") discriminates the VD input and automatically switches between the internal system and the line lock system.

The output configuration supports YCMIX analog output and YC separated analog output.

*1 When using a Type 1/3 CCD, an external H-Dr voltage step-up circuit is required for H1, H2 and RG clock voltage step-up (3.3 V -> 5.0 V).

*2 The MCK input clock is switched by the INT system and the LL system using the signals output from the port pins.

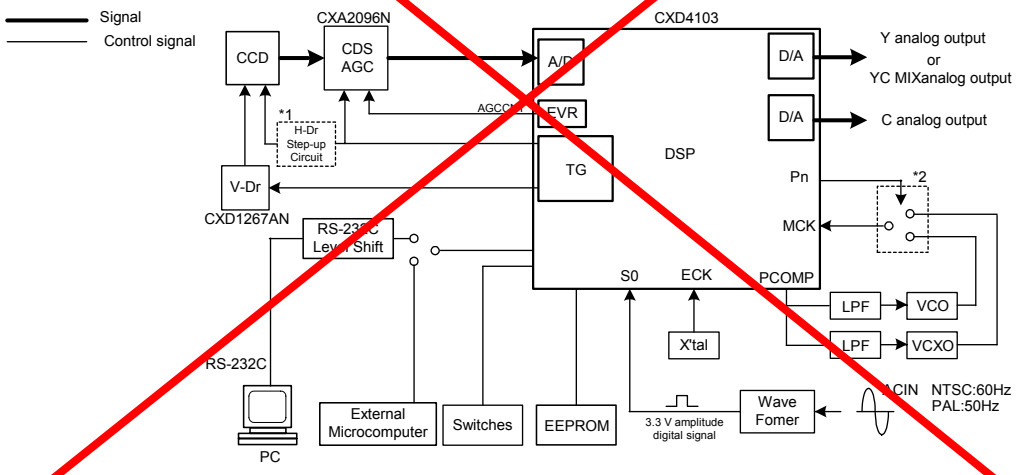


Fig 2.3-1 Internal / Line Lock Switching System Block Diagram

2.4. SS-11X System Setting Method

The setting method for each system is shown below.

See "**3.3 Oscillator Circuit Periphery**" under "**3 Peripheral Circuits**" for the circuits composition each system.

2.4.1. Internal System Settings

The setting procedure is as follows.

1. Select the crystal used for ECK input according to the TV system and the CCD type. (See "**Table 2.4-1**".)
2. Set the MODESEL value according to the crystal selected in step 1. (See"**Table 2.4-1**".)
3. Set SGMODE to 0[h]. (Selects INT mode.) (See "**Table 2.4-2**".)

Table 2.4-1 INT System Crystal and MODESEL Selection

TVsystem	Number of Pixels	MODESEL	X'tal(ECK)
NTSC	510H	0[h]	38.13986MHz
	760H	6[h]	28.63636MHz
PAL	510H	3[h]	37.87500MHz
	760H	9[h]	28.37500MHz

Table 2.4-2 INT / LL Switching Parameter

Parameter		Description
SGMODE	CAT17_Byte17_bit1	0[h] : Internal system 1[h] : Line lock system

* When the video cannot be synchronized, check the following items.

- Check again that the settings were made according to the procedure above.
- Check that the MODESEL value matches the TV standard and CCD type.
- The combination of MODESEL and the crystal used for ECK input may not be appropriate, so recheck this combination.
- Check that the ECK frequency is appropriate.

2.4.2. Line Lock System Settings

The setting procedure is as follows.

1. Set the crystal used for ECK input to 27.00000 MHz.
2. Set the MODESEL value according to the TV system and the CCD type. (See “**Table 2.4-3**”.)
3. Input a 3.3 V rectangular wave to the S0 pin. (This 3.3 V rectangular wave is obtained by converting the AC power supply using a WAVE FORMER.)
   (The 3.3 V rectangular wave frequency is 60 Hz for NTSC or 50 Hz for PAL.)
4. Configure the LPF and VCO (LC) for the external PLL according to the CCD type. (See "**3.3.2 Line Lock System** ".)
5. Set SGMODE to 1[h]. (Selects line lock system.) (See “**Table 2.4-2**”.)
6. Adjust the VCO (LC) frequency to lock the PLL. (See "**Line Lock System PLL** ".)

Table 2.4-3 LL System Crystal and MODESEL Selection Table

TV system	Number of Pixels	MODESEL	X’tal(ECK)
NTSC	510H	2[h]	27.00000MHz
	760H	8[h]	
PAL	510H	5[h]	
	760H	B[h]	

* When the video cannot be synchronized, check the following items.
- Check again that the settings were made according to the procedure above.
- Check that the MODESEL value matches the TV standard and CCD type.
- Check that the ECK frequency is appropriate.
- Check that the S0 pin input frequency is 60 Hz for NTSC or 50 Hz for PAL.
- Check the VCO and LPF circuit constants. For details, see “**3.3.2 Line Lock System**“.
- Adjust the VCO frequency and check that the PLL locks.

* In the line lock system, the sub-carrier does not lock.

Line Lock System PLL

In the line lock system, the CXD4103 internally compares the phases of the external power supply rectangular wave signal (S0 input) and the VD (MCK-VD) signal obtained by frequency-dividing MCK. These phase comparison results are output through PCOMP. The V direction PLL is configured by applying the PCOMP signal to an external LPF (for the V-PLL) and then feeding it back to VCO circuit in the MCK side.

"**Fig 2.4-1**"shows the PCOMP output waveform when a lock is applied, and "**Fig 2.4-2**"shows the PCOMP output waveform without a lock. Apply a trigger to the external power supply rectangular wave signal (S0 input) using an oscilloscope and adjust the VCO frequency while checking the PCOMP output waveform so that a lock is applied as shown in "**Fig 2.4-1**".

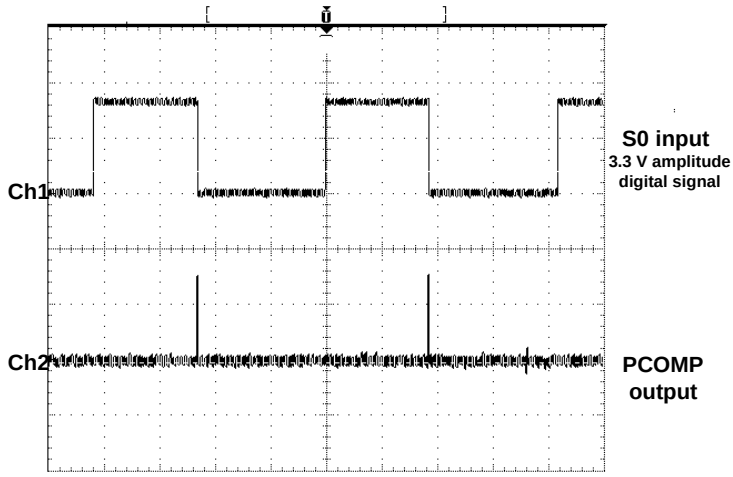


Fig 2.4-1 PCOMP Output Waveform (locked)

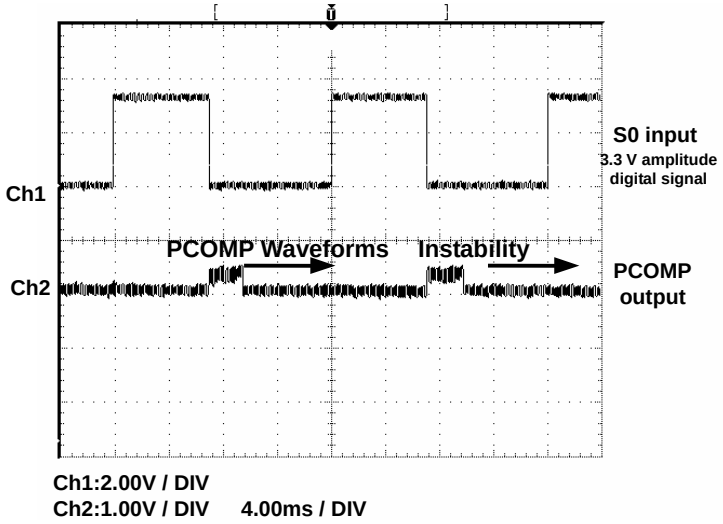


Fig 2.4-2 PCOMP Output Waveform (unlocked)

* The PCOMP signal polarity can be switched by PCMPINV (CAT7_Byte2_bit4).
* The PCOMP signal polarity can be switched by PCMPINV (CAT7_Byte2_bit4).
* Either active filtering or passive filtering can be selected for the external PLL LPF, but active filtering is recommended since it provides higher performance. (See "**3.3.1 Internal System**".)

Line Lock System Phase Adjustment

In the line lock system, the vertical phase can be adjusted by the shift function.

See ”**9.1 Port Driver Function**” for a description of the shift function setting and operation methods.

Parameters Affected by the Shift Function

The parameter values shown in “**Table 2.4-4**“ are changed by the shift function when the line lock system phase is adjusted.

Table 2.4-4 Parameters Affected by the Shift Function

Parameter		Description
CTRLSFTVL	CAT17_Byte3	Vertical phase adjustment value (LSB)
CTRLSFTVM	CAT17_Byte4_bit0-1	Vertical phase adjustment value (MSB)

Phase Adjustment Parameters when Preset

When the shift function is preset, the parameter setting values in “**Table 2.4-5**“ are reflected.

Table 2.4-5 Phase Adjustment Parameters when Preset

Parameter		Description
PRSTSFTVL	CAT17_Byte15	SFTV setting value (LSB) when preset
PRSTSFTVM	CAT17_Byte16_bit0-1	SFTV setting value (MSB) when preset

The specification changed.
Please refer to "INT/LL Combined System" in "Technical Document" of the homepage for details.

2.4.3 Internal / Line Lock Switching System Settings

The setting procedure is as follows.

1. Set the crystal used for ECK input to 27.00000 MHz.
2. Set the crystal for INT MCK input according to the TV system and the CCD type. (See "**Table 2.4-6**".)
3. Configure the external LPF and VCO (LC) for LL according to the CCD type.
   (See "**3.3.3 Internal/Line Lock Switching System** ".)
4. Set the MODESEL value according to the crystal selected in step 2. (See "**Table 2.4-6**".)
5. Assign the HVPLL parameter to the port driver (See **Pn in "Fig 2.3-1"**).
   See **"9.1 Port Driver Function"** for a description of the setting method.
6. Set ATMODEON = 1[h]. (Auto mode ON) (See "**Table 2.4-7**".)
7. The system switches to the line lock system when the 3.3 V rectangular wave obtained by passing the AC power supply through a WAVE FORMER is input to the S0 pin. When there is no input, the system operates as the internal system.
   (The 3.3 V rectangular wave frequency is 60 Hz for NTSC or 50 Hz for PAL.)
8. In line lock system mode, adjust the VCO to lock the PLL. (See "**Line Lock System PLL** ".)
9. In internal system mode, adjust the VCXO to lock the PLL.
   (See "**Internal/Line Lock Switching System (Internal System Mode) PLL**".)

Table 2.4-6 INT/LL Switching System Crystal and MODESEL Selection

TV system	Number of Pixels	MODESEL	X'tal(ECK)	X'tal(MCK)
NTSC	510H	2[h]	27.00000MHz	38.13986MHz
	760H	8[h]		28.63636MHz
PAL	510H	5[h]		37.87500MHz
	760H	B[h]		28.37500MHz

Table 2.4-7 INT/LL Switching System Setting Parameters

Parameter		Description
ATMODEON	CAT17_Byte17_bit5	0[h]: Auto mode OFF 1[h]: Auto mode ON
HVPLL	CAT7_Byte1_bit1	0[h]: Internal system 1[h]: Line lock system

* When the video cannot be synchronized, check the following items.

[When synchronization cannot be achieved in internal mode]

- Check again that the settings were made according to the procedure above.
- Check that the MODESEL value matches the TV standard and CCD type.
- Check the VCO and LPF circuit constants. See "**3.3 Oscillator Circuit Periphery**" for details.
- The combination of MODESEL and the crystal used for MCK input may not be appropriate, so recheck this combination.
- Adjust the VCXO frequency and check that the PLL locks.

[When synchronization cannot be achieved in line lock mode]

- Check again that the settings were made according to the procedure above.
- Check that the MODESEL value matches the TV standard and CCD type.
- Check the VCO and LPF circuit constants. See "**3.3 Oscillator Circuit Periphery**" for details.
- Check that the S0 pin input frequency is 60 Hz for NTSC or 50 Hz for PAL.
- Adjust the VCO frequency and check that the PLL locks.

* The sub-carrier does not lock in the INT/LL switching system.

The specification changed.
Please refer to "INT/LL Combined System" in "Technical Document" of the homepage for details.

Internal/Line Lock Switching System (Internal System Mode) PLL

When the INT/LL switching system is set to INT, the CXD4103 internally compares the phases of the ECK-HD signal obtained by frequency-dividing the ECK clock and the MCK-HD signal obtained by frequency-dividing MCK. These phase comparison results are output through PCOMP. Apply the PCOMP signal to the LPF (for H-PLL) and feed it back to the MCK side VCXO.

"**Fig 2.4-3**" shows the PCOMP output waveform when a lock is applied, and "**Fig 2.4-4**" shows the PCOMP output waveform without a lock. Apply a trigger to the ECK-HD output from S2 using an oscilloscope and adjust the VCXO frequency while viewing the PCOMP output waveform so that a lock is applied as shown in "**Fig 2.4-3**".

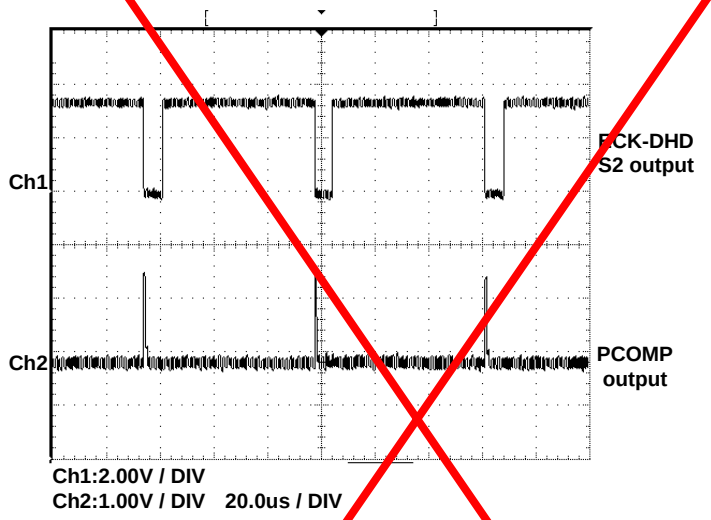


Fig 2.4-3 PCOMP Output Waveform (locked)

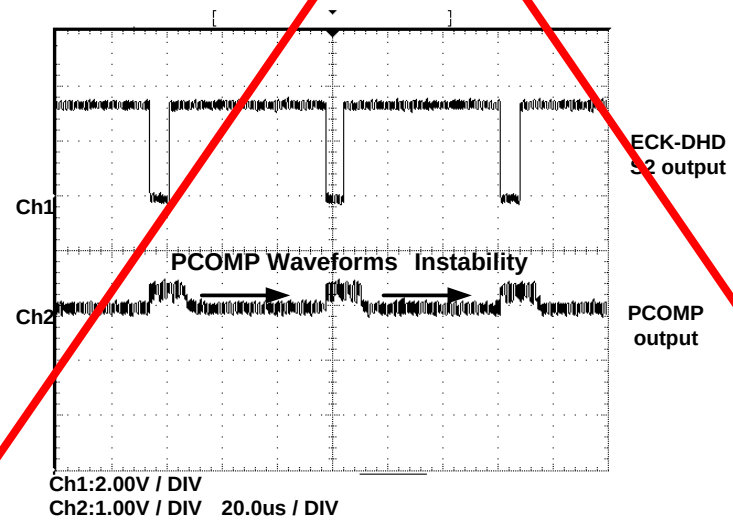


Fig 2.4-4 PCOMP Output Waveform (unlocked)

* The PCOMP signal polarity can be switched by PCMPINV (CAT7_Byte2_bit4).
* Either active filtering or passive filtering can be selected for the external PLL LPF, but active filtering is recommended since it provides higher performance. (See "**3.3.3 Internal/Line Lock Switching System**".)

2.5. ICs Comprising the System

The SS-11X is a digital signal processing system for single-panel CCD color cameras, and is comprised of the following three main LSIs.

Table 2.5-1 Main LSIs

Main LSIs	Type name	Outline	Package
DSP	CXD4103	・Luminance signal and chroma signal processing ・Built-in digital encoder ・Built-in microcontroller with AE/AWB ・Built-in AE/AWB integral circuit ・Built-in external synchronization function ・Built-in 10-bit A/D converter ・Built-in 10-bit D/A converter (Y/C 2ch) ・Built-in phase comparator ・Built-in EVR 3ch ・Built-in timing generator ・ Built-in serial communication circuit that supports RS-232C and microcomputer communication ・Built-in ITU REC656 conformity digital output function	LQFP 120 pin
CDS/AGC	CXA2096N	・Built-in correlated double sampling (CDS) circuit ・Built-in AGC circuit ・Built-in interface circuit for A/D converter	SSOP 24 pin
V-Dr	CXD1267AN	・Built-in CCD vertical clock driver ・Built-in shutter pulse driver	SSOP 20 pin

For details, see the product specifications of each LSI.

The peripheral ICs shown in "**Table 2.5-2**"are needed to configure the system in addition to the above-mentioned 3 LSIs.

Table 2.5-2 Peripheral ICs

Recommended peripheral IC	Type name (Manufacturer)	Description and applications
EEPROM	AK6480A (Asahi Kasei Microsystems) or BR9080 (ROHM)	8k-bit EEPROM (Note that other substitutions are not possible due to limitations in the communication format.)
RS-232C Transceiver	MAX3232 (or equivalent) (Maxim Integrated Products, Inc.)	PC control I/F
System Reset	PST9127 (or equivalent) (MITSUMI ELECTRIC CO., LTD.)	Vth 2.7 V

3. Peripheral Circuits

3.1. Initially Occupied Terminals

3.1.1. If No Valid Data in EEPROM

If no EEPROM is connected or there is no valid data in the EEPROM, data is read from the internal memory of the CXD4103.

At this time parameters are assigned from CXD4103 internal memory for the terminals indicated in the following table (the port driver). Thus, setup does not apply user-designated settings.

Table 3.1-1 Initially Occupied Terminals

Pin Name	Pin No	Parameter Name	Description
P0	109	AWBMODE	AWB operation mode switching
P1	110		
P2	111		
P3	112	CRLESSON	Switches anti-color rolling mode ON and OFF
P4	116	BLCOFF	Switches backlight compensation ON and OFF
P5	117	AEREF	Switches AE reference ON and OFF
P6	118	NORMFLC	Switches the flickerless function ON and OFF
P7	119	AGCMAX	Switches the AGC maximum value ON and OFF
P8	91	AEME	Switches between AE and ME
P9	92	AESHUT	Switches the electronic shutter fixed speed ON and OFF
P10	93	MIRROR	Switches MIRROR function ON and OFF
P11	94	GAMSEL	Switches the gamma parameters
P12	97	MODESEL	DSP operation mode switching
P13	98		
P14	99		
P15	100		

3.1.2. Port Driver pin Specification

During reset (XRST = L), the port driver pins (P0 – P7) become output pins. Please note that when using thise pins (P0 – P7) their value is unknown during the reset period.

Use of the port driver pins as INPUT requires a pull-up resistor.

Table 3.1-2 Port Driver pin Specification

	During reset(XRST=L)	Outside reset(XRST=H)
P0 – P7	OUTPUT (Unspecified)	INPUT
P8 – P15	INPUT	INPUT

3.2. Processing of Empty Pins

3.2.1. Processing of Empty Pins in case DAC is not used

When DAC are not used by YCMIX output (DACMODE=0[h]), digital output, etc. perform pin processing for the CXD4013 as follows.

Table 3.2-1 Processing of Empty Pins in case DAC is not used

Pin Name	Pin No	Digital output	YCMIX output
IOC	81	3.3V	
VREFC	82	GND	
IREFC	85		
IOY	90	3.3V	-
VREFY	89	GND	-
IREFY	86		

3.2.2. Processing of Empty Pins in case Internal EVR is not used

When Internal EVR is not used, perform pin processing for the CXD4103 as follows.

However, supply power to the power supply pin AVD even when there are channels that do not use the internal EVR.

Table 3.2-2 Processing of Empty Pins in case Internal EVR is not used

Pin Name	Pin No	When Internal EVR is not used
EVR0	74	Connects with GND through 0.1µF capacitor.
EVR1	76	
EVR2	77	

See the Application Circuit of each system for the processing of other open pins.

3.3. Oscillator Circuit Periphery

In the SS-11X, the oscillator circuit configuration differs for the internal system, the line lock system, and the internal/line lock switching system. The circuit configurations for each oscillator circuit periphery are shown below. Select the configuration to match the system used.

The circuit constants are scheduled to be verified in operation using a Sony evaluation board equipped with the crystal oscillator shown in "**Table 3.3-2**" . No guarantee of performance is implied for different board layouts, component selection, or temperature characteristics.

Table 3.3-1 Crystal Oscillator Used on the Evaluation Board

Component name	Manufacturer	Model	Frequency	Load capacitance
Crystal oscillator	RIVER ELETEC CORPORATION	HC-49/U03	28.63636MHz	12pF
			28.37500MHz	
			38.13986MHz	
			37.87500MHz	
			27.00000MHz	

3.3.1. Internal System

The internal system can operate by connecting only a single clock (crystal).

The frequency of the crystal oscillator connected to the ECK pin of the CXD4103 differs according to the CCD type and the TV system. "**Table 3.3-2**" shows the connected oscillator frequencies.

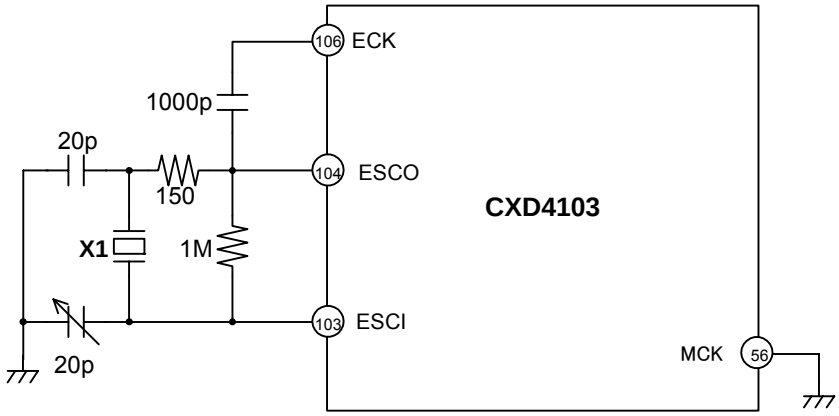


Fig 3.3-1 Example Internal System Oscillator Circuit

Table 3.3-2 Crystal Oscillator Frequency

Number of Pixels	TV system	X1
510H	NTSC	38.13986MHz
	PAL	37.87500MHz
760H	NTSC	28.63636MHz
	PAL	28.37500MHz

3.3.2. Line Lock System

The line lock system is a 2-clock system that inputs different frequencies to the ECK pin and the MCK pin.

Input a crystal oscillated clock to the ECK pin, and a LC (VCO) oscillated clock to the MCK pin. Use a crystal oscillator frequency of 27.00000 MHz. The LC (VCO) constant differs according to the CCD type. See "**Table 3.3-3**".

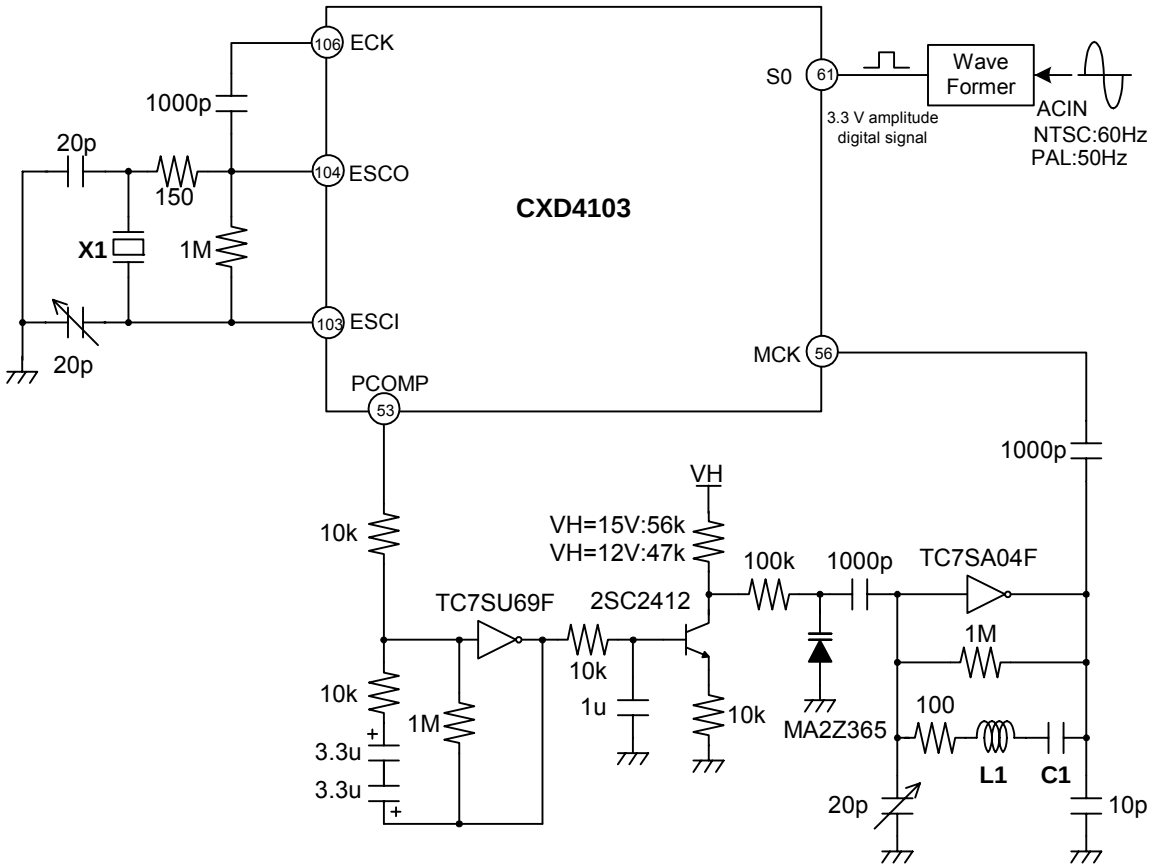


Fig 3.3-2 Example Line Lock System Oscillator Circuit

* See the "**WAVE FORMER Application Circuit**" for the WAVE FORMER.

Table 3.3-3 Crystal Oscillator Frequency and LC Oscillator Circuit Constants

Number of Pixels	TV system	X1	L1	C1
510H	NTSC	27.00000MHz	1.5uH	18pF
	PAL			
760H	NTSC		3.3uH	12pF
	PAL			

The specification changed.
Please refer to "INT/LL Combined System" in "Technical Document" of the homepage for details.

3.3.3. Internal/Line Lock Switching System

The internal/line lock switching system is a 2-clock system that inputs different frequencies to the ECK pin and the MCK pin, and switches the MCK input clock in internal mode and line lock mode.

Pn (port driver pin) outputs low in internal system mode, and high in line lock system mode. The MCK input clock is switched between crystal oscillation and LC oscillation using this signal.

Use 27.00000 MHz as the crystal oscillator frequency input to ECK. The crystal oscillator frequency input to MCK and the LC (VCO) constant differ according to the CCD type. See "**Table 3.3-4**".

Please substitute P8 to P15 for Pn. Refer to "**3.1.2 Port Driver pin Specification**" for more information.

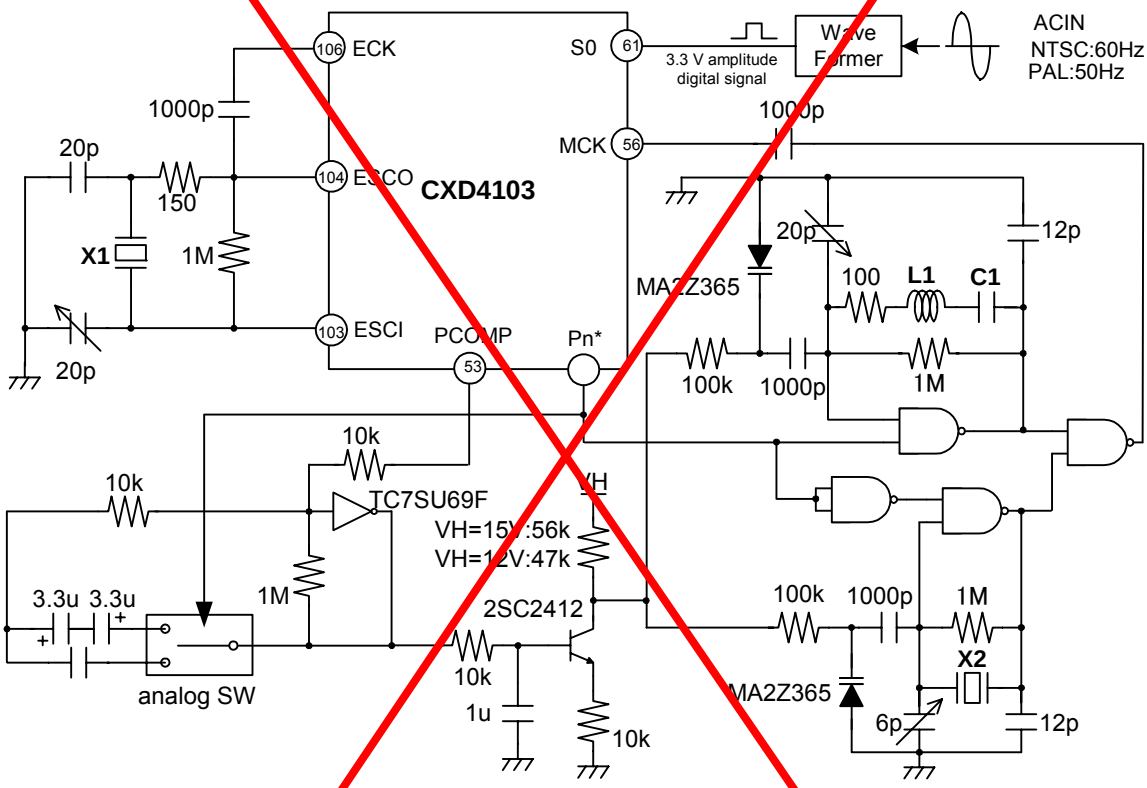


Fig 3.3-3 Internal/Line Lock Switching System Oscillator Circuit

* See the "**WAVE FORMER Application Circuit**" for the WAVE FORMER.

Table 3.3-4 Crystal Oscillator Frequency and LC Oscillator Circuit Constant

Number of Pixels	TV system	X1	X2	L1	C1
510H	NTSC	27.00000MHz	38.13986MHz	1.5uH	18pF
	PAL		37.87500MHz		
760H	NTSC		28.63636MHz	3.3uH	12pF
	PAL		28.37500MHz		

WAVE FORMER Application Circuit

The application circuit for the external rectangular wave pulse shaping circuit (WAVE FORMER) needed to configure the line lock system and the internal/line lock switching system is shown below.

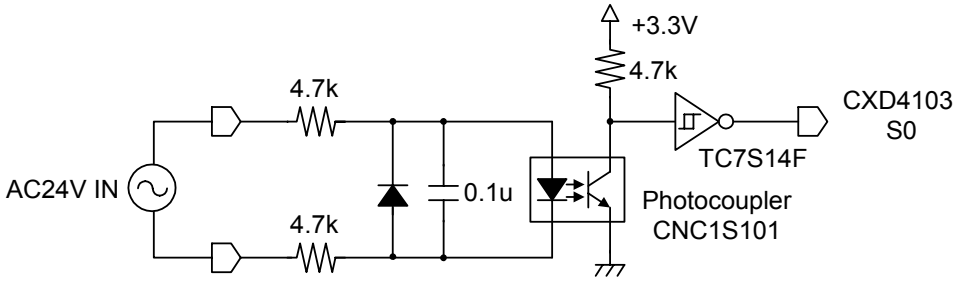


Fig 3.3-4 WAVE FORMER

3.4. Output Circuit Periphery

The SS-11X supports analog output (YCMIX output, YC separated output) and digital output. The peripheral circuits for each output configuration are shown below.

The circuit constants are scheduled to be verified in operation using a Sony evaluation board. No guarantee of performance is implied for different board layouts, component selection, or temperature characteristics.

3.4.1. Analog Output (YCMIX Output, YC Separated Output)

The analog signal output system can be selected from YCMIX output and YC separated output by the parameter in "**Table 3.4-1**". Select the parameter setting that matches the circuit configuration.

Table 3.4-1 DAC Mode Selection Method

Parameter		Setting value	Description
DACMODE	CAT1_Byte3_bit2	0[h]	YCMIX output
		1[h]	YC separated output

Circuit Configuration during YC Separated Output (DACMODE = 1[h])

During YC separated output, the Y and C signals from the CXD4103 internal DAC are output from the IOY pin and the IOC pin, respectively."**Fig 3.4-1**" shows the circuit example during YC separated output.

The signal level output from the IOY and IOC pins is decided depending on the voltage input to the VREFY and VREFC pins. So input the desired voltage value and adjust the level. The voltage value is input and adjusted so that Sync and Burst may become prescribed signal levels because of the following Video output of Video AMP of latter part.

When AMP of +12dB is connected like "**Fig 3.4-1**", the input voltage to the VREFY and VREFC pins becomes about 1 to 1.1V (As for the input voltage value, it is scheduled to evaluate it in the future). The input voltage is 1.1V (typ) in the CXD4103 internal DAC specifications. So use a configuration with an amplification circuit (Video AMP of +12dB) in the final stage. Do not use Video AMP other than +12dB. Note that the operation in that case cannot be guaranteed because the VREF input voltage might become outside the specification range of the CXD4103 internal DAC.

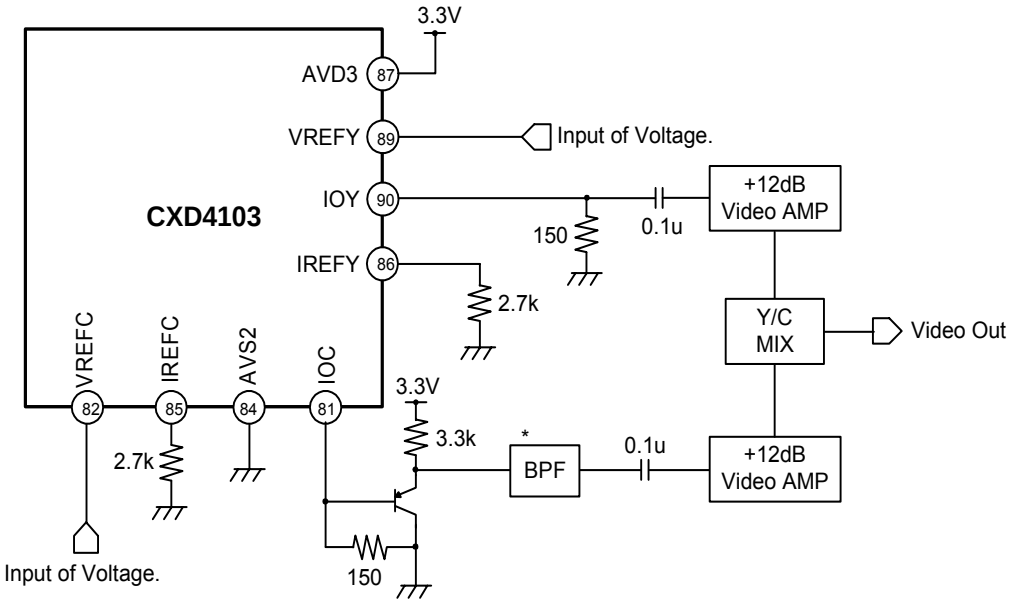


Fig 3.4-1 Example Circuit During YC Separated Output

* See "**3.4.3BPF Circuit Example**" for a description of the BPF.

Circuit Configuration during YCMIX Output (DACMODE = 0[h])

During YCMIX output, the Y and C signals are mixed inside the CXD4103 and output from the IOY pin. The IOC pin is not used at this time. "**Fig 3.4-2**"shows the circuit example during YCMIX output.

The BPF is not connected during YCMIX output, so note that the digital component of the sub-carrier signal cannot be completely eliminated. The signal level output from the IOY pin is decided depending on the voltage input to the VREFY pin. So input the desired voltage value and adjust the level. The voltage value is input and adjusted so that Sync and Burst may become prescribed signal levels because of the following Video output of Video AMP of latter part.

When AMP of +12dB is connected like "**Fig 3.4-2**", the input voltage to the VREFY pin becomes about 1 to 1.1V (As for the input voltage value, it is scheduled to evaluate it in the future). The input voltage is 1.1V (typ) in the CXD4103 internal DAC specifications. So use a configuration with an amplification circuit (Video AMP of +12dB) in the final stage. Do not use Video AMP other than +12dB. Note that the operation in that case cannot be guaranteed because the VREF input voltage might become outside the specification range of the CXD4103 internal DAC.

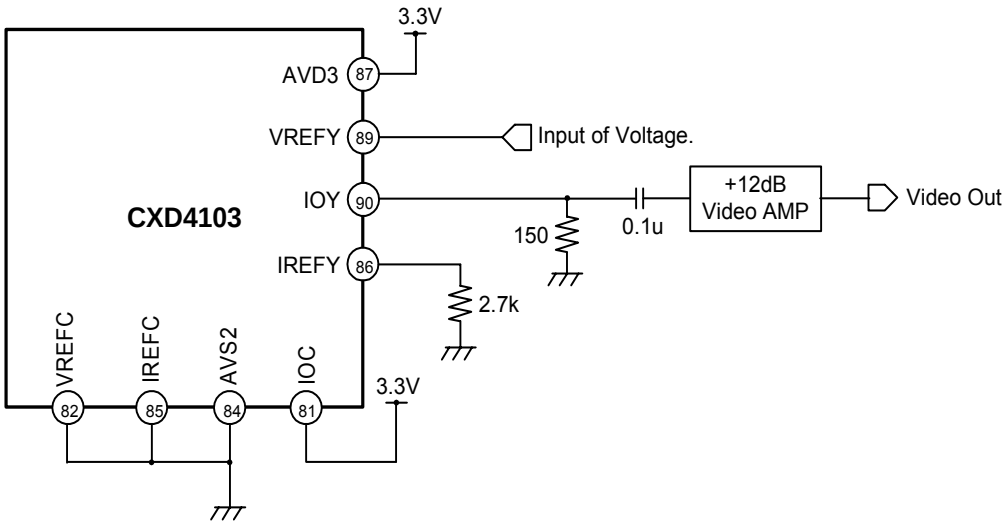


Fig 3.4-2 Example Circuit During YCMIX Output

3.4.2. Digital Output

Digital output can be used by the internal system. See ”**10.1.2 Parameters for Setting Digital Output**” for the parameter setting method. Note that analog output is also possible when performing digital output in the internal system.

The circuit configuration below shows the case when using only the digital output.

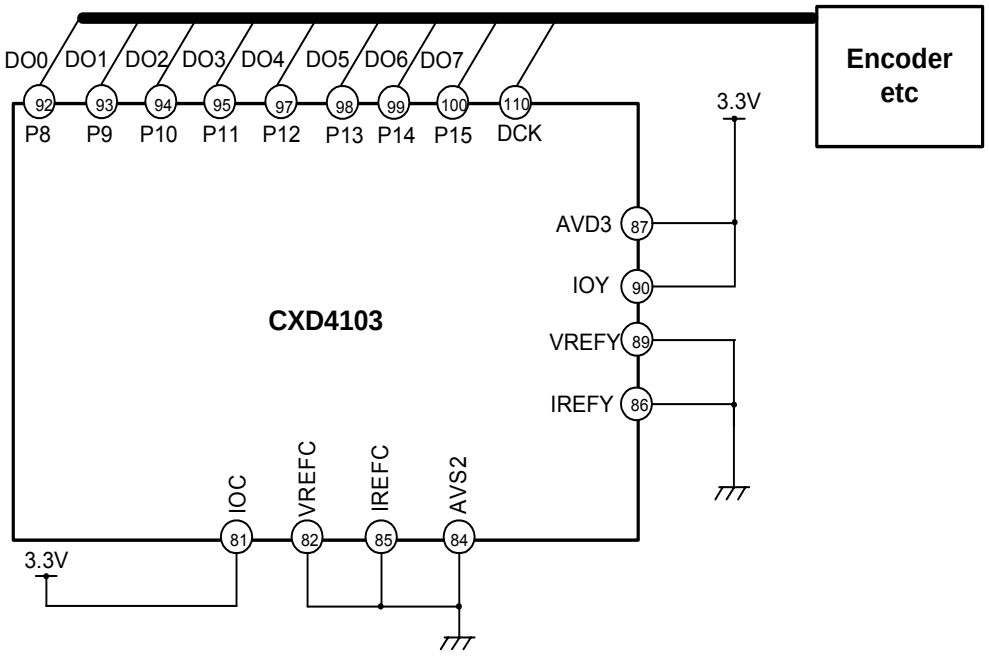


Fig 3.4-3 Example Circuit During Digital Output (when not using analog output)

3.4.3. BPF Circuit Example

When outputting an analog chroma signal from the IOC pin, add a band pass filter circuit to ensure that signal components other than the sub-carrier component are eliminated. This filter also shapes the sub-carrier signal, in which digital components remain, into a sine wave. An example of BPF Circuit is shown in ”**Fig 3.4-4**”.

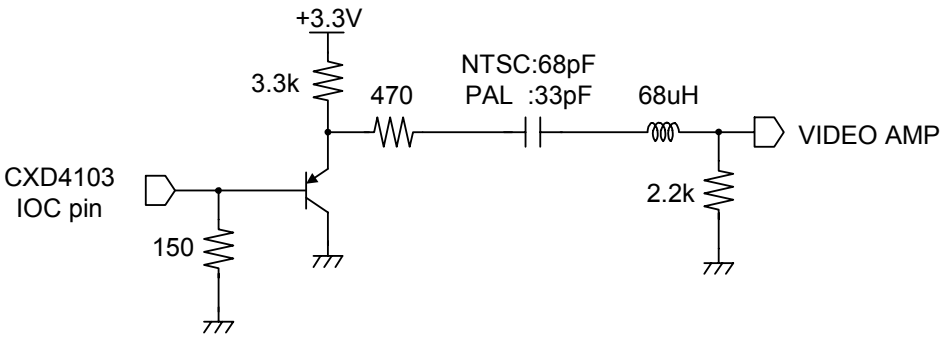


Fig 3.4-4 Example BPF Circuit

Example BPF Characteristics

The following graph shows example characteristics measured using the BPF formed in ”**Fig 3.4-4**”.

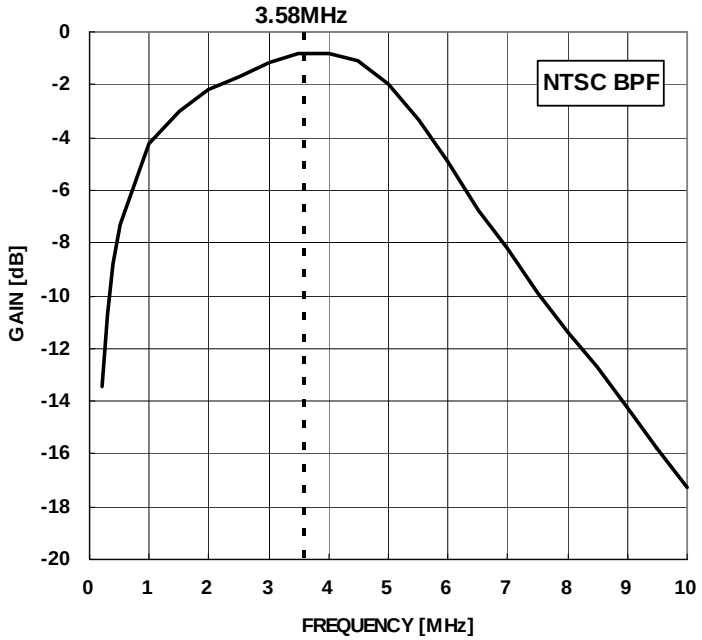


Fig 3.4-5 Example BPF Frequency Characteristics (NTSC)

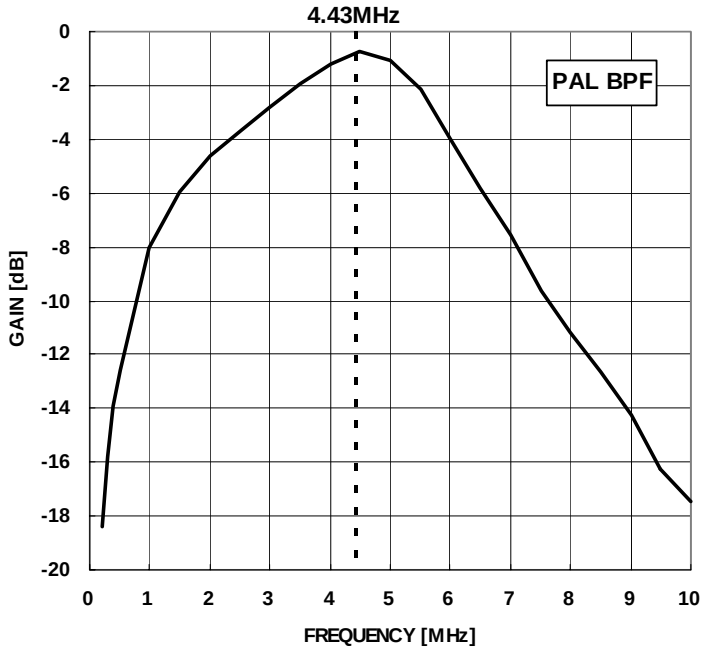


Fig 3.4-6 Example BPF Frequency Characteristics (PAL)

3.5. H-Driver Voltage Step-up Circuit

When using a Type 1/3 CCD with the SS-11X, the H1, H2 and RG clocks must be converted from 3.3 V -> 5 V.

"**Fig 3.5-1**" shows the circuit configuration. Each specification of the following product (SN74LVC1G14 made by TI) or the H level input voltage to power-supply voltage (5.0V), the response speed, and the drive ability must use equal to the following product goods for the pressure circuit.

In this example of the circuit, the H1, H2, and RG clocks are reversed from CXD4103 and it outputs it. Normal rotation/reversing clocks can be switched according to the parameter. (See "**Table 3.5-1**".)

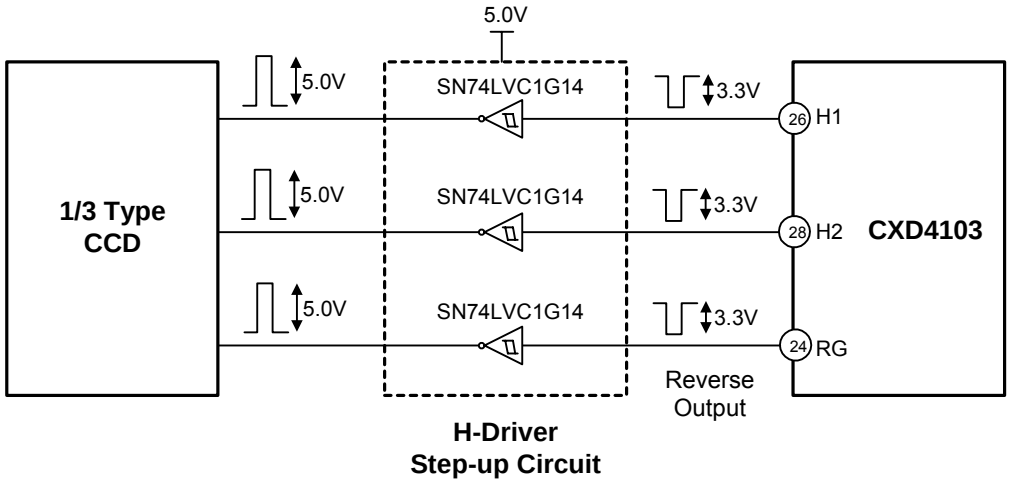


Fig 3.5-1 H-Driver Voltage Step-up Circuit Block Diagram

Table 3.5-1 Clocks Reversed Parameters

Parameter		Description	
H1INV	CAT6_Byte19_bit0	Reverse Control of H1 clock.	0[h] : Normal 1[h] : Reverse
H2INV	CAT6_Byte19_bit1	Reverse Control of H2 clock.	0[h] : Normal 1[h] : Reverse
RGINV	CAT6_Byte19_bit2	Reverse Control of RG clock.	0[h] : Normal 1[h] : Reverse

3.6. Communication Circuit

In SS-11X, the parameter is set according to the RS-232C communication and external microcomputer communication. "**Fig 3.6-1**" **and** "**Fig 3.6-2**" show the peripheral circuits for each type of communication.

3.6.1. RS-232C Communication

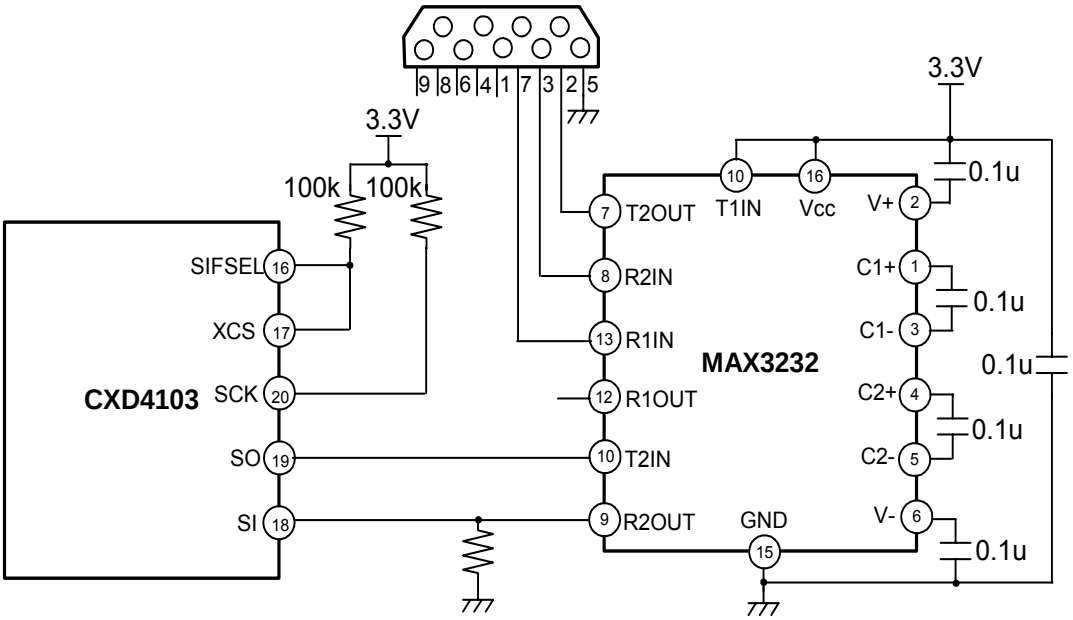


Fig 3.6-1 Example RS-232C Communication Circuit

3.6.2. External Microcomputer Communication

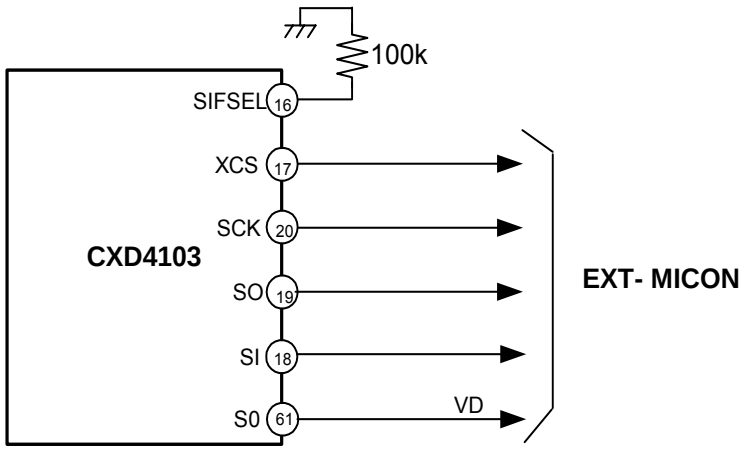


Fig 3.6-2 Example External Microcomputer Communication Circuit

3.7. Reset Circuit

3.7.1. Outline

This circuit performs system reset to enable stable operation when the CXD4103 and peripheral ICs start up after power is supplied. However, problems may also be caused by a transient power supply.

For a reliable way to avoid such problems, add a circuit that meets the following conditions (Timing chart).

The only IC used by the SS-11X system that requires reset is the CXD4103.

3.7.2. Example Reset Circuit and Timing Chart

The sample reset circuit is shown in ”**Fig 3.7-1**”.

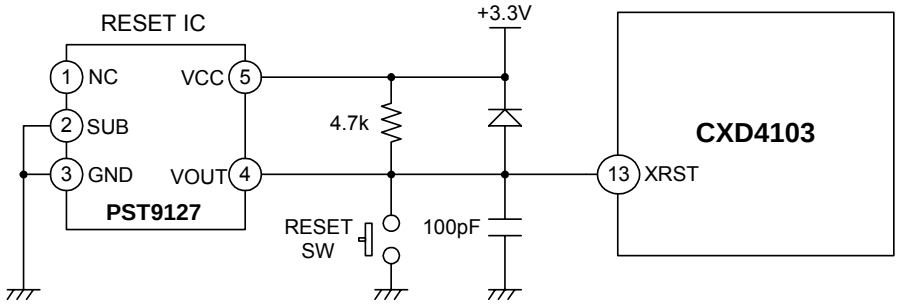


Fig 3.7-1 Example Reset Circuit

If the 3.3V voltage supply surges to exceed 2.7V after power is supplied or other events, set the CXD4103 XRST terminal to Low (at least 500ns) and be sure to reset it. Additionally, if the 3.3V power supply falls under 2.7V, set the XRST terminal to Low and be sure to reset it.

* The guaranteed voltage for DSP operation is 3.0 to 3.6V. For details refer to the product specifications.

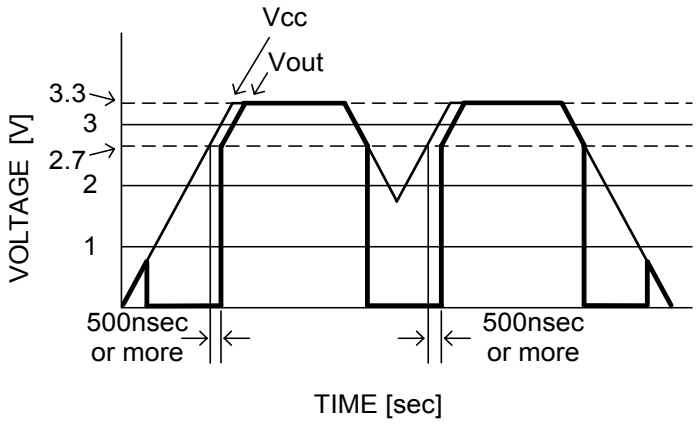


Fig 3.7-2 Timing Chart

3.8. EEPROM Connection

3.8.1. Outline

The SS-11X can connect an EEPROM for data storage. The AK6480A made by Asahi Kasei Microsystems or the BR9080 made by ROHM are recommended as the EEPROM due to limitations in the communication format.

3.8.2. Connection Method

When connecting the CXD4103 and the EEPROM, make the pin connections as shown in "**Fig 3.8-1**".

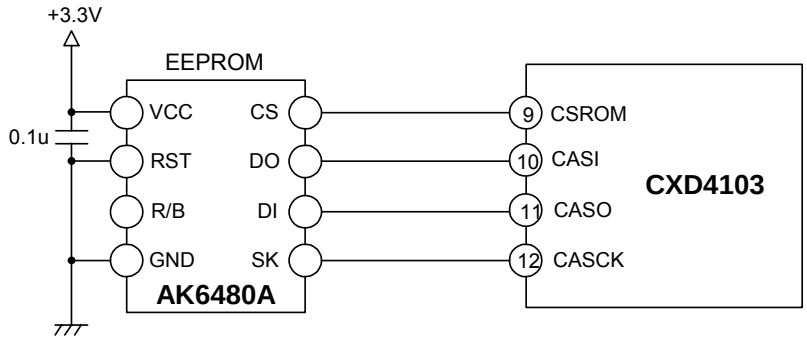


Fig 3.8-1 EEPROM Connections

3.9. Internal EVR

3.9.1. Outline

The CXD4103 has a built-in 3-channel, 8-bit D/A converter (EVR), and can output nearly linear voltage from approximately 0 V to 3.3 V.

3.9.2. Internal EVR Initial Settings

The internal EVR initial settings are as shown in "**Table 3.9-1**".

The CXD4103 performs AGC gain control for the CXA2096N, so EVR0 should be connected to AGCCNT (Pin 14) of the CXA2096N.

The 2 channels of EVR1 and EVR2 can be set optionally by the user.

Table 3.9-1 Internal EVR Initial Settings

ch	Parameter		Control details
EVR0	AGCCNT	CAT8_Byte3	AGC gain control
EVR1	EVR1CNT	CAT8_Byte4	User setting
EVR2	EVR2CNT	CAT8_Byte5	User setting

3.9.3. Internal EVR User Setting Method

When using EVR0 with a user setting, AE control must be stopped. Make the parameter setting shown in "**Table 3.9-2**", then set AGCCNT to an optional value.

Mechanical iris control can also be performed by the CXD4103. (For details, see "**9.6.7 AE Mechanical Iris Mode**".) However, when using EVR1 with a user setting, make the parameter setting shown in "**Table 3.9-2**" in the same manner as for EVR0, then set EVR1CNT to an optional value.

EVR2 can be used with a user setting by setting an optional value in EVR2CNT, even if other parameters are not set.

Table 3.9-2 Parameters of Note when Using the Internal EVR with User Settings

ch	Parameter		Setting value
EVR0	AEHOLD	CAT12_Byte5_bit2	1[h]:AE HOLD
EVR1	MIRIS	CAT14_Byte1_bit1	0[h]: Mechanical iris control OFF
EVR2	Other parameter settings are not required.		

When not using the internal EVR, set the parameters for each channel to optional values or set each channel to standby as shown in "**Table 3.9-3**" . When set to standby, the status of each channel is undetermined.

Table 3.9-3 When not Using the Internal EVR

ch	Parameter		Setting value
EVR0	EVR0STB	CAT8_Byte2_bit5	0[h]: EVR control 1[h]: EVR standby
EVR1	EVR1STB	CAT8_Byte2_bit6	
EVR2	EVR2STB	CAT8_Byte2_bit7	

3.10. Optical Filters

3.10.1. Outline

When a subject with a high spatial frequency is shot using a color camera containing CCDs, a moire effect (false signal) occurs. In order to suppress this moire effect (false signal), always use an optical low pass filter (optical LPF) which matches the type of CCD being used.

Sony uses optical LPF with a three-layer configuration for all function and performance evaluations. Note that Sony does not support two-layer configurations or optical LPF lacking an IR cut filter.

"**Fig 3.10-1**" shows example spectral characteristics of optical filter used by Sony, and "**Fig 3.10-2**" shows the pixel separation pattern (8 points) specification using optical LPF for your reference.

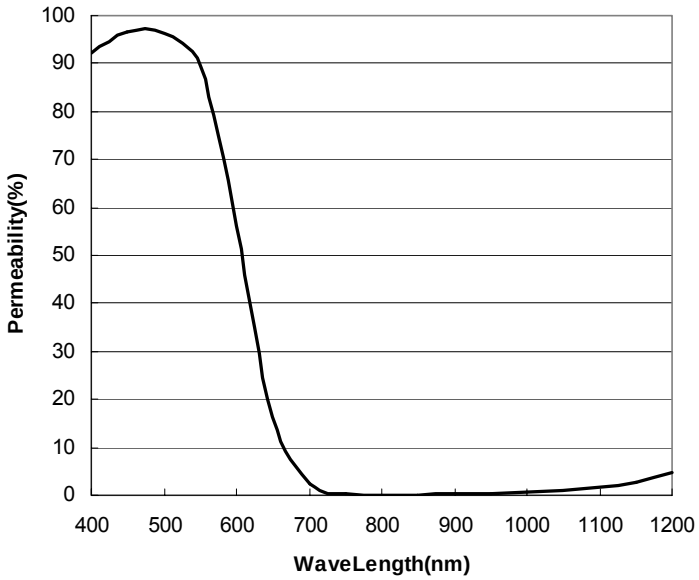


Fig 3.10-1 Example Spectral Characteristics of Sony Optical Filter

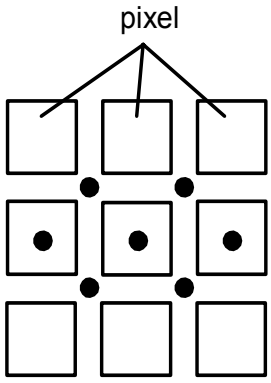


Fig 3.10-2 Pixel Separation Pattern (8 Points) Specification Using Optical LPF

4.Parameter Control Priority Ranking

4.1. Parameter Priority Ranking

In the SS-11X, the priority ranking in which parameter values are reflected differs according to the category. This priority ranking is as follows.

(PORT Driver) > Priority1 > Priority2

< Details >

1. When set by the port driver, changes to the Priority1 and Priority2 parameters are ignored.
2. Priority1 changes have priority for parameters that are subject to both Priority1 and Priority2 control.
   (See "**11.1 Parameters Subject to Priority1 Control**" for a list of parameters subject to Priority1 control.)

* When DSP's CPU processing is not necessary, using an external microcomputer or other, set the Priority1 parameters to OFF and perform adjustments using the Priority2 parameters.

4.1.1. Communication Categories

Table 4.1-1 Priority1 Communication Category Table

Control subject	Category number	Category name	Description
Priority1	CAT12	CPU	Built-in controller setting and operation mode setting
	CAT13	PICT2	Image quality setting parameters 2
	CAT14	AE2	AE related parameters 2
	CAT15	AWB2	AWB related parameters 2
	CAT16	OPDWND2	OPD window related parameters 2
	CAT17	EXTSYNC2	External synchronization parameters related 2
	CAT18	FIX	-
	CAT19	PREADJ	Adustment related parameters.
	CAT20	PORT	Port driver setting parameters
	CAT21	BLMDET2	Blemish detection related parameters.
	CAT23	SOUT2	Serial output setting parameters 2

Table 4.1-2 Priority2 Communication Category Table

Control subject	Category number	Category name	Description
Priority2	CAT1	SYSCON	Parameters related to general system settings
	CAT2	PICT1	Image quality setting parameters 1
	CAT3	FIX	-
	CAT4	AWB1	AWB related parameters 2.
	CAT5	OPDWND1	Nondisclosure parameters
	CAT6	TG	High-speed phase adjustment related parameters
	CAT7	EXTSYNC1	External synchronization parameters related 1
	CAT8	FEADJ(EVRI)	Internal EVR related parameters.
	CAT9	MASKPG	Mask function and PG related parameters.
	CAT10	DIF	Digital interface related parameters.
	CAT11	BLMDETS1	Blemish detection related parameters.
	CAT22	SOUT1	Serial output setting parameters 1
	CAT24	TEST	Test related parameters

4.2. EEPROM Write Method

The write procedure below describes the case when using the SS-11X control software, but the procedure is the same when using an external microcomputer. See ”**7.1.4 Communication Format**” for the external microcomputer command specifications.

4.2.1. Initial Write (EEPROM Empty State)

1. Set CPUHOLD (CAT12_Byte5_bit0) to 1[h].
2. All the parameters (all categories) send and write.
   EEPROM sub menu -> Select procedure "Send -> Write -> Read" -> All Select button -> Start button
   * Verify is executed immediately after EEPROM write, so check that the write results are OK. When write cannot be performed or when the results are NG, check whether trouble occurred in the EEPROM or the serial communication connection (CASI, CASO, CASCK, and CSROM).
3. Restart [Power-on reset (XRST: L -> H)].
4. Set CPUHOLD (CAT12_Byte5_bit0) to 0[h].
5. Send and write only CAT12.
   EEPROM sub menu -> Select procedure "Send -> Write -> Read" -> Click CAT12 -> Start button
6. Restart [Power-on reset (XRST: L -> H)].

< Note >

In the initial process the CXD4103 reads the EEPROM addresses 000[h] and 001[h] and compares the "Chip ID code". When the read data does not match the specified value, the EEPROM is recognized as invalid. Be sure to perform “**4.2.1 Initial Write (EEPROM Empty State)**” to write the "Chip ID code".

Initial process: The process performed by the DSP internal CPU the first time the power is turned on.
Restart: Power-on reset (XRST: L -> H)

4.2.2. Second and Subsequent Write (when not including CAT12)

1. Set CPUHOLD (CAT12_Byte5_bit0) to 1[h].
2. Select, send and write the arbitrary categories.
   EEPROM sub menu -> Select procedure "Send -> Write -> Read" -> Select arbitrary CAT -> Start button
3. Restart [Power-on reset (XRST: L -> H)].

< Note when writing CAT12 >

When CAT12 is written in the EEPROM with CPUHOLD = 1[h], CPU control stops. To use CPU control, set CPUHOLD = 0[h] and write only CAT12 in the EEPROM again.

When the verify process is performed with CPUHOLD = 0[h], the values of parameters subject to Priority1 control may differ from the EEPROM values. When performing control using an external microcomputer, CPU control must be stopped. See" **11.1 Parameters Subject to Priority1 Control**" for the parameters subject to Priority1 control.

< Procedure for note when writing CAT12 >

1. Set CPUHOLD (CAT12_Byte5_bit0) to 1[h].
2. Select, send and write the arbitrary categories including CAT12.
3. Set CPUHOLD (CAT12_Byte5_bit0) to 0[h].
4. Send and write only CAT12.
5. Restart [Power-on reset (XRST: L -> H)].

5. Power Source

5.1. Supply Voltage

The SS-11X requires the following five types of power sources as the system power supplies.

+1.8V : I/O power source for CXD4103R

+3.3V : Analog power source for CXD4103R
I/O power source for CXD4103R
Power source for CXA2096N
Power source for EEPROM
Power source for RS-232C transceiver

+5.0V : Power source of voltage regulator for 1/3 CCD image sensor

VH : Power source for CXD1267AN (V driver, shutter driver, Vsub generation circuit)
Power source for CCD image sensor

VL : Power source for CXD1267AN (V driver, shutter driver)
Protective transistor input voltage for CCD image sensor

*Care should be taken as the voltage (**+5.0V, VH, VL)** differs according to the drive specification of the CCD image sensor.

5.1.1. Supply Voltage Accuracy

When using SS-11X, the power source tolerances are as follows.

Table 5.1-1 SS-11X Supply Voltage and Accuracy

Supply Voltage (typ.)	Tolerance
+1.8V	±0.15V
+3.3V	±0.3V or Refer to the CCD data sheet
+5.0V	±0.25V or Refer to the CCD data sheet
VH	Refer to the CCD data sheet
VL	Refer to the CCD data sheet

5.1.2. Power Consumption

Examples of measured current consumption values when driving ICX408AK are shown in the table below. These values were measured using a Sony Semiconductor evaluation board, and should be used as reference values.

Table 5.1-2 Power Consumption Measurements(when driving ICX408AK)

	Pin name	Voltage [V]	PIN number	Current consumption [mA]	Power consumption [mW]
CXD4103R	DVDD 0,1,4,5,6,8	1.8	7,21,50,57,72,109	12.51	218.887
	DVDD 2,3		29,33	1.66	
	DVDD 7		101	9.04	
	VDE 0	3.3 (Logic)	15	0.00	
	VDE 10,11,2,3,4		23,27,35,39,45	4.87	
	VDE 50,51		54,66	0.01	
	VDE 6,7		96,105	7.72	
	VDE 8		115	0.00	
	AVD 0	3.3 (Analog)	6	26.55	
	AVD 1		79	0.50	
	AVD 2		83	7.75	
	AVD 3		87	6.27	
CXA2096N	Vcc 1,2,3	3.3	5,16,23	47.88	158.004
CXD1267AN	VH	15	2	0.83	26.100
	VL	-7	6	1.95	
CCD (ICX408AK)	VDD	15	-	4.20	63.000
	VL	-7	-	0.00	

5.1.3. Power-on Sequence

In order to properly power up the CCD input VL last. DSP power-up requires +1.8V followed by +3.3V to be applied with a 2 – 3 msec delay between applications.

The VH and +5V may be applied at any time before VL.

*Depending on the type of CCD sensor being used the voltage levels may change Please check the documentation.

6.CCD Type Selection

6.1. CCD type

Note that the types shown below are the types supported at the time these Application Notes were prepared. Some types may be added or eliminated due to CCD version upgrades or discontinued production.

Table 6.1-1 CCD Image Sensors Supported by the SS-11X

Optical size	Number of pixels	TV system	Product name
Type 1/3	510H	NTSC	ICX404AK
			ICX254AK
		PAL	ICX405AK
			ICX255AK
	760H	NTSC	ICX408AK
			ICX258AK
		PAL	ICX409AK
			ICX259AK
Type 1/4	510H	NTSC	ICX206AK
			ICX226AK
		PAL	ICX207AK
			ICX227AK
	760H	NTSC	ICX228AK
			ICX278AK
		PAL	ICX229AK
			ICX279AK

* Inquiry about CCD types not listed above may be answered by SONY Sales.

6.2. Operation Mode Selection for Each CCD

6.2.1. System Configuration and MODESEL

The basic clock system for the SS-11X basic consists of a clock system configured by the single oscillator (ECK) used by the internal system and a PLL clock system that uses the two types of oscillators (ECK and MCK) used by the line lock system.

In addition, a clock system can be configured for each type of CCD as an operation mode. The clock frequency (oscillator frequency) combinations for each CCD type are shown in ”**Table 6.2-1**”.

The MODESEL function switches the above-mentioned clock system operation modes using the P12 to P15 pins of the CXD4103 which are assigned as the initial settings (“**Table 3.1-1**”) and the pins for the port driver described hereafter (“**Table 9.1-1**”).

Table 6.2-1 Relationship between CCD Type and Clock Frequencies

TV system	Number of pixels	P15	P14	P13	P12	ECK	MCK	MODESEL
NTSC	510H	Low	Low	Low	Low	38.13986MHz	-	0[h]
		Low	Low	High	Low	27.00000MHz	38.13986MHz	2[h]
	760H	Low	High	High	Low	28.63636MHz	-	6[h]
		High	Low	Low	Low	27.00000MHz	28.63636MHz	8[h]
PAL	510H	Low	Low	High	High	37.87500MHz	-	3[h]
		Low	High	Low	High	27.00000MHz	37.87500MHz	5[h]
	760H	High	Low	Low	High	28.37500MHz	-	9[h]
		High	Low	High	High	27.00000MHz	28.37500MHz	B[h]

The internal clock of the CXD4103 is switched according to the operation mode. Set the P12 to P15 pins of the CXD4103 by wiring to the VDD or GND side and pulling up/down according to the system conditions to be used (TV system, supported CCD). Be sure to make these settings correctly as the clock system does not operate normally when the above setup is incorrect.

MODESEL is controlled by the CXD4103, and operation is determined and reflected to the parameter in ”**Table 6.2-2**” by making the P12 to P15 pin settings. Therefore, there is no need to set the parameter in the table below.

Table 6.2-2 MODESEL Parameter

Parameter		Description
MODESEL	CAT12_Byte1_bit0-3	0[h] to B[h]: DSP operation mode For details, see “**Table 6.2-1**”.

6.3. Important Information on Wiring

The drive circuit must be changed according to the type of CCD used. The main differences are as follows.

1. Changes in the drive circuit due to different CCD image sensor drive specifications
2. Changes in the clock system due to different CCD types and TV systems (NTSC/PAL)
3. Changes in the frequency response due to different CCD types
4. Changes in the modes due to different CCD types and TV systems (NTSC/PAL)

6.3.1. Drive Circuit Changes

The drive specifications of CCD image sensors that can be driven by the SS-11X are shown in the Table below.

Table 6.3-1 CCD Image Sensors and Drive Conditions

Optical size	Number of pixels	Product name	DC voltage specifications		AC voltage specifications			Drive circuit example
			Vsub voltage	RG voltage	H	RG	V	
Type 1/3	510H	ICX254AK	Generated internally, adjustment free	Generated internally, adjustment free	5.0V	5.0V	-7.0V	**Fig 6.3-1**
		ICX255AK						
		ICX404AK		Clamped high, adjustment free				
		ICX405AK						
	760H	ICX258AK		Generated internally, adjustment free				
		ICX259AK						
		ICX408AK		Clamped high, adjustment free				
		ICX409AK						
Type 1/4	510H	ICX206AK		Generated internally, adjustment free	3.3V	3.3V	-7.0V	**Fig 6.3-2**
		ICX207AK						
		ICX226AK						
		ICX227AK						
	760H	ICX228AK						
		ICX229AK						
		ICX278AK						
		ICX279AK						

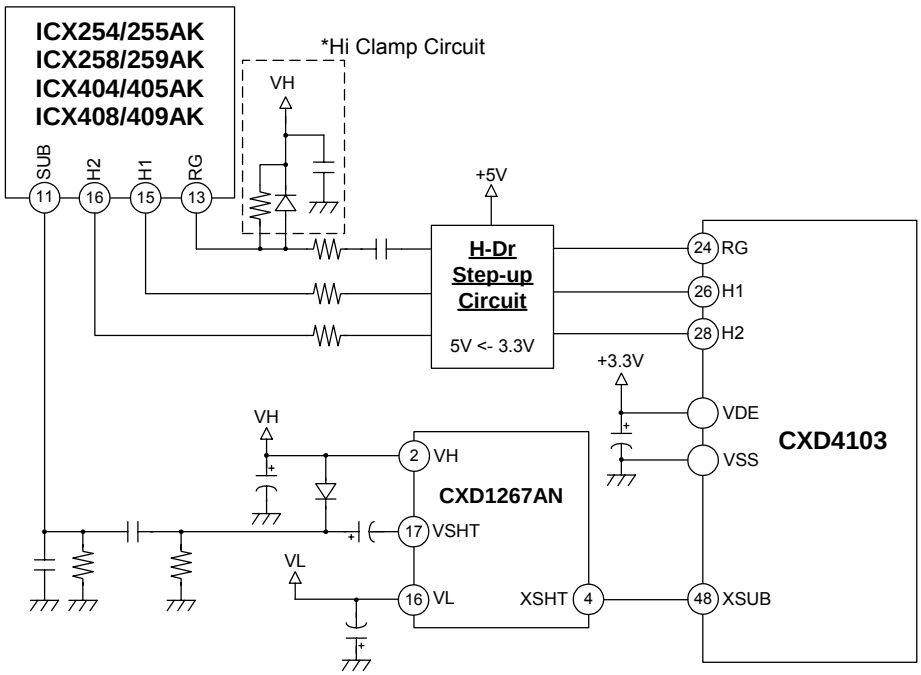


Fig 6.3-1 Example 1/3 Type CCD Drive Circuit

"**Fig 6.3-1**" shows the drive circuit when using 1/3 type CCD image sensors (ICX254/255AK, ICX404/405AK, ICX228/229AK, ICX408/409AK).

Both Vsub voltage and RG voltage are adjustment-free. Vsub is a voltage generated inside the CCD and is used to clamp the shutter pulse, so an external clamping circuit is not required. The SUB output is input via a capacitor to the CCD's SUB pin.

As for H1, H2, and RG, because the output of CXD4103 is 3.3V, the level conversion circuit of "3.3V -> 5.0V" is needed between CXD4103 and CCD.

RG is input to the CCD after its DC component is cut by a capacitor. The high clamp circuit might be needed.

*Please refer to CCD specification sheet.

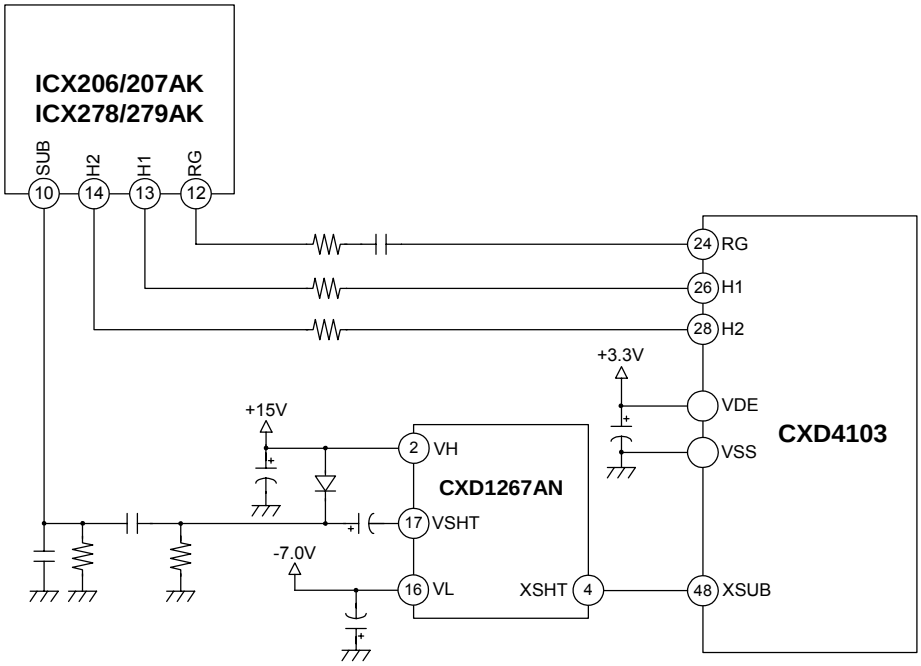


Fig 6.3-2 Example 1/4 Type CCD Drive Circuit

"**Fig 6.3-2**" shows the drive circuit for a Type 1/4 CCD (ICX206/207AK, ICX226/227AK, ICX228/229AK, ICX278/279AK). Both Vsub voltage and RG voltage are adjustment-free. Vsub is a voltage generated inside the CCD and is used to clamp the shutter pulse, so an external clamping circuit is not required. The SUB output is input via a capacitor to the CCD's SUB pin.

RG is input to the CCD after its DC component is cut by a capacitor.

*Please refer to CCD specification sheet.

6.3.2. Frequency Response Changes

The subcarrier frequencies differ with each other according to the NTSC/PAL of CCD image sensor used. It is necessary to also change the characteristics of the BPF connected to the rear end of the IOC pin.

6.4. CCD Primary Color Separation Matrix

6.4.1. Recommended Parameter's Value

The spectral characteristics of the color filter differ according to the type of CCD.

The CXD4103 initial setting values (DSP initial values) differ from the setting values for the CCD types in the table below, so reset the parameters in the table below and write this data in the EEPROM before using these CCD types.

In addition, set CPUHOLD (CAT12_Byte5_bit0) = 1[h] before changing primary color separation matrix parameter and linear matrix parameter values.

Table 6.4-1 CCD Types and Recommended Primary Color Separation Matrix Parameters

Type	Horizontal pixels	Name	Primary color separation matrix parameters			
			RMATY	RMATC	BMATY	BMATC
			CAT2_Byte31	CAT2_Byte32	CAT2_Byte33	CAT2_Byte34
1/3	510H	ICX404/405AK	2F[h]	14[h]	28[h]	DC[h]
	760H	ICX408/409AK				
	510H	ICX254/255AK	2B[h]	10[h]	2F[h]	CF[h]
	760H	ICX258/259AK				
1/4	510H	ICX206/207AK	2D[h]	00[h]	45[h]	BB[h]
		ICX226AK	21[h]	F9[h]	2C[h]	E0[h]
		ICX227AK	23[h]	05[h]	2C[h]	FC[h]
	760H	ICX228/229AK	27[h]	05[h]	30[h]	E0[h]
		ICX278/279AK	2F[h]	14[h]	2F[h]	DC[h]

Table 6.4-2 CCD Types and Linear Matrix Parameters (Reference Values)

Parameter	CCD type	Type 1/3		Type 1/4	
		510H	760H	510H	760H
		ICX404/405AK ICX254/255AK	ICX408/409AK ICX258/259AK	ICX206/207AK ICX226/227AK	ICX228/229AK ICX278/279AK
RYGAIN1	CAT2_Byte37	3F[h]			
BYGAIN1	CAT2_Byte38	21[h]			
RYHUE1	CAT2_Byte39	80[h]			
BYHUE1	CAT2_Byte40	FF[h]			

* The above linear matrix parameters are example setting determined with an emphasis on color reproducibility for skin color in representative samples of each CCD type. Please note that they are not intended to be adjusted to the target displayed on the vector scope.

* Use the above linear matrix parameters as reference values. In actual practice, we recommend that each user set their own values to match the color reproducibility they desire, according to factors such as the circuits/ICs to be connected at the rear end of the DSP, the gain settings, and the video camera screen makeup.

7. Communication Methods

7.1. RS-232C Communication

7.1.1. Interface

The SS-11X system supports the RS-232C format (half duplex mode) as a means of communication with external PCs. However, RS-232C communication requires an external IC for converting the 3.3 V logic to the RS-232C level (recommended product: MAX3232, made by Maxim), as well as pin settings. See the Application Circuit provided by Sony for information on the connections with the MAX3232 and the RS-232C connector (D-sub 9 pin).

The serial communication clock is generated by frequency-dividing the CXD4103's ECK. Therefore, it may not be possible to perform communication correctly when MODESEL is not set correctly or when the ECK frequency deviates significantly from the recommended value.

The CXD4103 pin settings used for RS-232C communication are shown in "**Table 7.1-1**".
When SIFSEL is switched, be sure to reset the system.

Table 7.1-1 Pin Settings for Communication

Signal name	Pin No	I / O	Description
XCS(XCTS)	17	IN	Fixed high
SI(RXD)	18	IN	Serial setting data input
SO(TXD)	19	OUT	Serial setting data output
SCK(XRTS)	20	IN	Pull up*1 (Pull up with a 100 k ohm resistor.)
SIFSEL	16	IN	Fixed high

*1 SCK becomes an input pin when SIFSEL = L, so pull up as a floating measure.

Note that if the communication speed set by the "SS-11X Control Software" provided by Sony does not match the communication speed parameter shown in "**Table 7.1-2**", communication is not possible. The BPSSEL initial value is set to 1[h] (19200 bps). This setting is the same even when there is no EEPROM.

Table 7.1-2 Communication Speed Setting

Parameter		Description
BPSSEL	CAT12_Byte10_bit0	0[h]:9600bps
		1[h]:19200bps

7.1.2. Control Software Communication Method

The "SS-11X Control Software" provided by Sony is designed for use with RS-232C communication. The sending and receiving processes, as well as EEPROM write/read processes, have been optimized for the SS-11X system, so there is no need to worry about factors such as communication format and byte length.

Set the PC side as shown in ”**Table 7.1-3**”.

Table 7.1-3 PC Settings for Communication

Item	Setting
COM PORT	Arbitrary (1 to 16)
Communication speed	19200 bps
PARITY	NONE
DATA bits	8 bit
STOP bits	1 bit
Handshaking	Nothing

See the "SS-11X Control Software Operation Manual" for a description of the "SS-11X Control Software".

7.1.3. Communication Timing

The CXD4103 acquires data in byte units at the timing determined by the communication speed from the falling edge of SI. Serial output is output after all the data have been acquired. Communication data is LSB-first.

If the number of received bytes from the first byte totals 33 or more, all the received data is discarded. In these cases, set the number of bytes to 32 or less and execute communication again.

If a communication error occurs, an error code is sent to the host after the reception of the valid byte count.

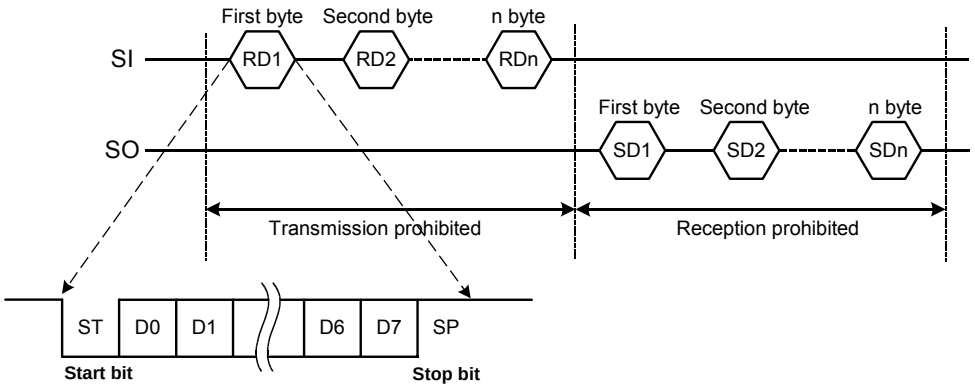


Fig 7.1-1 Communication Timing

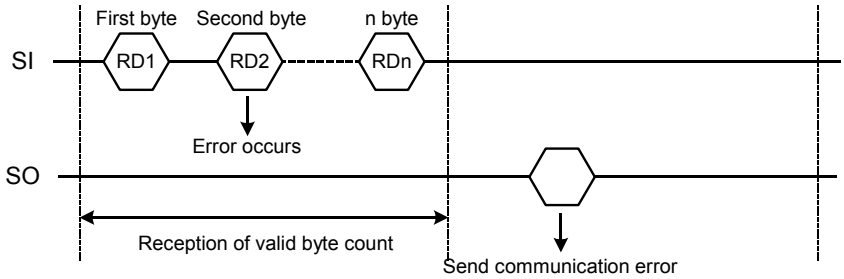


Fig 7.1-2 Communication Timing when Communication Error Occurs

If the received byte count does not change for 15 fields or more, an error code is sent to the host as a Timeout Error, after which the state shifts to the reception wait state.

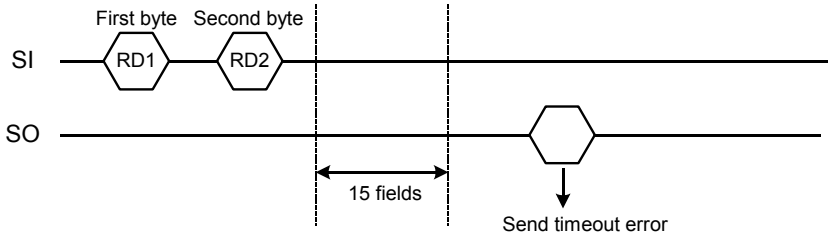


Fig 7.1-3 Communication Timing when Timeout Error Occurs

7.1.4. Communication Format

A single packet consists of 2 to 32 bytes. After receiving one packet of data, the CXD4103 analyzes the data and performs command execution control. See "**Table 7.1-4**" for the command specifications.

Data are sent in category increments. The byte count for the number of bytes to be sent is sent in the first byte. Commands are sent in the second byte, and communication data corresponding to the individual commands are sent in the third and subsequent bytes.

A maximum of 32 bytes can be sent and received, including headers for commands and the like, and the valid communication byte count.

Table 7.1-4 List of Command Specifications

Command	Description	Communication format						
		1	2	3	4	5	6-29	30-32
Register Category specification Read	CMD	05[h]	01[h]	CAT	Byte	Data Num 01[h]-1F[h]		
	Reply	Data Num +1	Read Data					
Register Category specification Write	CMD	Data Num +4	02[h]	CAT	Byte	Write Data		
	Reply	Data Num +1	Write Data					
EEPROM Category specification Read	CMD	05[h]	03[h]	CAT	Byte	Data Num 01[h]-1F[h]		
	Reply	Data Num +1	Read Data					
EEPROM Category specification Write	CMD	05[h]	04[h]	CAT	Byte	Data Num 01[h]-FF[h]		
	Reply	02[h]	01[h]					
EEPROM Actural Address specification Read	CMD	05[h]	05[h]	EEPROM Address MSB	EEPROM Address LSB	Data Num 01[h]-1F[h]		
	Reply	Data Num +1	Read Data					
EEPROM Actural Address specification Write	CMD	Data Num +4	06[h]	EEPROM Address MSB	EEPROM Address LSB	Write Data		
	Reply	02[h]	01[h]					
EEPROM Batch Write	CMD	05[h]	07[h]	00[h]	01[h]	02[h]		
	Reply	02[h]	01[h]					

* CMD: A command is sent from the PC to the CXD4103

Reply: A reply is sent to the PC after the CXD4103 receives a command

Note:

Data for CAT5, CAT22 and CAT23 are not written to the EEPROM, so it is not possible to specify 05[h], 16[h] and 17[h] in EEPROM category specification write/read commands.

An error occurs if the specified byte count exceeds the byte count for a given category in the category specification command (code 01[h], 02[h], 03[h], 04[h]).

<Explanation of command specifications>

- Data in byte 1: Total valid byte count in one packet
- Data in byte 2 (CMD): Command code
  Setting range: 01[h] to 07[h]
- CAT: Write/Read category number
  Setting range: 01[h] to 18[h] (note: 05[h],16[h], and 17[h] are excluded)
- BYTE: Write/Read start byte number
  Setting range: 01[h] ≦ BYTE ≦ Total byte count for the specified category
- Data Num: Write/Read byte count
  Setting range: Noted in "**Table 7.1-4**" (access across different categories is not allowed)
- EEPROM Address MSB/LSB: EEPROM actual address (byte units)
  Setting range: 0000[h] ≦ EEPROM address ≦ 02FF[h]

<Error codes>

When a command is received, if any of the following conditions apply an error is recognized and an error code is sent to the external PC.

FC[h]: Communication error (protocol violation such as over-run)
FD[h]: Timeout error (RS-232C only)
F0[h]: Illegal valid communication byte count
F1[h]: Illegal command code
F2[h]: Illegal category number
F3[h]: Illegal byte number
F4[h]: Illegal access (e.g., communication data are outside range)
F5[h]: EEPROM BUSY state

7.1.5. Serial Communication Prohibited Period

A serial communication prohibited period is established during the time period preceding and following the VD fall. External communication is not accepted during the periods shown in "**Fig 7.1-4**".

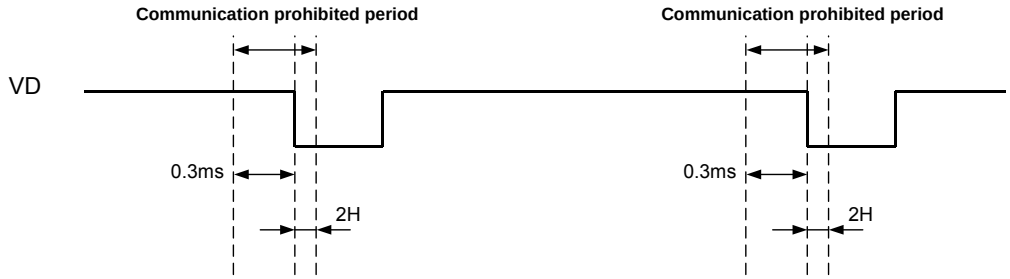


Fig 7.1-4 Serial Communication Prohibited Period

8. Basic Adjustments

When the set is complete, perform the following adjustment procedures.

1. TG phase adjustment (See "**8.1 TG Phase Adjustment**".)
2. AGCMIN adjustment (See "**8.2 AGC Minimum Adjustment**".)
3. Pre-WB adjustment (See "**8.3Pre-White Balance Adjustment**".)
4. Static blemish detection and compensation(See "**8.4 CCD Blemish Detection and Compensation**".)

8.1. TG Phase Adjustment

Adjust the phase of the high frequency TG pulses (H1, H2, RG, XSHP, XSHD, XRS) to obtain a suitable S/N ratio. The TG phase affects the video, and noise may be generated depending on the adjustment value, so be sure to adjust while checking the video on a monitor, etc.

Follow the procedures below to adjust the phase based on "**Fig 8.1-1**".

* See "**8.1.1 Phase and Drive Ability Adjustment Method**" for the delay and duty adjustment of each waveform.

1. Adjust the H1 and H2 delay and duty so that the H1 and H2 waveforms cross at a potential higher than 1/2 of each clock voltage as shown by (1) in the figure below.
2. Adjust the RG delay and duty so that RG rises approximately 1 ns before H1 rises as shown by (2) in the figure.
3. When the H1, H2 and RG adjustments are complete, check that the waveform is output in the manner of CCDOUT in the figure.
4. Adjust the XSHP delay and duty so that XSHP rises (Vth = 0.65 V) in the CCDOUT precharge block as shown by (3) in the figure.
5. Adjust the XSHD delay and duty so that XSHD rises (Vth = 0.65 V) in the CCDOUT data block as shown by (4) in the figure.
6. Adjust the XRS delay and duty so that XRS rises (Vth = 0.68 V) approximately 0.7 ns before XSHD falls (Vth = 0.65 V) as shown by (5) in the figure.

   * The values in this descriptive text are approximate and not guaranteed.

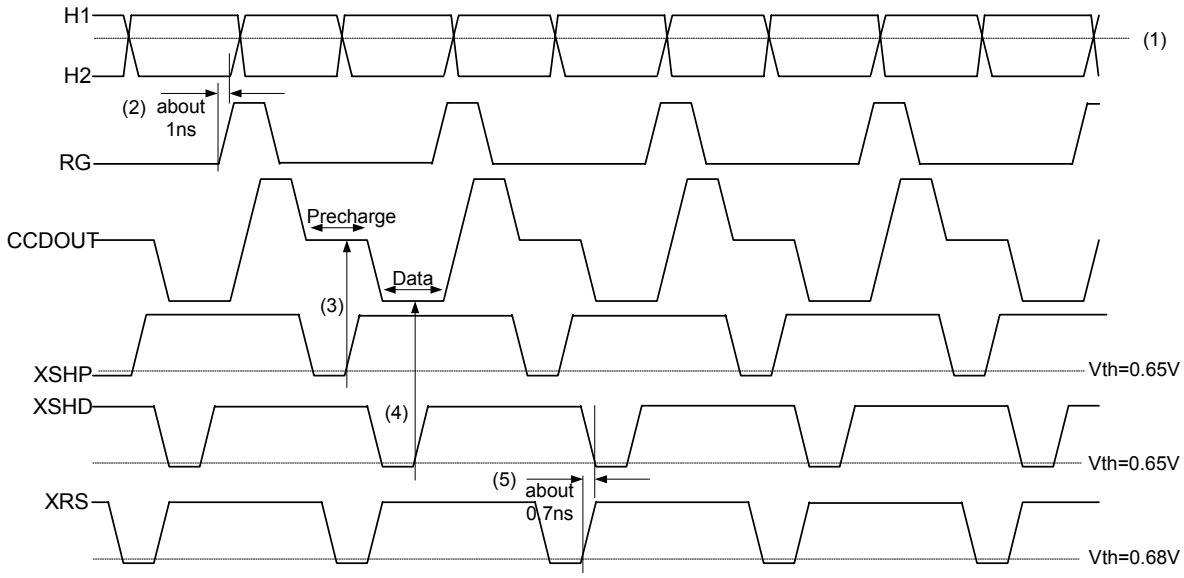


Fig 8.1-1 TG Waveform Adjustment

8.1.1. Phase and Drive Ability Adjustment Method

Adjusting the Delay

The delay can be changed by the parameters in "**Table 8.1-1**". In addition, the delay time can also be adjusted by changing the setting value as shown in "**Table 8.1-2**". See "**Fig 8.1-2**" "**Fig 8.1-3**" for the image of changing the delay.

Table 8.1-1 Delay Adjustment Parameters

Parameter		Description
DEH1	CAT6_Byte9_bit0-3	Adjustment of H1 pulse delay
DEH2	CAT6_Byte9_bit4-7	Adjustment of H2 pulse delay
DERG	CAT6_Byte10_bit0-3	Adjustment of RG pulse delay
DESHP	CAT6_Byte10_bit4-7	Adjustment of XSHP pulse delay
DESHD	CAT6_Byte11_bit0-3	Adjustment of XSHD pulse delay
DERS	CAT6_Byte11_bit4-7	Adjustment of XRS pulse delay
10NSDEH1	CAT6_Byte20_bit0-1	Adjustment of H1 pulse delay until +10ns
10NSDEH2	CAT6_Byte20_bit2-3	Adjustment of H2 pulse delay until +10ns
10NSDERG	CAT6_Byte20_bit4-5	Adjustment of RG pulse delay until +10ns
10NSDESHD	CAT6_Byte20_bit6-7	Adjustment of XSHD pulse delay until +10ns
10NSDESHP	CAT6_Byte21_bit0-1	Adjustment of XSHP pulse delay until +10ns
10NSDERS	CAT6_Byte21_bit2-3	Adjustment of XRS pulse delay until +10ns

Table 8.1-2 Adjustment Range

Setting value	Adjustment width (ns)	+10ns Adjustment width (ns)
0h	-8	0
1h	-7	+5
2h	-6	+10
3h	-5	
4h	-4	
5h	-3	
6h	-2	
7h	-1	
8h	0	
9h	+1	
Ah	+2	
Bh	+3	
Ch	+4	
Dh	+5	
Eh	+6	
Fh	+7	

* The adjustment widths shown in the table are approximate, and these values are not guaranteed.

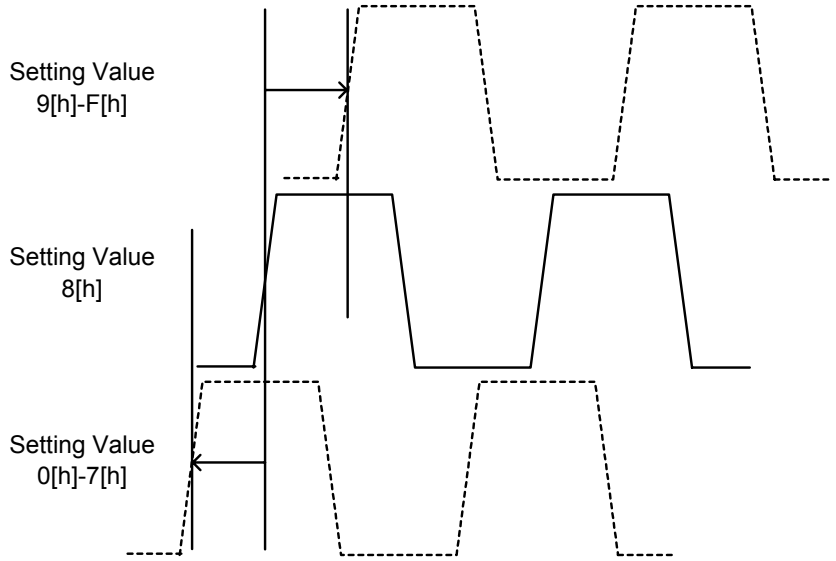


Fig 8.1-2 Delay Adjustment

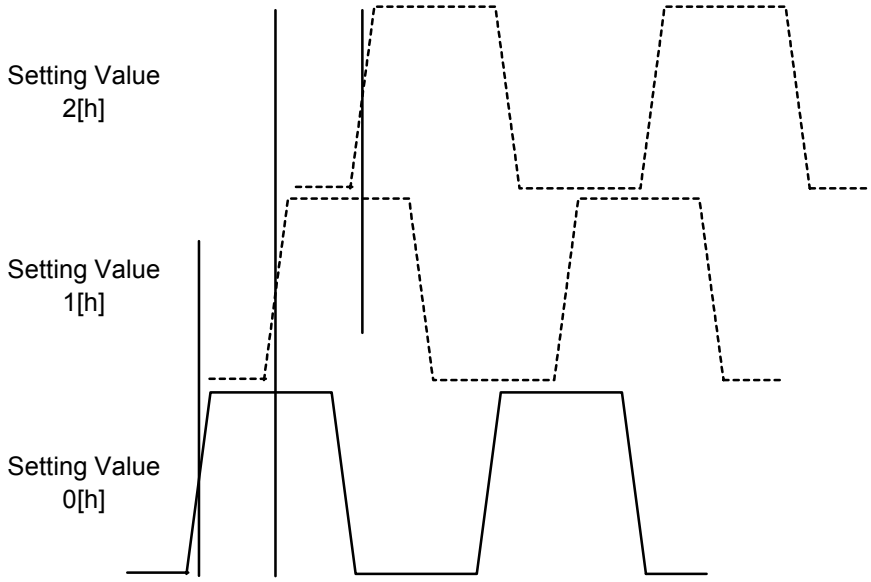


Fig 8.1-3 +10ns Delay Adjustment

Adjusting the Duty

The duty can be changed by the parameters in "**Table 8.1-3**". In addition, the duty level can also be adjusted by changing the setting value as shown in "**Table 8.1-4**". See "**Fig 8.1-4**" for the image of changing the duty.

Table 8.1-3 Duty Adjustment Parameters

Parameter		Description
DUH1	CAT6_Byte12_bit0-3	Adjustment of H1 pulse duty
DUH2	CAT6_Byte12_bit4-7	Adjustment of H2 pulse duty
DURG	CAT6_Byte13_bit0-3	Adjustment of RG pulse duty
DUSHP	CAT6_Byte13_bit4-7	Adjustment of XSHP pulse duty
DUSHD	CAT6_Byte14_bit0-3	Adjustment of XSHD pulse duty
DURS	CAT6_Byte14_bit4-7	Adjustment of XRS pulse duty

Table 8.1-4 Duty Adjustment Range

Setting value	Adjustment width (ns)	Changing point
0[h]	0	-
1[h]	+1	Falling edge
2[h]	+2	
3[h]	+3	
4[h]	+4	
5[h]	+5	
6[h]	+6	
7[h]	+7	
8[h]	0	-
9[h]	+1	Rising edge
A[h]	+2	
B[h]	+3	
C[h]	+4	
D[h]	+5	
E[h]	+6	
F[h]	+7	

* The adjustment widths shown in the table are approximate, and these values are not guaranteed.

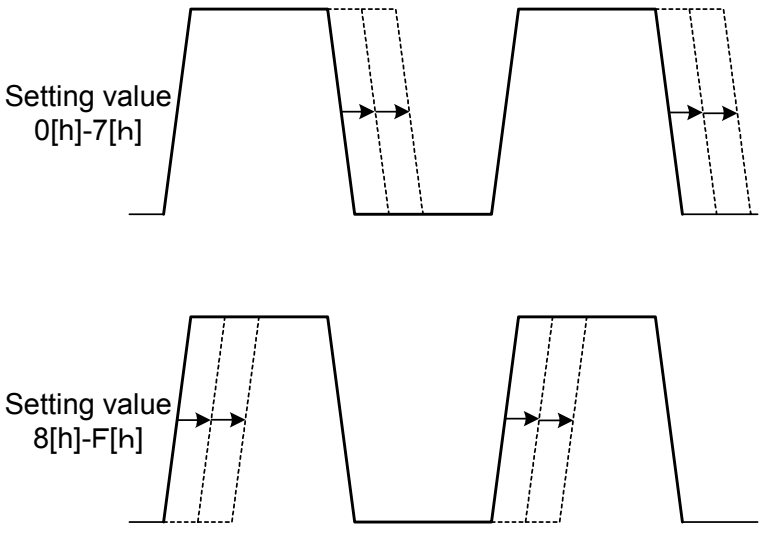


Fig 8.1-4 Duty Adjustment

Adjusting the Drive Ability

The drive ability can be changed by the parameters in "**Table 8.1-5**". When the drive ability is high, overshoot and undershoot may appear in the TG waveform depending on the board configuration as shown in "**Fig 8.1-5**". Adjust the drive ability as appropriate according to the board configuration and the wiring method.

The drive ability can be set from 0[h] (max.) to 6[h] (min.) for each parameter.

When the drive ability is set to 7[h], each TG output pin becomes high impedance, so a pulse is not output.

Table 8.1-5 Drive Ability Adjustment Parameters

Parameter		Description
DRBH1	CAT6_Byte15_bit4-6	Adjustment of H1 drive ability
DRBH2	CAT6_Byte16_bit0-2	Adjustment of H2 drive ability
DRBRG	CAT6_Byte16_bit3-5	Adjustment of RG drive ability
DRBSHP	CAT6_Byte17_bit0-2	Adjustment of XSHP drive ability
DRBSHD	CAT6_Byte17_bit3-5	Adjustment of XSHD drive ability
DRBRS	CAT6_Byte18_bit0-2	Adjustment of XRS drive ability

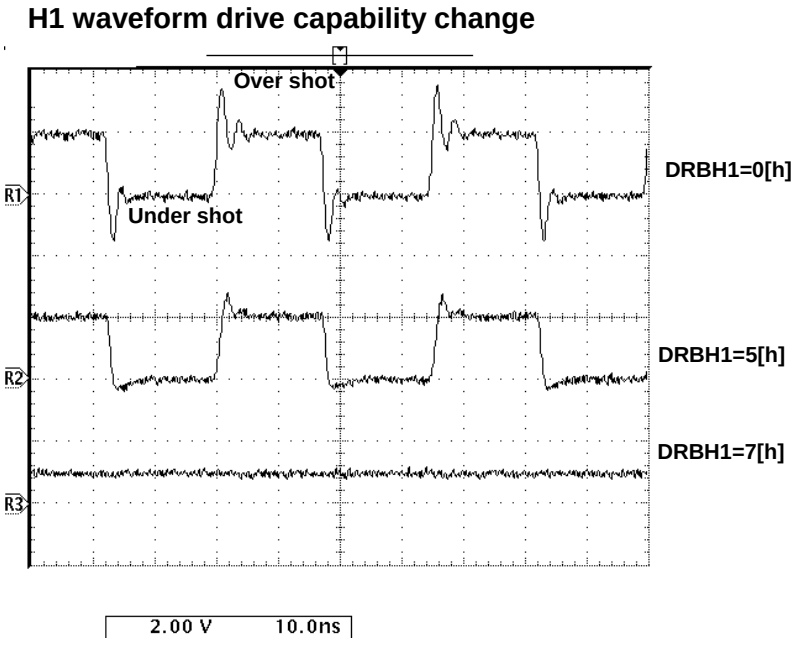


Fig 8.1-5 Drive Ability Adjustment

8.2. AGC Minimum Adjustment

CCD saturation unevenness can be prevented by performing AGC Minimum adjustment.

This adjustment adjusts the minimum AGC gain to allow A/D input of 400 [mVp-p] at the CCD standard output of 250 [mVp-p].

8.2.1. AGC Minimum Adjustment Method

The AGC Minimum adjustment procedure is as follows.

1. Image an all-white subject.
2. Set ADJMODE to 20[h] to set the adjustment mode to AGC Minimum adjustment mode.
3. Monitor the CCD-OUT signal with an oscilloscope and adjust the exposure level so that the CCD data block is 250 [mVp-p] as shown in "**Fig 8.2-1**". Adjust the exposure level using an ND filter or by changing the lens iris, etc.
4. Set CCDLEV to 1[h] (CCD level adjustment end).
5. If AGCMINFIN is 1[h], the AGCMIN adjustment has ended.
6. Write the AGCMIN setting value to the EEPROM.
7. Set ADJMODE to 00[h] (resets normal mode).

(CCDLEV and AGCMINFIN are automatically reset to 0[h].)

Table 8.2-1 AGC Minimum Adjustment Parameters

Parameter		Description
ADJMODE	CAT12_Byte2	Adjustment mode switching
CCDLEV	CAT12_Byte4_bit0	CCD level 250 mV manual adjustment end 0[h]: Not completed, 1[h]: Completed
AGCMINFIN	CAT12_Byte4_bit5	AGC Minimum automatic adjustment end flag
AGCMIN	CAT19_Byte1	AGC minimum value

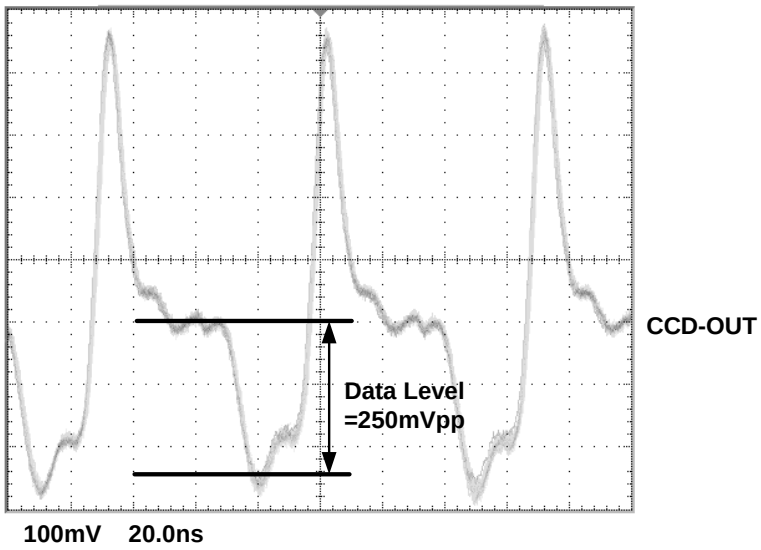


Fig 8.2-1 CCD-OUT Waveform

8.3. Pre-White Balance Adjustment

Pre-white balance consists of aligning the operation color temperature range of the built-in ATW and Manual White Balance with the three reference color temperatures for each CCD to be used.

Pre-white balance adjustment is to aligne the operation color temperature range of the built-in ATW and Manual White Balance.

Adjust using the three reference color temperatures for each CCD to be used.

8.3.1. Pre-White Balance Adjustment Method

The pre-white balance adjustment procedure is as follows. (The adjustment values are reflected after power-on.)

1. Image a light source of the reference color temperature (approximately 3200K) onto the entire screen.
2. Set ADJMODE to 21[h] to set Pre-white balance adjustment mode.
3. Set PREWBMODE (CAT12_Byte3) to 1[h] and confirm the pull-in operation convergence.
4. After setting PREWBMODE (CAT12_Byte3) to 2[h] in that condition (3200K), apply a color temperature conversion filter to the light source (approximately 3200K) to obtain a color temperature of approximately 2500K and confirm the pull-in operation convergence.
5. After setting PREWBMODE (CAT12_Byte3) to 3[h] in that condition (2500K), apply a color temperature conversion filter to the light source (approximately 3200K) to obtain a color temperature of approximately 9500K and confirm the pull-in operation convergence.
6. Return to normal mode (ADJMODE = 00[h]) in that condition (9500K) and remove the color temperature conversion filter.
7. Write CAT19 in the EEPROM.

The White Balance (ATW) and Manual White Balance operation color temperature range is determined by the above adjustment.

* Note: The order of setting a color temperature conversion filter is according to the above procedure.

Table 8.3-1 Pre-White Balance Adjustment Parameters

Parameter		Description
ADJMODE	CAT12_Byte2	Adjustment mode switching
AWBPRER	CAT19_Byte3	R gain in 3200K
AWBPREB	CAT19_Byte6	B gain in 3200K
ATWSTARTR	CAT19_Byte8	R gain at ATW startup
ATWSTARTB	CAT19_Byte9	B gain at ATW startup
MWBPRESETR	CAT19_Byte10	Preset R gain in MWB
MWBPRESETB	CAT19_Byte11	Preset B gain in MWB
PRERDIVG1	CAT19_Byte12 CAT19_Byte13	R/G as viewed from 3200K at high color temperature
PREBDIVG1	CAT19_Byte14 CAT19_Byte15	B/G as viewed from 3200K at high color temperature
PRERDIVG0	CAT19_Byte16 CAT19_Byte 17	R/G as viewed from 3200K at low color temperature
PREBDIVG0	CAT19_Byte18 CAT19_Byte19	B/G as viewed from 3200K at low color temperature
PRER1	CAT19_Byte4	R gain at high color temperature
PREB1	CAT19_Byte7	B gain at high color temperature
PRER0	CAT19_Byte2	R gain at low color temperature
PREB0	CAT19_Byte5	B gain at low color temperature

8.3.2. Operation Frame Offset Setting

Depending on luminance variation after Pre-White Balance correction; the corrected color temperature range Operation Frame may not be sufficient leading to a convergence failure.

When convergence fails to occur, please set the offset parameter in "**Table 8.3-2**".

Setting the offset parameter value found in "Table 8.3 2" to 1[h] – 2[h] enlarges the operation frame area.

Table 8.3-2 Offset Value

Color temperature	Parameter	OFFSET
2500K	PRERDIVG0H(CAT19_Byte17)	1[h] to 2[h]
9500K	PREBDIVG1H(CAT19_Byte15)	1[h] to 2[h]

Note:
The above offset values are used on Sony's evaluation board.

If the offset values are set to high, values exceeding the range 2500K – 9500K will be captured inside the Operation Frame and converge to white.

If after setting the "offset value" it still fails to converge, please re-do the Pre-white Balance adjustment, and evaluate the best offset value for your camera set.

When evaluating the offset value please use either a 2500K or a 9500K color temperature conversion filter.

8.4. CCD Blemish Detection and Compensation

Blemish specifications are established for spot blemishes, which are a type of pixel defect. During the production process, Sony CCDs are sorted based on these blemish specifications. However, white blemishes, in which the blemish level varies in proportion to the temperature, may be observed during use, especially at high temperatures, due to external factors and the like. The CCD blemish detection and compensation function automatically detects and corrects such white blemishes, so that high image quality can be maintained. The SS-11X automatically detects and corrects blemishes in order from the highest blemish level. It can detect and correct up to 8 blemishes.

8.4.1. CCD Blemish Detection Method Types and Setting Procedures

The SS-11X has the following two types of blemish detection functions.

1. Static detection : Initial blemishes (blemishes within the spot blemish standards) are detected and corrected mainly during the shipping adjustments.
2. Dynamic detection : Blemishes are detected and corrected in real time without the need to shield the CCD from light.

Static Detection Setting Method

The setting procedure is as follows.

1. Close the lens iris or otherwise shield the CCD from light.
2. Set DEFON to 1[h]. (Blemish compensation function ON) (See "**Table 8.4-1**".)
3. Set the blemish detection area. (See "**Table 8.4-2**".)
4. Use DETREFL/M to set the detection threshold levels. (See "**Table 8.4-3**".)
5. Set ADJMODE to 22[h]. (Starts blemish detection and compensation) (See "**Table 8.4-4**".)
6. Read the parameters. If BLMDETFIN = 1[h], detection and compensation are finished.
   (See "**Table 8.4-5**".)
7. Set ADJMODE to 0[h]. (Resets the normal operation mode.) (See "**Table 8.4-4**".)

* If blemishes are not corrected, check again that the setting parameters are set as specified in the above procedure.

When DEFMK is set to 1[h], a marker appears in locations where blemishes are detected. (See "**Table 8.4-9**".)
When DEFMK is set to 1[h], a marker appears in locations where blemishes are detected. (See "**Table 8.4-9**".)
If blemishes are not corrected in accordance with the setting, the DETREFL/M values in step 4 may be too large, so readjust these values.

Dynamic Detection Setting Method

The setting procedure is as follows.

1. Set the dynamic detection function to OFF. (DYNDETON = 0[h]) (See "**Table 8.4-6**".)
2. Set DEFON to 1[h]. (Blemish compensation function ON) (See "**Table 8.4-1**".)
3. Set the blemish detection area. (See "**Table 8.4-2**".)
4. Use DETREFL/M to set the detection threshold levels. (See "**Table 8.4-3**".)
5. Set the number of detection-wait fields. (See "**Table 8.4-8**".)
6. Set the blemish reference dark level DARKREFL/M. (See "**Table 8.4-7**".)
7. Turn the dynamic detection function ON. (DYNDETON = 1[h]) (See "**Table 8.4-6**".)

* If blemishes are not corrected, check again that the setting parameters are set as specified in the above procedure.
When DEFMK is set to 1[h], a marker appears in locations where blemishes are detected. (See "**Table 8.4-9**".)

If blemishes are not corrected in accordance with the setting, the DETREFL/M values in step 4 or the DARKREFL/M values in step 6 may not be appropriate, so readjust these values.

8.4.2. Blemish Detection Setting Parameters

Blemish Compensation Function ON/OFF

The following parameter is used to turn the blemish compensation function ON/OFF.

Table 8.4-1 Blemish Compensation Function ON/OFF Parameter

Parameter		Description
DEFON	CAT1_Byte1_bit6	0[h]: Turns blemish compensation function OFF 1[h]: Turns blemish compensation function ON

* This parameter can be used for both static detection and dynamic detection.

Detection Area Settings

These parameters set the blemish detection area. When AREA is set to 1[h], the detection area is displayed. The position and size of the displayed box can be changed by setting HSRTL/M, VSRTL/M, HWIDTHL/M, and VWIDTHL/M.

Table 8.4-2 Detection Area Setting Parameters

Parameter		Description
AREA	CAT11_Byte1_bit4	0[h]: Hides the blemish detection area 1[h]: Displays the blemish detection area
HSRTL	CAT11_Byte13(LSB)	Sets the horizontal start position of the blemish detection area
HSRTM	CAT11_Byte17_bit0-1(MSB)	
VSRTL	CAT11_Byte14(LSB)	Sets the vertical start position of the blemish detection area
VSRTM	CAT11_Byte17_bit2-3(MSB)	
HWIDTHL	CAT11_Byte15(LSB)	Sets the horizontal width of the blemish detection area
HWIDTHM	CAT11_Byte17_bit4-5(MSB)	
VWIDTHL	CAT11_Byte16(LSB)	Sets the vertical width of the blemish detection area
VWIDTHM	CAT11_Byte17_bit6-7(MSB)	

* These parameters can be used for both static detection and dynamic detection.

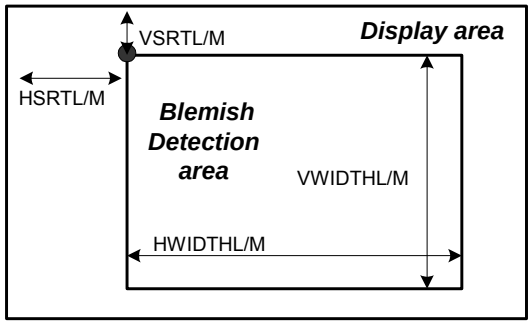


Fig 8.4-1 Detection Area Setting

Detection Threshold Level Settings

This parameter is used to set the blemish threshold level. Pixels exceeding the levels set by these parameters are recognized as being blemishes.

Table 8.4-3 Detection Threshold Level Setting Parameter

Parameter		Description
DETREFL	CAT11_Byte5(LSB)	Sets the detection threshold level
DETREFM	CAT11_Byte9_bit0-1(MSB)	

* This parameter can be used for both static detection and dynamic detection.

Adjustment Mode Dettings

The following parameter is used to switch the adjustment mode.

Table 8.4-4 Adjustment Mode Switching Parameter

Parameter		Description
ADJMODE	CAT12_Byte2	00[h]: Normal mode 22[h]: Blemish detection and compensation mode

* This parameter is valid only for modes used by static detection.

Static Detection Finished Flag

The following parameter is used to confirm that static blemish detection is completed.

Table 8.4-5 Static Detection Finished Flag Parameter

Parameter		Description
BLMDETFIN	CAT12_Byte4_bit6	0[h]: Not finished 1[h]: Finished

Dynamic Detection Function ON/OFF

The following parameter is used to turn the dynamic detection function ON/OFF.

Table 8.4-6 Dynamic Detection Function ON/OFF Parameter

Parameter		Description
DYNDETON	CAT 21_byte2_bit2	0[h]: Turns dynamic detection function OFF 1[h]: Turns dynamic detection function ON (default)

* Set this parameter to 1[h] even if the dynamic detection function is not used.

Dark Level Reference Value Setting

This parameter is used to set the dark level reference value, which serves as a reference during dynamic detection.

Table 8.4-7 Dark Level Reference Value Setting Parameter

Parameter		Description
DARKREFL	CAT11_Byte8(LSB)	Sets the dark level reference value
DARKREFM	CAT11_Byte9_bit6-7(MSB)	

* Enabled when DYNDETON = 1[h]

Dynamic Detection Wait field Count Setting

In dynamic detection mode, the address with the highest-level blemish in a frame is compared with the addresses N fields before and after, and is stored as a blemish only if it matches. This parameter is used to set the number of fields N.

Table 8.4-8 Dynamic Detection Wait Field Count Setting Parameter

Parameter		Description
FLDWAIT	CAT11_Byte4	Dynamic detection wait field count (in frame units, so only even numbers can be set)

* Enabled when DYNDETON = 1[h]

Displaying Blemish Markers

This parameter is used to display marks at points where blemishes are detected. Even if a blemish has been corrected and is no longer visible, when DEFMK = 1[h] the marker remains displayed, making it appear as if the blemish has not been corrected. To check whether blemishes have been corrected, set DEFMK to 0[h].

Table 8.4-9 Setting parameter for Displaying Blemish Markers

Parameter		Description
DEFMK	CAT11_Byte1_bit1	0[h]: Hides marker 1[h]: Displays marker

Blemish Detection Results

The detected blemish information (type, level, address) is written to these parameters. The detected blemish information is written in order of blemish level, starting with the highest blemish level.

Table 8.4-10 Parameters for Storing Detected Blemish Information

Parameter		Description	
SD**n***	CAT11_Byte20-147	Blemish detection type	0[h]: Static detection 1[h]: Dynamic detection
VCNT**n***		Blemish vertical address	10-bit data
HCNT**n***		Blemish horizontal address	
DETLV**n***		Blemish level	

*** n:0-7**

Blemish Address Resetting

This parameter is used to reset the information written in the parameters for storing detected blemish information ("**Table 8.4-10**"). (All values are set to 00[h].)

This is ideal for resetting the information of blemishes detected by dynamic detection.

The information of blemishes detected by static detection is written in the EEPROM so it is not reset. To reset this blemish information, set the parameters for storing detected blemish information to 00[h] and write to the EEPROM.

When this parameter is set to 1[h], the blemish detection operation is not performed, so normally it should be set to 0[h].

Table 8.4-11 Parameters for Resetting Blemish Addresses

Parameter		Description
ADDRRST	CAT11_Byte18_bit0	0[h]: Normal blemish detection operation 1[h]: Resets blemish detection results

* Enabled when DYNDETON = 0[h]

False Blemish Generating Function

False blemishes can be detected and corrected just like CCD blemishes. Use this function to check the operations of the blemish detection and correction function.

Table 8.4-12 Parameters for Generating False Blemishes

Parameter		Description
DEFPG	CAT11_Byte1_bit0	0[h]: No false blemishes 1[h]: Generate false blemish
DEFPGLVL	CAT11_Byte2(LSB)	Sets the false blemish level
DEFPGLVM	CAT11_Byte3_bit0-1(MSB)	

9. Description of Each Functions

9.1. Port Driver Function

9.1.1. Port Driver Function Description

The SS-11X system has port driver functions.

The port driver functions make it possible to connect switches to P0 to P15 of the CXD4103 and operate the functions of the parameters set for each port, and to monitor and check those parameter states.

Input Port Driver

Each port can be assigned arbitrary parameters, and the parameter setting values can be switched by switches connected to the respective ports, even without external communication.

Output Port Driver

Each port can be assigned arbitrary 1-bit parameters, and changes in the 1-bit parameters can be monitored from outside the system by sending the parameter status (High or Low) from the ports.

9.1.2. Port Driver Initial Settings, Depending on Presence of EEPROM

Port Driver Initial Settings when the EEPROM is Valid

The parameter initial settings are made by the data written in the EEPROM.

Port Driver Initial Settings when the EEPROM is inValid

When the EEPROM is invalid or not connected, the port drivers function according to the initial values stored in the CXD4103 ("**Table 9.1-1**").

Table 9.1-1 Port Driver Initial Settings when the EEPROM is Invalid

Port Name	Parameter		Description
P0	AWBMODE	CAT15_Byte1_bit0	AWB mode settings
P1		CAT15_Byte1_bit1	
P2		CAT15_Byte1_bit2	
P3	CRLESSON	CAT12_Byte11_bit0	Anti-color rolling mode
P4	BLCOFF	CAT14_Byte1_bit2	Backlight compensation mode
P5	AEREF	CAT14_Byte1_bit3	AE parameter reference switching
P6	NORMFLC	CAT14_Byte2_bit0	Flickerless mode
P7	AGCMAX	CAT14_Byte1_bit4	AGC switching
P8	AEME	CAT14_Byte1_bit0	Switches between AE and ME
P9	AESHUT	CAT14_Byte1_bit6	Switches the electronic shutter fixed speed ON and OFF
P10	MIRROR	CAT1_Byte1_bit4	Switches MIRROR function ON and OFF
P11	GAMSEL	CAT13_Byte7_bit0	Switches the gamma parameters
P12	MODESEL	CAT12_Byte1_bit0	DSP operation mode switching
P13		CAT12_Byte1_bit1	
P14		CAT12_Byte1_bit2	
P15		CAT12_Byte1_bit3	

9.1.3. Description of Port Driver Parameters

This section explains the parameters for using the port drivers.

Description of Port Driver Parameters

The port drivers are set by parameters in CAT20. Set the arbitrary parameters to be controlled by the port drivers as shown in ”**Table 9.1-2**” for each port P0 to P15.

Here, "n" in the parameter name represents the port number (0 to 15[d]).

Table 9.1-2 Description of Port Driver Parameters

Parameter	Description		Remarks
PnCAT	Specifies the category number	Sets the category number of the arbitrary parameter to be controlled.	*1
PnBYTE	Specifies the byte number	Sets the byte number of the arbitrary parameter to be controlled.	*1
PnLSB	Specifies LSB	Sets the LSB of the arbitrary parameter to be controlled.	If the parameter has a width of 1 bit, that parameter itself becomes the LSB.
PnWID	Specifies the bit width	Sets the bit width of the arbitrary parameter to be controlled. 0[h] to F[h]: 1 to 16 bit width	If the bit width is 1 bit or when PnIOSEL is set to output, PnWID is set to 0[h].
PnIOSEL	Specifies input/output	Sets input/output of the arbitrary parameter to be controlled. 0[h]: Input port setting 1[h]: Output port setting	-
PnADJ *2	Specifies the coefficient	Sets the coefficient to be applied to the arbitrary 2-bit or larger parameter to be controlled. This switches the coefficient used to multiply the arbitrary parameter value by 0 to 2 times.	If the bit width is 1 bit or when PnIOSEL is set to output, PnADJ is set to 0[h].

*1: The port driver is disabled for some PnCAT and PnBYTE setting values. See ”**9.1.8 Conditions for Disabling the Port Drivers**”.

*2: Detailed description of PnADJ

1. If the port input is Low

The value written in the EEPROM is reflected to the parameter.

If the port input is High

The value which is calculated by the following method using the value written in the EEPROM (EEPROM setting value) and the PnADJ setting value (Coefficient) is reflected to the parameter.

EEPROM setting value x Coefficient = Parameter value switched when port input is High

* The value below the decimal point is rounded off.

Table 9.1-3 Relationship between PnADJ Setting Value and Coefficients

PnADJ setting value	0[h]	1[h]	2[h]	3[h]	4[h]	5[h]	6[h]	7[h]
Coefficient	0	0.125	0.25	0.375	0.5	0.625	0.75	0.875
PnADJ setting value	**8[h]**	**9[h]**	**A[h]**	**B[h]**	**C[h]**	**D[h]**	**E[h]**	**F[h]**
Coefficient	1.125	1.25	1.375	1.5	1.625	1.75	1.875	2

< Note >

If the calculation results exceed the specified bit width, the data is reflected within the range of the bit width from the specified LSB. Therefore, make settings so that the calculation results do not exceed the specified bit width.

When the setting value is switched to a value other than 0[h], set the EEPROM value to a value other than 0[h] so that PnADJ is 0[h] when the port input is High, and perform switching with PnADJ as 0[h].

Calculations can be performed only with the coefficients shown in ”**Table 9.1-3**”. To switch to an arbitrary value, that value must be assigned to a number of ports equivalent to the bit width for that parameter. For example, to switch a parameter with a width of 3 bits to an arbitrary value, assign the respective bits to three port drivers.

9.1.4. Port Driver Setting Method

This section provides examples explaining the parameter setting method for using the port driver.

To Control a 1-bit Parameter with an Input Port Driver

(Example 1)

Assign PGON (CAT9_Byte36_bit3) to port driver P2, and perform pattern generator ON/OFF switching according to High or Low input to P2.

- P2=Low : Normal image (CAT9_Byte36_bit3 = 0[h])
- P2=High : Pattern generator display (CAT9_Byte36_bit3 = 1[h])

See "**9.1.7 Port Driver Setting Reflection Method**" for how to reflect the setting values.

Table 9.1-4 Setting Method for 1-bit Parameters

Parameter		Setting value	Description
P2ADJ	CAT20_Byte7_bit0-3	0[h]	PGON is a 1-bit parameter.
P2WID	CAT20_Byte7_bit4-7	0[h]	PGON bit width is 1 bit. -> Set the (bit width - 1) value.
P2BYTE	CAT20_Byte8_bit0-6	24[h]	PGON is in the 36th Byte. -> Set a hexadecimal value.
P2IOSEL	CAT20_Byte8_bit7	0[h]	P2 is set to input.
P2CAT	CAT20_Byte9_bit0-4	9[h]	PGON is in CAT9.
P2LSB	CAT20_Byte9_bit5-7	3[h]	LSB of PGON is the 3rd bit.

To Control a Multi-bit Parameter with an Input Port Driver

(Example 2)

Assign the 8-bit wide parameter RYGAIN1 (CAT2_Byte37) to port driver P1, and switch the RYGAIN1 gain value according to High or Low input to P1.

- P1=Low : Sets RYGAIN1 to 3F[h] (CAT2_Byte37 = 3F[h])
- P1=High : Sets RYGAIN1 to 1.5 times 3F[h] (5F[h]) (CAT2_Byte37 = 5F[h])

* First set the value of RYGAIN1 to 3F[h] and write to the EEPROM.
(Setting value when port input is Low) (See "**9.1.7 Port Driver Setting Reflection Method**".)

Table 9.1-5 Setting Method for Multi-bit Parameters

Parameter		Setting value	Description
P1ADJ	CAT20_Byte4_bit0-3	B[h]	***1**
P1WID	CAT20_Byte4_bit4-7	7[h]	RYGAIN1 bit width is 8 bits. -> Set the (bit width - 1) value.
P1BYTE	CAT20_Byte5_bit0-6	25[h]	RYGAIN1 is the 37th Byte. -> Set a hexadecimal value.
P1IOSEL	CAT20_Byte5_bit7	0[h]	P1 is set to input.
P1CAT	CAT20_Byte6_bit0-4	2[h]	RYGAIN1 is in CAT2.
P1LSB	CAT20_Byte6_bit5-7	0[h]	LSB of RYGAIN1 is the 0th bit.

***1** P1ADJ setting

P1ADJ is B[h] and the coefficient from "**Table 9.1-3**" is 1.5 times, so the value changes as follows.

(Formula) Parameter value = Value written to the EEPROM x Coefficient
= 3F[h] x 1.5
= 63[d] x 1.5
= 94.5[d] (The operation result below the decimal point is rounded off.)
= 95[d]
= 5F[h]

To Monitor the State of a Parameter with an Output Port Driver

(Example 3)

Assign HVPLL (CAT7_Byte1_bit1) to port driver P3, and switch the P3 output between High or Low according to the HVPLL parameter value.

- H-PLL (CAT7_Byte1_bit1 = 0[h]) : P3=Low output
- V-PLL (CAT7_Byte1_bit1 = 1[h]) : P3=High output

Table 9.1-6 Setting Method for Output 1-bit Parameters

Parameter		Setting value	Description
P3ADJ	CAT20_Byte10_bit0-3	0[h]	0[h] when set as an output port.
P3WID	CAT20_Byte10_bit4-7	0[h]	0[h] when set as an output port.
P3BYTE	CAT20_Byte11_bit0-6	1[h]	HVPLL is in the 1st Byte.
P3IOSEL	CAT20_Byte11_bit7	1[h]	P3 is set to output.
P3CAT	CAT20_Byte12_bit0-4	7[h]	HVPLL is in CAT7.
P3LSB	CAT20_Byte12_bit5-7	1[h]	LSB of HVPLL is the 1st bit.

* When monitoring parameter changes with the output port drivers, one port driver can monitor 1 bit. Therefore a number of ports equal to the number of bits are required to monitor multi-bit parameters.

9.1.5. Shift Function using the Port Drivers

Port Drivers and the Shift Function

The CXD4103 has a shift function.

This shift function makes it possible to easily perform the following controls by providing two external switches and connecting them to the port drivers.

- Manual White Balance gain adjustment (MWB) in the White Balance function
- Phase adjustment in the line lock system

Shift Function Method

The shift function is used for both manual White Balance gain adjustment in the White Balance function and phase adjustment in the line lock system. The controlled register is controlled by changing the SFTUP and SFTDWN parameter value combination as shown in "**Table 9.1-7**".

Table 9.1-7 SFTUP and SFTDWN Control Method

SFTDWN CAT17_Byte18_bit1	SFTUP CAT17_Byte18_bit0	Control specifications	Remarks
0[h]	0[h]	Control off	
0[h]	1[h]	Increment the controlled value	Write adjustment value to EEPROM at 01 -> 00
1[h]	0[h]	Decrement the controlled value	Write adjustment value to EEPROM at 10 -> 00
1[h]	1[h]	PRESET	*

* With the PRESET (1,1), PRSTSFTV, MWBPRESETR, and MWBPRESETB are reflected.
For a detailed description of the controlled parameters, see each control item.

In addition, the SFTUP and SFTDWN operation assignments are determined by the following parameters in order to perform the respective control using the shift function. That is to say, the SFTUP and SFTDWN parameters function as MWB when AWBMODE is set to 4[h], and operate as line lock phase adjustment for all other settings.

Table 9.1-8 SFTUP and SFTDWN Operation Assignments

AWBMODE CAT15_Byte1_bit0-2	MODE	SFTUP/SFTDWN operation assignments
0[h]	ATW	Line lock phase adjustment (SGMODE=1[h])
4[h]	MWB	MWB
2[h]	Push	Line lock phase adjustment (SGMODE=1[h])
6[h]	Hold	
1[h]	User fixed value 1	
5[h]	User fixed value 2	
3[h]	User fixed value 3	
7[h]	User fixed value 4	

Example Port Driver Settings for the Shift Function

The case where SFTUP is controlled from the P0 port and SFTDWN is controlled from the P1 port is shown below as an example of the settings when assigning the shift function to the port drivers.

Table 9.1-9 Example SFTUP Settings

Parameter		Setting value	Description
P0ADJ	CAT20_Byte1_bit0-3	0[h]	SFTUP is a 1-bit parameter.
P0WID	CAT20_Byte1_bit4-7	0[h]	SFTUP bit width is 1 bit. -> Set the (bit width - 1) value.
P0BYTE	CAT20_Byte2_bit0-6	12[h]	SFTUP is in the 18th Byte. -> Set a hexadecimal value.
P0IOSEL	CAT20_Byte2_bit7	0[h]	P0 is set to input.
P0CAT	CAT20_Byte3_bit0-4	11[h]	SFTUP is in CAT17.
P0LSB	CAT20_Byte3_bit5-7	0[h]	LSB of SFTUP is the 0th bit.

Table 9.1-10 Example SFTDWN Settings

Parameter		Setting value	Description
P1ADJ	CAT20_Byte4_bit0-3	0[h]	SFTDWN is a 1-bit parameter.
P1WID	CAT20_Byte4_bit4-7	0[h]	SFTDWN bit width is 1 bit. -> Set the (bit width - 1) value.
P1BYTE	CAT20_Byte5_bit0-6	12[h]	SFTDWN is in the 18th Byte. -> Set a hexadecimal value.
P1IOSEL	CAT20_Byte5_bit7	0[h]	P1 is set to input.
P1CAT	CAT20_Byte6_bit0-4	11[h]	SFTDWN is in CAT17.
P1LSB	CAT20_Byte6_bit5-7	1[h]	LSB of SFTDWN is the 1st bit.

Operation Speed Setting

The operation speed when incrementing and decrementing the controlled value can be adjusted by the following parameter. This parameter can be used for either the MWB or line lock phase adjustment setting.

Table 9.1-11 Parameter for Adjusting the Operation Speed

Parameter		Description
SFTSTEP	CAT17_Byte22_bit0-4	Shifter operation speed setting (STEP width)

9.1.6. Precautions for Port Driver Configuration

Parameters assigned to port drivers cannot be externally controlled. When external control is desired, control must be terminated by removing the port driver assignment or by completing the following parameter settings.

Table 9.1-12 Parameter for Stopping Port Driver Control

Parameter		Description
PDRHOLD	CAT12_Byte5_bit5	1[h]: Port driver hold
CPUHOLD	CAT12_Byte5_bit0	1[h]: CPU hold

The priority ranking of the parameter setting methods is as follows.

The port driver settings have the highest priority of the parameter settings as shown below, so note that the settings written in the EEPROM will be disabled at this time.

To enable the EEPROM settings, do not assign the parameters to port drivers.

1. Port driver control
2. External communication control (computer, external microcontroller, and so on)
3. EEPROM setting values
4. CXD4103 register setting values

9.1.7. Port Driver Setting Reflection Method

The method for reflecting the port driver settings is as follows.

1. Set the initial value when port input is Low in the parameter to be set by the port driver.
2. Set the parameter in the Pn port of CAT20. (See "**9.1.4 Port Driver Setting Method**".)
3. Write CAT20 in the EEPROM.
4. Reset. (Initialize the port driver.)
5. The value of the set parameter switches thereafter according to High or Low input to the Pn port.

9.1.8. Conditions for Disabling the Port Drivers

Port driver control is disabled under the following conditions.

Suppression by the Parameters

Port drivers do not function with port driver parameters CPUHOLD (CAT12_Byte5_bit0) = 1[h] or PDRHOLD (CAT12_Byte5_bit5) = 1[h].

Port Driver Disable Judgment Based on the CAT20 Setting Contents

* When parameter setting is corresponded following conditions, Port drive function is ignored by CAT20 set.

1. If the category number (PnCAT) is "0[h]".
2. If CAT5, CAT22 or CAT23 is set in the category number (PnCAT).
3. If the category number (PnCAT) exceeds the maximum category number.
4. If the byte number (PnBYTE) is "0[h]".
5. If the byte number (PnBYTE) exceeds the maximum byte number of each category.
6. If the byte number with MSB of the data to specify exceeds the maximum byte number of each category.

When the Other Functions are Enabled for Port Driver Pins that are Combined-use with Other Functions

Ports of the port drivers (P4 to P15) serve as combined-use output ports for digital out signal output, VDHD output, OPD Window output.

When the parameters shown in "**Table 9.1-13**" are set to 1[h], the respective functions have priority and the port driver functions are disabled for those ports.

Table 9.1-13 Combined-Use Terminals for Port Driver Output

Parameter		Setting value	Function given priority	Disabled port
YDSEL	CAT1_Byte7_bit4	1[h]	REC656	P8 - P15
VHOUT	CAT1_Byte11_bit6	1[h]	VDHD out	P5, P6
WINDOUT	CAT16_Byte8_bit7	1[h]	OPD Window out	P4

9.2. Y (Luminance Signal) Processing Flow

The Y (luminance signal) signal is processed through the block shown below.

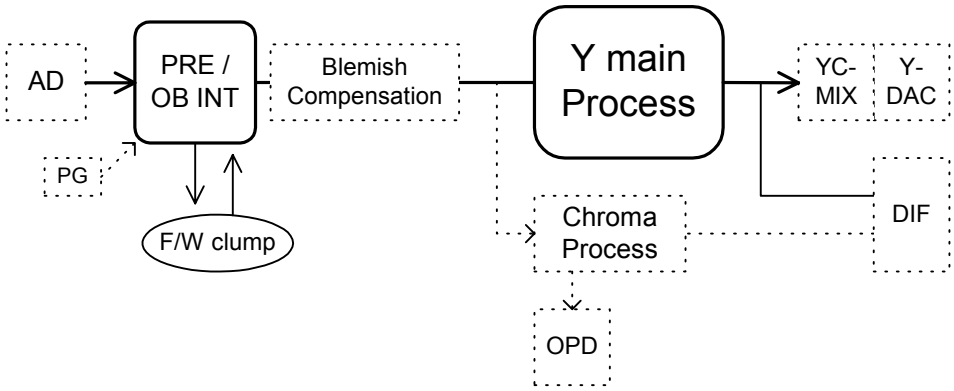


Fig 9.2-1 Overall Flow of Y Signal Processing

The Y signal processing is divided into two stages:

1. Common signal processing (pre-processing), which occurs before branching into OPD (detection integration) and chroma processing
2. Main processing, which applies only to the Y signal

9.2.1. Pre-Block Signal Processing

Pre-block (PRE / OB INT) signal processing includes the following:

- System delay adjustment
- Black level digital clamping
- Blemish detection and compensation. -> See ”**8.4 CCD Blemish Detection and Compensation**”.
- Mirror -> See “**9.13 Mirror Function**”.
- Replacement with built-in PG signal -> See “**9.15 Pattern Generator**”.

System Delay

System Delay is to set the signal processing reference points (effective video start positions) in the DSP.

If the reference points are offset, the system may not operate properly. Be sure to adjust the reference points based on”**Table 9.2-1**”.

Table 9.2-1 System Delay Correspondence Values

Parameter		510H NTSC	510H PAL	760H NTSC	760H PAL
SYSDLY	CAT8_Byte2_bit0-3	D[h]	D[h]	F[h]	F[h]

Black Level Digital Clamping

The black level (reference point) is calculated based on the optical black (OPB) integral value. This black level is used as the reference for the video signal.

The digital clamping process is controlled automatically by the built-in F/W.

9.2.2. Y Signal Main Process

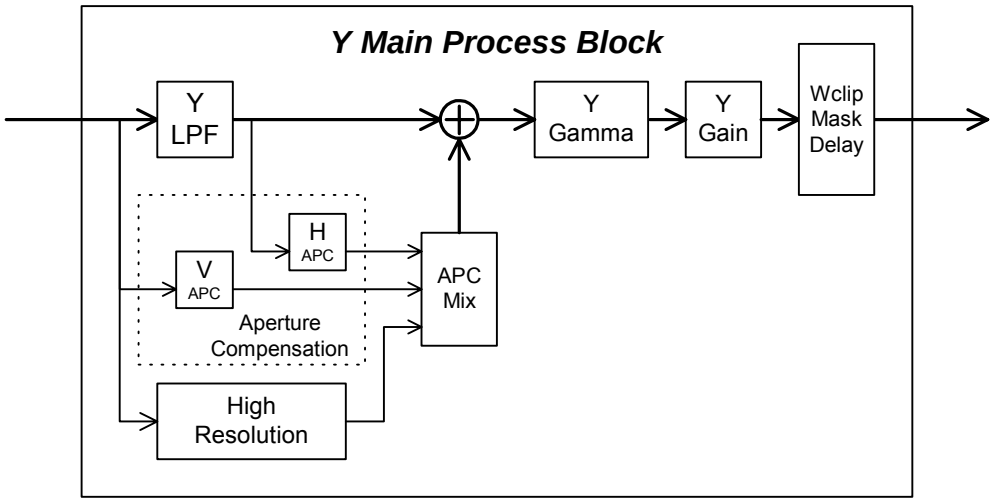


Fig 9.2-2 Y Signal Main Process Block

The Y signal main process includes the following:

- Low pass filter (Y-LPF)
- Detail enhancement
- Negative output
- SETUP level addition
- High luminance clip (White Clip)
- Output delay
- Aperture compensation -> See "**9.8 Aperture Correction**".
- Aperture compensation suppression -> See "**9.9 Suppress**".
- Gamma curve correction -> See "**9.4 Gamma Function**".

Y-LPF

This low pass filter removes the carrier component of the CCD color on-chip filter.

Set YLPFOFF to 0[h] to prevent carrier component interference when using aperture correction processing, etc.

Table 9.2-2 Y Signal LPF Process Parameter

Parameter		Description	Setting value
YLPFOFF	CAT2_Byte1_bit3	Y signal LPF process	0[h]: ON 1[h]:OFF

Detail Enhancement

The built-in detail enhancer operates to enhance faint signals that are hidden by normal aperture correction.
Make the setting with the following parameter.

Table 9.2-3 Y Signal Detail Enhancer Process Parameter

Parameter		Description	Setting value
DEON	CAT2_Byte10_bit7	Detail enhancer process ON/OFF	0 [h]: ON 1 [h]: OFF
DELVSEL	CAT2_ Byte11_bit0	Detail enhancer process strong/weak setting	0[h]: Weak 1[h]: Strong

Negative Output

This function black/white inverts the Y signal after gamma curve correction.
Make the setting with the following parameter.

Table 9.2-4 Positive/Negative Inversion Parameter

Parameter		Description	Setting value
POSNEG	CAT2_Byte10_bit6	Positive/negative inversion function	0[h]: Positive 1[h]: Negative

SETUP Level Addition

A setup level can be added to the video output pedestal.
* This is not affected by gamma curve correction.

Table 9.2-5 SETUP Level Parameter

Parameter		Description	Setting value
SETUP	CAT2_ Byte10_bit0-5	Sets the setup level	0[h] to 3F[h] (0 IRE to 39.5 IRE) Default value: NTSC: C[h] = 7.5 IRE PAL: 00[h] = 0%

High Luminance Clip (White Clip)

The high luminance level can be clipped as a maximum output limiter for the Y signal. Clipping the high luminance makes it possible to prevent white-out.

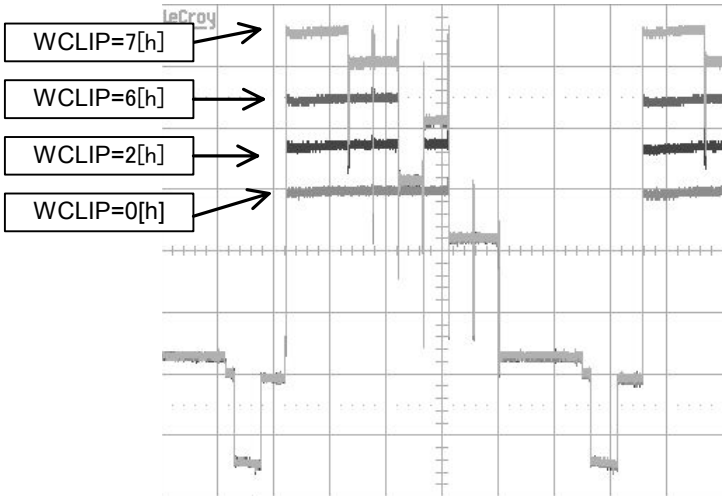


Fig 9.2-3 Example of High Luminance Clip (White Clip)

Table 9.2-6 High Luminance Clip (White Clip) Parameter

Parameter		Description	Setting value
WCLIP	CAT2_Byte9_bit4-6	Clips luminance signal output level	0 [h]: 78%, 1 [h] : 89%, 2 [h]: 100%, 3 [h]: 105%, 4 [h] :111%, 5 [h]: 116%, 6 [h]: 120%, 7 [h]: 153%

Output Delay

The Y signal output can be independently delayed. This function can be used to add a delay difference compared to the chroma signal output or sync signal output.

Table 9.2-7 Y Signal Output Delay Parameter

Parameter		Description	Setting value
YDLY	CAT2_Byte11_bit1-4	Independently delays the luminance signal output	0 [h] -F [h]: 0- 15 pixel delay

9.3. Chroma Signal Processing Block diagram

Extracts RGB primary color signal from the output signal of complementary color filter CCD, performs white balance and gamma processing, and generates R-Y signal and B-Y signal for video output.

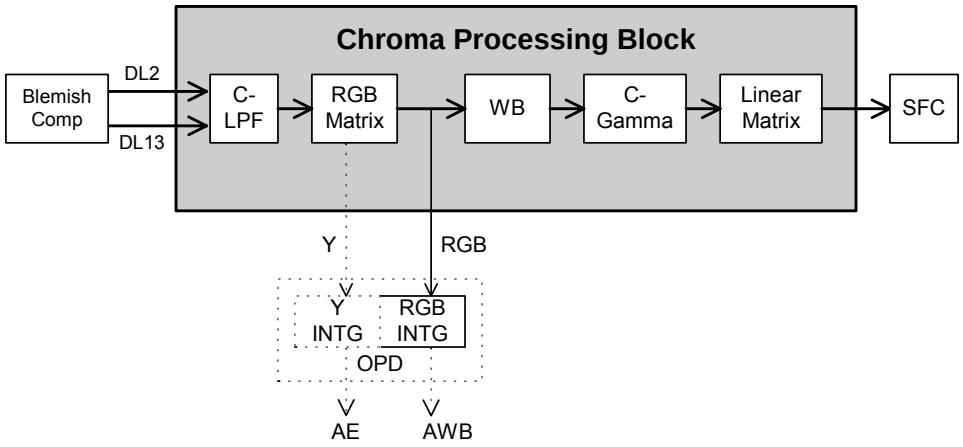


Fig 9.3-1 Chroma Signal Processing Block

9.3.1. Block Description

C-LPF (Chroma Low Pass Filter)

Removes high frequency components and prevents false colors. The complementary color pixel clipping function can also be activated at the same time. See ”**9.3.2 Complementary Color Pixel Clipping**”.

RGB Matrix (Complementary Color Filter CCD Primary Color Separation Circuit)

Color signals (R, G, B) are extracted from the raw data (Mg, Ye, G, Cy) of complementary color filter CCD by matrix operation.

The spectral characteristics of complementary color filter vary with the type of CCD. Therefore, matrix values that correspond to each CCD are necessary. For proper color reproduction and WB operation, see ”**6.4 CCD Primary Color Separation Matrix**” and set the recommended matrix values.

The output signals of RGB matrix are also branched and output to OPD (RGB-INTG), and integrated for AWB. Signals (Y) of luminance components are also generated in the RGB matrix and output to OPD (Y-INTG). These are used in the integration for AE.

WB (White Balance Gain Circuit)

The change in white color under conditions of the photographed subject such as color temperature, are corrected by changing the gain ratio of R, G, B in F/W control (AWB). See ”**9.7 WB Operation**”.

C-Gamma (Chroma-Gamma Correction Circuit)

Gamma/ Knee can be corrected independent of luminance signal processing. See “**9.4 Gamma Function**”.

Linear Matrix (Linear Matrix Circuit)

The final primary color signals R, G, B are converted to color difference signals (R-Y), (B-Y).

Reference values are given in"**Table 6.4-2**" of "**6 CCD Type Selection**" . However, adjust the parameter values to suit the color reproducibility of the connected equipment. Also, see "**9.10 Using Four-Quadrant Independent Control**".

(R-Y) and (B-Y) signals can be suppressed while interlocked with AGC gain. See "**9.9 Suppress**".

9.3.2. Complementary Color Pixel Clipping

Color saturation unevenness can be prevented by changing the saturation difference among the four pixels S1R, S2R, S1B, and S2B. This can be achieved by setting a different clip level for each data prior to chroma signal processing.

Clip levels can be set using the following parameters. The function can be turned off by setting CLSOFF to 1[h].

Table 9.3-1 Complementary Color Pixel Clip Settings

Parameter		Description
CLSOFF	CAT2_Byte29_bit5	Clip function 0[h]: ON 1[h]:OFF
CLS1RL	CAT2_Byte20(LSB)	S1R clip level
CLS1RM	CAT2_Byte25_bit0-2(MSB)	
CLS1BL	CAT2_Byte21(LSB)	S1B clip level
CLS1BM	CAT2_Byte25_bit4-6(MSB)	
CLS2RL	CAT2_Byte22(LSB)	S1R clip level
CLS2RM	CAT2_Byte26_bit0-2(MSB)	
CLS2BL	CAT2_Byte23(LSB)	S1B clip level
CLS2BM	CAT2_Byte26_bit4-6(MSB)	

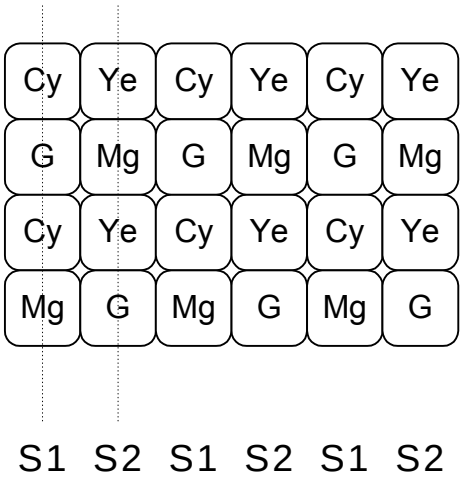


Fig 9.3-2 (Reference) CCD Pixel Array and S1 and S2 Series

9.3.3. Highlight Edge Color Compensation Function

When a subject with very large contrast differences is shot, the edges of the subject may be colored. Set the following parameter to ON to reduce the amount of edge coloring.

* Given that the chroma LPF characteristics are being changed, caution is needed because the function may act to degrade picture quality in the detected area depending on the subject.

Table 9.3-2 Parameters Related to Highlight Edge Color Compensation Function

Parameter		Description
HLEDDL13	CAT2_Byte27_bit4	Operates the color compensation circuit based on horizontal detection in the delay line output after (1+3HD)/2. 0[h]:OFF 1[h]:ON
HLEDDL2	CAT2_Byte27_bit5	Operates the color compensation circuit based on horizontal detection in the delay line output after 2HD. 0[h]:OFF 1[h]:ON
HLEDV	CAT2_Byte27_bit6	Operates the color compensation circuit based on vertical detection in the delay line output after 2HD and (1+3HD)/2. 0[h]:OFF 1[h]:ON

9.4. Gamma Function

9.4.1. Gamma Knee Curve Selection

The SS-11X system has two Gamma knee curves by arbitrary user. The two gamma knee curves are switched by GAMSEL (CAT12_Byte7_bit0).

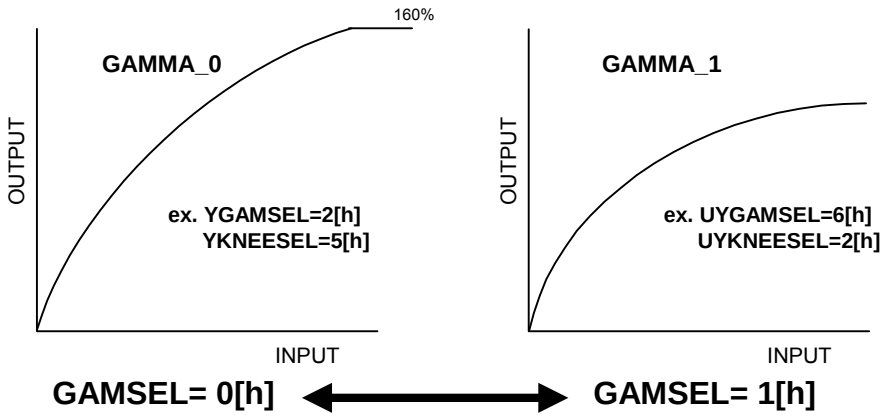


Fig 9.4-1 Gamma Curve Selection

< Note >

The curves shown in "**Fig 9.4-1**" are model curves, and do not represent actual measurements. This is an example when select YGAMSEL=2[h], YKNEESEL=5[h] as GAMMA_0, and UYGAMSEL=6[h], UYKNEESEL=2[h] as GAMMA_1.

See "**9.4.2 Y gamma Knee Curve Setting Method**", "**9.4.4 Chroma Gamma Knee Curve Setting Method**" for the parameter setting method.

Table 9.4-1 Gamma knee Curve selection Parameter

Parameter	Description	Setting value	Applications
GAMSEL (CAT12_Byte7_bit0)	Gamma knee Curve selection	0[h] : GAMMA_0 curve selected	Setting a Gamma knee curve for arbitrary user through following parameters. YGAMSEL(CAT2_Byte7_bit2-4) YKNEESEL(CAT2_Byte7_bit5-7) CGAMMA(CAT2_Byte30_bit0-2) CKNEE(CAT2_Byte30_bit5-7)
		1[h] : GAMMA_1 curve selected	Setting a Gamma knee curve for arbitrary user through following parameters. UYGAMSEL(CAT13_Byte52_bit2-4) UYKNEESEL(CAT13_Byte52_bit5-7) UCGAMMA(CAT13_Byte53_bit0-2) UCKNEE(CAT13_Byte53_bit5-7)
Note Under the default setting (initial setting with no EEPROM), GAMSEL is set to input through port P11.			

9.4.2. Y gamma Knee Curve Setting Method

An arbitrary Y Gamma knee Curve can be set by the user by combinations of YGAMSEL(or UYGAMSEL) (8 types) and YKNEESEL(or UYKNEESEL) (6 types).

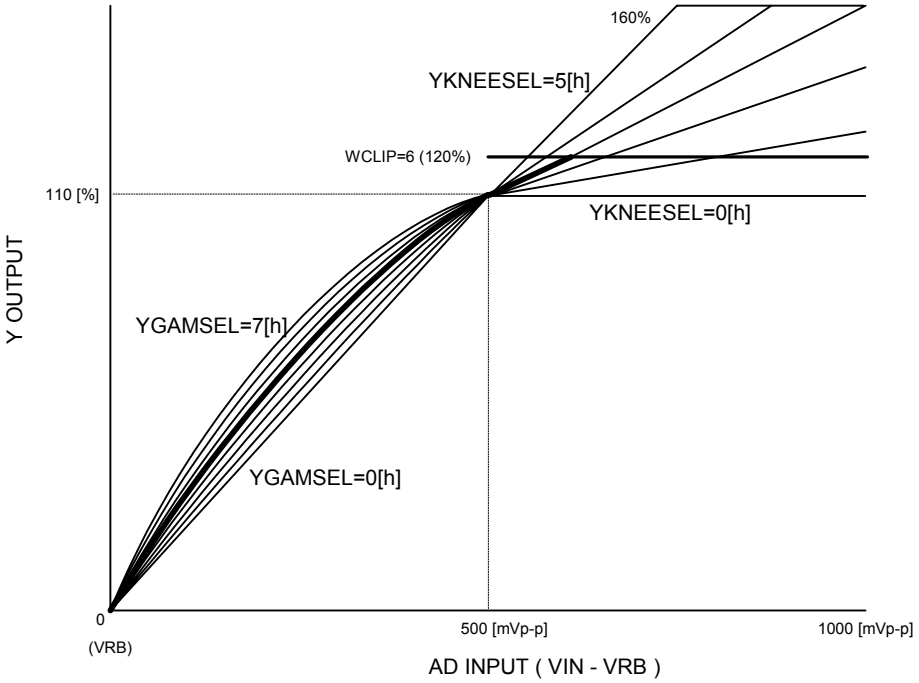


Fig 9.4-2 Y Gamma Curve Setting

Note: The curves in"**Fig 9.4-2**" are model curves, and do not represent actual measurements.

Y Gamma Curve Setting Method

1. Set GAMSEL (CAT12_Byte7_bit0) to 0[h].
   If GAMSEL is assigned for Port Driver, set Port Driver of GAMSEL to 0[h].
2. CPUHOLD (CAT12_Byte5_bit0) to 1[h].
3. Select two Gamma knee curve parameter values using YGAMSEL and YKNEESEL.
   The selected parameter values assign GAMMA_0 (CAT2: YGAMSEL, YKNEESEL) and GAMMA_1 (CAT13: UYGAMSEL, UYKNEESEL).
   (ex. Assign YGAMSEL=2[h], YKNEESEL =5[h] as GAMMA_0, and UYGAMSEL=6[h], UYKNEESEL =2[h] as GAMMA_1)
4. Write CAT2 and CAT13 in the EEPROM, and then restart.
   * See "**4.2 EEPROM Write Method**" for the method of writing to the EEPROM.
5. Switch the two Gamma knee curve by GAMSEL = 0[h] or 1[h]

Table 9.4-2 Y Gamma Knee Curve Parameters (Luminance Signal)

Type	Address	Parameter	Description	Setting value
Parameters for GAMMA_0, which is enabled when GAMSEL = 0[h]	CAT2_Byte7_bit2-4	YGAMSEL	Y gamma selection	0[h] to 7[h]
	CAT2_Byte7_bit5-7	YKNEESEL	Y knee selection	0[h] to 7[h]
	CAT2_Byte6_bit7	YGAMSON	Y Gamma knee Curve compression function for low luminance areas	0[h]: OFF 1[h]: ON
	CAT2_Byte7_bit0	YGAMSLV	Y Gamma knee Curve compression level selection for low luminance areas	0[h]: Strong 1[h]: Weak
Parameters for GAMMA_1, which is enabled when GAMSEL = 1[h]	CAT13_Byte52_bit2-4	UYGAMSEL	Y gamma selection	0[h] to 7[h]
	CAT13_Byte52_bit5-7	UYKNEESEL	Y knee selection	0[h] to 7[h]
	CAT13_Byte54_bit1	UYGAMSON	Y Gamma knee Curve compression function for low luminance areas	0[h]: OFF 1[h]: ON
	CAT13_Byte52_bit0	UYGAMSLV	Y Gamma knee Curve compression level selection for low luminance areas	0[h]: Strong 1[h]: Weak

<Y gamma curve compression in low luminance areas (S compression)>

The contrast can be improved by compressing the Y gamma curve in low luminance areas. Use this function according to the application.

[Setting method]

- UYGAMSON = 1[h] (Y gamma curve compression function ON)
- UYGAMSLV = 0[h]: Strong, 1[h]: Weak (Compression level selection)

<Supplemental explanation>

When using a CRT monitor, select UYGAMSEL = 4[h] and UYKNEESEL = 3[h] to approach the most standard value (gamma = 0.45). This results in Y output of 100 [%] (equivalent to 100 [IRE] in NTSC mode) at AD input of 400 [mVp-p] (100 [%] of standard input).

The gamma characteristics differ for LCD monitors, so select the gamma curve that suits the monitor used.

Y Gamma Curve Confirmation Method

The Y gamma knee curve characteristics can be checked using the built-in pattern generator function.

- Output the pattern generator (Raster Horizontal Ramp).
- Check the Y gamma curve characteristics using an oscilloscope or a waveform monitor.

* See "**9.15 Pattern Generator**" for how to use the pattern generator.

** Note that GAMSEL setting is ignored when CPUHOLD = 1[h]

9.4.3. Y Gamma OFF

A linear Y gamma can be selected when using digital output or when using a monitor with a gamma correction function. (See "**Fig 9.4-3**".)

When YKNEESEL (or UYKNEESEL) is set to 6[h] or 7[h], the curve becomes a "Y Gamma OFF" (6[h]: Standard linear). When set to Y Gamma OFF, YGAMSEL (or UYGAMSEL) setting is ignored.

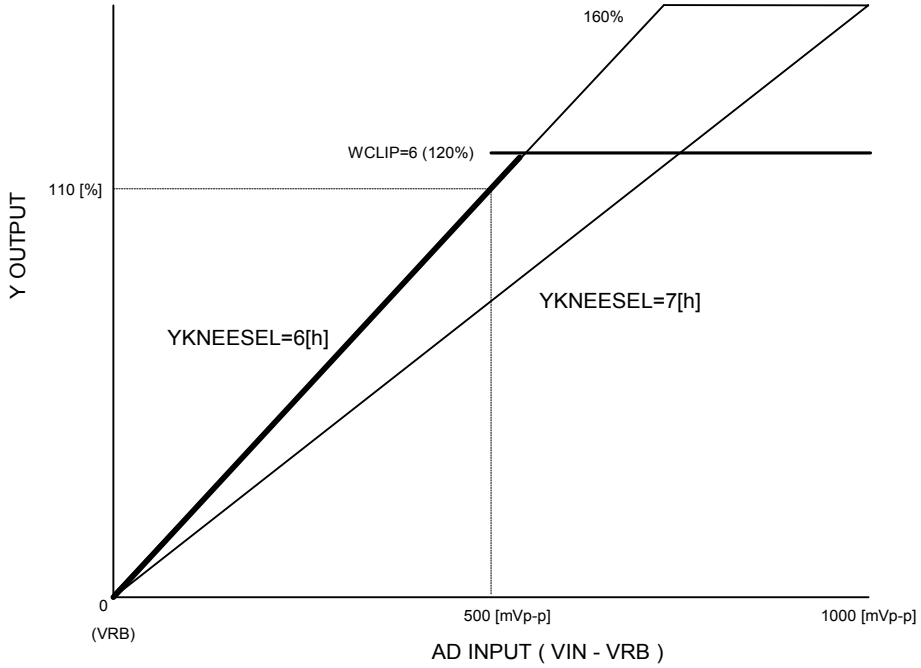


Fig 9.4-3 Y Gamma OFF

9.4.4. Chroma Gamma Knee Curve Setting Method

An arbitrary chroma Gamma knee Curve can be set by the user by combinations of CGAMMA(or U CGAMMA) (8 types) and CKNEE(or UCKNEE) (6 types).

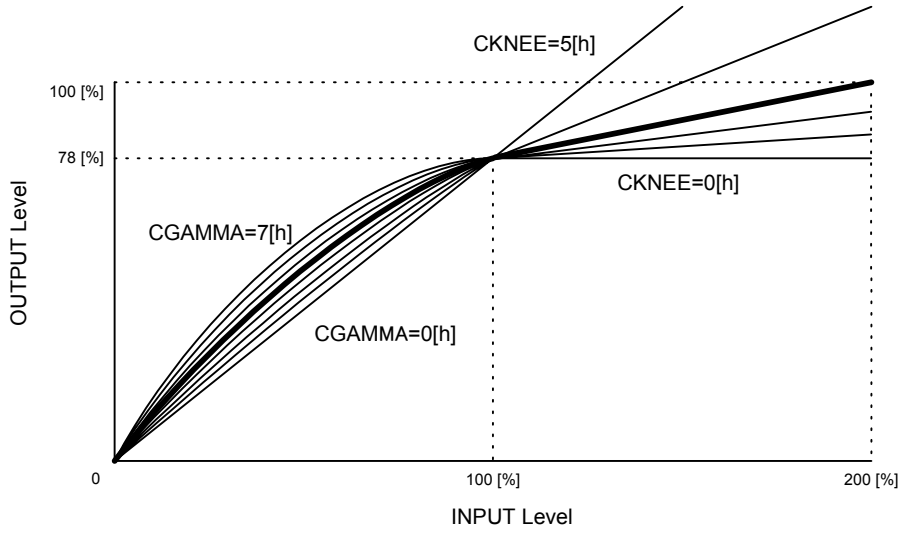


Fig 9.4-4 Chroma Variable Gamma

Note: The curves shown in "**Fig 9.4-4** " are model curves, and do not represent actual measurements.

Chroma Gamma Knee Curve Selection Method

1. Set GAMSEL (CAT12_Byte7_bit0) to 0[h].
   If GAMSEL is assigned for Port Driver, set Port Driver of GAMSEL to 0[h].
2. CPUHOLD (CAT12_Byte5_bit0) to 1[h].
3. Select two Gamma knee curve parameter values using CGAMMA (CAT2_Byte30_bit0-2) for input signal levels up to 100 [%] (1024[d] converted to digital) and CKNEE (CAT2_Byte30_bit5-7) for input signal levels of 100 [%] or more.
   The selected parameter values assign GAMMA_0 (CAT2: CGAMMA, CKNEE) and GAMMA_1 (CAT13: UCGAMMA, UCKNEE).
   (ex. Assign CGAMMA = 2[h], CKNEE = 5[h] as GAMMA_0, and UCGAMMA = 6[h], UCKNEE = 2[h] as GAMMA_1)
4. Write CAT2 and CAT13 in the EEPROM, and then restart.
   * See "**4.2 EEPROM Write Method**" for the method of writing to the EEPROM.
5. Switch the two Gamma knee curve by GAMSEL = 0 or 1[h]

Input signal: RGB signal after white balance correction inside the DSP
Output signal: RGB signal before R-Y and B-Y color difference conversion inside the DSP

Table 9.4-3 Chroma Gamma Knee Curve Parameters

Type	Address	Parameter	Description	Setting value
Parameters for GAMMA_0, which is enabled when GAMSEL = 0[h]	CAT2_Byte30_bit0-2	CGAMMA	Chroma signal variable gamma selection	0[h] to 7[h]
	CAT2_Byte30_bit5-7	CKNEE	Chroma signal variable knee selection	0[h] to 7[h]
Parameters for GAMMA_1, which is enabled when GAMSEL = 1[h]	CAT13_Byte53_bit0-2	UCGAMMA	Chroma signal variable gamma selection	0[h] to 7[h]
	CAT13_Byte53_bit5-7	UCKNEE	Chroma signal variable knee selection	0[h] to 7[h]

<Supplemental explanation>

When using a CRT monitor, select UCGAMMA = 4[h] and UCKNEE = 3[h] to approach the most standard value (gamma = 0.45). This results in an output level of 78 [%] at an input signal level of 100 [%].

Chroma Gamma Curve Confirmation Method

The input and output signals are DSP internal signals, so direct measurement is not possible.

9.4.5. Chroma Gamma OFF

Like Y gamma OFF, chroma gamma OFF can be used to select a linear (straight) chroma gamma curve. (See"**Fig 9.4-5**".)

When CKNEE (or UCKNEE) is set to 6[h] or 7[h], the curve becomes a "Chroma Gamma OFF" (7[h]: Standard linear). When set to Chroma Gamma OFF, CGAMMA (or UCGAMMA) setting is ignored.

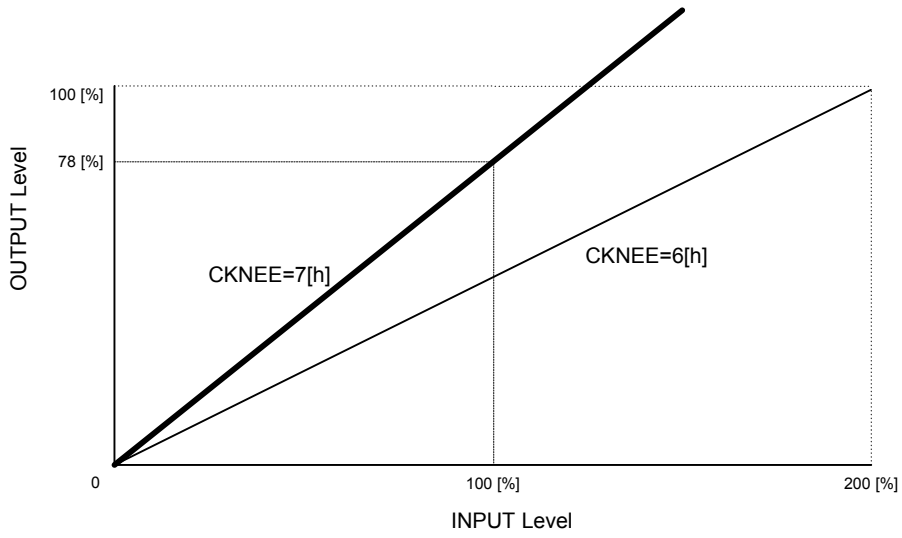


Fig 9.4-5 Chroma Gamma OFF

Note: The curves shown in "**Fig 9.4-5**" are model curves, and do not represent actual measurements.

9.5. OPD Window Setting and Display

The CXD4103's OPD (detection integrating circuit) has an AE/AWB common detection window generation circuit.

9.5.1. Detection Window Setting Method

The entire detection window screen consists of a 15x15 grid extending in the horizontal and vertical directions. It is divided into five areas: WINDOW0, WINDOW1, WINDOW2, WINDOW3 and WINDOW4. Different weightings can be set for each area.

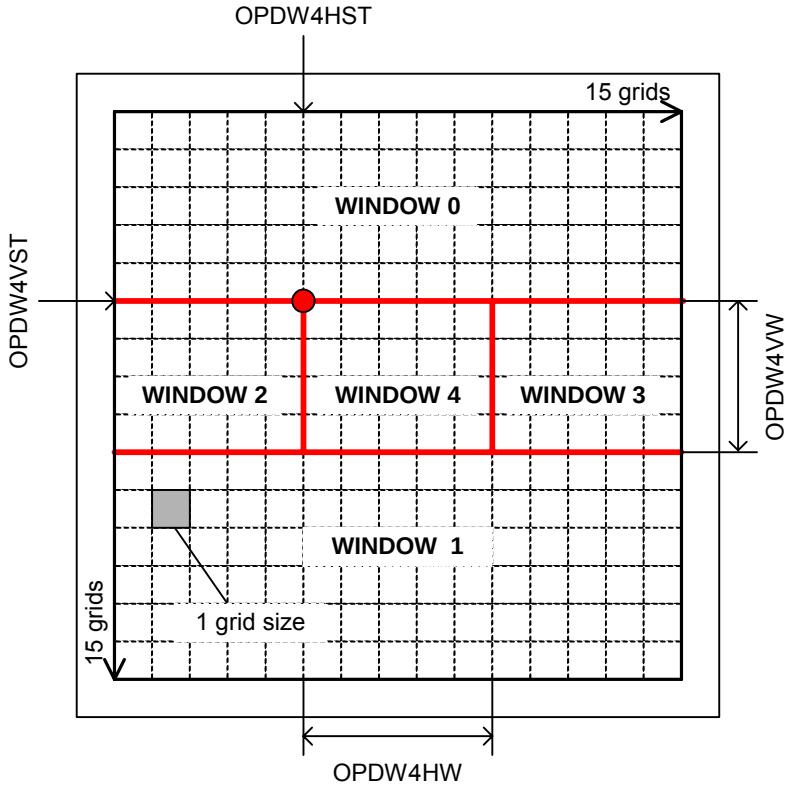


Fig 9.5-1 SS-11X Detection Window

9.5.2. Detection Window Screen Display

We recommend displaying markers on the screen when adjusting the detection window.

Table 9.5-1 Detection Window Display Parameters

Parameter	Description	Remarks
OPDWMK (CAT16_Byte8_bit0)	Displays detection window on monitor when set to "1[h]"	
OPDDISP (CAT16_Byte8_bit1-3)	Selects detection window to be displayed on monitor 1[h]: WINDOW 0 2[h]: WINDOW 1 3[h]: WINDOW 2 4[h]: WINDOW 3 5[h]: WINDOW 4	0,6,7[h]: NONE
WINDOUT (CAT16_Byte8_bit7)	When set to “1[h]”, outputs “High” from “PX” for the WINDOW period set in OPDDISP.	Port X driver control is turned off for the duration of WINDOUT=1[h].

Detection window display (OPDDISP) also permits the display of integration area windows other than weighted windows (WINDOW0 through WINDOW4).

9.5.3. Detection Window Setting Method

When the WINDOW4 starting grid and grid length are setting, the positions and sizes of WINDOW0, WINDOW1, WINDOW2 and WINDOW3 are set automatically.

Table 9.5-2 Detection Window Setting Parameters

Parameter	Description	Setting unit
OPDW4HST (CAT16_Byte5_bit0-3)	(Normal) WINDOW4 horizontal start position	grid
OPDW4VST (CAT16_Byte5_bit4-7)	(Normal) WINDOW4 vertical start position	grid
OPDW4HSTM (CAT16_Byte6_bit0-3)	(Mirror) WINDOW4 horizontal start position	grid
OPDW4VSTM (CAT16_Byte6_bit4-7)	(Mirror) WINDOW4 vertical start position	grid
OPDW4HW (CAT16_Byte7_bit0-3)	(Common) WINDOW4 horizontal grid width	grid
OPDW4VW (CAT16_Byte7_bit4-7)	(Common) WINDOW4 vertical grid width	grid

<Supplemental explanation>

When the mirror function is used, the detection window is set with respect to the horizontally flipped video signal. The window starting position is in the upper left corner after the flip. Adjust the horizontal position of the detection window using the mirror horizontal start position parameters OPDWHSTM and OPDW4HSTM in order to link the mirror function and detection window. The horizontal starting position automatically switches to OPDWHSTM and OPDW4HSTM in conjunction with the MIRROR(CAT1_Byte1_bit4)=1[h] setting. For OPDW4VSTM (mirror WINDOW4 vertical starting position), set the same value as for OPDW4VST (normal WINDOW4 vertical starting position).

9.6. AE Operation

9.6.1. AE Modes

The SS-11X system's AE consists of Normal AE, backlight compensation, flickerless and ME functions. Two types of backlight compensation methods and three types of flickerless methods can be selected. In addition, AE control consists of the AE speed, AGC, AESHUT, AE hysteresis, AEREF and mechanical iris. "**Table 9.6-1**" shows the different function combinations that can be used by AE.

The AE mode parameters are assigned to the ports during the initial settings, and can be turned on and off by DIP switches. (See"**Table 9.6-2**".)

Table 9.6-1 Function Combinations

Control \ Function	Normal AE	Backlight compensation	Flickerless			ME
			NORMFLC	LLFLC	FIXSHTFLC	
AE speed	Yes	Yes	Yes	Yes		
AGC	Yes	Yes	Yes	Yes	Yes	Yes
AESHUT	Yes	Yes	Yes	Yes		Yes
AE hysteresis	Yes	Yes	Yes	Yes	Yes	
AEREF	Yes	Yes	Yes	Yes		Yes
Mechanical iris	Yes	Yes	Yes	Yes	Yes	Yes

Table 9.6-2 Parameters and DIP Switches

Parrameter Name	DIP SW NAME
BLCOFF(CAT14_Byte1_bit2)	BLCOFF(P4)
AEREF(CAT14_Byte1_bit3)	AEREF(P5)
NORMFLC(CAT14_Byte2_bit0)	FLC[0](P6)
AGCMAX(CAT14_Byte1_bit4)	AGCMAX(P7)
AEME(CAT14_Byte1_bit0)	AEME(P8)
AESHUT(CAT14_Byte1_bit6)	AESHUT(P9)

9.6.2. Normal AE

Normal AE can be activated by setting AEME (CAT14_Byte1_bit0) to 0[h]. This mode performs AE control using the electronic iris and AGC.

The AE speed and AGC gain during AE control can be set.

AE Speed

The AE response speed can be set by changing the AESPEED (CAT14_Byte12) value.

Table 9.6-3 AE Speed Setting Parameter

Parameter	Description
AESPEED(CAT14_Byte12)	Adjusts the AE response speed. Set a smaller value for a faster speed, and a larger value for a slower speed.

AGC Control

AGC control realizes the optimum luminance level by increasing the AFE gain in accordance with the luminance.

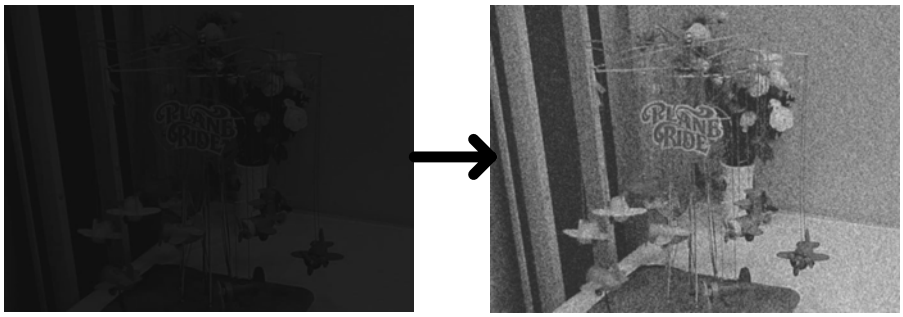


Fig 9.6-1 Image of AGC Control

Note: The photographs above show example images of operation, and may differ from the actual images.

AGC Control Adjustment Parameter

Table 9.6-4 AGC Gain Setting Parameter

Parameter	Description	Settings range
AGCMAX(CAT14_Byte1_bit4)	Switches the AGC maximum gain between two types of values.	0[h]:AGCMAXL 1[h]:AGCMAXH

Table 9.6-5 AGCMAXL

AGCMAXL	ae AGC MAXimum gain Low
Parameter Category	CAT14_Byte15 (8bit)
Outline	Sets the AGC maximum gain.
Conditions	AGCMAX=0[h]
Available settings range	00[h] to FF[h]
Description	The AGC gain maximum value limiter when AGCMAX is 0[h] can be set as shown in the figure "Correspondence of AGCMIN, AGCMAXL, AGCMAXH, and AGC Gain."
Notes	Valid when AGCMAX is 0[h]. Set the AGCMIN value or higher.

Table 9.6-6 AGCMAXH

AGCMAXH	ae AGC MAXimum gain High
Parameter Category	CAT14_Byte16 (8bit)
Outline	Sets the AGC maximum gain.
Conditions	AGCMAX=1[h]
Available settings range	00[h] to FF[h]
Description	The AGC gain maximum value limiter when AGCMAX is 1[h] can be set as shown in the figure "Correspondence of AGCMIN, AGCMAXL, AGCMAXH, and AGC Gain."
Notes	Valid when AGCMAX is 1[h]. Set the AGCMIN value or higher.

Table 9.6-7 AGCMIN

AGCMIN	ae AGC MINimum gain
Parameter Category	CAT19_Byte1 (8bit)
Outline	Sets the AGC minimum gain.
Conditions	
Available settings range	00[h] to FF[h]
Description	The AGC gain minimum value limiter can be set as shown in the figure "Correspondence of AGCMIN, AGCMAXL, AGCMAXH, and AGC Gain."

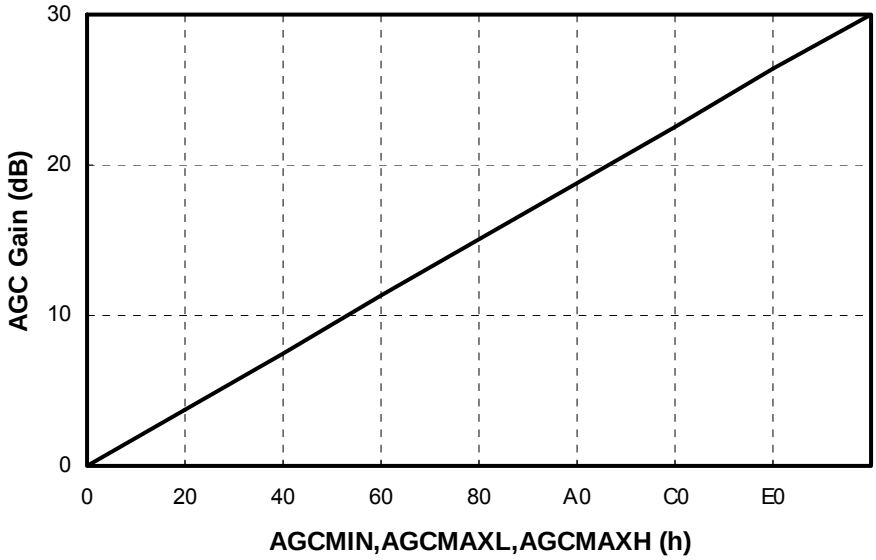


Fig 9.6-2 Correspondence of AGCMIN, AGCMAXL, AGCMAXH, and AGC Gain

9.6.3. Fixed Shutter

Fixed shutter mode can be activated in Normal AE mode by setting AESHUT (CAT14_Byte1_bit6) to 1[h]. At this time, the AE shutter speed is set by SHUTMAX, SHTSEL, and LLFLC. (See "**Table 9.6-8**".)

Table 9.6-8 Electronic Shutter Speed Setting Parameters

Parameter	Description	Settings range
AESHUT(CAT14_Byte1_bit6)	AE shutter mode ON/OFF	0[h]:OFF 1[h]:ON
SHUTMAX(CAT14_Byte17)	Electronic shutter speed maximum value	0[h] to FF[h]
SHTSEL(CAT14_Byte3_bit2-4)	Electronic shutter speed selector	0[h] to 7[h]
LLFLC(CAT14_Byte2_bit1)	Low-speed shutter limiter flickerless	0[h]:OFF 1[h]:ON

Table 9.6-9 Example of Setting the Shutter Speed (NTSC)

Shutter Speed [sec]	LLFLC	SHUTMAX	SHTSEL
1/60	0[h]	FF[h]	0[h]
1/100	1[h]	FF[h]	0[h]
1/250	0[h]	31[h]	7[h]
1/500	0[h]	AA[h]	3[h]
1/1,000	0[h]	A9[h]	4[h]
1/2,000	0[h]	D3[h]	4[h]
1/4,000	0[h]	CA[h]	5[h]
1/10,000	0[h]	CD[h]	6[h]
1/100,000	0[h]	FF[h]	7[h]

Table 9.6-10 Example of Setting the Shutter Speed (PAL)

Shutter Speed [sec]	LLFLC	SHUTMAX	SHTSEL
1/50	0[h]	FF[h]	0[h]
1/120	1[h]	FF[h]	0[h]
1/250	0[h]	BD[h]	2[h]
1/500	0[h]	B4[h]	3[h]
1/1,000	0[h]	B0[h]	4[h]
1/2,000	0[h]	AD[h]	5[h]
1/4,000	0[h]	93[h]	7[h]
1/10,000	0[h]	F9[h]	5[h]
1/100,000	0[h]	FF[h]	7[h]

*LLFLC is set 1[h](=ON) when using Flickerless Function. See “**9.6.5 Flickerless Function**”.

9.6.4. Backlight Compensation

The SS-11X system offers a backlight compensation function.

This backlight compensation mode can be activated by setting BLCOFF (CAT14_Byte1_bit2) to 0[h].

Backlight compensation mode is effective for a backlighted subject such as shown in the left side of "**Fig 9.6-3**" . The subject is compensated and appears as shown in the right side of "**Fig 9.6-3**".

In addition, there are two methods, Weighted average mode and Compensation Gain Fixed mode for backlight compensation.

Backlight compensation method can be selected by switching BLCSEL(CAT14_Byte4_bit0).

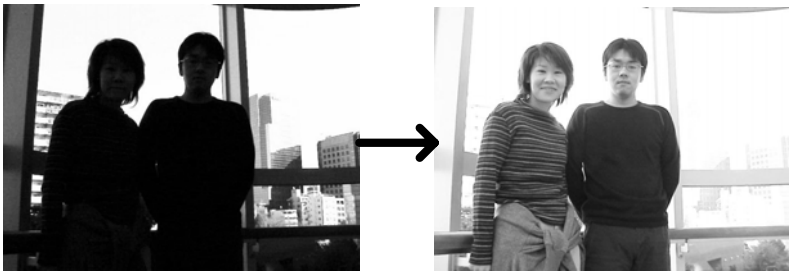


Fig 9.6-3 Backlight Compensation

Note: The photographs above show example images of operation, and may differ from the actual images.

Table 9.6-1 BLCSEL

Parameter	Description
BLCSEL(CAT14_Byte4_bit0)	Selection backlight compensation method 0[h] : Weighted average mode 1[h] : Compensation Gain Fixed mode

Weighted Average mode

Weighted average mode for backlight compensation can be accessed by making BLCSEL = 0[h].

The screen is divided into five detection windows. Each window's integral value for exposure is multiplied by the weighting value for backlight compensation based on the weighted average. It is suitable for when the main subject remains motionless on screen. (See “**Fig 9.6-4**”.)

For windows 0 to 4, the weighting to be applied can be assigned separately. The range is 0[h] to F[h]. Each window's weighting value is specified in the parameters shown in the ”**Table 9.6-11**” For details on how to specify OPD detection windows, see ”**9.5 OPD Window Setting and Display**”.

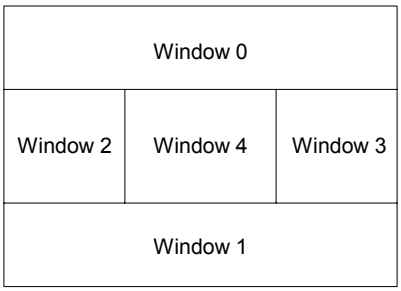


Fig 9.6-4 AE Detection Windows of OPD

Note

If set so that the size of window 4 is extremely small and the weighting of windows 0 to 3 is 0[h], it will cause rounding errors from the internal calculation. Care should be taken because this worsens the accuracy of AE operation, resulting in an effect like oscillation.

Table 9.6-11 Detection Windows Weighting Values

Parameter	Description
AEW0 (CAT14_Byte6_bit0-3)	Window 0 weighting value
AEW1 (CAT14_Byte6_bit4-7)	Window 1 weighting value
AEW2 (CAT14_Byte7_bit0-3)	Window 2 weighting value
AEW3 (CAT14_Byte7_bit4-7)	Window 3 weighting value
AEW4 (CAT14_Byte8_bit0-3)	Window 4 weighting value

Compensation Gain Fixed mode

Compensation gain fixed mode for backlight compensation can be accessed by making BLCSEL = 1[h].

Backlight compensation is performed in compensation gain fixed mode by reducing the luminance integral average value only by the compensation gain (fixed value) specified in the parameter FBLCGAIN (CAT14_Byte5).

The available compensated gain range by FBLCGAIN is depended on FBLCGAINSEL (CAT14_Byte4_bit1). When FBLCGAINSEL (CAT14_Byte4_bit1) sets to 0[h], the range x0.0 to x4.0, and the other when FBLCGAINSEL (CAT14_Byte4_bit1) sets to 1[h], the range x1.0 to x1024.(See "fig8.6-13")

Table 9.6-12 FBLCGAIN

Parameter	Description
FBLCGAIN (CAT14_Byte5)	Compensation gain adjustment

Table 9.6-13 FBLCGAINSEL

Parameter	Description
FBLCGAINSEL(CAT14_Byte4_bit1)	Adjustment compensation range 0[h] : x0.0～x4.0 1[h] : x1.0～x1024.0

9.6.5. Flickerless Function

A flickerless function is available with the SS-11X system.

Modes are selected through the parameters for NORMFLC, LLFLC, and FIXSHTFLC as indicated in the table. (See "**Table 9.6-14**") The flickerless mode is selected by setting one of NORMFLC, LLFLC or FIXSHTFLC to 1[h]. When multiple modes are set to be ON, the mode with the smaller value for the priority ranking value is selected.

Flickerless mode performs control using AGC and the electronic shutter as shown in the table below.

Table 9.6-14 Flickerless Mode

Parameter	Description	Settings range	Priority
NORMFLC(CAT14_Byte2_bit0)	Flickerless mode	0[h]:OFF 1[h]:ON	3
LLFLC(CAT14_Byte2_bit1)	Low-speed shutter limiter mode	0[h]:OFF 1[h]:ON	2
FIXSHTFLC(CAT14_Byte2_bit2)	Electronic shutter fixed flickerless mode NTSC:1/100[sec] PAL:1/120[sec]	0[h]:OFF 1[h]:ON	1

Table 9.6-15 Flickerless Control Devices

Mode	AGC	Electronic shutter	Mode switching
Flickerless mode	Yes	Yes	
Low-speed shutter limiter mode	Yes	Yes	Yes
Electronic shutter fixed flickerless mode		Yes	

Flickerless Mode

When NORMFLC (CAT14_Byte2_bit0) is 1[h] and AGCOFF (CAT14_Byte1_bit7), SHUTFLOF (CAT14_Byte2_bit4), and AGCFLOF (CAT14_Byte2_bit3) are all 0[h], flickerless mode results.

This mode performs control using both AGC and the electronic shutter.

Low-Speed Shutter Limiter Mode

Low-speed shutter limiter flickerless mode is activated by setting LLFLC to 1[h].

In this mode, the electronic shutter is controlled and the longest exposure time is set at 1/100 [s] for NTSC and 1/120 [s] for PAL. When the subject is dark, control is the same as for electronic shutter fixed flickerless mode, and when bright, control is the same as for flickerless mode.

Electronic Shutter Fixed Flickerless Mode

Electronic shutter fixed flickerless mode is activated by setting FIXSHTFLC to 1[h]. In this mode, the shutter speed is fixed at 1/100 [s] for NTSC and 1/120 [s] for PAL. This mode controls flicker by making the shutter speed in each TV mode match the emission cycle for the fluorescent light, which is the cause of flicker.

9.6.6. AE Hysteresis Function

AE hysteresis function is available with the SS-11X system. Using this function can enhance AE stability, even in moments when the luminance level changes, such as when objects momentarily cross in front of the screen.

Table 9.6-16 AESTAB

AESTAB	AE STABility
Parameter Category	CAT14_Byte9 (8bit)
Outline	The threshold value at which AE control stops can be set.
Conditions	AEHYST>0, AEWAIT>0, AEHYST>AESTAB
Available settings range	00[h] - FF[h]
Description	This setting specifies the threshold value for AE operation to stop after it is in effect. 0[h] (none) to FF[h] (maximum)
Notes	

Table 9.6-17 AEHYST

AEHYST	AE HYSTeresis
Parameter Category	CAT14_Byte10 (8bit)
Outline	The threshold value at which AE control starts can be set.
Conditions	AEHYST>0, AEWAIT>0, AEHYST>AESTAB
Available settings range	00[h] - FF[h]
Description	Specifies the dead zone relevant to fluctuations in subject luminance. 0[h] (no dead zone) to FF[h] (dead zone maximum) If the setting value is too small, AE tracks even minimal fluctuations in the luminance, and the hysteresis function is less effective. Excessive values, on the other hand, make differences in the luminance level obvious when AE reaches convergence.
Notes	When AEHYST = 0[h], the AE hysteresis function is deactivated.

Table 9.6-18 AEWAIT

AEWAIT	AE WAIT time
Parameter Category	CAT14_Byte11 (8bit)
Outline	The hysteresis counter can be set.
Conditions	AEHYST>0, AEWAIT>0, AEHYST>AESTAB
Available settings range	00[h] - FF[h]
Description	The greater the value, the less responsive AE is with respect to momentary fluctuations of the subject's luminance level. The smaller the value, the more responsive the reaction.
Notes	

9.6.7. AE Mechanical Iris Mode

This is an example of a lens with an automatic iris which operates using a power supply and video signal.

In AE mode, if MIRIS (CAT14_Byte1_bit1) is set to 1[h], then Mechanical Iris Mode is set.

In this mode, the shutter speed is always 1/60 sec for NTSC and 1/50 sec for PAL, and the backlight compensation amount is output and supplied as a voltage to an external circuit using the CXD4103's internal EVR1 according to EVR1CNT(CAT8_Byte4). The AE operation is performed using AGC control based on the microcontroller's AE, and the mechanical iris inside the external lens.

Example Configuration of Mechanical Iris using EVR1CNT

The CCDLEVEL signal of CXA2096N is used as the video signal. Exposure can be controlled using the lens iris by adjusting the level of this signal with a pre-amp circuit and then controlling the signal amplitude with a VCA (voltage control amplifier) that is controlled by the EVR1CNT voltage.

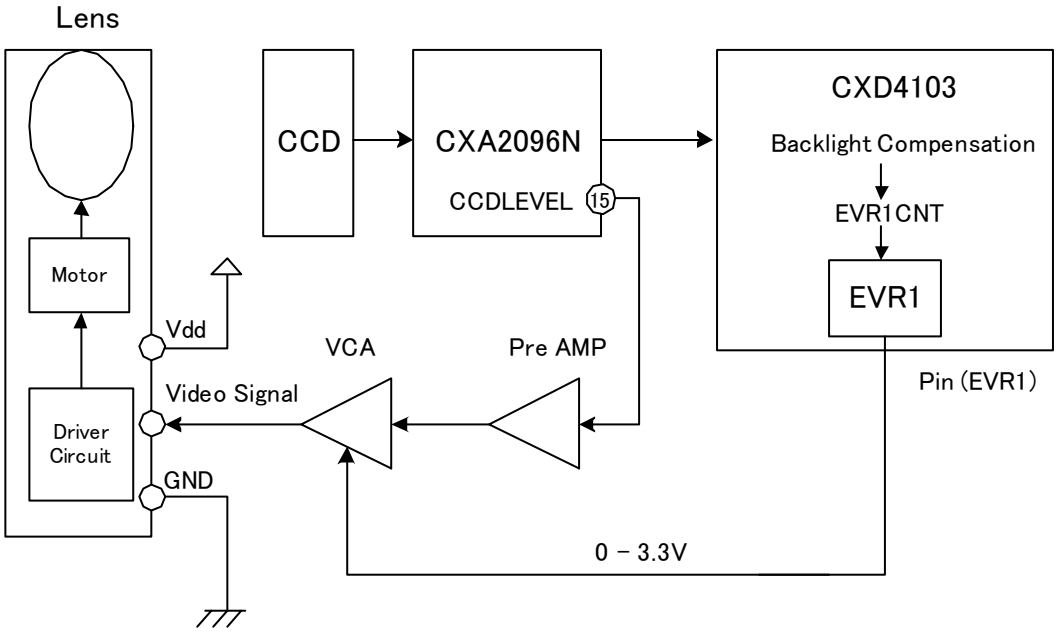


Fig 9.6-5 Example Configuration of Video Servo Mechanical Iris

Parameters for Setting VCA Characteristics for Mechanical Iris Control

The voltage to be output to VCA(Voltage Control Amplifier) is set through the following parameters.

The characteristics set through the following parameters are output through EVR1 (EVR1CNT). (See "**Fig 9.6-6**".)

Set the VCA characteristics setting parameters according to the characteristics of the VCA (Voltage Control Amplifier) used.

Table 9.6-19 Parameters for Setting VCA Characteristics for Mechanical Iris Control

Parameter	Description
VCAM12(CAT14_Byte21)	EVR value when mechanical iris backlight compensation is -12dB
VCAM6(CAT14_Byte22)	EVR value when mechanical iris backlight compensation is -6dB
VCA0(CAT14_Byte23)	EVR value when mechanical iris backlight compensation is 0dB

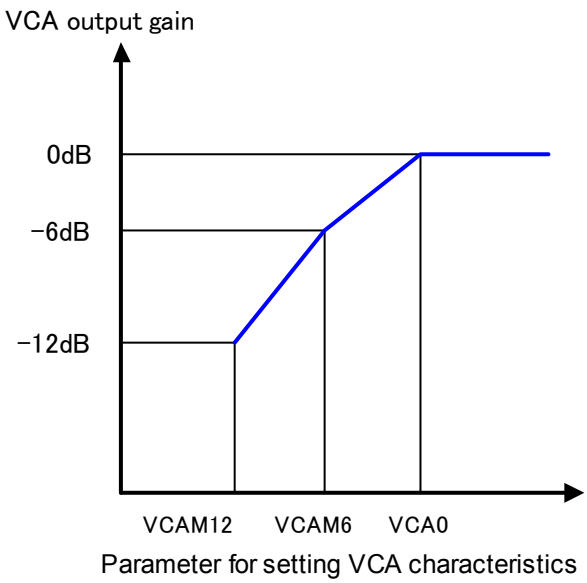


Fig 9.6-6 Example VCA settings (control range: -12dB to 0dB)

Note

"**Fig 9.6-6**"is an example in which a Rohm BA7655AF is used as the VCA, and a control range of -12dB to 0dB is used when there is backlight. The maximum value is 0dB, with VCA0=VCAP6=VCAP12.

Sony has only evaluated controls (with backlight) in the range of VCA -12dB to 0dB.

9.6.8. AE Reference

AE reference mode is activated by setting AEREF (CAT14_Byte1_bit3) to 1[h].
In this mode, the AE convergence level (AE reference) can be selected by AEUSER (CAT14_Byte13).
See "**Table 9.6-21**" for the references that can be selected.

Table 9.6-20 AEUSR

AEUSR	AE USR setting level
Parameter Category	CAT14_Byte13 (4bit)
Outline	Sets the AE convergence exposure (AE reference).
Conditions	AEREF=1[h] (USR)
Available settings range	0[h] - F[h]
Description	The white video level when shooting a test chart can be set as shown in "**Table 9.6-21**".
Notes	

Table 9.6-21 AEUSR and AE Convergence Values

AEUSR	Convergence level [IRE]
0[h]	Approx. 60
1[h]	65
2[h]	70
3[h]	75
4[h]	80
5[h]	85
6[h]	90
7[h]	95
8[h]	100
9[h]	105
A[h]	110
B[h]	115
C[h]	120
D[h]	400 mV adjustment reference for AGCMIN
E[h] and F[h]	100

9.6.9. ME Mode

ME (Manual Exposure) mode is activated by setting AEME (CAT14_Byte1_bit0) to 1[h]. In manual mode, a fixed shutter speed and a fixed gain are selected and sent to the TG and AGC.

Shutter Speed

In ME mode, the shutter speed can be set with SHUTMAX, SHTSEL, and LLFLC in the same manner as Normal AE mode. (See "**Table 9.6-9**" and "**Table 9.6-10**".)

AGC Gain

The AGC gain can be set by AEREF (CAT14_Byte1_bit3) and BLCOFF (CAT14_Byte1_bit2). (See "**Table 9.6-22**".)

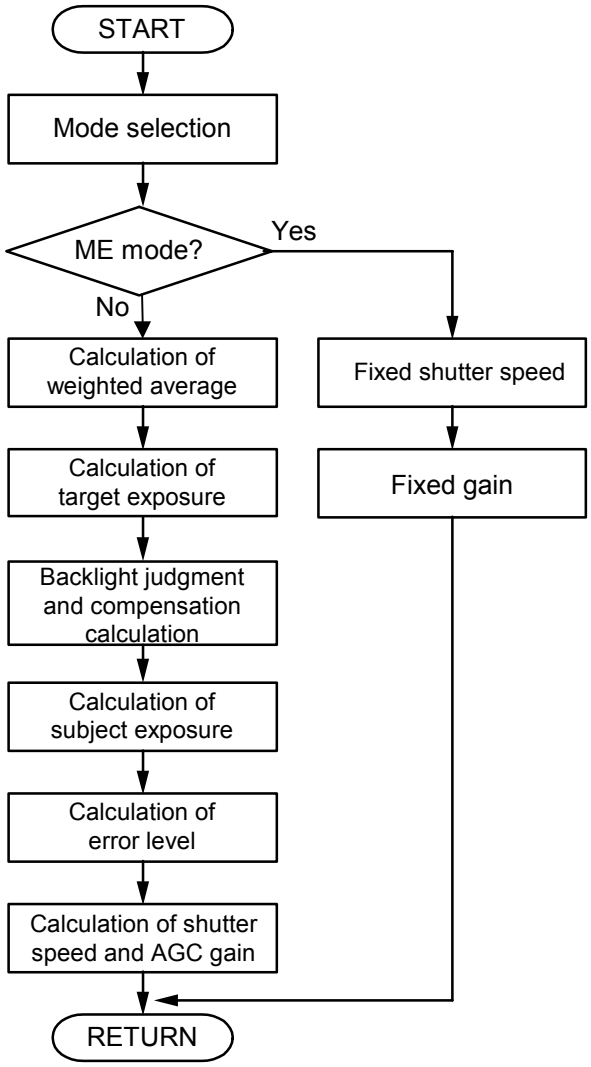
Table 9.6-22 AGC Gain in ME Mode

Parameter	Combinations of BLCOFF and AEREF			
BLCOFF(CAT14_Byte1_bit2)	0[h]	1[h]	0[h]	1[h]
AEREF(CAT14_Byte1_bit3)	0[h]	0[h]	1[h]	1[h]
AGC gain (dB)	Approx. 5	Approx.13	Approx.22	Approx.30

The AGC gain values in the above "**Table 9.6-22**" are the values when AGCMAX = FF[h] and AGCMIN = 28[h].

9.6.10. Detailed Description of AE Operation

Sequence of AE Operation



Processing is branched in modes accepting from DIP switches or serial communication input.

In ME mode, fixed shutter speed and fixed gain are selected before sending to TG and AGC.

A judgment regarding backlight conditions is made based on the data from OPD, and compensation for it is calculated.

In AE mode, the subject exposure is calculated from the integral value of each OPD window.

Shutter speed and AGC gain are obtained from the subject exposure.

Fig 9.6-7 AE Flowchart

AE Scale

AE control performs calculation from the electronic shutter region to the AGC region using a single AE scale. The control devices used to perform AE control include the electronic shutter, AGC gain and Y gain. (See ”**Fig 9.6-8**”.)

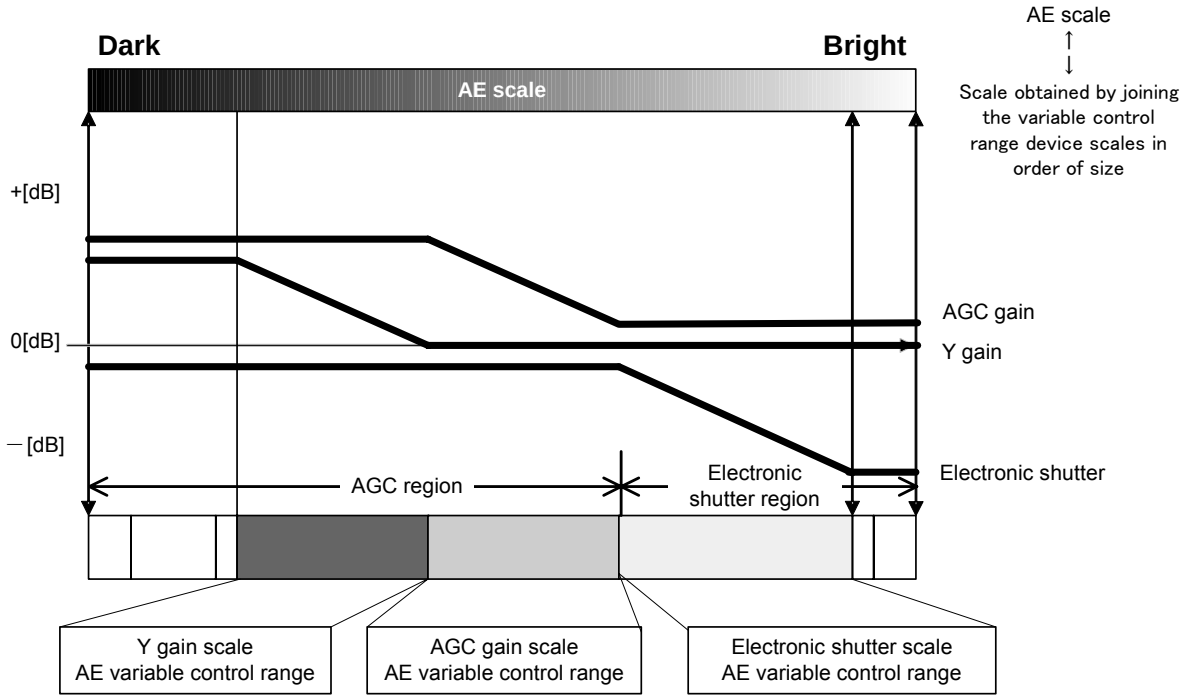


Fig 9.6-8 AE Scale (Model Image)

9.7. WB Operation

Always perform pre white balance adjustment to ensure proper WB operation. Pre white balance adjustment is performed to create the operation frame used by WB.

See "**8.3 Pre-White Balance Adjustment**".

9.7.1. WB Modes

The modes shown in "**Table 9.7-1**" can be selected by switching AWBMODE (CAT15_Byte1_bit0-3) or by the port 0 to port 2 settings.

When switching the mode with the parameter, change the value of AWBMODE (CAT15_Byte1_bit0-3). When switching the mode with the port drivers, the mode can be changed with port 0 to port 2.

Table 9.7-1 WB Modes

MODE	Port0	Port1	Port2	AWBMODE
ATW	0	0	0	0[h]
Manual White Balance	0	0	1	4[h]
Push	0	1	0	2[h]
Hold	0	1	1	6[h]
User fixed value 1	1	0	0	1[h]
User fixed value 2	1	0	1	5[h]
User fixed value 3	1	1	0	3[h]
User fixed value 4	1	1	1	7[h]

9.7.2. ATW

ATW is the Auto Trace White balance mode.

ATW detects the R, G and B before the white balance gain amplifier and automatically aligns the white balance based on those results. (feedforward control system)

9.7.3. MWB (Manual White Balance)

When adjusting the R gain, the B gain is also adjusted following the black body radiation curve.

Adjustment is performed using the parameters SFTUP (CAT17_Byte18_bit0) and SFTDWN (CAT17_Byte18_bit1). (See "**Table 9.7-2**" .)

Setting SFTUP (CAT17_Byte18_bit0) to 1[h] shifts toward the high color temperature side, and setting SFTDWN (CAT17_Byte18_bit1) to 1[h] shifts toward the low color temperature side.

The adjustable color temperature range is low color temperature (approximately 2500K) to high color temperature (approximately 9500K) saved at the time of pre-white balance adjustment.

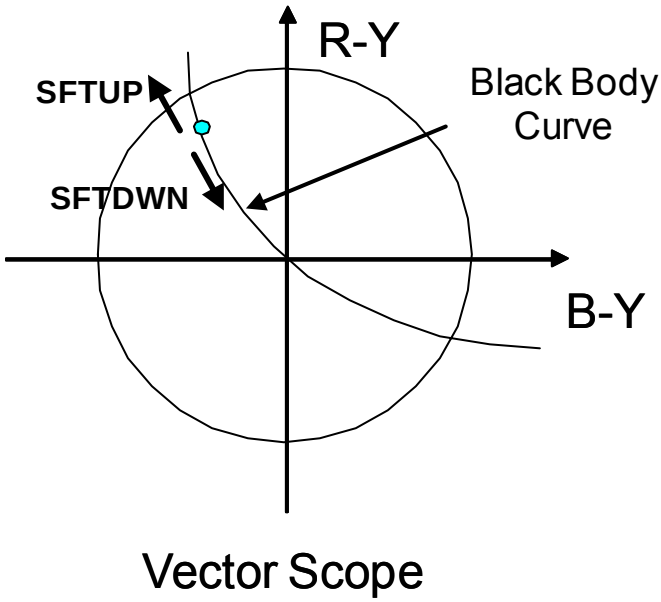


Fig 9.7-1 Trace Curve for Manual White Balance (image)

In MWB mode, the value when adjustment is performed with SFTUP and SFTDWN is reflected to WBR and WBB. (See "**Table 9.7-3**".)

When adjustments are made with SFTUP and SFTDWN and then these parameters are set to 0[h], the gain at that time is saved in PLRGAIN and PLBGAIN, and written in the EEPROM. (See "**Table 9.7-4**" .) To start up using the gain value written to EEPROM, perform a reset start while in MWB mode.

If both SFTUP and SFTDWN are set to 1[h], the preset values which are set in advance (MWBPRESETR and MWBPRESETB in "**Table 9.7-5**"are reflected to WBR or WBB.

Table 9.7-2 MWB Related Parameters

Parameter	Description	Settings range
SFTUP(CAT17_Byte18_bit0)	Increment	1[h]:R gain UP (B gain linked)
SFTDWN(CAT17_Byte18_bit1)	Decrement	1[h]:R gain DOWN (B gain linked)

Table 9.7-3 Parameters Controlled by SFTUP/SFTDWN Adjustment Values

Parameter	Description
WBR(CAT4_Byte1)	White balance gain R
WBB(CAT4_Byte3)	White balance gain B

Table 9.7-4 Parameter for Saving WBR/WBB Adjustment Value

Parameter	Description
PLRGAIN(CAT15_Byte33)	Saving WBR adjustment value
PLBGAIN(CAT15_Byte34)	Saving WBB adjustment value

Table 9.7-5 WB Gain Parameters When Using Presets

Parameter	Description
MWBPRESETR(CAT19_Byte10)	WBR setting for presets
MWBPRESETB(CAT19_Byte11)	WBB setting for presets

9.7.4. Push

Push mode has no operation frame, and performs correction so that the R:G:B evaluation value is always 1:1:1.

In addition, the convergence speed can be adjusted by ALLSTEP (CAT15_Byte32). Reducing this parameter value increases the convergence speed.

Note that luminance specific integration is not performed in this mode.

Table 9.7-6 Push Related Parameter

Parameter	Description	Settings range
ALLSTEP(CAT15_Byte32)	Adjusts the push convergence speed	0[h]: Maximum speed FF[h]: Minimum speed

9.7.5. Hold

When operation shifts to hold mode, white balance control is stopped and the gain value is held in the condition before the mode transition. Also, when shifting to hold mode from push mode, the gain value at that time is stored in the EEPROM, so push lock mode can be realized by using hold mode in combination with push mode.

In addition, conventional push lock mode and trigger system push lock mode can be switched by switching the parameter AWBTRG (CAT15_Byte2_bit1).

1. Conventional push lock mode (AWBTRG=0[h])
   Operation is performed in push mode while the button is pressed and shifts to hold mode when the button is released, the white balance gain at that point is set in the parameters in "**Table 9.7-4**".

2. Trigger system push lock mode (AWBTRG=1[h])
   Operation shifts to push mode when the button is pressed and convergence operation continues even if the button is released. When convergence is automatically judged to be completed, the white balance gain at that point is set in the parameters in "**Table 9.7-4**" and written to the EEPROM. To start up using the gain value written to EEPROM, perform a reset start while in HOLD mode.

9.7.6. User Fixed Value

In this mode, the white balance gain is set to a preset value. Four different patterns of setting values can be stored. The default values are as shown in the "**Table 9.7-7**".

Table 9.7-7 User Fixed Value

Parameter	Description	Initial Value
WBUSRR1(CAT15_Byte35)	User R gain 1	76[h] (approx. 4700K)
WBUSRB1(CAT15_Byte36)	User B gain 1	34[h] (approx.4700K)
WBUSRR2(CAT15_Byte37)	User R gain 2	53[h] (approx.3200K)
WBUSRB2(CAT15_Byte38)	User B gain 2	44[h] (approx.3200K)
WBUSRR3(CAT15_Byte39)	User R gain 3	65[h] (approx.4200K)
WBUSRB3(CAT15_Byte40)	User B gain 3	39[h] (approx.4200K)
WBUSRR4(CAT15_Byte41)	User R gain 4	8F[h] (approx.6300K)
WBUSRB4(CAT15_Byte42)	User B gain 4	2A[h] (approx.6300K)

9.7.7. Monitor Function

White Balance Gain Output Mode

White Balance gain output mode is activated by setting ADJMODE to 31[h].

This mode outputs the white balance gain value during AWB operation on AWBOUT1 to 3. See ”**Table 9.7-8**” for a detailed description.

Note that this mode can be used in combination with all AWBMODE settings. In addition, AWB operates normally.

Table 9.7-8 Outputs in White Balance Gain Output Mode

Parameter	WB gain value
AWBOUT1(CAT23_Byte1)	R gain (WBR(CAT4_Byte1))
AWBOUT2(CAT23_Byte2)	G gain (WBG(CAT4_Byte2))
AWBOUT3(CAT23_Byte3)	B gain (WBB (CAT4_Byte3))
AWBOUT4(CAT23_Byte4)	Fixed to "0[h]"

OPD Evaluated Value Output Mode

OPD evaluated value output mode is activated by setting ADJMODE to 32[h].

OPD evaluated value output mode outputs the AWB control OPD evaluation value on AWBOUT1 to AWBOUT4. See ”**Table 9.7-9**” for the respective output values.

Table 9.7-9 Outputs in OPD Evaluated Value Output Mode

Parameter	Output value
AWBOUT1(CAT23_Byte1)	R/G as viewed from 3200K (lower)
AWBOUT2(CAT23_Byte2)	R/G as viewed from 3200K (upper)
AWBOUT3(CAT23_Byte3)	B/G as viewed from 3200K (lower)
AWBOUT4(CAT23_Byte4)	B/G as viewed from 3200K (upper)

Note

In this mode, AWB control other than OPD integration is stopped, regardless of AWBMODE.

9.7.8. ATW Related Parameters

Adjusting the Operation Frames

The operation color temperature range (R-B axis direction) for the standard operation frame is from approximately 2500 K to approximately 9500 K.

The operation frame adjustments are set by the parameters in ”**Table 9.7-10**” through ”**Table 9.7-16**”.

See ”**Fig 9.7-2**” for the relationship between the ATW operation frames (model image) and the parameters.

Table 9.7-10 FRAMRMIN

FRAMRMIN	
Parameter Category	CAT15_Byte19 (8bit)
Outline	Sets the R/G direction of ATW operation frame 2.
Conditions	ATWFRM2OF=0[h]
Available settings range	0[h] - FF[h]
Description	Increasing the value facilitates convergence in the Cy direction.

Table 9.7-11 FRAMBMIN

FRAMBMIN	
Parameter Category	CAT15_Byte20 (8bit)
Outline	Sets the B/G direction of ATW operation frame 2.
Conditions	ATWFRM2OF=0[h]
Available settings range	0[h] - FF[h]
Description	Increasing the value facilitates convergence in the Ye direction.

Table 9.7-12 FRAMRMAX

FRAMRMAX	
Parameter Category	CAT15_Byte21 (8bit)
Outline	Sets the R/G direction of ATW operation frame 3.
Conditions	ATWFRM3OF=0[h]
Available settings range	0[h] - FF[h]
Description	Increasing the value facilitates convergence in the R direction.

Table 9.7-13 FRAMMG

FRAMMG	
Parameter Category	CAT15_Byte22 (8bit)
Outline	Sets the Mg direction of ATW operation frame 3.
Conditions	ATWFRM3OF=0[h]
Available settings range	0[h] - FF[h]
Description	Increasing the value facilitates convergence in the Mg direction.

Table 9.7-14 FRAMFL

FRAMFL	
Parameter Category	CAT15_Byte25 (8bit)
Outline	Sets the fluorescent light frame of ATW operation frame 1.
Conditions	ATWFRM1OF=0[h]
Available settings range	0[h] - FF[h]
Description	Increasing the value facilitates convergence in the G direction.

Table 9.7-15 AWBRBWE

AWBRBWE	
Parameter Category	CAT15_Byte26 (8bit)
Outline	Sets the R-B direction of ATW operation frame 1.
Conditions	ATWFRM3OF=1[h]
Available settings range	0[h] - FF[h]
Description	Increasing the value facilitates convergence of the high color temperature side.

Table 9.7-16 AWBMGWE

AWBMGWE	
Parameter Category	CAT15_Byte27 (8bit)
Outline	Sets the Mg-G direction of ATW operation frame 1.
Conditions	ATWFRM3OF=1[h]
Available settings range	0[h] - FF[h]
Description	Increasing the value facilitates convergence of the high color temperature side.

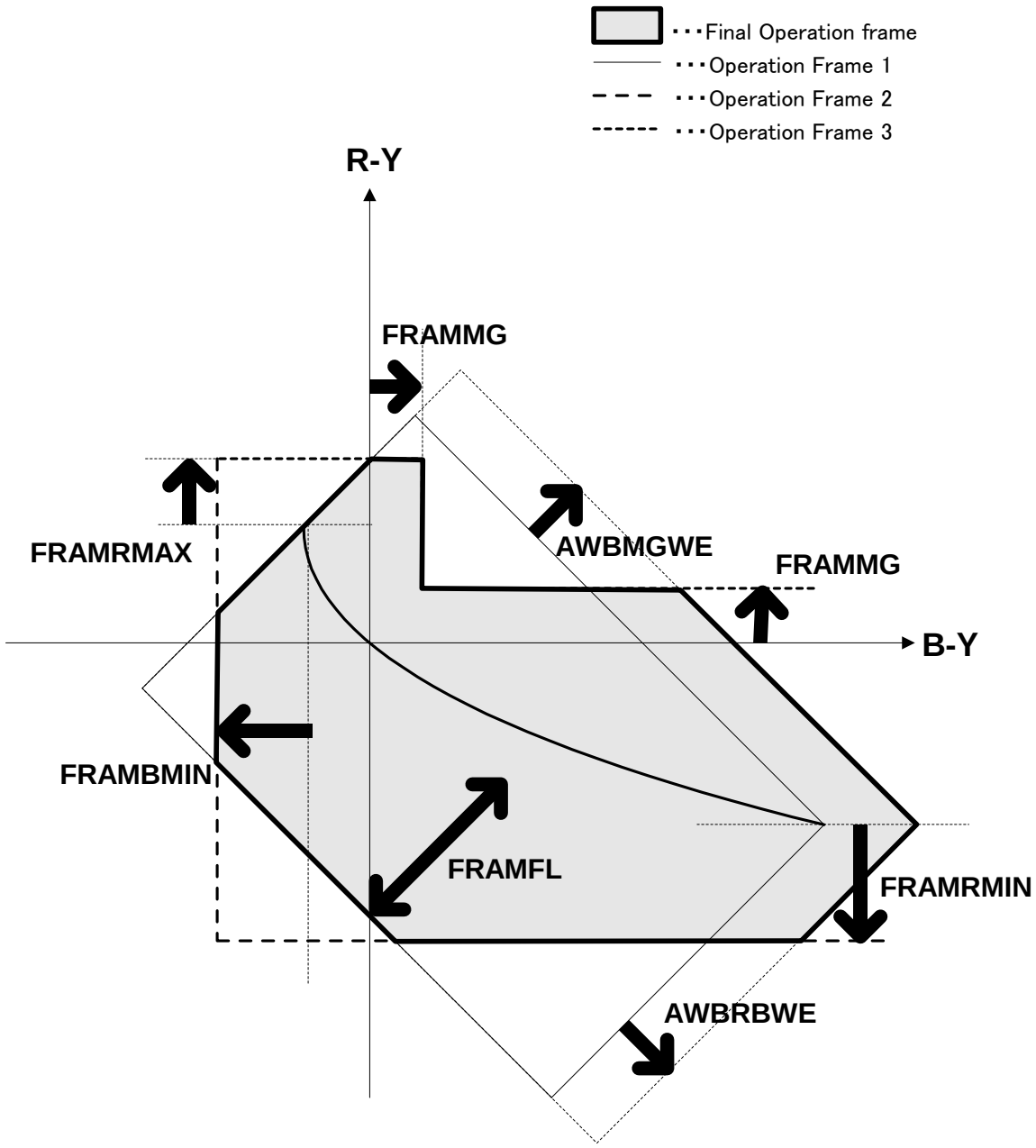


Fig 9.7-2 ATW Operation Frames (Model Image)

Note:
"**Fig 9.7-2**" image is an approximate representation of what you will see on a vectorscope.
It is not an accurate measurement.

Operation Frame Enlargement

The ATW operation frames (all frames 1 to 3) can be enlarged by setting ATWLARGFRM (CAT15_Byte3_bit4) to 1[h]. In addition, when ATWLARGFRM is 1[h], the convergence range can be changed by setting LARGFRMR (CAT15_Byte23) and LARGFRMB (CAT15_Byte24). The color temperature range during operation frame enlargement is from 2400K to 11000K.

See "**Fig 9.7-3**" for the relationship between the enlarged operation frame (model image) and the parameters.

Table 9.7-17 ATWLARGFRM

ATWLARGFRM	
Parameter Category	CAT15_Byte3_bit4 (1bit)
Outline	ON/OFF setting for ATW operation frame enlargement (all frames 1 to 3).
Conditions	
Available settings range	0[h], 1[h]
Description	0[h]: Normal, 1[h]: Enlarged The operation frames (all frames 1 to 3) adjusted by pre white balance can be enlarged by setting ATWLARGFRM to 1[h].

Table 9.7-18 LARGFRMR

LARGFRMR	
Parameter Category	CAT15_Byte23 (8bit)
Outline	Expands the R direction of the low color temperature side for the enlarged frame.
Conditions	ATWLARGFRM=1[h]
Available settings range	0[h] - FF[h]
Description	Increasing the value facilitates convergence of the low color temperature side.

Table 9.7-19 LARGFRMB

LARGFRMB	
Parameter Category	CAT15_Byte24 (8bit)
Outline	Expands the B direction of the low color temperature side for the enlarged frame.
Conditions	ATWLARGFRM=1[h]
Available settings range	0[h] - FF[h]
Description	Increasing the value facilitates convergence of the high color temperature side.

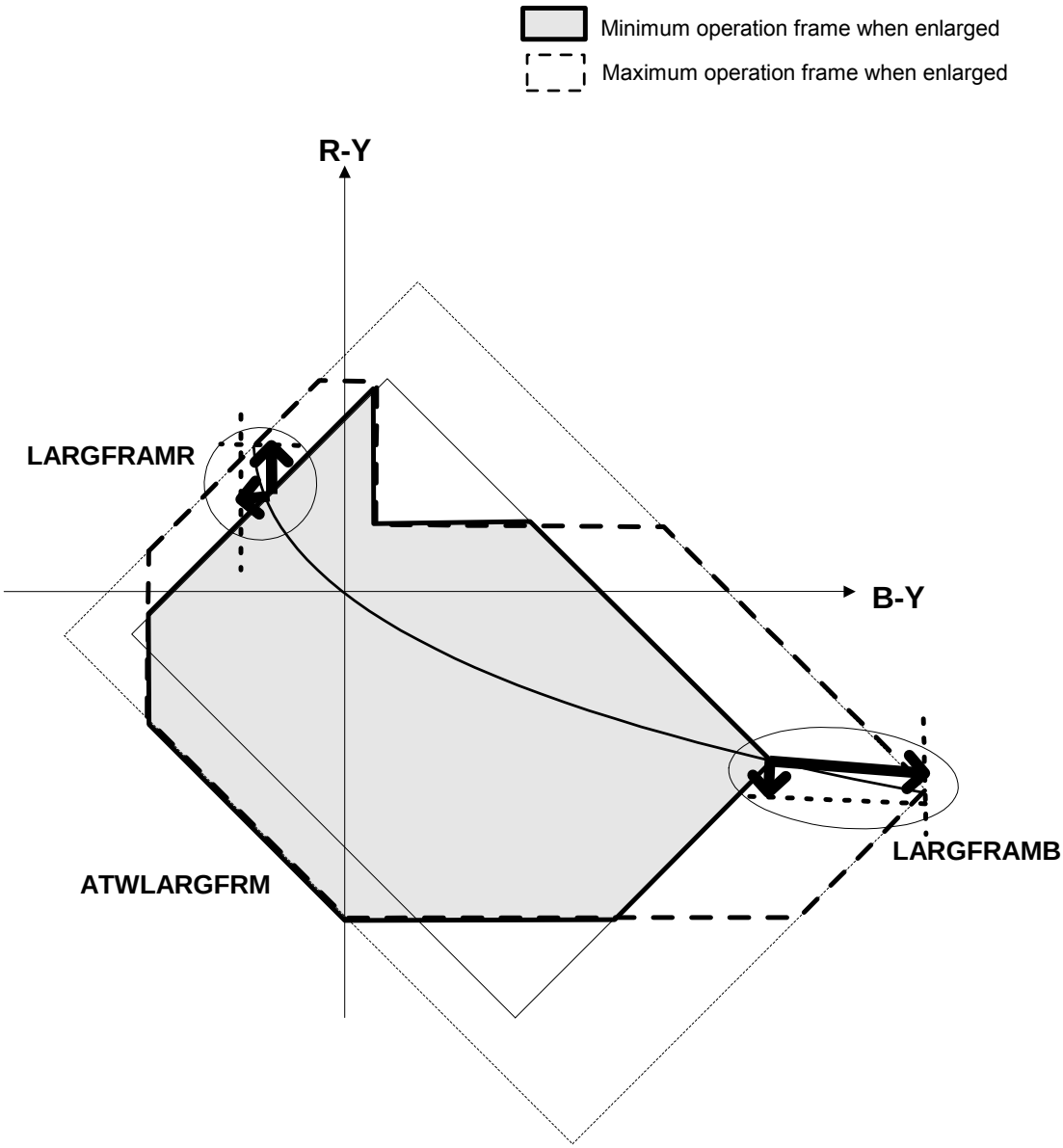


Fig 9.7-3 Operation Frame Enlargement (Model Image)

Note:

"**Fig 9.7-3**" image is an approximate representation of what you will see on a vectorscope.
It is not an accurate measurement.

Operation Frame ON/OFF

The SS-11X system can perform ON/OFF switching for the individual ATW operation frames 1 to 3.

Table 9.7-20 ATWFRM1OF / ATWFRM2OF / ATWFRM3OF

ATWFRM1OF / ATWFRM2OF / ATWFRM3OF	
Parameter Category	CAT15_Byte3_bit1, 2, 3 (各 1bit)
Outline	ON/OFF setting for ATW operation frames type 1 to 3 each.
Conditions	
Available settings range	0[h], 1[h]
Description	0[h]: ON, 1[h]: OFF ATWFRM1OF turns off frame 1. ATWFRM2OF turns off frame 2. ATWFRM3OF turns off frame 3. See ”**Fig 9.7-2**” for frames 1, 2 and 3.

9.7.9. Convergence Point Shift

The SS-11X has a function for shifting the convergence point.

This function shifts the ATW convergence point. Using this function makes it possible to converge the ATW convergence point to an arbitrary location.

Table 9.7-21 ATWRSFT/ATWBSFT

ATWRSFT / ATWBSFT	ATW Red ShiFT / ATW Blue ShiFT
Parameter Category	CAT15_Byte12,13 (8 bits each)
Outline	ATW convergence point shift Sets the shift amount in the R and B directions.
Conditions	
Available settings range	0[h] to FF[h]
Description	Shifts the convergence point to an arbitrary preset point.
Notes	When this value is too large, convergence operation is not performed. This parameter is only valid in ATW mode.

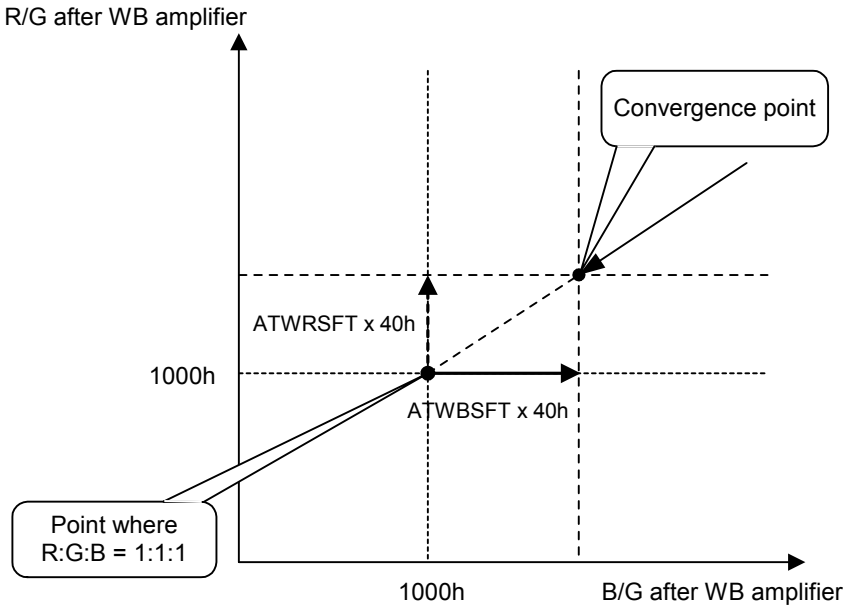


Fig 9.7-4 Point Setting Method

9.7.10. Anti Color-Rolling Mode

When shooting with a NTSC (59.94 Hz) camera under fluorescent lighting with a 60 [Hz] power supply, cyclic color changes with a long period appear. This is called color-rolling.

Anti-color-rolling mode can be set regardless of AWBMODE by setting CRLESSON to 1[h]. This enables the color-rollingless operation frame and performs color-rolling countermeasures.

The operation frame shown in ”**Fig 9.7-5**” is provided in consideration of color transition during the color-rolling countermeasures.

In addition, in anti-color-rolling mode the following parameters can be controlled independently from ATW.

- Operation frame
- Parameter for adjustment of convergence speed.
- Parameter for adjustment of response speed.
- Dead band width for determination of convergence start.
- Convergence point shift.(Select 1 point only)

Table 9.7-22 CRLESSON

CRLESSON	Color-Rolling LESS ON
Parameter Category	CAT12_Byte11_bit0 (1bit)
Outline	ON/OFF setting for anti-color-rolling mode.
Conditions	
Available settings range	0[h],1[h]
Description	0[h] : OFF / 1[h] : ON
Notes	When the port setting has been made, the port has priority.

9.7.11. Color-rollingless AWB mode Related Parameters

Adjusting the Operation Frames

In addition to the ATW operation frames, the SS-11X also has operation frames for color-rollingless AWB mode. Three types of operation frames can be set and turned on and off independently.

Table 9.7-23 CRFRMOFF

CRFRMOFF	anti Color-Rolling FRaMe OFF
Category	CAT15_Byte44_bit0 (1bit)
Outline	ON/OFF setting for color-rollingless AWB operation frames.
Conditions	CRLESSON=1[h]
Available settings range	0[h],1[h] 1bit
Description	0[h] : ON / 1[h] : All OFF When this is 1[h], frame 1 and frame 2 are both turned off. See "**Fig 9.7-5**" for frame 1 and frame 2.
Notes	

Table 9.7-24 CRFRM1OFF / CRFRM2OFF / CRFRM3OFF

CRFRM1OFF / CRFRM2OFF / CRFRM3OFF	anti Color-Rolling FRaMe1 OFF / anti Color-Rolling FRaMe2 OFF / anti Color-Rolling FRaMe3 OFF
Category	CAT15_Byte44_bit1, 2, 3 (1 bit each)
Outline	ON/OFF settings for color-rollingless AWB operation frames.
Conditions	CRLESSON=1[h] CRFRMOFF=0[h]
Available settings range	0[h],1[h] 1bit
Description	0[h] : ON / 1[h] : OFF Frame 1 is turned off by CRFRM1OFF. Frame 2 is turned off by CRFRM2OFF. Frame 3 is turned off by CRFRM3OFF. See "**Fig 9.7-5**" for frame 1, frame 2 and frame3.
Notes	

Table 9.7-25 CRRGMAXL / CRRGMAXM / CRRGMINL / CRRGMINM

CRRGMAXL / CRRGMAXM / CRRGMINL / CRRGMINM	
Category	CAT15_Byte45,46,47,48 (8 bit each)
Outline	Sets the color-rollingless AWB operation frames.
Conditions	CRLESSON=1[h] CRFRMOFF=0[h]
Available settings range	0[h]-FF[h] 8bit
Description	These parameters set the maximum R/G value (MSB/LSB) and minimum R/G value (MSB/LSB) of the color-rollingless AWB operation frames.
Notes	

Table 9.7-26 CRBGMAXL / CRBGMAXM / CRBGMINL / CRBGMINM

CRBGMAXL / CRBGMAXM / CRBGMINL / CRBGMINM	
Category	CAT15_Byte49,50,51,52 (8 bit each)
Outline	Sets the color-rollingless AWB operation frames.
Conditions	CRLESSON=1[h] CRFRMOFF=0[h]
Available settings range	0[h]-FF[h] 8bit
Description	These parameters set the maximum B/G value (MSB/LSB) and minimum B/G value (MSB/LSB) of the color-rollingless AWB operation frames.
Notes	

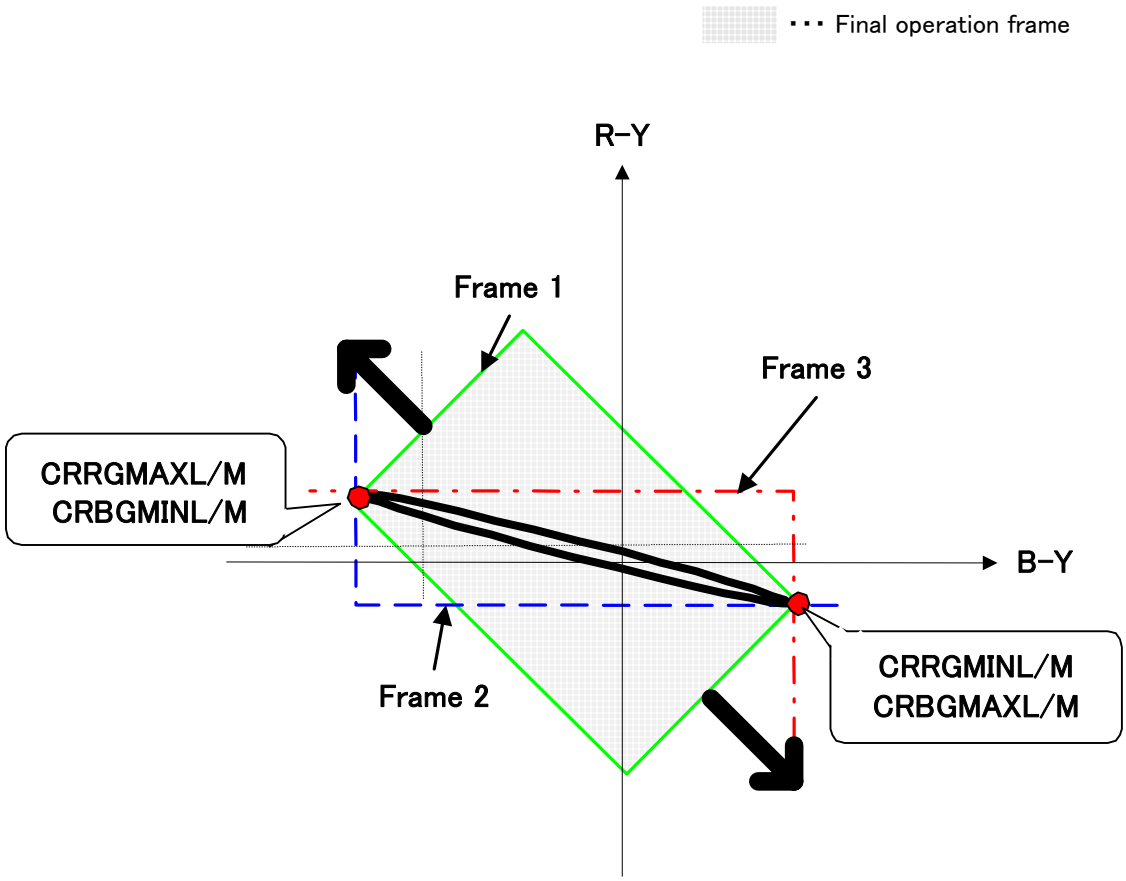


Fig 9.7-5 Operation Frame of Color-rollingless (Model Image)

Note:
"**Fig 9.7-5**" image is an approximate representation of what you will see on a vectorscope.
It is not an accurate measurement.

Please change the following parameters to adjust the frame of the low color temperature side (2500K).

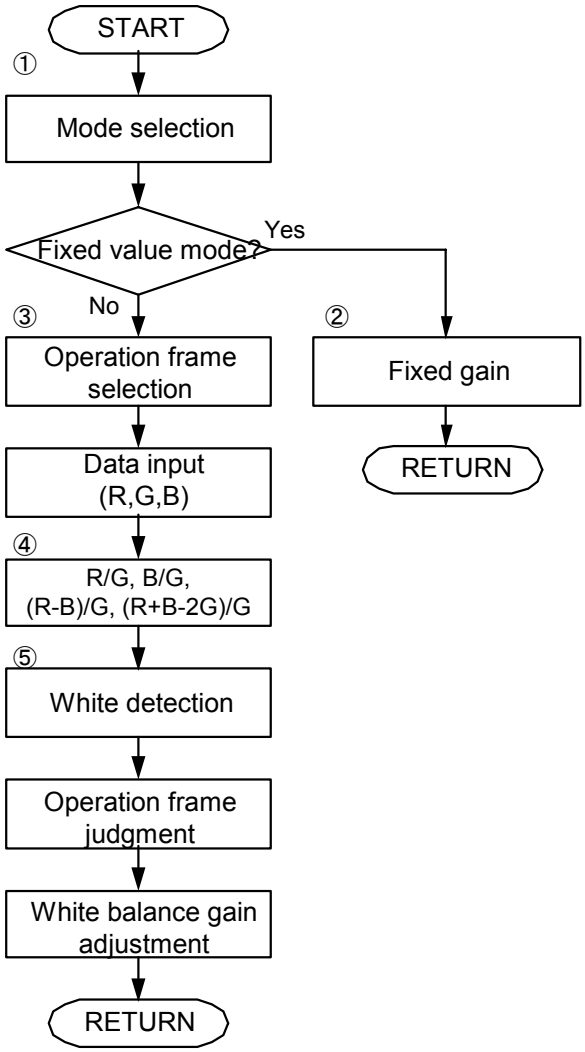
Adjusting the CRRG*** values allow adjustment of the R-Y axis.
Adjusting the CRBG*** values allow adjustment of the B-Y axis.

Low Color Temperature Side (2500K) Frame Adjustment
CRRGMAXL/M(CAT15_Byte45,46) – Increase the value
CRBGMINL/M(CAT15_Byte51,52) – Decrease the value

High Color Temperature Side (9500K) Frame Adjustment
CRRGMINL/M(CAT15_Byte47,48) – Decrease the value
CRBGMAXL/M(CAT15_Byte49,50) – Increase the value

9.7.12. Detailed Description of WB Operation

Sequence of AWB Operation



(1) Processing branches according to the mode input by the DIP switches or serial input.

(2) In fixed value mode, the fixed gain is selected, the signal is sent to the WB gain amplifier.

(3) In ATW mode, the operation frame is selected. Next, operations are performed using the data from the OPD.

(4) The detection data from the OPD is converted to R/G, B/G and (R-B)/G, (R+B-2G)/G format.

(5) In ATW mode, after performing white detection, the operation frame is judged and operation shifts to convergence processing.

Fig 9.7-6 WB Flow Chart

Luminance Specific Integration

When AWBMODE (CAT15_Byte1_bit0-3) is 0[h] (Normal mode), the integral range for luminance specific integration can be set when AWBSEPOF (CAT15_Byte2_bit0) is 1[h].

The integral range is set by UWBYREFL (CAT15_Byte28), INTSLICE (CAT15_Byte29) and UWBYREFH (CAT15_Byte30). In addition, the high luminance area for luminance specific integration can be set by HLCUT (CAT15_Byte31).

"**Fig 9.7-7**" shows an example image of the parameter settings for luminance specific integration.

Table 9.7-27 AWBSEPOF

AWBSEPOF	AWB SPEcific OFf
Parameter Category	CAT15_Byte2_bit0 (1bit)
Outline	ON/OFF setting for luminance specific integration.
Conditions	AWBMODE=0[h]
Available settings range	0[h],1[h]
Description	0[h]:Luminance specific integration ON 1[h]:OFF
Notes	This parameter affects both the ATW response characteristics and the convergence speed.

Table 9.7-28 UWBYREFL

UWBYREFL	
Parameter Category	CAT15_Byte28 (8bit)
Outline	Sets the integral range (luminance lower limit) for luminance specific integration.
Conditions	AWBMODE=0[h]
Available settings range	0[h] - FF[h]
Description	When AWBSEPOF = 0[h]: The integral range is fixed to UWBYREFL to UWBYREFH. When AWBSEPOF = 1[h]: Detection is performed on the medium luminance region UWBYREF to INTSLICE and the high luminance region INTSLICE to UWBYREFH, and the optimum region is selected for ATW control.
Notes	Please set value like UWBYREF < INTSLICE < UWBYREFH

Table 9.7-29 INTSLICE

INTSLICE	
Parameter Category	CAT15_Byte29 (8bit)
Outline	Sets the integral range slice level for luminance specific integration.
Conditions	AWBMODE=0[h], AWBSEPOF=1[h]
Available settings range	0[h] - FF[h]
Description	When AWBSEPOF = 1[h]: Detection is performed on the medium luminance region UWBYREF to INTSLICE and the high luminance region INTSLICE to UWBYREFH, and the optimum region is selected for ATW control.
Notes	Please set value like UWBYREF < INTSLICE < UWBYREFH

Table 9.7-30 UWBYREFH

UWBYREFH	
Parameter Category	CAT15_Byte30 (8bit)
Outline	Sets the integral range (luminance upper limit) for luminance specific integration.
Conditions	AWBMODE=0[h]
Available settings range	0[h] - FF[h]
Description	When AWBSEPOFL = 0[h]: The integral range is fixed to UWBYREFL to UWBYREFH. When AWBSEPOF = 1[h]: Detection is performed on the medium luminance region UWBYREF to INTSLICE and the high luminance region INTSLICE to UWBYREFH, and the optimum region is selected for ATW control.
Notes	Please set value like UWBYREFL < INTSLICE < UWBYREFH

Table 9.7-31 HLCUT

HLCUT	
Parameter Category	CAT15_Byte31 (8bit)
Outline	Sets the high luminance area for luminance specific integration.
Conditions	AWBMODE=0[h], AWBSEPOF=1[h]
Available settings range	0[h] - FF[h]
Description	Reducing this parameter makes easier to use high luminance portions.
Notes	

Luminance specific integration performs detection by dividing the picture into the two areas of the medium luminance region and the high luminance region, and automatically selects one of these detection values for white balance control.

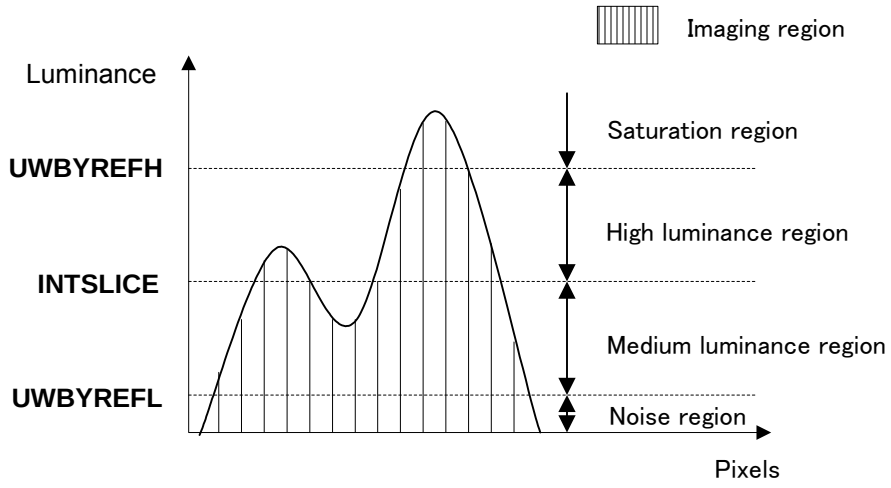


Fig 9.7-7 Parameter Settings for Luminance Specific Integration (Model Image)

Adjustment of ATW Control Speed

Table 9.7-32 AWBSPED

AWBSPED	AWB SPEeD
Parameter Category	CAT15_Byte5 (8bit)
Outline	Sets the ATW control speed.
Conditions	
Available settings range	0[h] - FF[h]
Description	0[h]: Maximum speed FF[h]: Minimum speed
Notes	This parameter affects both the ATW response characteristics and the convergence speed.

Table 9.7-33 WBDLY

WBDLY	White Balance DeLaY
Parameter Category	CAT15_Byte6 (8bit)
Outline	Sets the ATW response speed.
Conditions	
Available settings range	0[h] - FF[h]
Description	0[h]: Maximum speed FF[h]: Minimum speed This parameter sets the WAIT time until convergence operation starts.
Notes	

Table 9.7-34 ATWSTEP

ATWSTEP	
Parameter Category	CAT15_Byte7 (8bit)
Outline	Sets the ATW convergence step width.
Conditions	
Available settings range	0[h] - FF[h]
Description	0[h]: Maximum step width, FF[h]: Minimum step width This parameter sets the time from when convergence operation starts until convergence operation ends.
Notes	

Dead Band Adjustment

A dead band is provided to stabilize WB operation by not performing WB operation with respect to minute color temperature fluctuations after convergence operation has been performed.

Table 9.7-35 WBDBAND

WBDBAND	White Balance DeadBAND
Parameter Category	CAT15_Byte14 (8bit)
Outline	Sets the frame for the convergence point complete judgment.
Conditions	
Available settings range	0[h] to FF[h]
Description	Setting a large WBDBAND value is effective for stabilizing operation.
Notes	

Table 9.7-36 DBANDR / DBANDB / DBANDM / DBANDG

DBANDR / DBANDB / DBANDM / DBANDG	DeadBAND Red / DeadBAND Blue / DeadBAND Magenta / DeadBAND Green
Parameter Category	CAT15_Byte15,16,17,18 (8 bits each)
Outline	Sets the frame for the re-convergence start judgment in the R, B, Mg and G directions.
Conditions	
Available settings range	0[h] to FF[h]
Description	The dead band can be adjusted in the four directions of R, B, Mg and G. These parameters are the dead band widths used to make the next convergence start judgment after convergence has been performed. The dead band width can be set in four directions, which makes it difficult for convergence operation to start even when the color changes in that direction.
Notes	

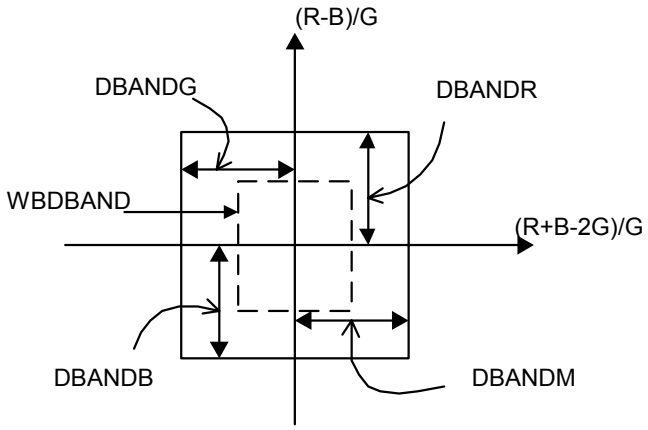


Fig 9.7-8 Dead Band of ATW

9.8. Aperture Correction

Aperture correction processing performed by the SS-11X includes H aperture correction processing, V aperture correction processing, VH aperture correction processing which adds V and H aperture correction processing, and highlight aperture correction processing which boosts the aperture correction of highlighted portions after gamma.

The CAT2 parameters are subject to Priority1 control. Also, the aperture correction values may be overwritten when the suppress function is ON.

Table 9.8-1 Aperture Correction Related Parameters

Parameter		Description	Initial value
VHAPGCTL	CAT12_Byte8_bit0	Turns VH aperture correction gain external control ON and OFF. 0[h] : OFF 1[h] : ON	0[h]

Table 9.8-2 Horizontal Aperture Correction Related Parameters

Parameter		Description	Initial value
HAPGH	CAT2_Byte1_bit4-5	Sets the horizontal aperture correction high frequency gain. 0[h] : x0 1[h] : x1 2[h] : x2 3[h] : x4	2[h]
HAPGL	CAT2_Byte1_bit6-7	Set the horizontal aperture correction low frequency gain. 0[h] : x0 1[h] : x1/2 2[h] : x1 3[h] : x2	2[h]

Table 9.8-3 Vertical Aperture Correction Related Parameters

Parameter		Description	Initial value
VAPG	CAT2_Byte2_bit0-3	Sets the vertical aperture correction gain. x0(0[h]) to x1(F[h])	A[h]
VAPSL	CAT2_Byte2_bit4-6	Applies slice to vertical aperture correction. 0[h] : Slice level 0 -> 7[h] : Slice level Max.	2[h]

Table 9.8-4 VH Aperture Correction Related Parameters

Parameter		Description	Initial value
VHAPG	CAT2_Byte4_bit2-5	Sets the gain after adding V and H aperture correction. x0(0[h]) to x2(F[h])	6[h]
VHAPSL	CAT2_Byte5_bit0-3	Applies slice after adding V and H aperture correction.	4[h]

・ To output images with sharp edges

1. Set VHAPGCTL to 1[h].
2. Adjust HAPGH (CAT2_Byte1_bit4-5), HAPGL (CAT2_Byte1_bit6-7), VAPG (CAT2_Byte2_bit0-3) and VHAPG (CAT2_Byte4_bit2-5).
3. Write CAT2 and CAT12 in the EEPROM.
4. Restart.

* The suppress function does not operate when VHAPGCTL is 1[h].

・ To boost aperture correction and also active the suppress function.

1. Set VHAPGCTL to 1[h].
2. Adjust HAPGH (CAT2_Byte1_bit4-5), HAPGL (CAT2_Byte1_bit6-7), VAPG (CAT2_Byte2_bit0-3) and VHAPG (CAT2_Byte4_bit2-5).
3. Write CAT2 in the EEPROM.
4. Restart.
5. Set aperture correction suppress start AGCCNT using ASPRSTA (CAT13_Byte16).
6. Write CAT13 in the EEPROM.

* The aperture correction gain value is suppressed by the suppress function so set the suppress start position using ASPRSTA (CAT13_Byte16).

9.9. Suppress

9.9.1. Aperture Correction Suppress

This suppresses the aperture correction level in accordance with the AGC gain.

The settings (Aperture correction suppress ON/OFF, start AGCCNT, end AGCCNT, minimum level) are changed by using the following parameters.

ASPR : Aperture correction suppress ON/OFF
ASPRSTA : Aperture correction suppress start AGCCNT
ASPREND : Aperture correction suppress end AGCCNT
ASPRMIN : Aperture correction suppress minimum level

Table 9.9-1 ASPR

ASPR	Apcon SuPpRess
Parameter Category	CAT12_Byte6_bit3 (1bit)
Outline	Switches the aperture correction suppress ON and OFF
Conditions	
Available setting range	0[h] : OFF, 1[h] : ON
Initial value	1[h]
Description	
Notes	

Table 9.9-2 ASPRSTA

ASPRSTA	Apcon SuPpRess STArt level
Parameter Category	CAT13_Byte16 (8bit)
Outline	Aperture correction suppress start AGCCNT
Conditions	ASPR=1[h]
Available setting range	00[h] - FF[h]
Initial value	A0[h]
Description	
Notes	Don’t set a value larger than ASPREND.

Table 9.9-3 ASPREND

ASPREND	Apcon SuPpRess END level
Parameter Category	CAT13_Byte17 (8bit)
Outline	Aperture correction suppress end AGCCNT
Conditions	ASPR=1[h]
Available setting range	00[h] - FF[h]
Initial value	D0[h]
Description	
Notes	Don’t set a value smaller than ASPRSTA.

Table 9.9-4 ASPRMIN

ASPRMIN	Apcon SuPpRess MINimum level
Parameter Category	CAT13_Byte18 (8bit)
Outline	Aperture correction suppress minimum level
Conditions	ASPR=1[h]
Available setting range	00[h] - FF[h]
Initial value	8A[h]
Description	00[h]: Complete suppress, FF[h]:No suppress
Notes	

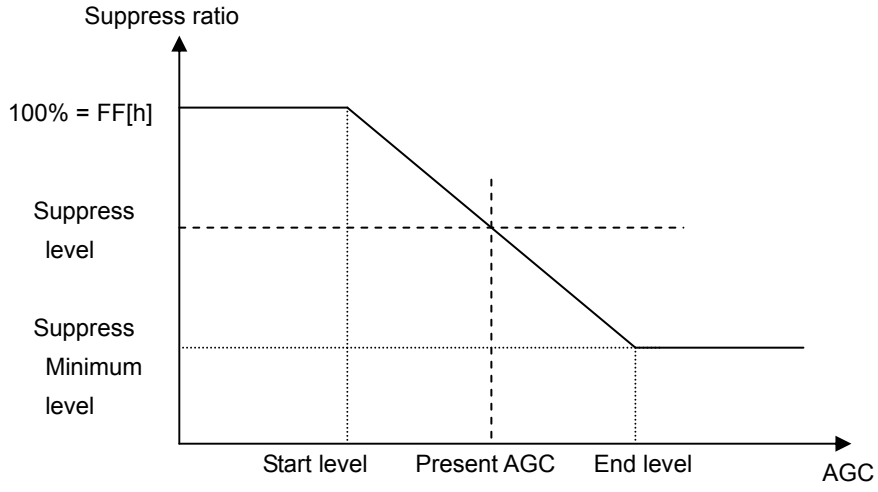


Fig 9.9-1 Suppress Characteristics Diagram

9.9.2. Chroma Suppress

This suppresses the chroma signal level (RYGAIN and BYGAIN) in accordance with AGC gain.

The settings (Chroma suppress ON/OFF, start AGCCNT, end AGCCNT, minimum level) are changed by using the following parameters.

CSPR : Chroma suppress ON/OFF
CSPRSTA : Chroma suppress start AGCCNT
CSPREND : Chroma suppress end AGCCNT
CSPRMIN : Chroma suppress minimum level

Table 9.9-5 CSPR

CSPR	Chroma SuPpRess
Parameter Category	CAT12_Byte6_bit4 (1bit)
Outline	Switches the chroma suppress ON and OFF
Conditions	
Available setting range	0[h],1[h]
Initial value	1[h]
Description	
Notes	

Table 9.9-6 CSPRSTA

CSPRSTA	Chroma SuPpRess STArt level
Parameter Category	CAT13_Byte19 (8bit)
Outline	Chroma suppress start AGCCNT
Conditions	
Available setting range	00[h] - FF[h]
Initial value	A0[h]
Description	
Notes	Don’t set I value larger than CSPREND.

Table 9.9-7 CSPREND

CSPREND	Chroma SuPpRess END level
Parameter Category	CAT13_Byte20 (8bit)
Outline	Chroma suppress end AGCCNT
Conditions	
Available setting range	00[h] - FF[h]
Initial value	D0[h]
Description	
Notes	Don’t set a value smaller than CSPRSTA.

Table 9.9-8 CSPRMIN

CSPRMIN	Chroma SuPpRess MINimum level
Parameter Category	CAT13_Byte21 (8bit)
Outline	CSPR=1[h]
Conditions	Chroma suppress minimum level
Available setting range	00[h] - FF[h]
Initial value	8A[h]
Description	00[h]: Complete suppress, FF[h]: No suppress
Notes	

9.10. Using Four-Quadrant Independent Control

The CXD4103 can set HUE/GAIN for R-Y and B-Y data independently in four quadrants.

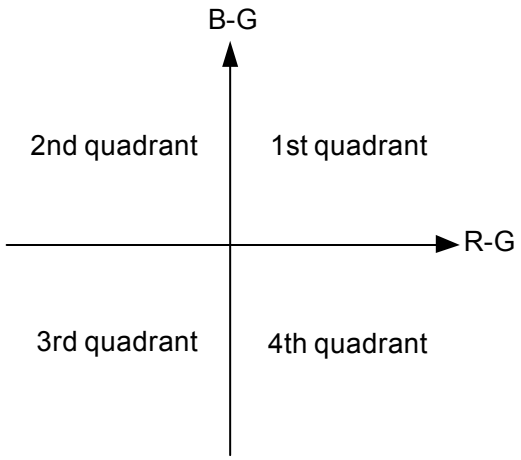


Fig 9.10-1 Four Quadrants on the R-G/B-G Axes

<Adjustment procedure>

1. Turn off the DSP CPU control. (CPUHOLD = 1[h])

Table 9.10-1 Enable HUE/GAIN control

Parameter		Description
CPUHOLD	CAT12_Byte5_bit0	0[h]: CPU operates 1[h]: CPU hold

2. Select four-quadrant independent control.
   Set HUE/GAIN control to four-quadrant simultaneous with the following parameter.

Table 9.10-2 HUE/GAIN adjustment parameters

Parameter		Description
RBQUADON	CAT2_Byte29_bit7	0[h]: Four-quadrant simultaneous 1[h]: Four-quadrant independent

3. Adjust HUE/GAIN for each quadrant through parameters.
   Adjust HUE/GAIN for each quadrant through the parameters listed below.
   The HUE/GAIN adjustment parameters for the first quadrant (RYGAIN1, BYGAIN1, RYHUE1, BYHUE1) also serve as the HUE/GAIN adjustment parameters for four-quadrant simultaneous control.

Table 9.10-3 HUE/GAIN Adjustment Parameters

Parameter		Description
RYGAIN1	CAT2_Byte37	First quadrant : R-Y Gain adjustment
BYGAIN1	CAT2_Byte38	First quadrant : B-Y Gain adjustment
RYHUE1	CAT2_Byte39	First quadrant : R-Y Hue adjustment
BYHUE1	CAT2_Byte40	First quadrant : B-Y Hue adjustment
RYGAIN2	CAT2_Byte41	Second quadrant : R-Y Gain adjustment
BYGAIN2	CAT2_Byte42	Second quadrant : B-Y Gain adjustment
RYHUE2	CAT2_Byte43	Second quadrant : R-Y Hue adjustment
BYHUE2	CAT2_Byte44	Second quadrant : B-Y Hue adjustment
RYGAIN3	CAT2_Byte45	Third quadrant : R-Y Gain adjustment
BYGAIN3	CAT2_Byte46	Third quadrant : B-Y Gain adjustment
RYHUE3	CAT2_Byte47	Third quadrant : R-Y Hue adjustment
BYHUE3	CAT2_Byte48	Third quadrant : B-Y Hue adjustment
RYGAIN4	CAT2_Byte49	Fourth quadrant : R-Y Gain adjustment
BYGAIN4	CAT2_Byte50	Fourth quadrant : B-Y Gain adjustment
RYHUE4	CAT2_Byte51	Fourth quadrant : R-Y Hue adjustment
BYHUE4	CAT2_Byte52	Fourth quadrant : B-Y Hue adjustment

Note: If the gain or phase difference in an individual quadrant is set to a large value, the color changes at the quadrant borders will be large.

9.11. False Color Suppress Function (High Luminance Chroma Suppress Function)

The chroma block has a function for suppressing the chroma signal using the hardware according to the luminance level or V aperture correction level after conversion to R-Y/B-Y.

This function is provided to suppress “false color” during saturation under high luminance or when there is a luminance difference in the vertical direction.

This related parameters are as follows.

Table 9.11-1 Setting the False Color Suppress Amount when the V Aperture Correction is Detected

Parameter		Description
CSVLV	CAT2_Byte53_bit0-1	0[h]: No Suppression 1[h]: Signal suppressed by 50% 2[h]: Signal suppressed by 75% 3[h]: Signal suppressed by 100%

Table 9.11-2 Setting the V-Aperture Correction Level at which False Color Suppress Starts

Parameter		Description
CSVTH	CAT2_Byte53_bit2-3	0[h]: Detection at 25% 1[h]: Detection at 44% 2[h]: Detection at 63% 3[h]: Detection at 81%

Table 9.11-3 Setting the False Color Suppress Amount when the Luminance Level is Detected

Parameter		Description
CSHLV	CAT2_Byte53_bit4-5	0[h]: No Suppression 1[h]: Signal suppressed by 50% 2[h]: Signal suppressed by 75% 3[h]: Signal suppressed by 100%

Table 9.11-4 Setting the Luminance Level at which False Color Suppress Starts

Parameter		Description
CSHTH	CAT2_Byte53_bit6-7	0[h]: Detection at 75% 1[h]: Detection at 81% 2[h]: Detection at 88% 3[h]: Detection at 94%

The Initial value for CSVLV and CSHLV are "0[h]", so suppress is not activated. When only one side is activated, the suppress amount is as indicated in the tables above. However, note that when suppress is set for CSVLV or CSHLV at the same time, if the luminance and V aperture correction are both detected at the same time while CSVLV and CSHLV are set to combination of "1[h]" and "2[h]", the suppress level becomes "100%”.

9.12. OUTGAIN Function

The SS-11X system has OUTGAIN function. This function sets Chroma gain and Y gain Up/Down at the same time.

The gain values (RYGAIN, BYGAIN, and YGAIN) are reflected through RYGAINRATE (CAT13_Byte13), BYGAINRATE (CAT13_Byte14), and YGAINRATE (CAT13_Byte15) showing in the following calucrated expression, when OUTGAIN (CAT12_Byte6_bit1) is setting to 1[h]. RYGAINRATE, BYGAINRATE, and YGAINRATE values are until OUTGAINMAX values.

And then, the parameter values of RYGAIN 1 - 4 and BYGAIN 1 - 4 are substituted the following calucrated expression when using Four-Quadrant Independent Control.

RYGAIN = RYGAIN setting value x OUTGAINMAX x RYGAINRATE / FF[h]
BYGAIN = BYGAIN setting value x OUTGAINMAX x BYGAINRATE / FF[h]
YGAIN = YGAIN setting value x OUTGAINMAX x YGAINRATE / FF[h]

Table 9.12-1 OUTGAIN Function Related Parameters

Parameter		Description
OUTGAIN	CAT12_Byte6_bit1	OUTGAIN Function ON/OFF 0[h]:OFF / 1[h]:ON
OUTGAINMAX	CAT13_Byte12	0[h] - FF[h] : x0 to xFF (Enable when OUTGAIN=1[h])
RYGAINRATE	CAT13_Byte13	0[h] - FF[h]（Enable when OUTGAIN=1[h]）
BYGAINRATE	CAT13_Byte14	0[h] - FF[h]（Enable when OUTGAIN=1[h]）
YGAINRATE	CAT13_Byte15	0[h] - FF[h]（Enable when OUTGAIN=1[h]）

9.13. Mirror Function

The SS-11X contains a mirror function.

The video signal which reversed right and left as shown in the following figure can be outputted by using the mirror function.

Notes : It has no top / bottom reversal function.

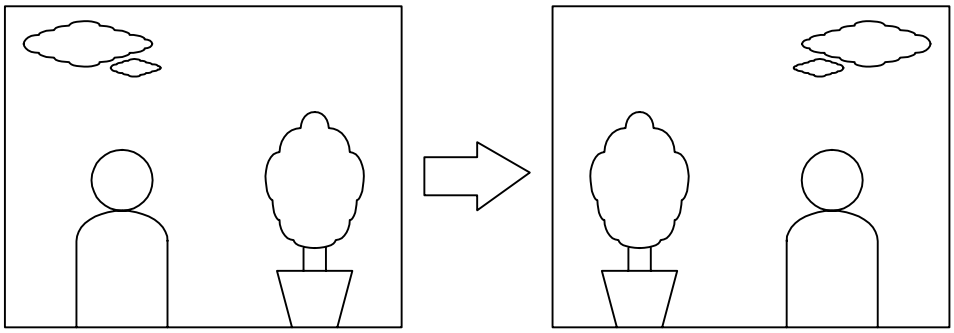


Fig 9.13-1 Mirror Function (Model Image)

<Setting Procedure>

Set the mirror function with the following parameter.

Parameter		Description	Initial value
MIRROR	CAT1_Byte1_bit4	Turns the mirror function ON and OFF. 0[h]: Mirror function OFF, 1[h]: Mirror function ON	0[h]

9.14. Privacy Masking

9.14.1. Setting Procedure

The CXD4103 is equipped with a mask function. Eight masks can be produced from the serial communication data settings. The following table presents the parameters related to the mask function settings.

Table 9.14-1 Mask Function Setting Parameters

Parameter		Description
MSK**n**HSET *	CAT9_Byte1-8	Mask horizontal direction start position (1 step = 4 pixels)
MSK**n**HRST *	CAT9_Byte9-16	Mask horizontal direction end position (1 step = 4 pixels)
MSK**n**VSET *	CAT9_Byte17-24	Mask vertical direction start position (1 step = 4 lines)
MSK**n**VRST *	CAT9_Byte25-32	Mask vertical direction end position (1 step = 4 lines)
MSKBYLV	CAT9_Byte33	Color (B-Y) setting
MSKRYLV	CAT9_Byte34	Color (R-Y) setting
MSKYLVL	CAT9_Byte35	Luminance level (LSB)
MSKYLVM	CAT9_Byte36_bit0	Luminance level (MSB)
MSKON	CAT9_Byte36_bit2	Show mask: 0[h] : OFF / 1[h] : ON
MSKHLD	CAT9_Byte36_bit3	Uses background color as master color 0h:OFF 1h:ON
MSKDLY	CAT9_Byte38_bit0-3	Mask signal Y-side delay adjustment
MSKDLC	CAT9_Byte38_bit4-7	Mask signal CR-side delay adjustment

* Mask number indicated by "n"

<The mask setting procedure is as follows.>

1. Set MSKON to 1[h].
2. Set the mask display positions in MSKnHSET, MSKnHRST, MSKnVSET, and MSKnVRST.
3. Set the brightness in MSKYLV and the colors in MSKBYLV and MSKRYLV.

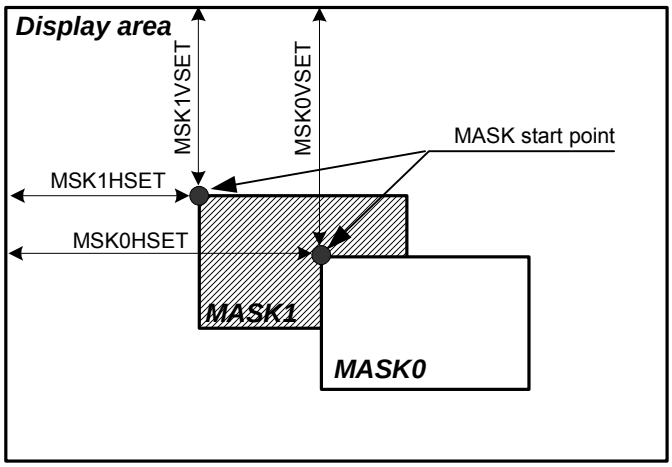


Fig 9.14-1 Mask Function Setting Parameters

Background color reflection function (0th hold function)

To apply the color at the mask start position of MSKnHSET and MSKnVSET to the entire mask, set Background color reflection function MSKHLD (CAT9_Byte36_bit3) to ON (1[h]). Accordingly, during Background color reflection function, the mask color settings are disabled.

If there are overlapping masks, the mask with the smaller number is given priority, as shown in the following figure. In this case, the colors of MASK0 and MASK1 are not subject to the hold function. MASK0 "holds" the image color under MASK1.

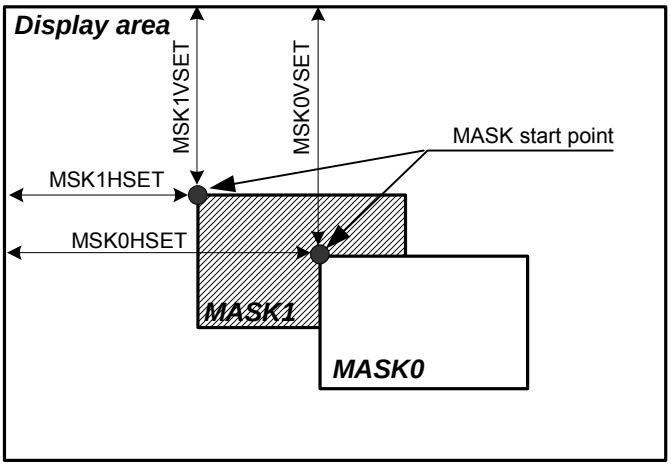


Figure 9.14-1 Background color reflection (0th hold function)

9.14.2. Important

1. Eight masks can be simultaneously displayed or stacked on top of each other, but it is not possible to change the brightness signal level and colors separately for each mask. (Background color reflection does change individual masks.)
2. Masks are not linked to MIRROR.
3. Note that the mask will not be displayed if the MSKnHRST value is smaller than the MSKnHSET value, or if the MSKnVRST value is smaller than the MSKnVSET value.
4. Set the MSKnHSET parameter values to 2[h] or higher. (If set to less than 2[h], the mask is not displayed.)
5. Set MSKnVSET parameter values at 7[h] or higher. (If they are set under 7[h], the mask start position during Background color reflection would exceed the period of the effective video signal, so the "held" color would be incorrectly displayed.)
6. With Background color reflection function, shooting in dark conditions (when the iris is closed, for example) may make the masked areas appear to oscillate. This is caused by random noise, not a problem with the mask function.
7. Under regular mask settings, the mask edges may appear blurred in some cases. This is due to a mismatch of the mask Y and CR delay adjustments. Adjust them by the following parameters.
   - MSKDLY (CAT9_Byte37) Mask signal Y-side delay adjustment
   - MSKDLC (CAT9_Byte38) Mask signal CR-side delay adjustment

9.15. Pattern Generator (PG)

9.15.1. Pattern Generator (PG) Usage Method

The CXD4103 incorporates a pattern generator (PG) that can output various types of patterns according to the serial data settings.

・PG Parameter Settings

When using the PG, first set the parameters as shown in "**Table 9.15-1**".

* Before making these settings, first set CPUHOLD (CAT12_Byte5_bit0) to 1[h].

Table 9.15-1 PG Parameter Settings

Parameter		Setting value
RMATY	CAT2_Byte31	40[h]
RMATC	CAT2_Byte32	C0[h]
BMATY	CAT2_Byte33	40[h]
BMATC	CAT2_Byte34	C0[h]
RYGAIN1	CAT2_Byte37	26[h]
BYGAIN1	CAT2_Byte38	1B[h]
RYHUE1	CAT2_Byte39	D5[h]
BYHUE1	CAT2_Byte40	E9[h]
MODEPARA8	CAT2_Byte55	00[h]
MODEPARA9	CAT2_Byte56	00[h]
WBR	CAT4_Byte1	40[h]
WBG	CAT4_Byte2	40[h]
WBB	CAT4_Byte3	20[h]

PG display ON/OFF

The following parameter is used to turn the PG display ON/OFF.

Table 9.15-2 PGON

Parameter		Setting value	Description
PGON	CAT9_Byte36_bit3	0[h]	PG display OFF
		1[h]	PG display ON

PG Gain Settings

The following parameter can be used to adjust the PG gain.

Table 9.15-3 PGGAIN

Parameter		Setting value	Description
PGGAIN	CAT9_Byte36_bit6-7	0[h]	Sets PG data gain value to x0
		1[h]	Sets PG data gain value to x1
		2[h]	Sets PG data gain value to x2
		3[h]	Sets PG data gain value to x4

9.15.2. Pattern Settings

Pattern Settings

The patterns that can be output by the PG are listed in the table below. The color settings for monochrome raster are shown in "**Table 9.15-5**".

Table 9.15-4 Pattern Types (Pattern Settings)

Parameter		Setting value	Pattern
PGPAT	CAT9_Byte37_bit0-1	0[h]	Color bar
		1[h]	Monochrome raster
		2[h]	Impulse
		3[h]	Serial setting (see "**Table 9.15-9**" for information on how to make this setting)

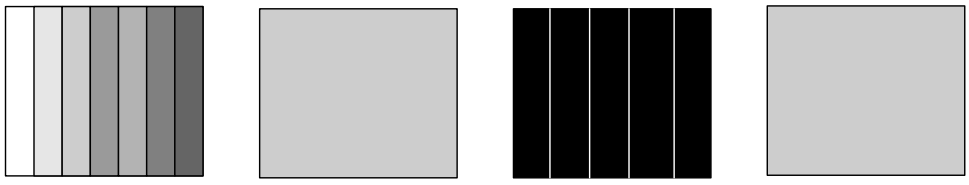


Fig 9.15-1 Pattern Types (Pattern Settings)

* Note that the images shown above are for reference purposes only. The patterns that are actually output by the PG will differ slightly from them.

Table 9.15-5 Raster Color Settings

Parameter		Setting value	Description
PGCOLOR	CAT9_Byte37_bit5-7	0[h]	Sets raster color to W
		1[h]	Sets raster color to Ye
		2[h]	Sets raster color to Cy
		3[h]	Sets raster color to G
		4[h]	Sets raster color to Mg
		5[h]	Sets raster color to R
		6[h]	Sets raster color to B
		7[h]	Sets horizontal simple ramp (high setting priority)

Ramp Addition

PGRION add a ramp to the selected PG pattern.

Table 9.15-6 Pattern Settings (with Ramp Added)

Parameter		Setting value	Pattern
PGRION	CAT9_Byte37_bit3	0[h]	Displays the PG selected by PGPAT
		1[h]	Adds a ramp to and displays the PG selected by PGPAT (if impulse is set, then the display is reversed)

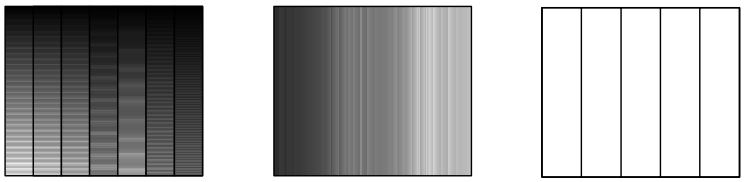


Fig 9.15-2 Pattern Types (with Ramp Added)

* Note that the images shown above are for reference purposes only. The patterns that are actually output by the PG will differ slightly from them.
* It is not possible to add a ramp under serial settings.

H/V Settings

PGHV can switch the selected PG pattern display between the horizontal and vertical directions.

Table 9.15-7 Pattern Settings (H/V Settings)

Parameter		Setting value	Pattern
PGHV	CAT9_Byte37_bit2	0[h]	Displays the PG selected by PGPAT in the horizontal direction
		1[h]	Displays the PG selected by PGPAT in the vertical direction

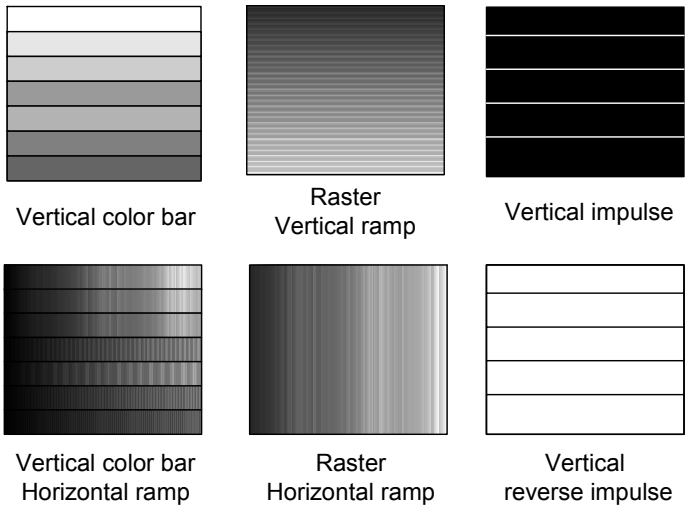


Fig 9.15-3 Pattern Types (H/V Settings)

* Note that the images shown above are for reference purposes only. The patterns that are actually output by the PG will differ slightly from them.
* The PG and ramp are linked together, so if the PG is changed between horizontal and vertical, the ramp will also change between vertical and horizontal. Therefore, it is not possible to display combinations in which a horizontal ramp is added to a horizontal color bar, or a vertical ramp is added to a vertical color bar.

PGRAWMIX Settings

PGRAWMIX can divide the display between a PG area and an imaging area, as shown below.

Table 9.15-8 Pattern Settings (PGRAWMIX Settings)

Parameter		Setting value	Pattern
PGRAWMIX	CAT9_Byte37_bit4	0[h]	No imaging area (only PG is output)
		1[h]	Imaging area included (PG and MIX are output)

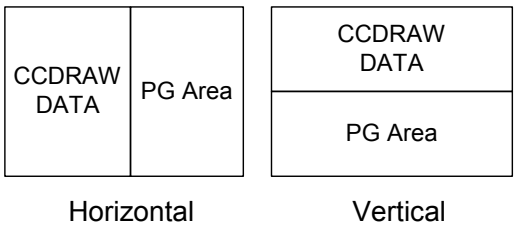


Fig 9.15-4 Pattern Types (PGRAWMIX Settings)

Serial Settings

The CXD4103 can set the CR line and CB line information through serial communication. Use the parameters in "**Table 9.15-9**" to make these settings. "**Table 9.15-10**" shows color reproduction setting values which are nearly ideal.

Table 9.15-9 Parameters for Setting CR and CB Line Information

Parameter		Setting value	Description
PGSDCRS2	CAT9_Byte39	00[h]-FF[h]	CR_S2 serial setting (Ye+Mg)
PGSDCRS1	CAT9_Byte40	00[h]-FF[h]	CR_S1 serial setting (Cy+G)
PGSDCBS2	CAT9_Byte41	00[h]-FF[h]	CB_S2 serial setting (Ye+G)
PGSDCBS1	CAT9_Byte42	00[h]-FF[h]	CB_S1 serial setting (Cy+Mg)

Table 9.15-10 Ideal Color Bar Levels

Parameter	Setting value						
	W	Ye	Cy	Mg	G	R	B
PGSDCRS2	80[h]	60[h]	40[h]	60[h]	20[h]	40[h]	20[h]
PGSDCRS1	60[h]	40[h]	60[h]	20[h]	40[h]	00[h]	20[h]
PGSDCBS2	60[h]	60[h]	40[h]	20[h]	40[h]	20[h]	00[h]
PGSDCBS1	80[h]	40[h]	60[h]	60[h]	20[h]	20[h]	40[h]

10. Supporting Functions for Applications (Digital Output)

10.1. SS-11X Digital Output

The SS-11X supports ITU-REC656-compliant output. The chroma signal, luminance signal. blanking signal, and TRC are multiplexed and output as 8 bits from the port pins. (See the option "**10.1.3 Details of Digital Output**" for details.)

Note that the output rate is that of the encoder clock (ECK). (27 MHz output is not supported.)

10.1.1. Digital Output (ITU-REC656-Compliant Output) Settings

The setting procedure is as follows.

1. Select the crystal for ECK input from the table below according to the TV standard and the CCD type.
2. Set PDRHOLD to 1[h]. (Port driver function OFF) (See "**9.1 Port Driver Function**".)
3. Set the MODESEL value to match the crystal selected in step 1. (See "**Table 10.1-1**".)
4. Set the YDSEL to 1[h. (To set the YUV Digital terminal to port terminal.) (See "**Table 10.1-2**".)
5. Set the DIFON to 1[h]. (Digital signal processing operation ON) (See "**Table 10.1-3**".)
6. Write CAT1, CAT10 and CAT12 in the EEPROM.
7. Set PDRHOLD to 0[h]. (Port driver function ON) (See "**9.1 Port Driver Function**".)
8. Write CAT12 in the EEPROM.
9. Adjust the DCK output. (See "**Table 10.1-4**".)
   (The DCK output frequency differs according to the MODESEL setting. See "**Table 10.1-1**".)
10. Adjust the Y, R-Y and B-Y gain values of the digital output. (See "**Table 10.1-5**".)

Table 10.1-1 Crystal and MODESEL Selection Table for Digital Output

TV SYSTEM	NUMBER OF PIXELS	MODESEL	X'tal(ECK)	DCK output frequency
NTSC	510H	0[h]	38.13986MHz	19.06993MHz
	760H	6[h]	28.63636MHz	28.63636MHz
PAL	510H	3[h]	37.87500MHz	18.93750MHz
	760H	9[h]	28.37500MHz	28.37500MHz

* When problems occur in digital output operation, check the following items.

[Digital output is not output]

・Check again that the settings were made according to the procedure above.

・ Check that the YUV output (port pin output) and the DCK output are input to the rear-end system (encoder, etc.). (See "**3.4 Output Circuit Periphery**".)

[The video is not synchronized]

・ Check that the combination of the crystal and MODESEL is corrected.

・ Readjust DCK output. It may not match the rear-end system (encoder, etc.).

10.1.2. Parameters for Setting Digital Output

Port Pin Switching

The digital output pins also function as the port pins, so when performing digital output, set these pins to YUV digital signal output with the following parameters. (When this setting is made, the applicable port pins does not function as port drivers.)

Table 10.1-2 Port Pin Switching Parameter

Parameter		Description
YDSEL	CAT1_Byte7_bit4	Switches the port pin setting. 0[h]: Port driver, 1[h]: YUV digital signal output

Digital Signal Process Operation ON/OFF

This turns digital signal process operation ON/OFF. In addition, the DCK output is also turned ON/OFF at the same time.

Table 10.1-3 Digital Signal Process ON/OFF Control Parameter

Parameter		Description
DIFON	CAT10_Byte14_bit7	DCK output and digital signal process operation ON/OFF control. 0[h]:OFF 1[h]:ON

DCK Adjustment Parameters

The following parameters are used to adjust the DCK output, and operate output inversion and delay adjustment.

Table 10.1-4 DCK Adjustment Parameters

Parameter		Description
DCKINV	CAT10_Byte14_bit4	DCK output reversal 0[h]: Normal 1[h]: Reverse
DCKDL	CAT10_Byte14_bit5-6	DCK output delay adjustment 0[h]:0ns 1[h]:5ns 2[h]:10ns 3[h]:15ns

* Valid when DIFON is 1[h].

Digital Gain Adjustment Parameters

The digital output gain can be set independently of analog output, using the following parameters.

Table 10.1-5 Digital Gain Adjustment Parameters

Parameter		Description
RECYGAIN	CAT10_Byte8	Digital Y gain setting Setting range: 0-x1.99
RECRYGAIN	CAT10_Byte9	Digital R-Y gain Setting range: 0-x3.99
RECBYGAIN	CAT10_Byte10	Digital B-Y gain Setting range: 0-x3.99

10.1.3. Details of Digital Output

ITU-REC656

TRC Settings

When ITU-REC656-compliant output is set, a timing reference code (TRC) indicating the horizontal and vertical blanking periods is multiplexed and output with the Y/Cr/Cb data.

The SS-11X uses the following ITU-REC-compliant codes as codes for the TRC fourth word.

Table 10.1-6 ITU-REC656 TRC (Fourth word)

7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit	HEX
1fixed	F	V	H	P3	P2	P1	P0	
1	0	0	0	0	0	0	0	80[h]
1	0	0	1	1	1	0	1	9D[h]
1	0	1	0	1	0	1	1	AB[h]
1	0	1	1	0	1	1	0	B6[h]
1	1	0	0	0	1	1	1	C7[h]
1	1	0	1	1	0	1	0	DA[h]
1	1	1	0	1	1	0	0	EC[h]
1	1	1	1	0	0	0	1	F1[h]

F=0 Field 1 period F=1 Field 2period

V=0 Active video period V=1 Vertical blanking period

H=0 SAV(Start of Active Video) H=1 EAV (End of Active Video)

P0-P3 : Error correction bits

The following table summarizes the serial settings related to TRC settings.

Table 10.1-7 Serial Settings Related to TRC Output

Parameter		Description
EAVSTAL	CAT10_Byte2(LSB)	Variable EAV start position setting Variable value : 1[h] = 1dck
EAVSTAM	CAT10_Byte3_bit0-2(MSB)	
SAVSTAL	CAT10_Byte4(LSB)	Variable SAV start position setting Variable value : 1[h] = 1dck
SAVSTAM	CAT10_Byte5_bit0-2(MSB)	
FLD1FSTA	CAT10_Byte6_bit0-2	Field 1 valid video period start position setting Variable value : 1[h] = 1DHD
FLD1VSTA	CAT10_Byte6_bit3-7	Field 1 vertical blanking period start position setting Variable value : 1[h] = 1DHD
FLD2FSTA	CAT10_Byte7_bit0-2	Field 2 valid video period start position setting Variable value : 1[h] = 1DHD
FLD2VSTA	CAT10_Byte7_bit3-7	Field 2 vertical blanking period start position setting Variable value : 1[h] = 1DHD

The TRC output related parameter setting values differ according to the TV standard and the CCD type. The respective setting values are shown in the table below.

Table 10.1-8 Blanking Parameter Recommended Values

Parameter	Setting value			
	NTSC		PAL	
	510H	760H	510H	760H
EAVSTAL	0[h]	0[h]	0[h]	0[h]
EAVSTAM	0[h]	0[h]	0[h]	0[h]
SAVSTAL	CF[h]	18[h]	17[h]	33[h]
SAVSTAM	0[h]	1[h]	1[h]	1[h]
FLD1FSTA	3[h]		3[h]	
FLD1VSTA	12[h]		18[h]	
FLD2FSTA	3[h]		2[h]	
FLD2VSTA	13[h]		18[h]	

Horizontal Timing

"**Fig 10.1-1**" summarizes the relationships between DCK, DHD, and the output data (DOUT).
During horizontal synchronization, DHD falling is detected and the counter is reset.

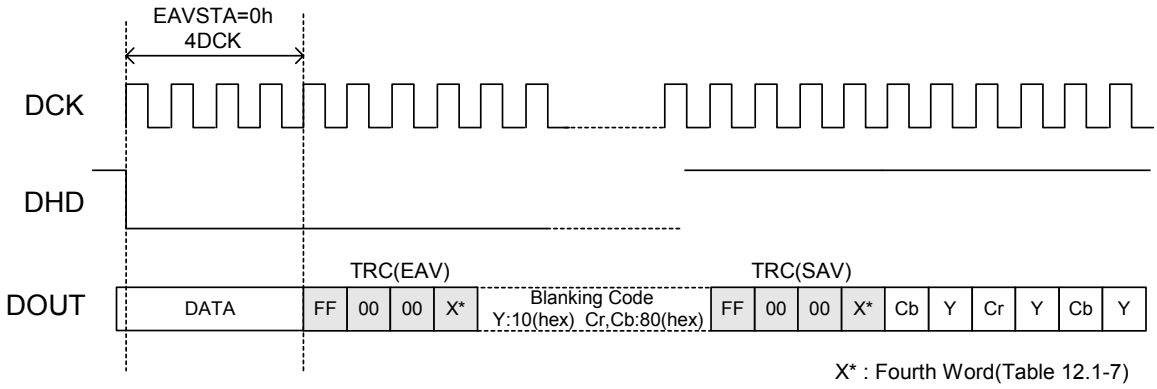


Fig 10.1-1 ITU-REC656 Relationships Between DCK, DHD and Output Data

Vertical Timing

During vertical synchronization, as in horizontal synchronization, the counter is reset when DVD falls and incremented when HD falls ("**Fig 10.1-2**" and "**Fig 10.1-3**")

Set the Field 1 and Field 2 blanking periods separately for each TV system in the blanking start parameters in "**Table 10.1-7**".

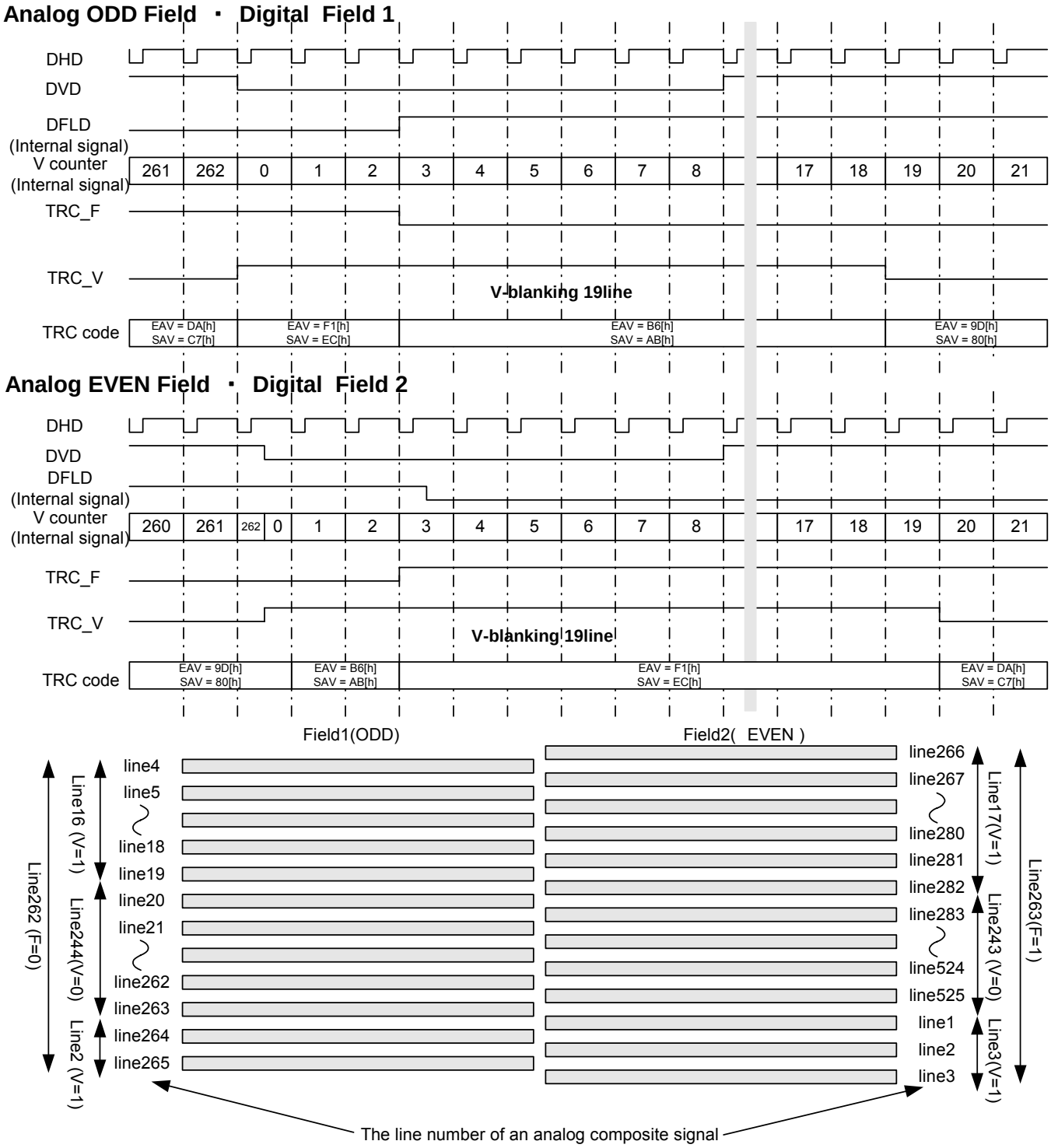


Fig 10.1-2 Vertical Direction Timing NTSC

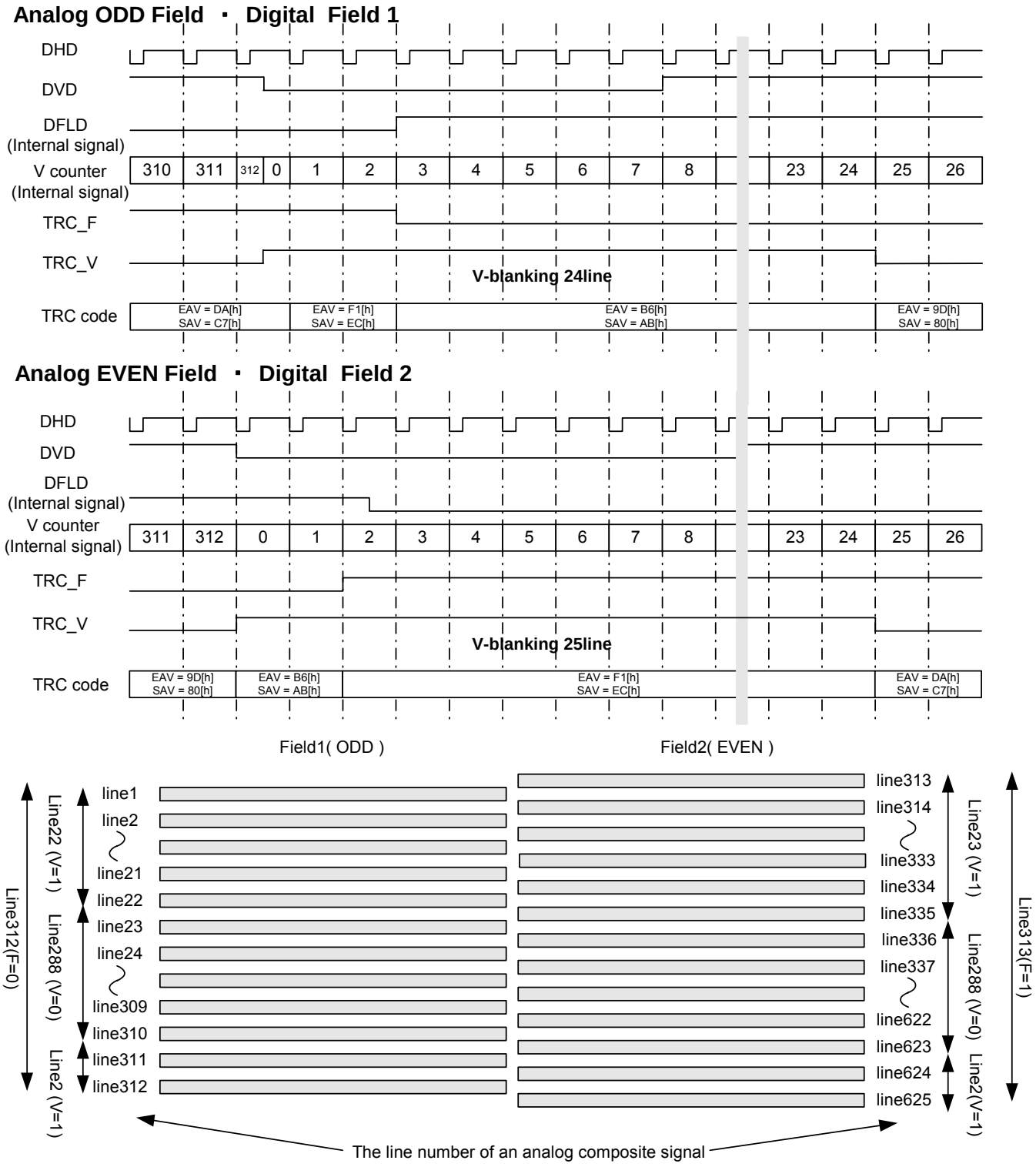


Fig 10.1-3 Vertical Direction Timing PAL

10.2. Sync Signal Output Setting Method

This section describes the parameters related to signal switching for the sync signal input/output pins S0 to S4.

Follow the procedure below to change the S0 to S4 pin settings from the initial values.

1. Set SSELOFF (CAT12_Byte12_bit5) to 1[h]. (S pins control by SGMODE is off)
2. Set up the parameters of each S* pins. (CAT1_Bite7-8)
3. Write CAT1 into EEPROM.
4. Set SSELOFF to 0[h] back.

Table 10.2-1 Sync Signal Output Setting Method

Parameter		Description		Initial Value
S0IN	CAT1_Byte7_bit6	Switches the S0 pin input/output setting.	0[h] : DHD Output 1[h] : VRI Input	1[h]
S1IN	CAT1_Byte7_bit7	Switches the S1 pin input/output setting.	0[h] : DVD Output 1[h] : Fix to High (Test Input)	1[h]
S2SEL	CAT1_Byte8_bit0-2	Switches the S2 pin input/output setting.	0[h] : Test Output 1[h] : DHD Output 2[h] : DVD Output 3[h] : SYNC Output 4[h] : Test Output 5[h] : Test Output 6[h] : FLD Output 7[h] : Setting Prohibition (Test Input)	0[h]
S3SEL	CAT1_Byte8_bit3-5	Switches the S3 pin input/output setting.	0[h] : DHD Output 1[h] : DVD Output 2[h] : HD Output 3[h] : VD Output 4[h] : Test Output 5[h] : Test Output 6[h] : FLD Output 7[h] : Setting Prohibition (Test Input)	0[h]
S4SEL	CAT1_Byte8_bit6-7	Switches the S4 pin input/output setting.	0[h] : Test Output 1[h] : Test Output 2[h] : HD Output 3[h] : VD Output	0[h]

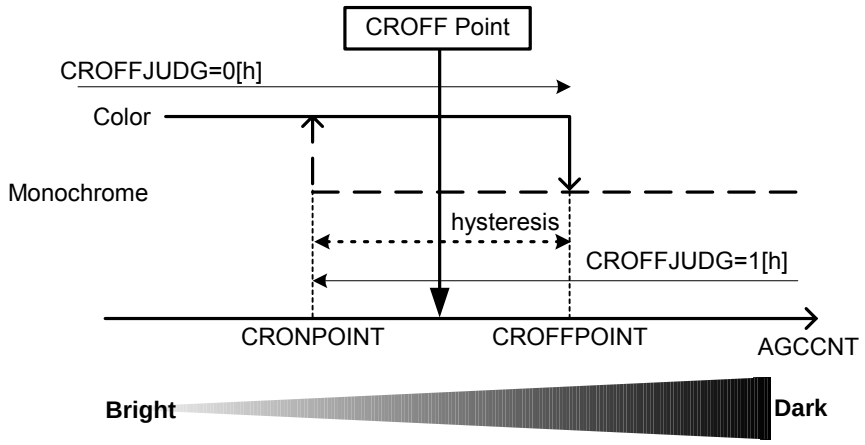
10.3. Color/Black-and-White Switching Function

10.3.1. Outline

The CXD4103 has a function for switching the video between color and black-and-white.

This function detects the surrounding luminance and switches the video from color to black-and-white by turning OFF the chroma gain. The AGCCNT value is used to detect the surrounding luminance, and the chroma gain is turned OFF by setting the RYGAIN1 and other linear matrix parameter values to "0[h]".

In addition, there are two AGCCNT switching points, and hysteresis is also provided. "**Fig 10.3-1**" shows a model image of color/black-and-white switching function control.



Note that this function can also be used as the Day/Night function.

Fig 10.3-1 Color/Black-and-White Switching Function Control (Model Image)

10.3.2. Setting Method

"**Table 10.3-1**" shows the parameters for controlling the color/black-and-white switching function. The setting procedure is as follows.

1. Read the AGCCNT (CAT8_Byte3) value at the brightness at which the color/black-and-white switching function is to operate (CROFF Point in "**Fig 10.3-1**"), and set the two points CRONPOINT and CROFFPOINT.
   Set CRONPOINT < CROFFPOINT at this time.
2. Set CROFFCTLON to 1[h] to activate the color/black-and-white switching function.
3. CROFFJUDG switches to 0[h] in color mode and 1[h] in black-and-white mode, allowing the current mode to be monitored externally.

Table 10.3-1 Description of Color/Black-and-White Switching Parameters

Parameter		Description	
CROFFCTLON	CAT12_Byte13_bit3	Color/black-and-white switching function control	0[h]: Control OFF 1[h]: Control ON
CRONPOINT	CAT13_Byte55	Sets the black-and-white -> color transition point.	Set CRONPOINT < CROFFPOINT
CROFFPOINT	CAT13_Byte56	Sets the color -> black-and-white transition point.	
CROFFJUDG	CAT12_Byte13_bit4	Color/black-and-white switching judgment flag	0[h]: Color mode 1[h]: Black-and-white mode

10.4. When Using the External Microcomputer

10.4.1. External Microcomputer-SS-11X System Interface

System Composition (Connection of External Microcomputer, DSP, and EEPROM)

Be sure to include the DSP EEPROM in the serial communication line, even if EEPROM is available for use with an external microcomputer.

DSP(CXD4103) cannot read or write in EEPROM for an external microcomputer.

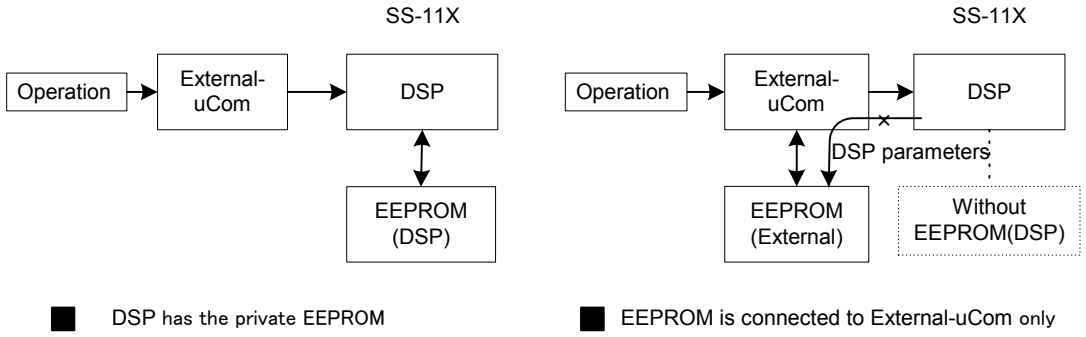


Fig 10.4-1 External Microcomputer-DSP EEPROM Interface

Connection Method

The wiring for each pin is given in the table below.

Table 10.4-1 CXD4103 Wiring with a Microcomputer

Pin name	Pin No	Description
SIFSEL	16	Low
XCS	17	Chip selection input
SI	18	Serial settings input
SO	19	Serial data output
SCK	20	Serial clock input

Note

"L" and "H" of SIFSEL are recognized only during initial operation.

If they are changed, be sure to reset the system.

10.4.2. Communication Protocol with External Microcomputers

Communication Speed

Keep the transfer rate at 400 kbps or less (1SCK > 2.5[us]).

The required transfer rate is such that 32-byte transmissions are less than (1 field - communication prohibited period).

Communication Timing

The CXD4103 loads data in 8-bit units at the rising edge of SCK when XCS is low. The serial output is sent at the falling edge of SCK in synchronization with the serial input. You must leave at least SCK 1 clock division between byte data. The communication data is LSB first. Additionally, make SCK "H" (or pull-up) before making XCS low.

For details on data strings, see the following sections on command specifications and the communication format.

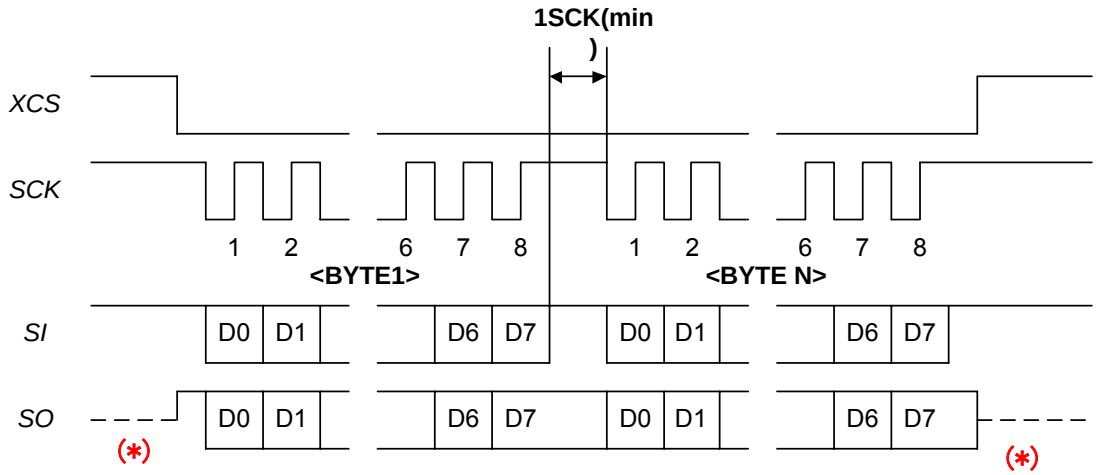


Fig 10.4-2 Communication Timing (External Microcomputers)

(*) The S0 terminal state is maintained after communication (High or Low).

Command Specifications

See "**7.1.4 Communication Format**" for the transmission command specifications (external microcomputer -> DSP) and the reception command specifications (DSP -> external microcomputer).

External Microcomputer Communication Format

The communication format supports packets up to 32 bytes. (The size varies according to the command.) The CXD4103 receives a packet of data, analyzes it, and then performs control to execute a command. Further commands cannot be received until execution of that command is complete. For the command processing time, see "**Table 10.4-2**" and "**Table 10.4-3**".

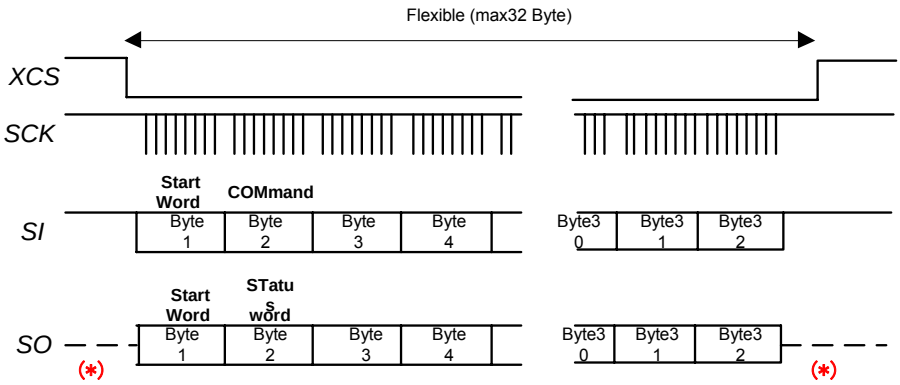


Fig 10.4-3 Microcomputer Communication Format

(*) The S0 terminal state is maintained after communication (High or Low).

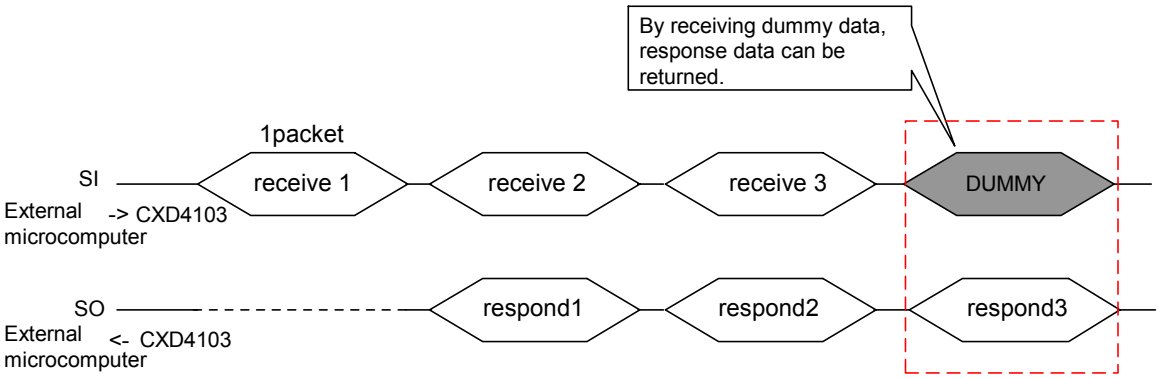


Fig 10.4-4 DSP Response Timing

After the DSP receives a packet, it responds when it receives the next.

Serial Data Latch and Incorporation of Data

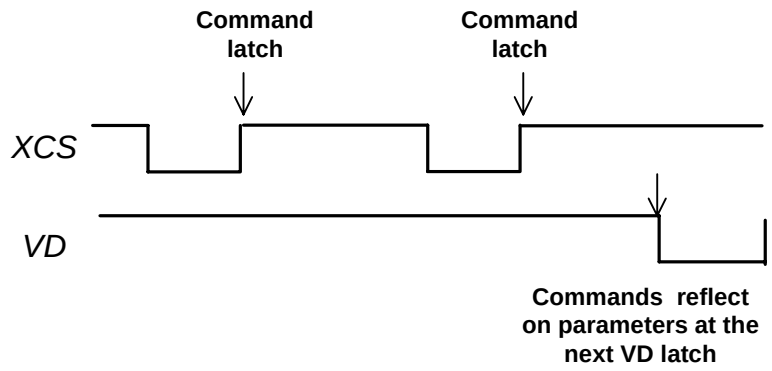


Fig 10.4-5 Serial Data Latch and Parameter Incorporate Timing

Commands are latched and executed after packets are complete (XCS="H"). However, parameter updates from register WRITE commands occur after VD latching of the next field. All latching is performed during the communication prohibited period.

Serial Communication Prohibited Period (Power on/DSP initialization)

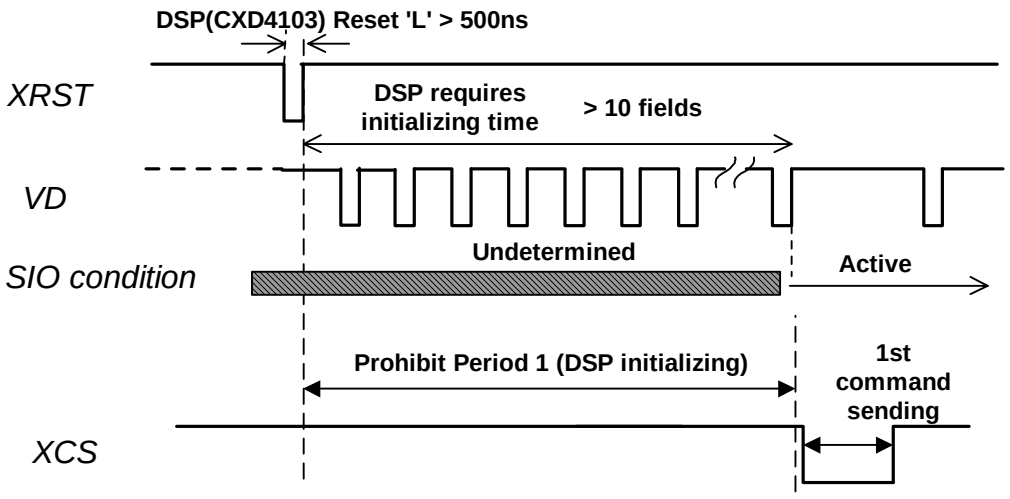


Fig 10.4-6 Communication Prohibited Period during CXD4103 Initialization

Serial communication cannot be received in the initial period (from reset to 10 fields).
Monitor the VD pulse, for example, and wait until the initial period is over.

Serial Communication Prohibited Period (Register Read/Write, EEPROM Read)

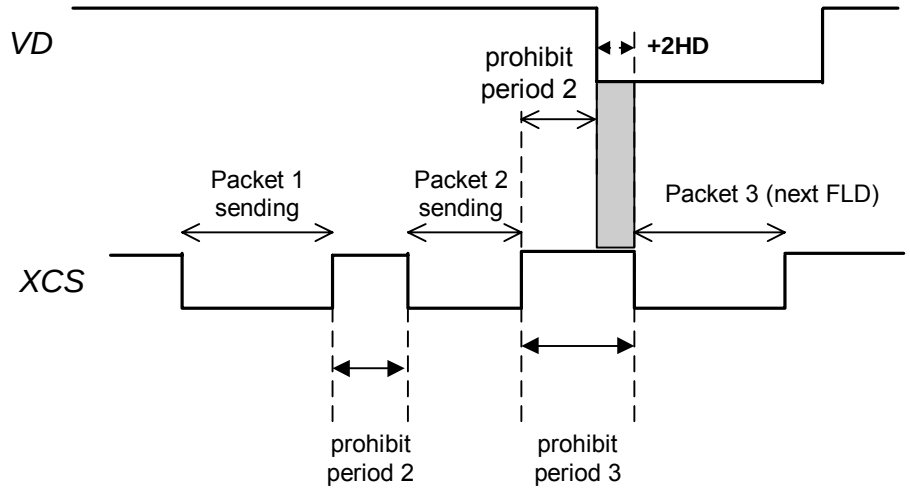


Fig 10.4-7 Communication Prohibited Period during Register Read/Write or EEPROM Read Commands

After a packet is sent, there must be a communication prohibited period (prohibit_period_2) for command processing.

Table 10.4-2 Communication Prohibited Period (Other Than for EEPROM Write)

Command	prohibit_period_2	Prohibit_period_3
Register READ	500 [us]	If it depends on the VD falling edge, communication is also prohibited for +2HD.
Register WRITE		
EEPROM category READ	3.0[ms]	
Specify and Read EEPROM direct address		

To allow for firmware processing for each field, ensure a prohibit_period_3 including a 2HD period after the VD falling edge.

Serial Communication Prohibited Period (EEPROM Write)

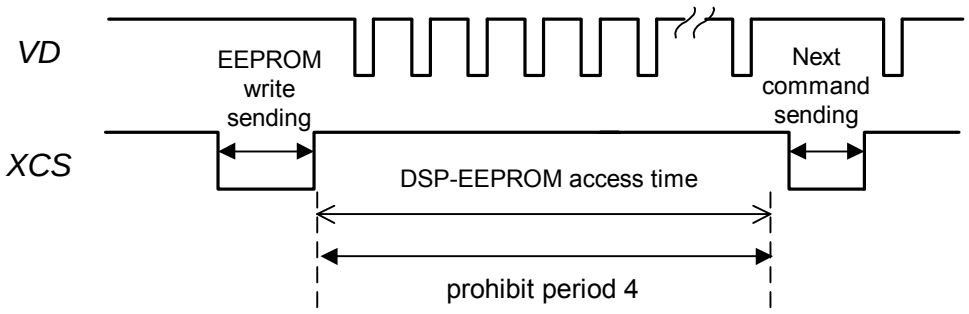


Fig 10.4-8 Communication Prohibited Period of EEPROM Write Commands

When EEPROM write command is received, the next command cannot be received more than 18 fields until the EEPROM write is complete.

Table 10.4-3 Communication Prohibited Period of EEPROM Write

Command	prohibit_period_4
Specify and Write EEPROM direct address	18 field
Specify and Write EEPROM category	
Write all EEPROM categories	360 field

11. Appendix

11.1. Parameters Subject to Priority1 Control

CAT1 SYSCON

Byte, bit	Parameter	Control timing	Control methods (Except CPUHOLD=1[h])
Byte7_bit6	S0IN	Every field	SGHOLD(CAT12_Byte5_bit4)=1[h] or SSELOFF(CAT12_Byte12_bit5)=1[h]
Byte7_bit7	S1IN		
Byte8_bit0-2	S2SEL		
Byte8_bit3-5	S3SEL		
Byte8_bit6-7	S4SEL		

CAT2 PICT1

Byte, bit	Parameter	Control timing	Control methods (Except CPUHOLD=1[h])
Byte4_bit2-5	VHAPG	Every field	VHAPGCTL(CAT12_Byte8_bit0)=1[h]
Byte6_bit7	YGAMSON		
Byte7_bit0	YGAMSLV		
Byte7_bit2-4	YGAMSEL		
Byte7_bit5-7	YKNEESEL		
Byte8	YGAIN		
Byte10_bit0-5	SETUP		
Byte11_bit1-4	YDLY		
Byte30_bit0-2	CGAMMA		
Byte30_bit5-7	CKNEE		
Byte31	RMATY		
Byte32	RMATC		
Byte33	BMATY		
Byte34	BMATC		
Byte37	RYGAIN1		
Byte38	BYGAIN1		
Byte39	RYHUE1		
Byte40	BYHUE1		
Byte41	RYGAIN2		
Byte42	BYGAIN2		
Byte43	RYHUE2		
Byte44	BYHUE2		
Byte45	RYGAIN3		
Byte46	BYGAIN3		
Byte47	RYHUE3		
Byte48	BYHUE3		
Byte49	RYGAIN4		
Byte50	BYGAIN4		
Byte51	RYHUE4		
Byte52	BYHUE4		

CAT4 AWB1

Byte, bit	Parameter	Control timing	Control methods (Except CPUHOLD=1[h])
Byte1	WBR	Every field	AWBHOLD(CAT12_Byte5_bit1)=1[h]
Byte2	WBG	Reset	AWBHOLD(CAT12_Byte5_bit1) = 1[h] or Set the GGAIN(CAT15_Byte4).
Byte3	WBB	Every field	AWBHOLD(CAT12_Byte5_bit1)=1[h]
Byte6	WBYUP		
Byte7	WBYDWN		

CAT7 EXTSYNC1

Byte, bit	Parameter	Control timing	Control methods (Except CPUHOLD=1[h])
Byte1_bit0	INTEXT	Every field	These parameters are controlled by SGMODE. Please do not change parameters.

CAT8 FEADJ(EVRI)

Byte, bit	Parameter	Control timing	Control methods (Except CPUHOLD=1[h])
Byte3	AGCCNT	Every field	AEHOLD(CAT12_Byte5_bit2)=1[h]
Byte4	EVR1CNT		If you set AEHOLD(CAT12_Byte5_bit2) to 1[h] or MIRIS(CAT14_Byte1_bit1) to 0[h], the setting value can be changed.

CAT11 BLMDETS1

Byte, bit	Parameter	Control timing	Control methods (Except CPUHOLD=1[h])
Byte10	IBLKS1L	Every field	CLMPHOLD(CAT12_Byte5_bit3)=1[h]
Byte11	IBLKS2L		
Byte12_bit0	IBLKS1M		
Byte12_bit1	IBLKS2M		

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