SS-11RM Application Notes

Ver.1.1.4. . . June 30, 2005

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CONTENTS

0. New Functions of SS-11RM

0.1. MIRROR (CAT3-Byte9-bit7)

MIRROR (CAT3-Byte9-bit7) is the parameter which makes the mirror Image for Video output singnal.

MIRROR(CAT3-Byte9-bit7) = "0" : Normal
MIRROR(CAT3-Byte9-bit7) = "1" : Mirror

0.2. OFFSET25 (CAT7-Byte12-bit7)

OFFSET25 (CAT7-Byte12-bit7) is the parameter which puts 25Hz OFFSET on the subcarrier in PAL system.

OFFSET25(CAT7-Byte12-bit7) = "0" : PAL OFFSET 25Hz OFF
OFFSET25(CAT7-Byte12-bit7) = "1" : PAL OFFSET 25Hz ON

0.3. PLLSW (CAT9-Byte14-bit4)

PLLSW (CAT9-Byte14-bit4) is the parameter which makes the clock "CK(PIN43)" the double frequency clock which drives the circuits in YCmix block.
It realizes the excellent performance in Line-Lock mode.

PLLSW(CAT9-Byte14-bit4) = "0" : 19MHz(Normal)
PLLSW(CAT9-Byte14-bit4) = "1" : 38MHz

1. IC Configuration

1.1. Basic Block Diagram

The SS-11RM is a digital signal processing system for single-chip CCD color cameras, and is comprised from the following three main ICs.

<1> CXD3142R: Signal Processor LSI for a Single-Chip CCD Color Camera

- Built-in timing signal generation circuit for CCD drive (supports 250K pixel CCD image sensors)
- Built-in sync signal generation circuit that supports external synchronization (supports NTSC/PAL systems)
- Luminance and Chroma signal processing
- Built-in digital encoder
- Built-in AE/AWB integral circuit
- Built-in microcontroller with AE/AWB control functions
- Built-in 9-bit A/D converter
- Built-in 10-bit D/A converter (analog composite output)
- Built-in YUV 8-bit multiplex digital output circuit
- Built-in serial communication circuit that supports a microcomputer
- Built-in circuit for communication with peripheral ICs

<2> CXD1267AN: CCD horizontal clock drivers

- Built-in CCD vertical clock driver and shutter pulse driver

<3> CXA2096N: CDS/AGC IC for CCD Camera

- Built-in correlated double sampling (CDS) circuit
- Built-in AGC circuit
- Built-in A/D converter interface circuit

In addition to the above three ICs, the following ICs are also necessary to comprise the system.

<4> MB88347L: 8-bit D/A Converter for Generating 8-channel DC Voltage.....Fujitsu Limited.

or

M62367: 8-bit D/A Converter for Generating 8-channel DC Voltage

..... Renesas Technology Co.Ltd

Application: The MB88347L/M62367 is used to generate the various DC voltages used by the SS-11RM system.

Specific DC voltages include the AGC control voltage adjustment, etc.

This IC may not be used for some cameras with special specifications where AGC is not used, etc. However, it is generally necessary to comprise the system.

Note that other substitutions are not possible due to limitations in the communication format.

* Note that the end symbol may be changed due to version upgrade, etc.

<5> AK6420A: 128-word x 16-bit EEPROM..... Asahi Kasei Microsystems CO., LTD.

or

CAT64LC40JI: 256-word x 16-bit EEPROM .....Catalyst Semiconductor, Inc.
(only 128 words used)

Application: This IC is used to save the various SS-11RM parameters. This IC may not be required in some cases such as when the CXD3142R is reset by serial communication each time the system is started up, but it should be used for other normal systems.

Note that other substitutions are not possible due to limitations in the communication format.

* Note that the end symbol may be changed due to version upgrade, etc.

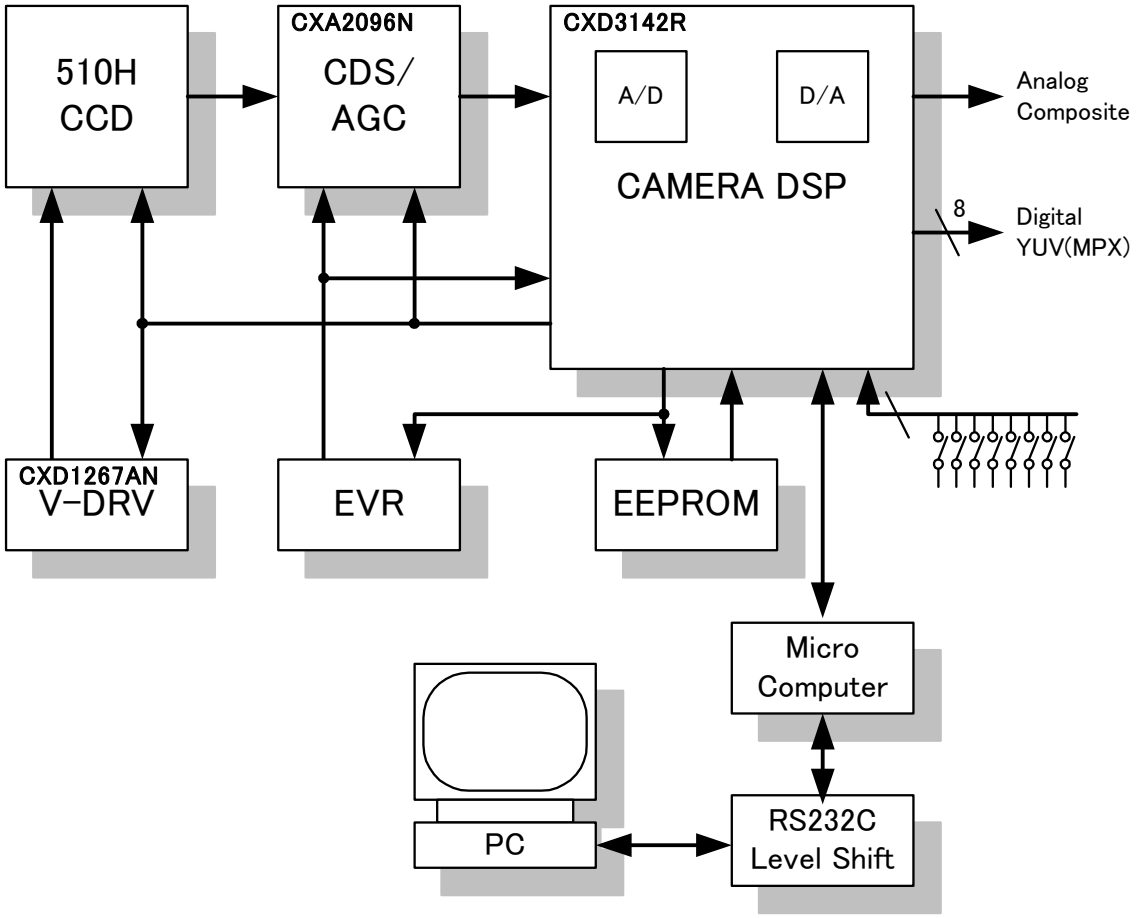


Fig. 1.1-1 SS-11RM Basic Block Diagram

The basic block configuration of the SS-11RM is shown in “Fig. 1.1-1 SS-11RM Basic Block Diagram”.

Overall SS-11RM system operation has the following features.

(1) The microcontroller built into the camera DSP is equipped with basic AE/AWB algorithms, making it possible to design a digital color camera without an external microcomputer.

(2) The microcontroller controls the entire SS-11RM system via the serial interface circuit. One example of this is that AGC gain settings are performed by controlling the EVR (electronic volume) from the microcontroller in accordance with the AE algorithm.

(3) The serial interface circuit built into the CXD3142R is equipped with microcomputer 3-wire serial communication functions. All setting parameters for the SS-11RM can be transmitted and set by communication from an external microcomputer. Also, parameter values set via the serial bus in (2) above can be written to an external EEPROM. Data stored in the EEPROM is read into the CXD3142R when the system is started up and functions as the system’s initial settings.

(4) The CXD3142R contains the initial parameter values for the SS-11RM system. Therefore, basic images can be obtained without serial communication or an EEPROM. However, an EEPROM should be used for parameter adjustment of picture quality. Also, the CXD3142R has switch input pins for setting the basic color camera modes. This function makes it possible to select basic camera modes without serial communication or an EEPROM.

1.2. Overall System Operation

As described in “Fig. 1.1-1 SS-11RM Basic Block Diagram”, the SS-11RM is able to specify basic camera modes using external switch settings. In addition, the system can be initialized to the desired settings during power-on by writing the setting parameters to an external EEPROM.

When the SS-11RM is connected to an external EEPROM that is written with valid data, preference is given to initializing the various settings by reading the EEPROM data when the system is started up. The data written in the front address (00[h]) of the EEPROM is used to determine whether the EEPROM is connected and whether the internal data is valid. This data is specified as the SS-11RM code, and the CXD3142R determines that the EEPROM exists only when this data is **92[h]**, and ignores the EEPROM when any other data is written.

When an EEPROM is not connected, or if the SS-11RM code is **other than 92[h]** even when an EEPROM is connected, initialization operation reflects the TV system switch settings and the DSP internal setting when the SS-11RM system is started up.

When setting the mode and parameters by microcomputer communication from an external host, use the CXD3142R pins shown below for serial communication.
See the descriptions of “7. Communication Specifications” for details.

Table. 1.2-1 Microcomputer Communication Pin Description

Symbol	Pin No.	Description
SI	37	Serial data input
SO	38	Serial data output
SCK	39	Serial clock input
XCS	36	Chip select input

As described in “Fig. 1.1-1 SS-11RM Basic Block Diagram”, the basic SS-11RM configuration is such that the entire system is controlled by the microcontroller built into the CXD3142R. The ICs controlled by the CXD3142R and the control contents are as shown in “Table. 1.2-2 ICs Controlled by the CXD3142R and Control Contents”.
The camera SIO pins are used for communication with each IC. (See “Table. 1.2-3 CXD3142R Camera SIO Pin Functions and Connections”).

Table. 1.2-2 ICs Controlled by the CXD3142R and Control Contents

Product name	Function	Control contents
MB88347L M62367	Electronic volume (EVR8-ch)	Various DC control voltages
AK6420A	EEPROM	Writing and reading various setting parameters

Table. 1.2-3 CXD3142R Camera SIO Pin Functions and Connections

Symbol	Pin No.	Function	Connections
CASO	33	Peripheral serial data output	MB88347L 14pin DI M62367
			AK6420A 5pin DI
CASI	32	Peripheral serial data input	AK6420A 6pin DO
CASCK	34	Peripheral serial clock output	MB88347L 13pin CLK M62367
			AK6420A 4pin CK
CSEVR	30	EVR chip select output	MB88347L 12pin LD M62367
CSROM	31	EEPROM chip select output	AK6420A 3pin CS

When controlling or setting SS-11RM system operation by serial communication, the CXD3142R internal settings are changed by sending data from the microcomputer to the CXD3142R using the microcomputer communication port (See “Table. 1.2-1 Microcomputer Communication Pin Description”). Also, peripheral IC settings are changed by communication using the camera SIO pins noted above (See “Table. 1.2-3 CXD3142R Camera SIO Pin Functions and Connections”), and data is written/read through communication with the EEPROM.

2. Parameter Configuration

2.1. Communication Category Concepts

SS-11RM communication categories are divided by control subject.

Table. 2.1-1 List of CXD3142R Serial Communication Categories

Category number	Symbol	Communication contents
CAT1	SYSCON	Overall system setting parameters
CAT2	CPU	Internal controller setting, operating mode setting, and port driver setting parameters
CAT3	PICT	Picture quality adjustment parameters
CAT4	AE	AE parameters
CAT5	AWB	AWB parameters
CAT6	ADJUST	Line adjustment parameters
CAT7	TIMING	Timing adjustment and detect correction setting parameters
CAT8	SOUT	Serial out setting parameters
CAT9	EXTCONT	External control parameters

2.2. Microcontroller Parameters

Microcontroller Outline

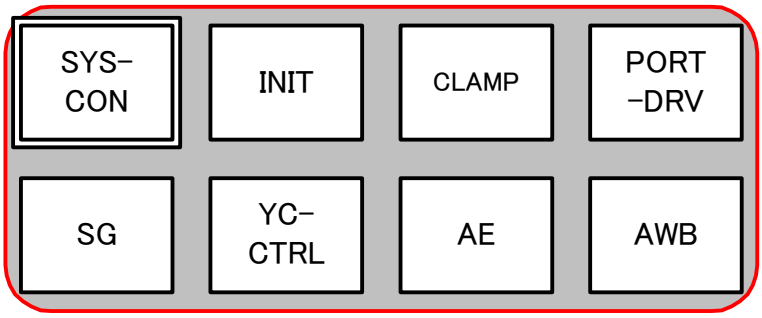


Fig. 2.2-1 Microcontroller Block Names

This section describes the operation of each microcontroller block shown in “Fig. 2.2-1”.

(1) The CXD3142R has a built-in microcontroller in order to realize the various camera controls without using an external microcomputer.

This microcontroller has the following seven main control functions (represented by the block names).

1. INIT:
   This initializes the parameters of the internal blocks during power-on.
   The EEPROM is read and initialization is performed according to these contents.
2. AE:
   This controls TG and EVR inside the CXD3142R, and achieves electronic iris and AGC feedback control.
3. AWB:
   This controls the white balance amplifier based on the results of integrating the RGB inside the screen to realize feedback type AWB control.
4. YC-CTRL:
   This controls the VH aperture correction gain and color difference gain based on the AGC gain to realize low-illumination suppress.
5. CLAMP:
   This realizes YC digital clamping based on the results of integrating the CCD optical black signal.
6. PORT-DRV:
   This reads the settings of the DIP switches connected to the CXD3142R pins and transfers these settings to the internal blocks.
7. SG:
   This reads the shifter switch settings (UP/DOWN) during during external synchronization mode to control the synchronization phase.

(2) Each microcontroller function has a switch that can be used to stop the control operation. (CAT2-Byte 4)
For example, to control AE/AWB and other operating mode switching by serial communication, turn off the microcontroller's PORT-DRV block to allow mode switching by serial communication from the external microcomputer.
This ON/OFF function is controlled by the system controller (SYS-CON) block of the microcontroller.
The system manager has the following three main functions.

1. ON/OFF function that stops all microcontroller functions. (CPUEXT: CAT2-Byte 4-bit 0)
2. ON/OFF function that stops some microcontroller function. (CPU*: CAT2-Byte 4* = AE, AWB, SPRS, SG, and DIP)

3. Coprocessor mode that outputs the microcontroller control status and operation results by serial communication. (CPUCMD: CAT2-Byte 1)

Microcontroller Control Parameters

This section describes the communication parameters controlled by the microcontroller.

(1) Each microcontroller block controls the corresponding communication category at a field cycle. (See “Table. 2.2-1”)

Table. 2.2-1 Communication Parameters Controlled by the Microcontroller

Block name	Corresponding parameters	Block function ON/OFF bit (CAT2-Byte 4)
AWB	CAT9: EXTCON Bytes 5, 6 and 7	CPUAWB
YC-CTRL	CAT3: PICT Bytes 3, 10 and 11	CPUSPRS
SG	CAT7: TIMING Byte 9, Byte 10-Bit2	CPUSG
PORT-DRV	Target parameters set by the following CAT2: CPU Bytes 8 to 23	CPUDIP
SYS-CON	CAT3: PICT Bytes 7, 12 and 13 CAT9: EXTCON Bytes 16 and 17, 18 and 19	CPUEXT

(The INIT block controls CAT 1 to 9 only during the reset operation.)

(2) Each microcontroller block controls the corresponding parameters shown in “Table. 2.2-1 Communication Parameters Controlled by the Microcontroller” at a field cycle, so communication or setting changes from an external source are invalid. (Because the external communication settings are overwritten by the microcontroller.)

Therefore, the microcontroller control functions can be turned off in block units so that overwriting is not performed. (See “Block function ON/OFF bit” in “Table. 2.2-1 Communication Parameters Controlled by the Microcontroller”.) These block function ON/OFF bits (CPU***) are used to perform external settings. Set the desired CPU*** bits to 1 to stop the respective block functions and then perform the settings using an external microcomputer.

2.3. How to use the CPU commands

2.3.1. List of the commands

CPUCMD (CAT2-Byte 1)

00[h] : Normal Operation

01[h] : Switching of application mode

21[h] : AGCMIN adjustment mode -> Please refer to AE adjustment.

31[h] : AWB monitor mode -> Please refer to Pre-white balance adjustment.

32[h] : AWB coprocess mode -> Please refer to Pre-white balance adjustment.

50[h] : EEPROM readout mode

CPUADRS (CAT2-Byte 2)

00[h] : Application mode（Normal Operation）

01[h] : Initializing mode

02[h] : EERPOM writing mode

2.3.2. How to write the data into the EEPROM

How to write the date into EEPROM is shown below. We recommand that all the adjustments are done before writing into EEPROM.

1.…… Set **CPUEXT** (CAT2-Byte 4-bit 0) to 1.

2.…… Send the date of each category.

3.…… Set **CPUADRS**（CAT2-Byte 2）to 2.

4.…… Set **CPUCMD** (CAT2-Byte 1) to 1.

5.…… Set **CPUCMD** (CAT2-Byte 1) to 0.

This writing is done in 4 or 5 seconds. Then **CPUEXT, CPUADRS** must be changed as they were.

2.3.3. How to read out the data from the EEPROM

The date written on EEPROM is available to read out by serial communication. How to read out is shown below. A parameter received is just one for each transfer. Repeat the operations from the operation 4 to receive several parameters.

1. Set **CPUADRS** (CAT2-Byte 2) to 1.
2. Set **CPUCMD** (CAT2-Byte 1) to 1, and set it to 0.
   By this operation, DSP is initialized as the configuration written on EEPROM.
3. Set **CPUCMD** (CAT2-Byte 1) to **50**[h].
4. Input the lower address to **CPUADRS** (CAT2-Byte 2) and the the upper address to **CPUDATA** (CAT2-Byte 3).
5. Set **SOBYTE** (CAT8-Byte 1) to 1. The parameter indicated by the data **E2RDATA** (CAT8-Byte 9) of the serial output are received.
6. Repeat the operations from 4 to receive more parameters.
7. Set **CPUCMD** (CAT2-Byte 1) to **0**[h]**.**

Ex)

When **GGAIN** (CAT5-Byte 3) are read out, set **CPUADRS** to 47[h] and **CPUDATA** to 2[h].

3. Application Circuits

3.1. Oscillator Circuit and Surrounding Areas

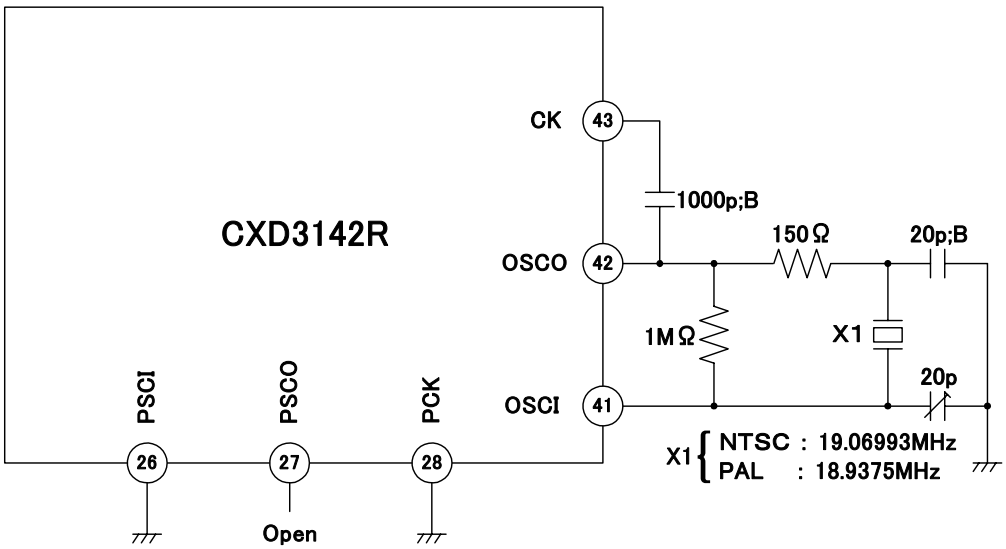


Fig. 3.1-1 Oscillator Circuit Configuration in Internal Sync Mode

"Fig. 3.1-1 Oscillator Circuit Configuration in Internal Sync Mode" shows the oscillator circuit example introduced with the SS-11RM Evaluation Board. Note that operation using the circuit constants noted here has been confirmed for Sony evaluation boards employing the crystal oscillators listed in "Table. 3.1-1 Evaluation Board Components", and performance including temperature characteristics is not guaranteed if the board layout is changed or different components are selected.

PSCI (CXD3142R Pin 26), PSCO (CXD3142R Pin 27) and PCK (CXD3142R Pin 28) are not used in internal sync mode, so connect PSCI and PCK to GND and leave PSCO open as shown in "Fig. 3.1-1 Oscillator Circuit Configuration in Internal Sync Mode".

In the SS-11RM (CXD3142R), the CCD drive clock and subcarrier generation clock are generated from a single crystal oscillator. Therefore, a subcarrier PLL is not required.

Table. 3.1-1 Evaluation Board Components

Component name	Manufacturer name	Model No.	Frequency	Load capacitance
Crystal oscillator	RIVER ELETEC CORPORATION	HC-49/U03	19.06993 [MHz]	16 [pF]
Crystal oscillator	RIVER ELETEC CORPORATION	HC-49/U03	18.9375 [MHz]	16 [pF]

Adjusting trimmer capacitor

Adjust trimmer capacitor in "Fig. 3.1-1 Oscillator Circuit Configuration in Internal Sync Mode" so that the RG frequency is aligned accurately. See "Table. 3.1-2 RG Frequency" below for the RG frequency.

Table. 3.1-2 RG Frequency

System	Frequency
NTSC	9.534965 [MHz]
PAL	9.46875 [MHz]

3.2. Noise Countermeasures

A 4-layer board design is recommended in order to reduce noise as much as possible in the board design stage. With a 2-layer board design, the power supply and GND impedance tend to rise due to area limitations, thus lowering resistance to beat and other noise.

In addition, unused input pins should be pulled up or down as necessary. See “3.5Open Pin Processing for Each Mode”.

Care should be taken for the following items when designing the board in order to reduce noise.

3.2.1. CXD3142R and Surrounding Areas

1. Connect LC filters close to the power supplies input to VDD and AVD so that there is no interference due to cross talk from other circuits. Note that VDD2 and VDD4 should input the power supply output from a single filter, and other pins should input the power supply output from separate filters. Also, connect by-pass capacitors as close as possible between each pin and GND. Connect 47 uF by-pass capacitors to AVD2 and AVD4.
2. The crystal oscillator circuit has a high frequency, so make the signal lines as short as possible and surround them with a GND shield as a countermeasure against noise.
3. The internal structure of the trimmer capacitor used to fine adjust the frequency is such that the pins which are conductive with the variable knob portion should be connected to GND.
4. Note that the signal lines between CCD drive pins RG, H1 and H2 and the CCD image sensor should be individually shielded by GND, and earth coupling should be strengthened by providing a large number of GND pins.
5. VRB (CXD3142R Pin 5) and VRT (CXD3142R Pin 1) are ADC reference voltage inputs. Noise easily enters these signals, so be sure to connect by-pass capacitors near to these pins.

3.2.2. CXA2096N and Surrounding Areas

1. Connect LC filters close to the power supply input to VCC so that there is no interference due to cross talk from other circuits. Also, connect by-pass capacitors as close as possible between each pin and GND.
2. PIN (CXA2096N Pin 21) and DIN (CXA2096N Pin 22) are CCD signal input pins, so make the signal lines as short as possible and surround them with a GND shield.
3. VRB (CXA2096N Pin 7) and VRT (CXA2096N Pin 8) are ADC reference voltage outputs. Noise easily enters these signals, so be sure to connect by-pass capacitors immediately after these pins.
4. Crosscut clamp noise can be reduced by increasing the capacitance of the capacitor between AGCCLP (CXA2096N Pin 13) and GND. However, note that if the capacitance is too large, the response will be slow resulting in inadequate clamp operation during startup. Approximately 1 uF is recommended.

3.2.3. CXD1267AN and Surrounding Areas

1. Connect LC filters close to the power supplies input to VH and VL so that there is no interference due to cross talk from other circuits. Also, connect by-pass capacitors as close as possible between each pin and GND.
2. Note that the signal lines between CCD drive pins VSHT, Vϕ4, Vϕ3, Vϕ2, and Vϕ1 and the CCD image sensor should be individually shielded by GND, and earth coupling should be strengthened by providing a large number of GND pins.

3.2.4. If Noise Occurs

When noise is confirmed on the screen when the signal is displayed on a monitor using the designed board, the possible causes are listed below for reference.

1. Power supply

   Noise countermeasures such as reviewing the power supply bock layout, strengthening the GND shielding, and adding power supply filters should be investigated to prevent noise from the power supply from interfering with other circuits.

2. Boards and circuits

   Investigate reviewing and further strengthening noise countermeasures for the ICs and surrounding areas noted above.

3. External sync

   The external sync circuit and PLL circuit may be affecting other circuits, so investigate strengthening the GND and improving the layout.

3.3. CXD3142R Power Reset Circuit

3.3.1. Outline

This circuit resets the system so that operation starts in a stable manner after the CXD3142R is turned on.

Note that the transient characteristics of the used power supplies may cause some problems. Therefore, circuits that satisfy the following conditions should be added in order to reliably avoid these problems.

* The XRST pin of the CXD3142R should be set low when the CXD3142R's 3.3 V power supply falls below 2.7 V.
  Also, the XRST pin should remain low for a minimum of 500 ns or more when the 3.3 V power supply rises above 2.7 V.

3.3.2. Circuit Example

The timing chart is shown in “Fig. 3.3-1 Timing Chart”, and the reset circuit is shown in “Fig. 3.3-2 Reset Circuit Example”.

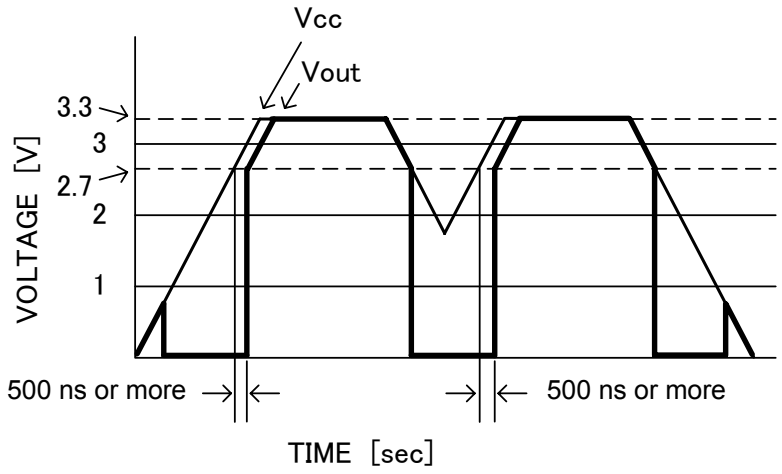


Fig. 3.3-1 Timing Chart

*(The relationship between the circuit constants and the timing is not guaranteed.)

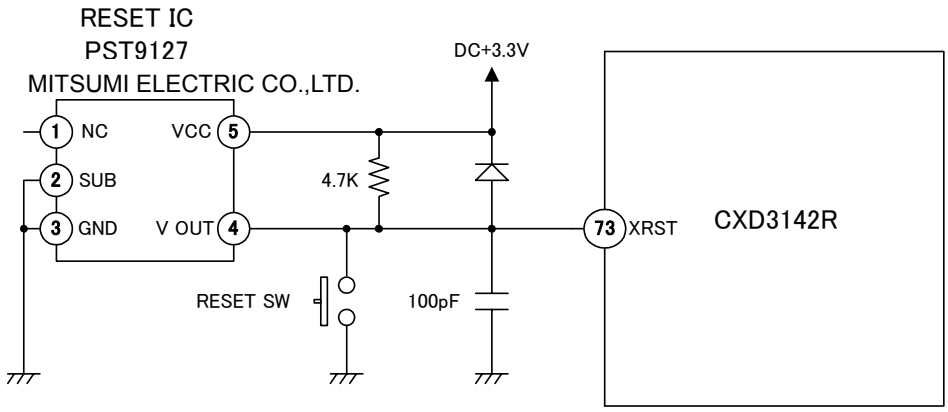


Fig. 3.3-2 Reset Circuit Example

3.4. External LPF Characteristics and Circuit Example

3.4.1. Necessity of the LPF

LPF features

A composite signal circuit LPF is recommended to remove the excess clock signal.

Table. 3.4-1 Trap Frequency

System	Trap frequency
NTSC	4.767 [MHz]
PAL	6.75 [MHz]

Relationship between the limit resolution and the LPF

The resolution is greatly influenced by the size of LPF transfer characteristic Q. When designing the system, be sure to make Q as large as possible through cascade connections.

Phenomenon occurring when an LPF is not used

1. The excess clock signal is mixed with the video signal and appears in the video as vertical stripe noise.
2. The frequency band stretches wider than is necessary causing a reflected signal to appear.
3. A high frequency component remains in the subcarrier signal.

3.4.2. Example of LPF Characteristics

Filter characteristics for each system (for both NTSC and PAL)

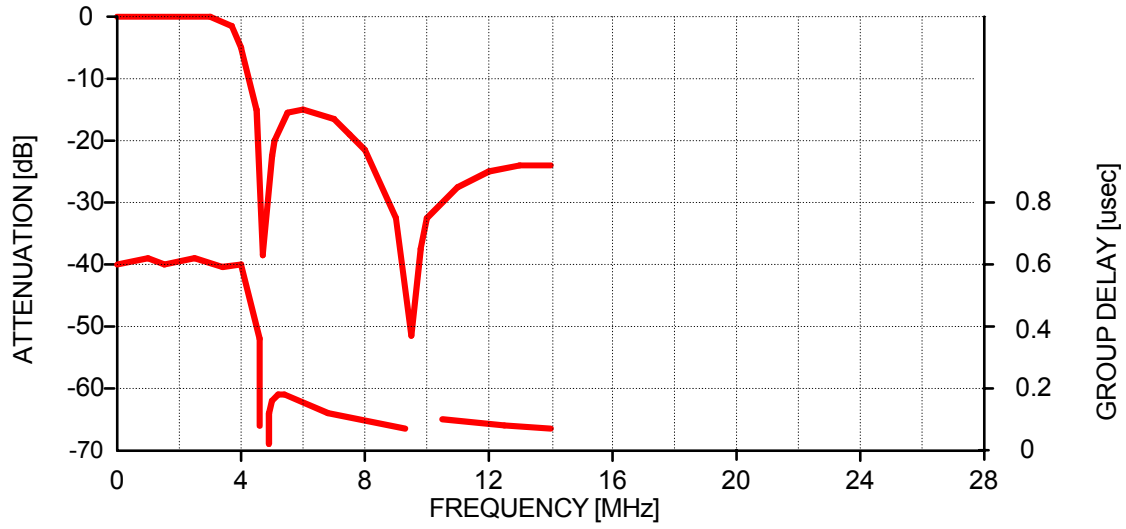


Fig. 3.4-1 NTSC (H355LDK-8291, G355ENK-8292) Characteristics Diagram

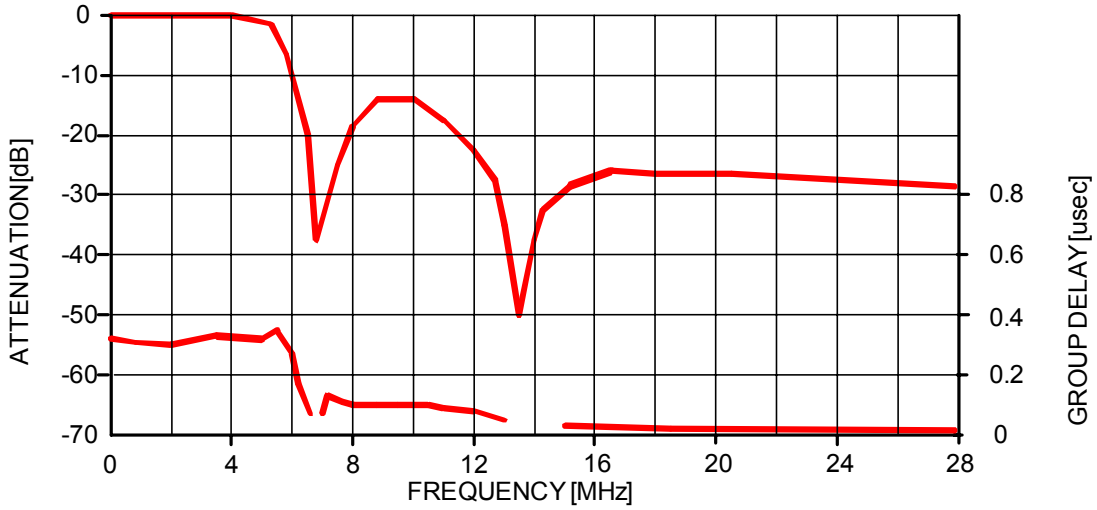


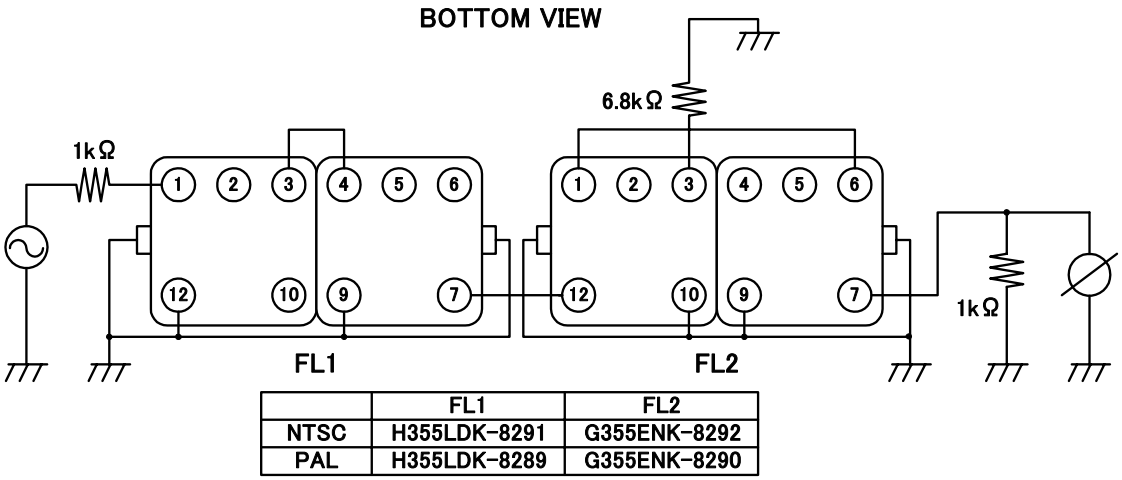
Fig. 3.4-2 PAL (H355LDK-8289 G355ENK-8290) Characteristics Diagram

Filter configuration for each system

Table. 3.4-2 Example of Filters Used with Each CCD Type

System	FL1 (type)	FL2 (type)	External resistance (R68)
NTSC	*H355LDK-8291	* G355ENK-8292	6.8 [KΩ]
PAL	*H355LDK-8289	* G355ENK-8290	6.8 [KΩ]

(made by TOKO CO., INC.)*



	FL1	FL2
NTSC	H355LDK-8291	G355ENK-8292
PAL	H355LDK-8289	G355ENK-8290

Fig. 3.4-3 Characteristics Measurement Circuit Example

Notes on operation

1. Module filters generally have a specified I/O impedance, and must be matched according to the specified constants when incorporated into circuits. If this is not done, the expected characteristics cannot be obtained.

2. Module shield cases should be connected to the board GND in order to stabilize the characteristics.

3. Filters have low input impedance and the gain is also attenuated by approximately 10 dB, so care should be taken for the connected amplifier.

3.5. Open Pin Processing for Each Mode

Perform the following pin processing according to the mode.

3.5.1. During Internal Synchronization Mode

Table. 3.5-1 Pin Processing during Internal Synchronization Mode

Processed symbol (Pin No.)	Processing method
PSCI (26)	GND
PSCO (27)	OPEN
PCK (28)	GND

3.5.2. When not Communicating with an External Microcomputer

Table. 3.5-2 Pin Processing when not Communicating with an External Microcomputer

Processed symbol (Pin No.)	Processing method
XCS (36)	VDD
SI (37)	VDD or GND
SO (38)	OPEN
SCK (39)	VDD or GND

3.5.3. When Using Digital Output (when not using DAC output)

Table. 3.5-3 Pin Processing when not Using DAC Output

Processed symbol (Pin No.)	Processing method	Processed symbol (Pin No.)	Processing method
VB (54)	OPEN	VG (58)	AVD
AVS5 (55)	GND	AVD5 (59)	AVD
IREF (56)	AVD	IO (60)	AVD or OPEN
VREF (57)	AVD		

4. CCD Type Selection

4.1. Supported CCD Types

The SS-11RM supports the following CCD image sensors. (However, note that the types shown below are the types supported when these Application Notes were prepared, and that additions or deletions may occur due to CCD version upgrades or discontinued production, etc.)

Table. 4.1-1 CCD Image Sensors Supported by the SS-11RM

CCD type	Optical size	TV system	Product name
510H	Type 1/4	NTSC	ICX206AK
			ICX226AK
		PAL	ICX207AK
			ICX227AK
	Type 1/3	NTSC	ICX254AK
			ICX404AK
		PAL	ICX255AK
			ICX405AK
	Type 1/6	NTSC	—
		PAL	—

• Lineup as of October 1, 2001.

4.2. Wiring Changes

The drive circuit must be changed according to the type of CCD used.

The main differences are changes in the drive circuit due to different CCD image sensor drive specifications.

4.2.1. Drive Circuit Changes

The drive specifications of CCD image sensors that can be driven by the SS-11RM are shown in the table below.

Table. 4.2-1 CCD Image Sensors and Drive Conditions

CCD type		Product name	DC voltage specifications		AC voltage specifications (typ.)				Drive circuit example
Optical size			Vsub voltage	RG voltage	ϕH	ϕRG	VL	VH	
510H	Type 1/4	ICX206AK	Generated internally, adjustment free	Generated internally, adjustment free	3.3V	3.3V	-7.0V	15.0V	Fig. 4.2-1
		ICX207AK							
		ICX226AK				3.3V	-5.0V	12V	Fig. 4.2-2
		ICX227AK							
	Type 1/3	ICX404AK	Generated internally, adjustment free	Clamped high, adjustment free	5.0V	5.0V	-7.0V	15.0V	Fig. 4.2-3
		ICX405AK							
		ICX254AK		Generated internally, adjustment free		5.0V	-7.0V	15.0V	Fig. 4.2-4
		ICX255AK							
	Type 1/6	—	—	—	—	—	—	—	—
		—							

As mentioned above, the following drive circuit points must be changed when the CCD type differs.

<1> RG clamp circuit

<2> CXD1267AN supply voltage

<3> CXD3142R supply voltage

See the drive circuit examples on the following pages for each change.

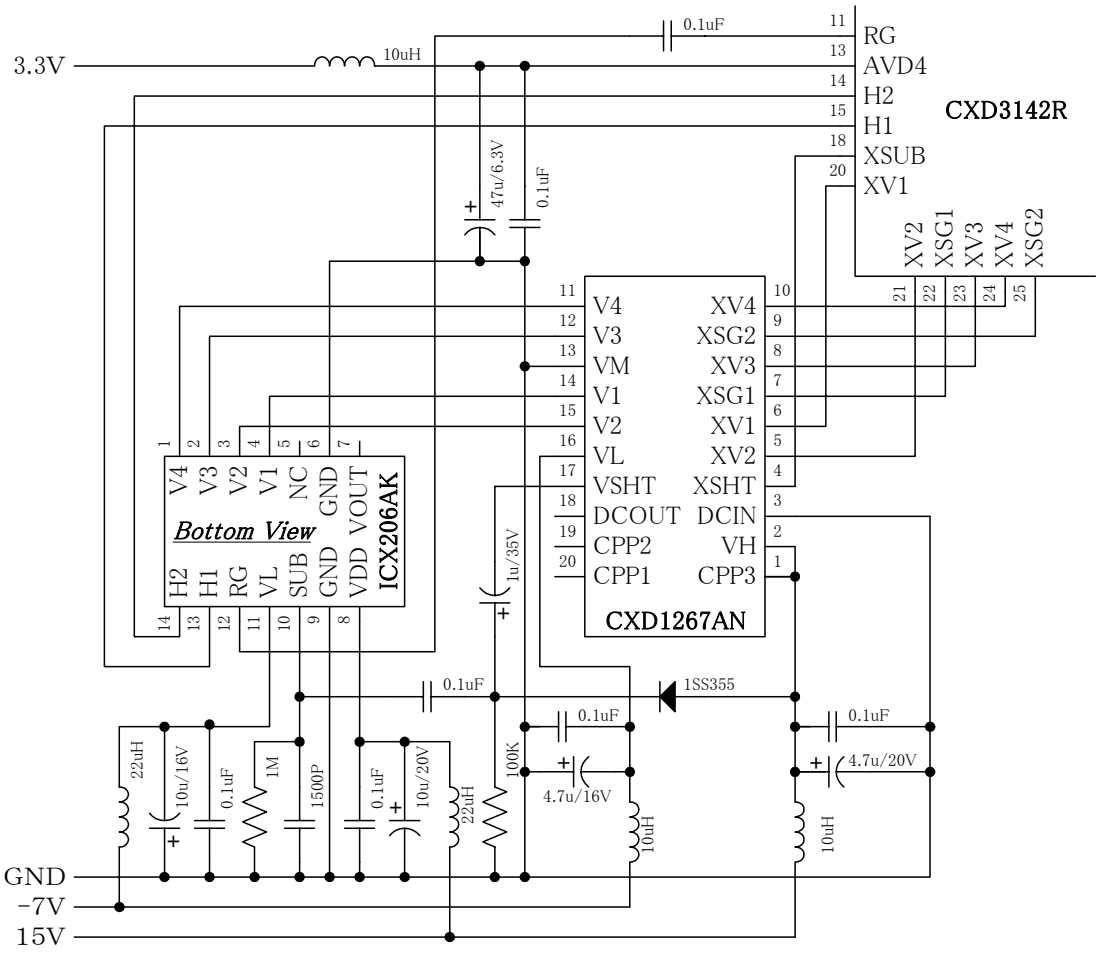


Fig. 4.2-1 CCD Drive Circuit Example 1

"Fig. 4.2-1 CCD Drive Circuit Example 1" shows the drive circuit configuration when using 1/4" CCD image sensors (ICX206/207AK). The Vsub and RG voltages are both adjustment-free.

The drive circuit requires three types of supply voltages: 3.3 V, 15 V and –7 V.

The RG pulse should be input to the CCD RG pin after cutting the DC component with a capacitor.

Vsub Voltage is clamped and generated inside the CCD, and the CXD1267AN VSHT (Pin 17) output is input to the CCD SUB pin via a capacitor.

The CXD1267AN DCOUT (Pin 48) should be left open and DCIN (Pin 1) should be connected to GND.

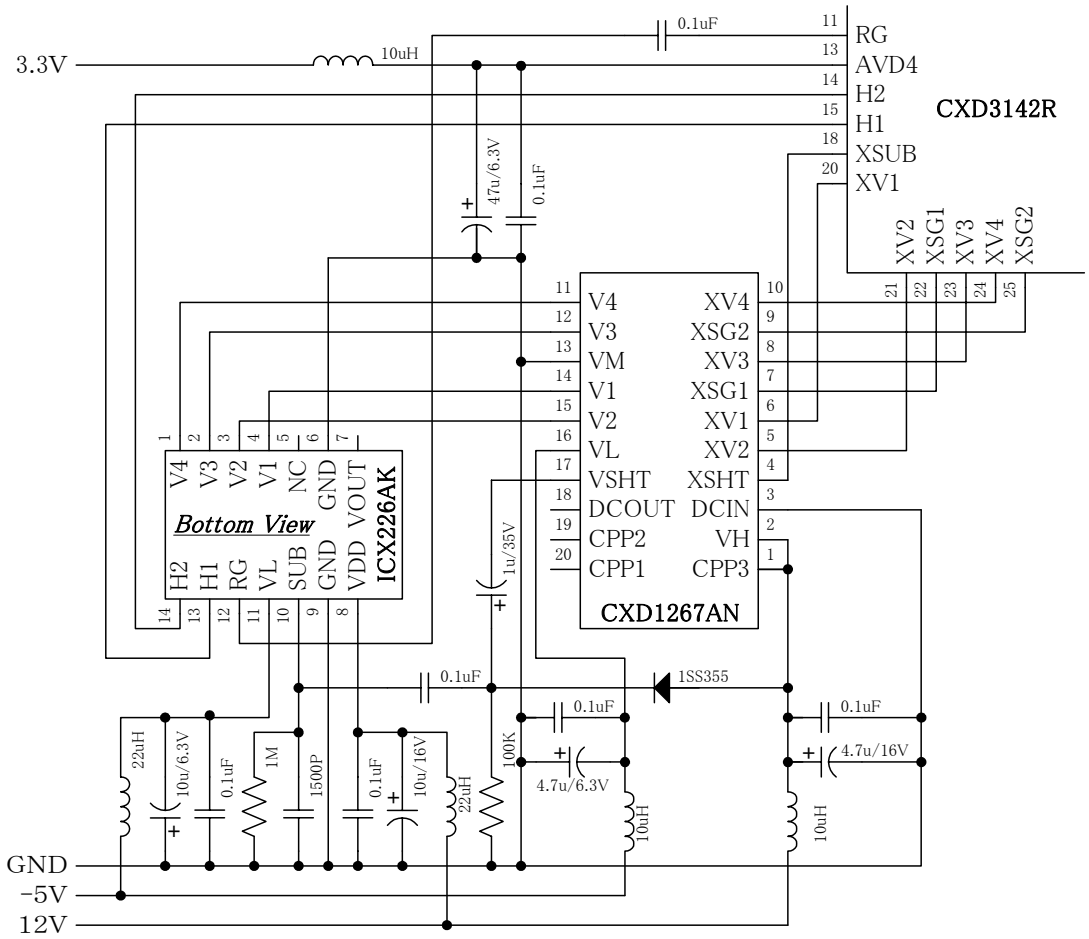


Fig. 4.2-2 CCD Drive Circuit Example 2

"Fig. 4.2-2 CCD Drive Circuit Example 2" shows the drive circuit configuration when using 1/4" CCD image sensors (ICX226/227AK). The Vsub voltage and RG voltages are adjustment-free.

The drive circuit requires three types of supply voltages: 3.3 V, 12 V and –5 V.

The RG pulse should be input to the CCD RG pin after cutting the DC component with a capacitor.

Vsub Voltage is clamped and generated inside the CCD, and the CXD1267AN VSHT (Pin 17) output is input to the CCD SUB pin via a capacitor.

The CXD1267AN DCOUT (Pin 48) should be left open and DCIN (Pin 1) should be connected to GND.

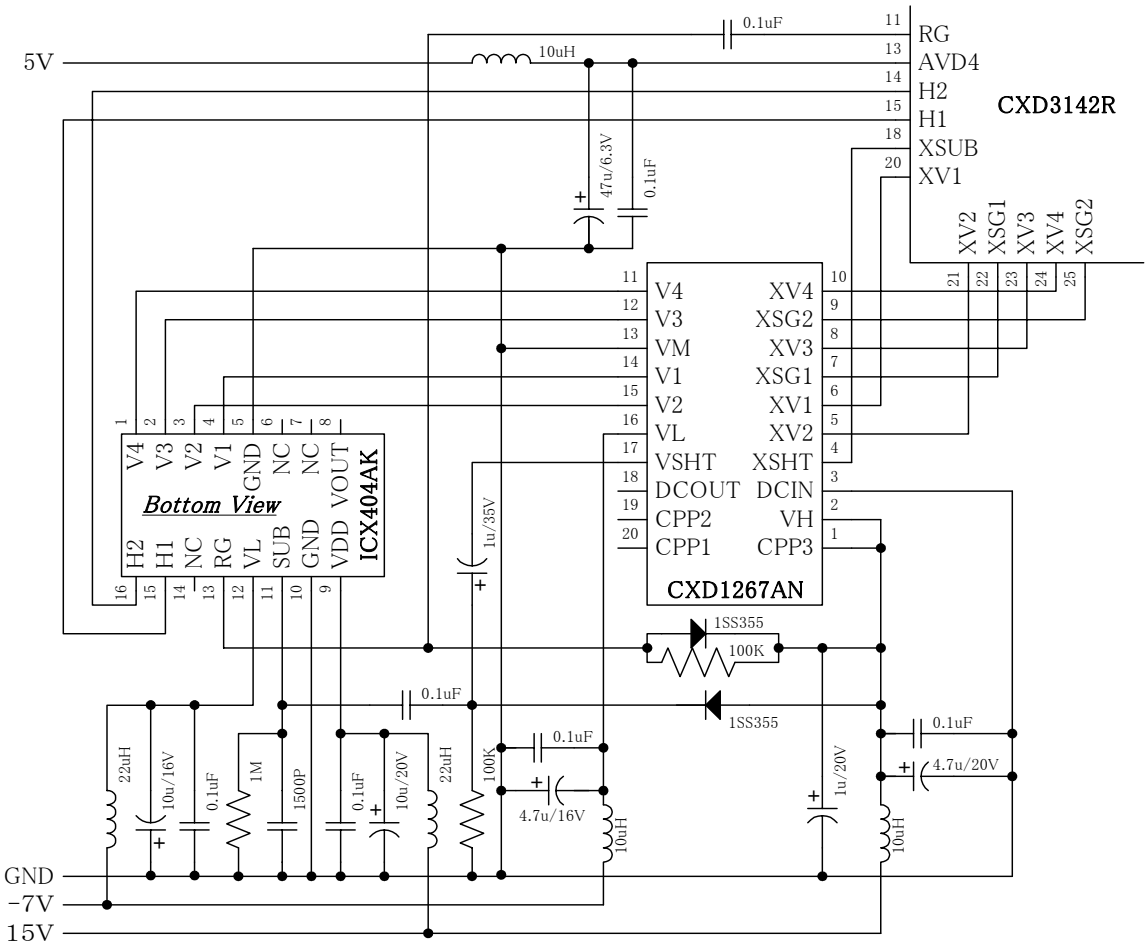


Fig. 4.2-3 CCD Drive Circuit Example 3

“Fig. 4.2-3 CCD Drive Circuit Example 3” shows the drive circuit configuration when using 1/3” CCD image sensors (ICX404/405AK). The Vsub voltage is adjustment-free and the RG voltage is adjustment-free and clamped high.

The drive circuit requires three types of supply voltages: 5 V, 15 V and –7 V.

Clamp the RG pulse high level to 15 V with the diode clamping circuit.

Vsub Voltage is clamped and generated inside the CCD, and the CXD1267AN VSHT (Pin 17) output is input to the CCD SUB pin via a capacitor.

The CXD1267AN DCOUT (Pin 18) should be left open and DCIN (Pin 3) should be connected to GND.

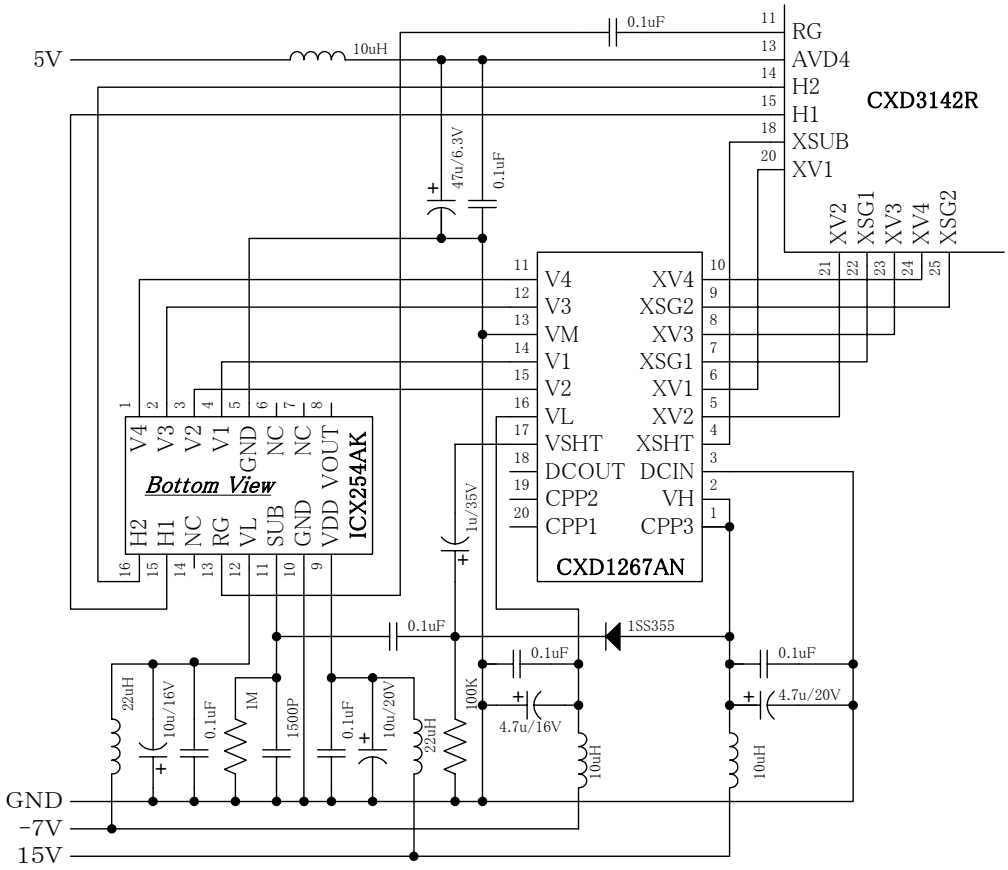


Fig. 4.2-4 CCD Drive Circuit Example 4

"Fig. 4.2-4 CCD Drive Circuit Example 4" shows the drive circuit configuration when using 1/3" CCD image sensors (ICX254/255AK). The Vsub and RG voltages are both adjustment-free.

The drive circuit requires three types of supply voltages: 5 V, 15 V and –7 V.

The RG pulse should be input to the CCD RG pin after cutting the DC component with a capacitor.

Vsub Voltage is clamped and generated inside the CCD, and the CXD1267AN VSHT (Pin 17) output is input to the CCD SUB pin via a capacitor.

The CXD1267AN DCOUT (Pin 48) should be left open and DCIN (Pin 1) should be connected to GND.

4.2.2. Frequency Response Changes

The subcarrier frequency differs for NTSC and PAL, making it necessary to change the characteristics of the LPF connected to the rear end of the CXD3142R IO (Pin 60) as well.

See “3.Application Circuits” for the recommended LPF characteristic for each CCD mode.

4.3. Parameter Changes

When changing the parameters such as when using a different CCD type, the values should be reset by serial communication after starting up the system or an external EEPROM should be connected and the various parameters should be written to the EEPROM.

The following parameters are changed together with the CCD type and NTSC/PAL settings. (See “Table. 4.2-1” for details.) When not connecting an external EEPROM, these parameters are automatically set internally according to the CXD3142R NTPAL (Pin 75) setting.

The spectral characteristics of the color filter differ according to the type of CCD image sensor. The SS-11RM initial settings are designed in consideration of the spectral characteristics of a 1/4” CCD image sensor. Therefore, resetting the parameters and writing this data to the EEPROM is recommended when using other types of CCD image sensors.

Table 4.3-1 TV System and Setting Parameters

Category		1	9	3
Byte		1	13	9
Bit		0	7	0 to 4
EEPROM address		01[h]	73[h]	23[h]
Parameter name		NTPAL	IDINV	BSTLV
TV system	NTSC	0	0	12[h]
	PAL	1	1	13[h]

Table 4.3-2 CCD Type and Recommended Primary Color Separation Matrix Parameters

Category			9			
Byte			16	17	18	19
Bit			0 to 7	0 to 7	0 to 7	0 to 7
EEPROM address			76[h]	77[h]	78[h]	79[h]
Parameter name			RMATY	RMATC	BMATY	BMATC
510H	1/4”	ICX206/207AK	2D[h]	00[h]	45[h]	BB[h]
		ICX226AK	21[h]	F9[h]	2C[h]	E0[h]
		ICX227AK	23[h]	05[h]	2C[h]	FC[h]
	1/3”	ICX404/405AK	2F[h]	14[h]	28[h]	DC[h]
		ICX254/255AK	2B[h]	10[h]	2F[h]	CF[h]
	1/6”	—	—	—	—	—

Table. 4.3-1 CCD Type and Linear Matrix Parameters (Reference value)

Category			3			
Byte			10	11	12	13
Bit			0 to 7	0 to 7	0 to 7	0 to 7
EEPROM address			24[h]	25[h]	26[h]	27[h]
Parameter name			RYGAIN	BYGAIN	RYHUE	BYHUE
Type 1/4	NTSC	ICX206AK	2F[h]	1C[h]	FF[h]	FE[h]
		ICX226AK				
	PAL	ICX207AK	18[h]	0E[h]	FF[h]	FE[h]
		ICX227AK				
Type 1/3	NTSC	ICX254AK	2F[h]	1C[h]	FE[h]	FE[h]
		ICX404AK				
	PAL	ICX255AK	18[h]	0E[h]	FF[h]	FE[h]
		ICX405AK				
Type 1/6	NTSC	—	—	—	—	—
	PAL	—	—	—	—	—

* Note that the above linear matrix parameters were just example of setting arrived at by focusing on the color reproductivity for flesh tone using a representative sample of each CCD type, and not by conforming to the target (田) displayed on the vectorscope.

* Note that the above linear matrix parameters should be handled as reference setting. In actual use, those must be respectively changed in accordance with the gain settings of the circuits and ICs connected to the rear end of the DSP and color reproductivity desired by customer's request.

5. Power Supply

5.1. Supply Voltage

The SS-11RM requires the following three types of power supplies as the system power supplies. The supply voltages in the ICX226AK are shown as reference.

Supply voltages when using the ICX226AK.

+3.3 V: Analog logic power supply for CXD3142R
Power supply for CXA2096N
Power supply for AK6420HF
Power supply for MB88347LPFV/M62367
Power supply for PST9127

+12.0 V: Power supply for CXD1267AN (V driver, shutter driver, Vsub generation circuit)
Power supply for CCD image sensor (ICX226AK)

–5.0 V: Power supply for CXD1267AN (V driver, shutter driver)
Protective transistor input voltage for CCD image sensor (ICX226AK)

* The supply voltages may change in some locations depending on the CCD image sensor. See the specifications for each CCD image sensor.

5.1.1. Supply Voltage Accuracy

The supply voltages differ according to the CCD type. Use power supplies within the following tolerance ranges.

Table. 5.1-1 SS-11RM Supply Voltage and Accuracy

	CCD type name	Supply Voltage (typ.)	Tolerance
Type 1/4	ICX206AK ICX207AK	+3.3 [V]	+/-0.3 [V]
		+15.0 [V]	+/-0.45 [V]
		-7.0 [V]	+0.5 [V] -1.0 [V]
	ICX226AK ICX227AK	+3.3 [V]	+/-0.3 [V]
		+12.0 [V]	+/-0.36 [V]
		-5.0 [V]	+/-0.5 [V]

	CCD type name	Supply Voltage (typ.)	Tolerance
Type 1/3	ICX404AK ICX405AK	+3.3 [V]	+/-0.3 [V]
		+5.0 [V]	+/-0.25 [V]
		+15.0 [V]	+/-0.45 [V]
		-7.0 [V]	+0.5 [V] -1.0 [V]
	ICX254AK ICX255AK	+3.3 [V]	+/-0.3 [V]
		+5.0 [V]	+/-0.25 [V]
		+15.0 [V]	+/-0.45 [V]
		-7.0 [V]	+0.5 [V] -1.0 [V]

5.1.2. Power Consumption

Examples of measured current consumption values in each device when driving Type 1/3 (ICX404AK) and Type 1/4 (ICX206AK, ICX226AK) CCD image sensors are shown in “Table. 5.1-2”, and examples of measured current consumption values for the overall Sony evaluation board are shown in “Table. 5.1-3”.

These values were measured using a Sony Semiconductor evaluation board, and should be used as reference values.

Table. 5.1-2 SS-11RM Current Consumption Measurements (when driving a CCD)

Unit: mA

	Item	Pin No.	Pin description	ICX206AK		ICX226AK		ICX404AK	
				Input voltage	Current consumption	Input voltage	Current consumption	Input voltage	Current consumption
CXD3142R	AVD1	2	A/D converter	3.3[V]	17.78	3.3[V]	17.7	3.3[V]	17.82
	AVD2	8	Sample-and-hold pulse	3.3[V]	3	3.3[V]	3	3.3[V]	3
	AVD4	13	Horizontal drive pulse	3.3[V]	12.81	3.3[V]	10.28	5.0[V]	17.15
	AVD5	59	D/A converter	3.3[V]	6.83	3.3[V]	6.85	3.3[V]	6.85
	AVD6	69	A/D converter during digital output	3.3[V]	0	3.3[V]	0	3.3[V]	0
	VDD1	19	Logic power supply	3.3[V]	1.26	3.3[V]	1.27	3.3[V]	1.27
	VDD2, 4	35, 74	Logic power supply	3.3[V]	21.1	3.3[V]	19.38	3.3[V]	19.64
	VDD3	44	Logic power supply	3.3[V]	21.8	3.3[V]	22.2	3.3[V]	22.3
CXA2096N	Vcc1, 2, 3	16, 23, 5	Logic power supply	3.3[V]	37.44	3.3[V]	41.33	3.3[V]	38.08
CXD1267AN	VH	2	Logic power supply	15[V]	1.53	12[V]	1.11	15[V]	1.55
	VL	6	Logic power supply	-7.0[V]	2.14	-5.0[V]	1.56	-7.0[V]	2.7
CCD	VDD	-	Circuit power supply	15[V]	3.34	12[V]	2.58	15[V]	2.61
	VL	-	Protective transistor bias	-7.0[V]	0	-5.0[V]	0	-7.0[V]	0

Table. 5.1-3 Example of Current Consumption Measurements in an Evaluation Board (SS-140B) (when driving a CCD)

Unit: mA

Evaluation board	Item	ICX206AK		ICX226AK		ICX404AK	
		Input voltage	Current consumption	Input voltage	Current consumption	Input voltage	Current consumption
SS-140B	VH	15[V]	17.78	12[V]	17.7	15[V]	17.82
	5.0V	5.0[V]	32.6	5.0[V]	33.2	5.0[V]	45.8
	3.3V	3.3[V]	106.4	3.3[V]	108	3.3[V]	108.2
	VL	-7.0[V]	2.15	-5.0[V]	1.58	-7.0[V]	2.73

5.1.3. Power-on Sequence

(Example: when using the ICX226/227AK)

When turning on the power, be sure to **turn on the VL (–5.0 V) power supply last**. The **+3.3 V and VH (+12.0 V)** power supplies may be turned on in any order.

When **turning off the power, the –5.0 V, +3.3 V and +12.0 V** power supplies may be turned off in any order.

* Note that these supply voltages change for different CCD image sensors.

6. Standard Signal Levels

6.1. SS-11RM Level Diagram

Signal Standard Level Diagram

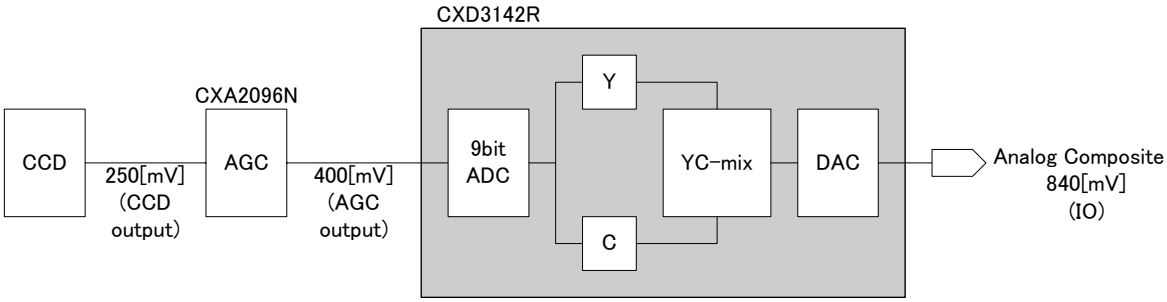


Fig. 6.1-1 SS-11RM System Configuration

The SS-11RM performs AE and AWB processing using the microcontroller built into the CXD3142R. In particular, AE processing automatically applies feedback to converge the luminance signal level to the target value from the CCD output to the AGC output (A/D converter input) = DSP input.

As target values for the SS-11RM, the following signal level settings are specified as the standard levels. The CXD3142R signal lines are also designed with the picture quality parameters and dynamic range design based on these standard levels.

Operation has been confirmed for the recommended values and signal levels noted here using a Sony evaluation board, but note that this is not a guarantee of performance including for board layout changes, parts selection and temperature characteristics.

CCD output: 250 mV (Y level)

The saturation signal level differs for each type of CCD image sensor. The color camera picture quality design generally ensures a dynamic range of two to three times the standard level.

The SS-11RM is mainly designed for CCD image sensors with a saturation signal level of 700 to 800 mV, and has a standard CCD output (Y level) level of 250 mV.

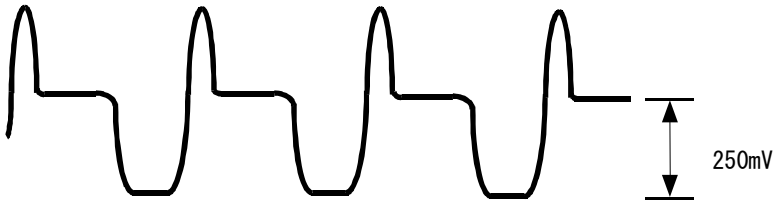


Fig. 6.1-2 CCD Output Signal

AGC output = A/D converter input: 400 mV (Y level)

The CXA2096N generates two voltages (VRT = 2.35 V, VRB = 1.35 V) as reference voltages for the rear-end A/D converter. These voltages are input to the VRT and VRB pins of the 9-bit A/D built into the CXD3142R, and the 1 Vp-p dynamic range is set to the A/D converter input.

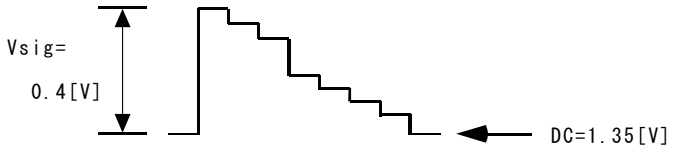


Fig. 6.1-3 A/D converter input sinnal

IO output: 840 mV (Y level)

When the above A/D input is the standard input of 400 mV under the standard parameter conditions noted below, the luminance signal D/A output IO is 840 mV. (IO termination resistance 220 Ω)

CAT3-Byte 7 YGAIN = 5Ah

CAT6-Byte 5 DAVRF = 59h

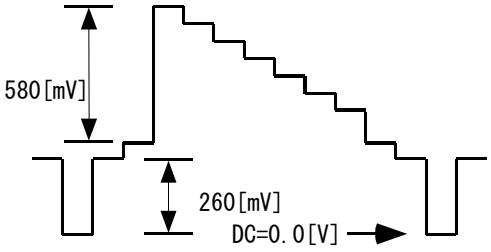


Fig. 6.1-4 A/D Converter Input Signal

When attenuated or amplified by the circuit including the rear-end LPF and video driver and sync is added, the level is 1 Vp-p.

The chroma signal differs according to the spectral characteristics of the CCD image sensor and the imaged subject, and is therefore not discussed here.

6.2. Built-in A/D Converter

The signal input to the built-in A/D converter is the signal that has been CDS and AGC processed by the camera head amplifier IC (CXA2096N).

The dynamic range of the signal output from the CXA2096N is 1 V from VRB (1.35 V) to VRT (2.35 V), and the input signal is converted in gradations from 0 to 511 “Fig. 6.2-1 Example of A/D Conversion”. However, the black level is set several tens of mV higher than VRB by the control voltage of the AGC amplifier (CXA2096N) offset pin. The CXA2096N offset pin is automatically controlled through an electronic attenuator by the CPU inside the DSP.

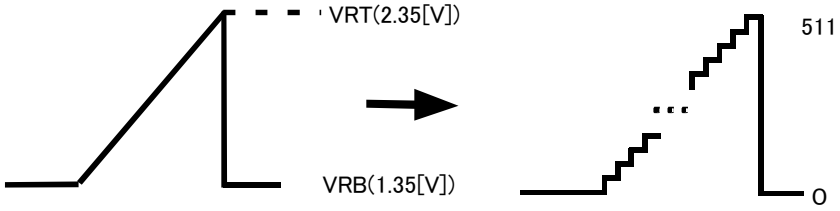


Fig. 6.2-1 Example of A/D Conversion

6.3. Built-in D/A Converter

The relation between the 9-bit (0 to 511) A/D converted signal and the luminance signal input to the D/A converter is shown below. The signal level is 240[d] (matches with sync level = 40 IRE) with respect to black (0[d]) input, 564[d] (94 IRE) with respect to 204[d] input, and 783[d] (130 IRE) with respect to 511[d] input.

The values in “Fig. 6.3-1 Y D/A Output” are the theoretical values for the CXD3142R design specifications, and do not include signal level error due to the variance of peripheral circuits, etc.

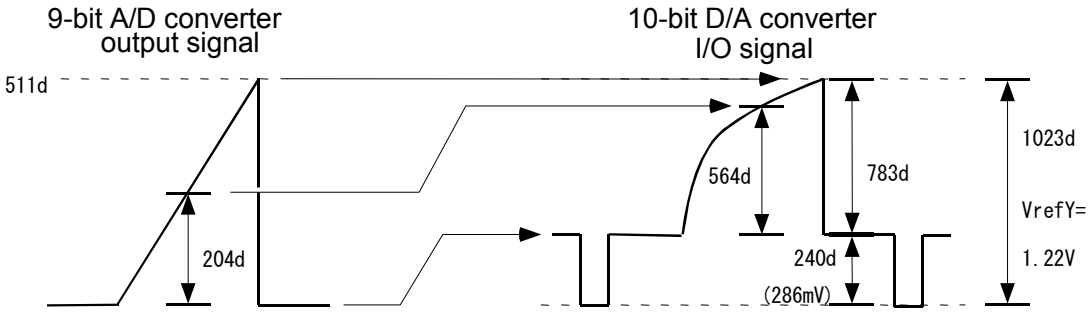


Fig. 6.3-1 Y D/A Output

7. Communication Specifications

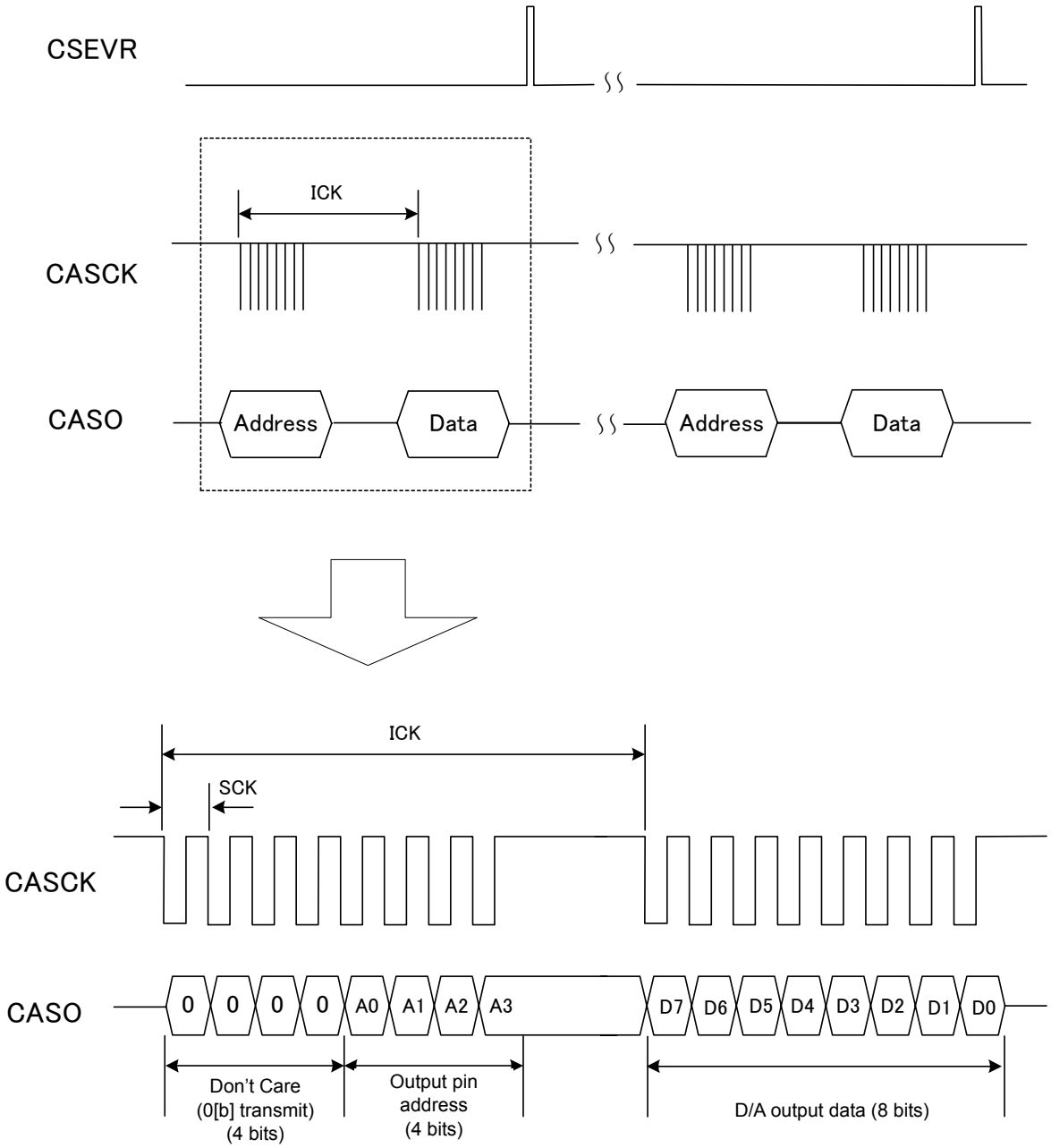
7.1. Communication with Peripheral ICs

The SS-11RM incorporates two types of communication functions: clock synchronous 3-wire serial communication for transmitting and receiving parameters, and a clock synchronous 3-wire serial bus for communication with peripheral ICs (EVR: MB88347L/M62367, EEPROM: AK6420).
This section describes the specifications for communication with peripheral ICs.

7.1.1. EVR (MB88347L/M62367) Communication

The EVR (MB88347L/M62367) internally latches the bit data received by the 12-bit shift register by setting the latch trigger (CSEVR) high. The EVR then performs D/A conversion based on this data and outputs the results to an optional output port.

* See “Fig. 7.1-1 EVR (MB88347L/M62367) Communication Format”.
  However, the address (4 bit) is LSB first, and the data is MSB first.



Serial Clock (SCK) = 0.839[us]@19.06993[MHz] (NTSC)
0.844[us]@18.93975[MHz] (PAL)

Interval Clock (ICK) = 13.424[us]@19.06993[MHz] (NTSC)
13.516[us]@18.93975[MHz] (PAL)

Fig. 7.1-1 EVR (MB88347L/M62367) Communication Format

7.1.2. EEPROM (AK6420) Communication

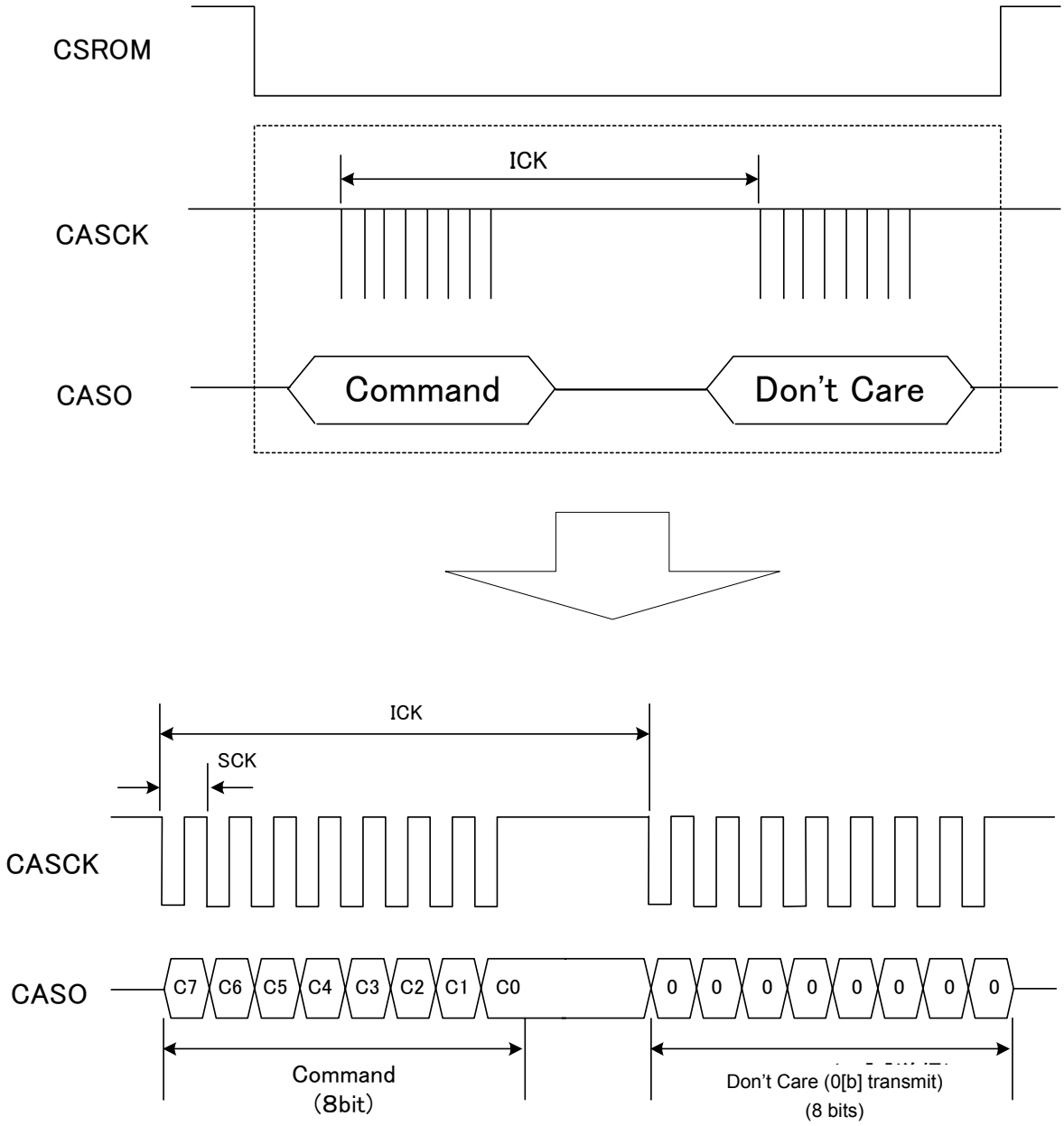
The EEPROM (AK6420) recognizes that the communication data on the bus is for itself (EEPROM) when chip select (CSROM) is low.

There are three types of communication format as follows.

1. Write enable command format
   * See “Fig. 7.1-2 EEPROM Write Enable Command Format”.

2. Write command format
   * See “Fig. 7.1-3 EEPROM Write Command Outline”.
     See “Fig. 7.1-5 EEPROM Write Command Format”.

3. Read command format
   * See “Fig. 7.1-4 EEPROM Read Command Outline”.
     See “Fig. 7.1-6 EEPROM Read Command Format”.



Serial Clock (SCK) = 0.839[us]@19.06993[MHz] (NTSC)
0.844[us]@18.93975[MHz] (PAL)

Interval Clock (ICK) = 13.424[us]@19.06993[MHz] (NTSC)
13.516[us]@18.93975[MHz] (PAL)

Fig. 7.1-2 EEPROM Write Enable Command Format

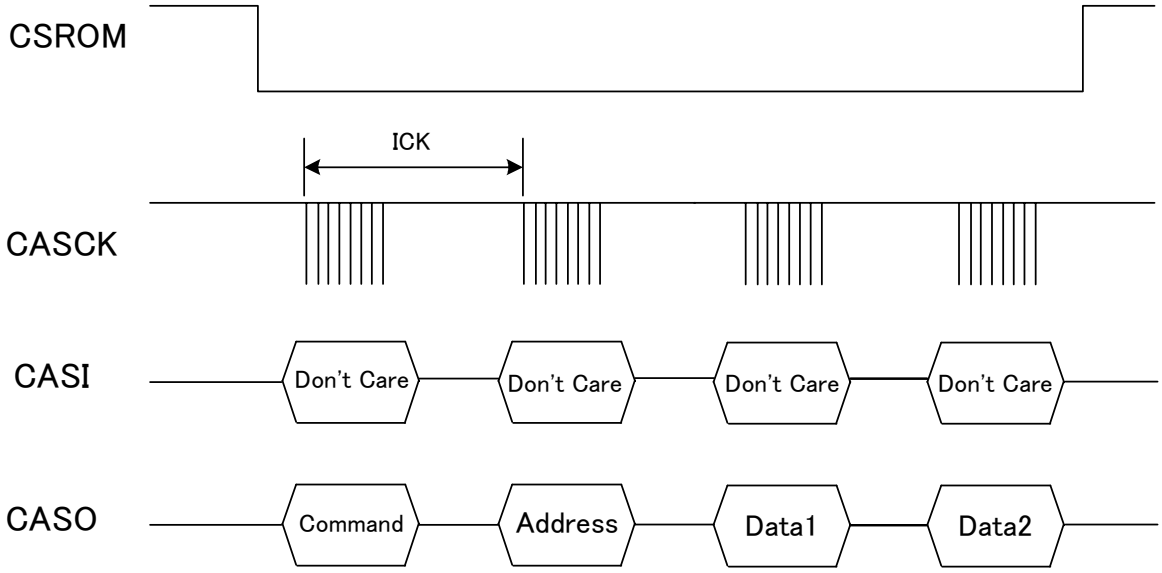


Fig. 7.1-3 EEPROM Write Command Outline

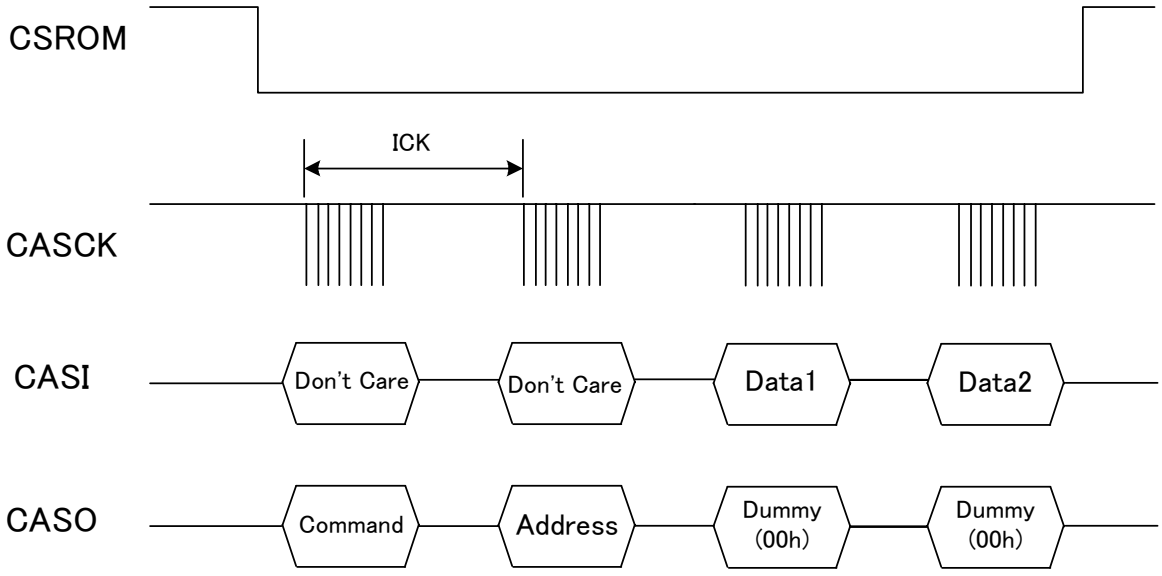
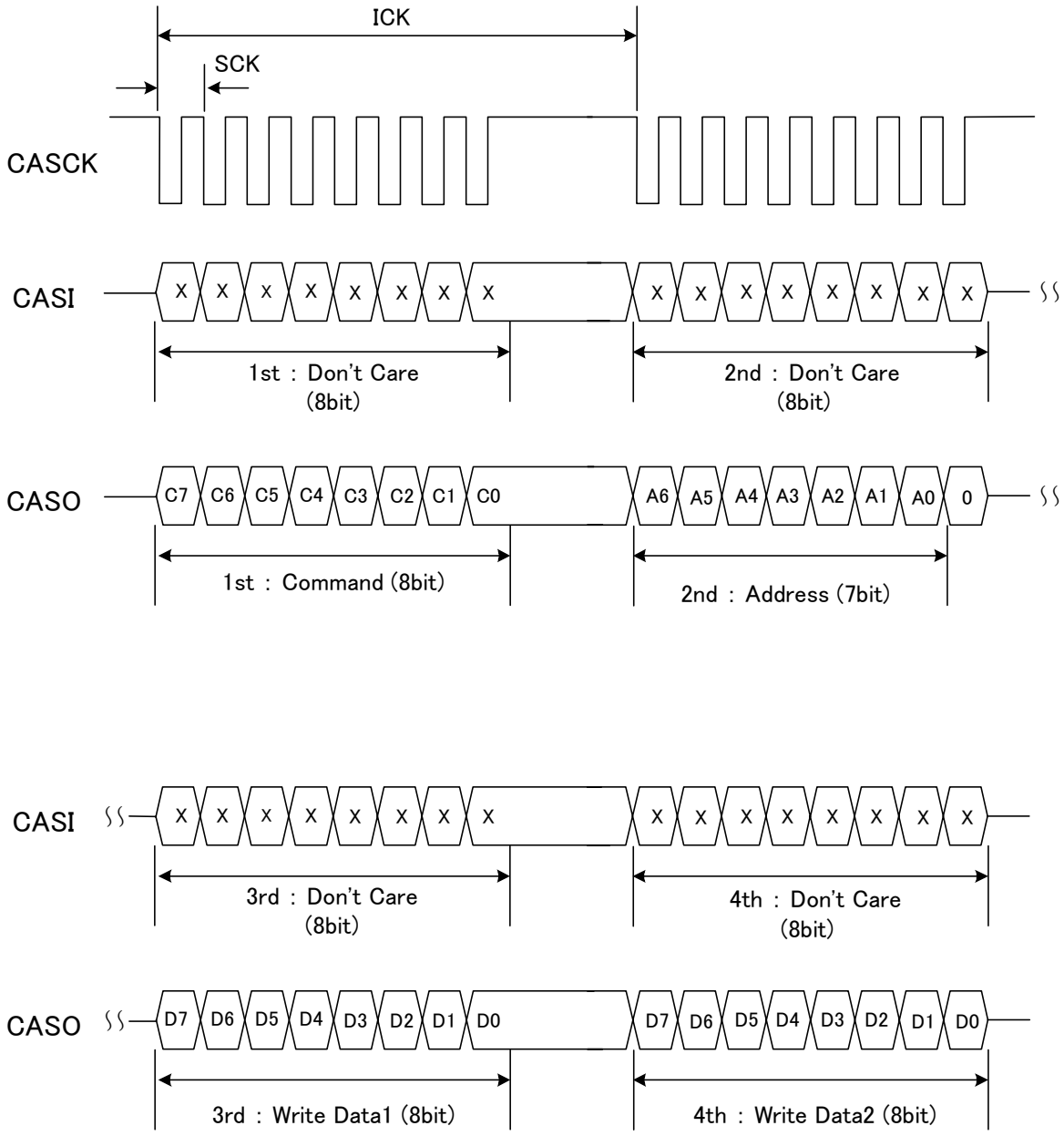


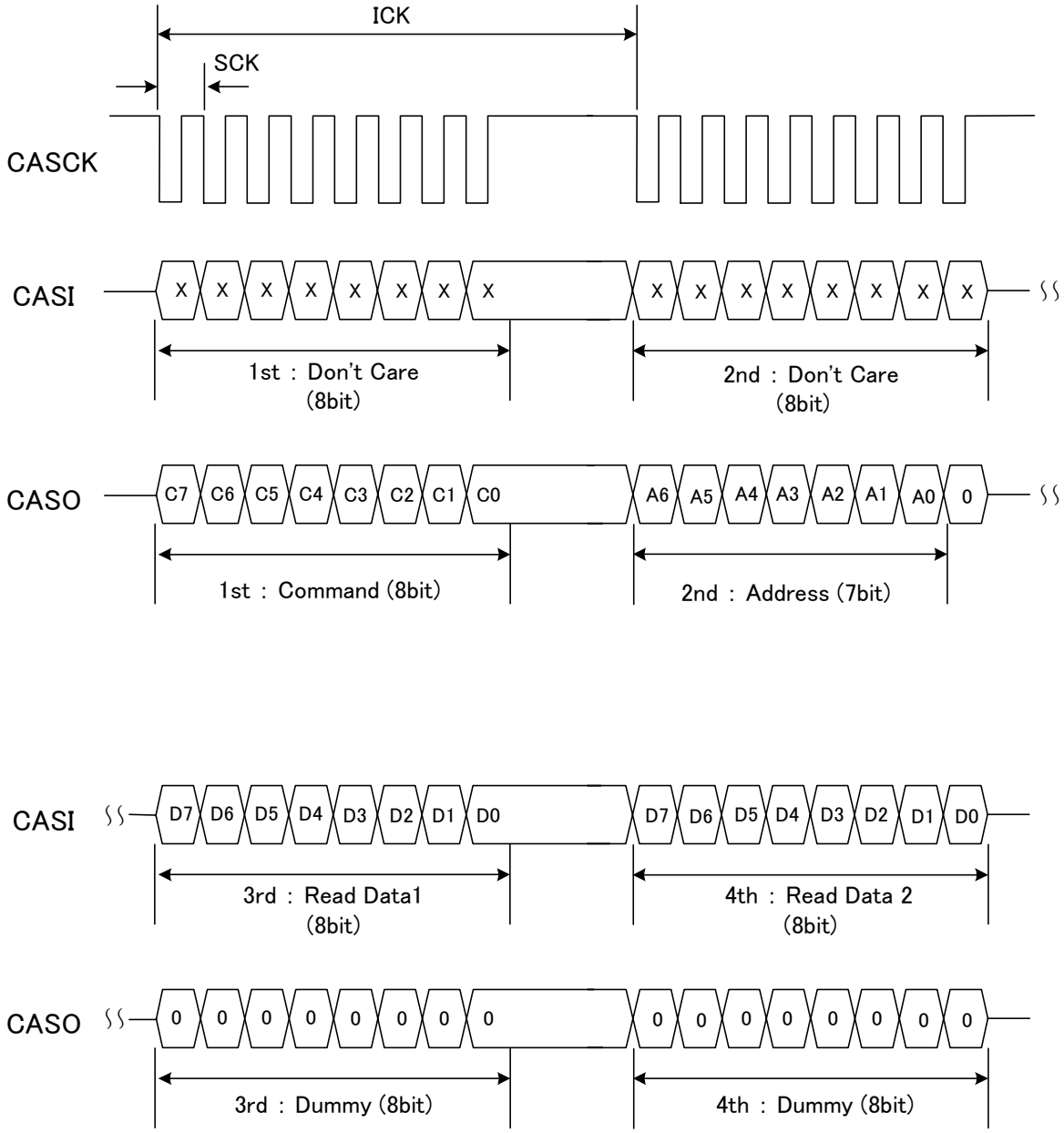
Fig. 7.1-4 EEPROM Read Command Outline



Serial Clock (SCK) = 0.839[us]@19.06993[MHz] (NTSC)
0.844[us]@18.93975[MHz] (PAL)

Interval Clock (ICK) = 13.424[us]@19.06993[MHz] (NTSC)
13.516[us]@18.93975[MHz] (PAL)

Fig. 7.1-5 EEPROM Write Command Format



Serial Clock (SCK) = 0.839[us]@19.06993[MHz] (NTSC)
0.844[us]@18.93975[MHz] (PAL)

Interval Clock (ICK) = 13.424[us]@19.06993[MHz] (NTSC)
13.516[us]@18.93975[MHz] (PAL)

Fig. 7.1-6 EEPROM Read Command Format

7.2. Parameter Communication

This section describes clock synchronous 3-wire serial communication for transmitting and receiving parameters.

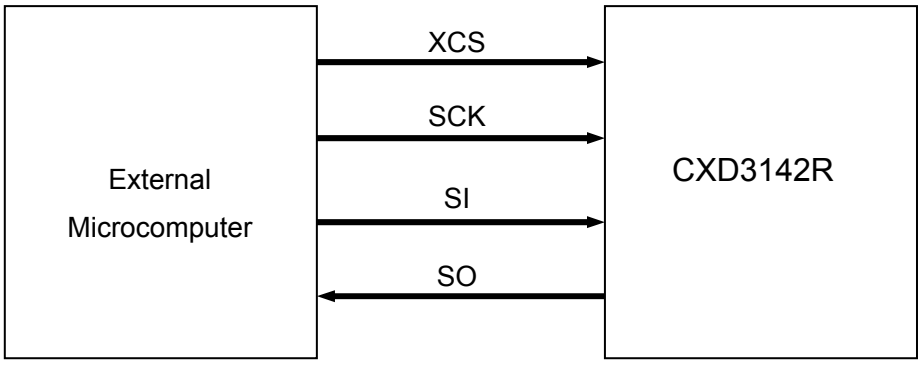


Fig. 7.2-1 Parameter Communication Input/Output

<Input/output signals>

XCS: Chip select

SCK: Communication clock

SI: Serial input data

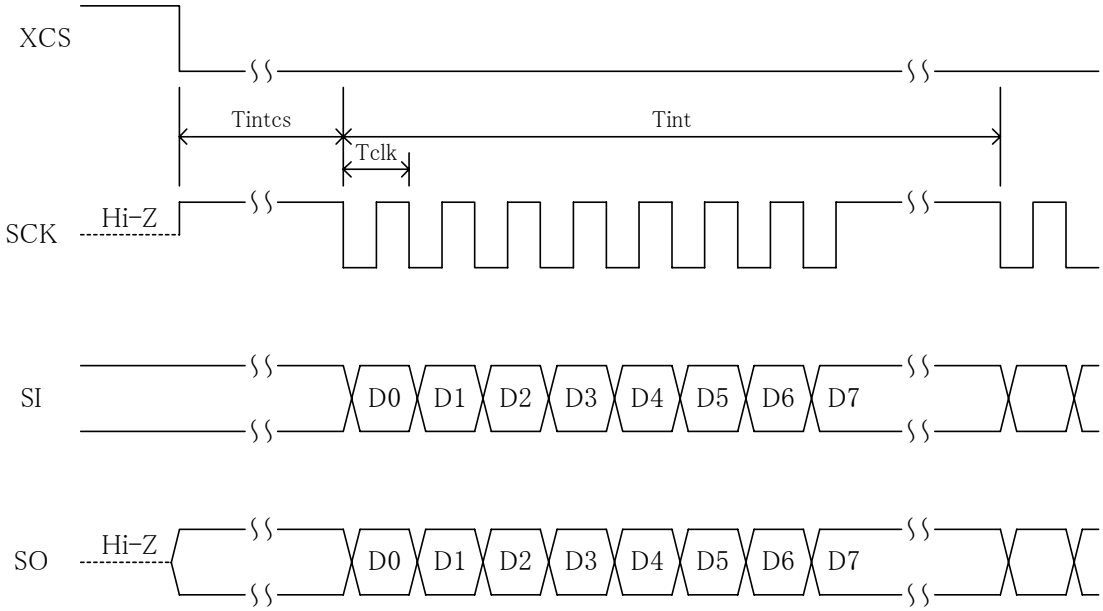
SO: Serial output data

7.2.1. Chip Select and Communication Clock

The CXD3142R starts communication by inputting the communication clock from an external source after detecting the falling edge of the XCS pin. The clock wait status is established until communication of 16 bytes is completed, so even when there are less than 16 bytes of valid data, always input the clock for all 16 bytes as dummy data. Also, note that inputting the clock for more than 16 bytes results in an overrun error.

To perform communication again after finishing communication of 16 bytes, always set XCS high and then low again, and oscillate the clock.

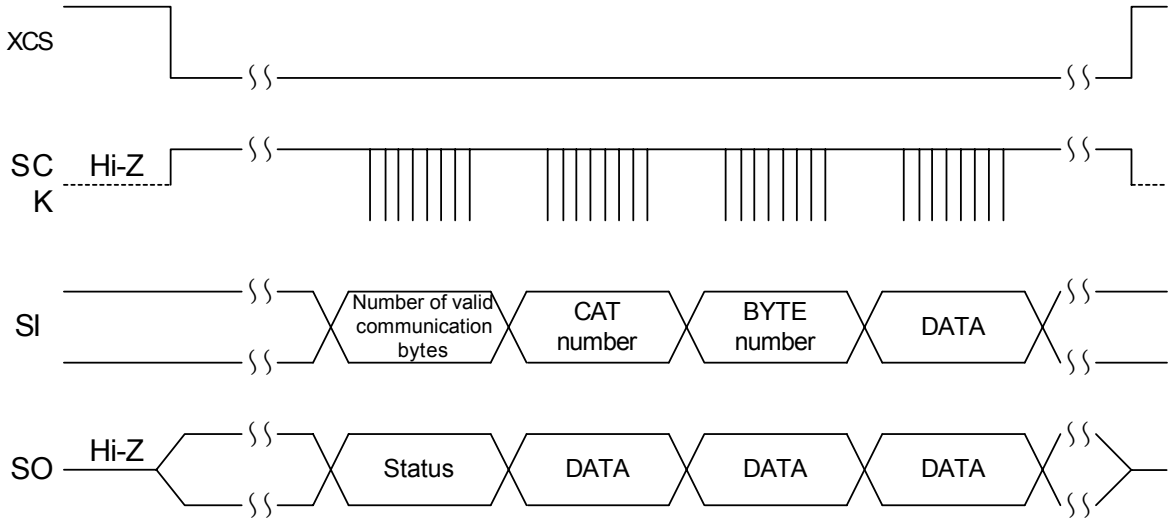
The clock and data serial timing are shown on the following page.



Tclk: Serial clock period
700 [kHz] + - 200 [kHz] (Approximately 1.1 [us] to 2.0 [us])
Tint: Interval clock period (Min. 22 [us])
Tintcs: Tint to 2 Tint

Fig. 7.2-2 Serial Shift Timing

7.2.2. Communication Format



* Always 16-byte communication

Fig. 7.2-3 Parameter Communication Format

The status code returns the number of valid communication bytes (1[h] to F[h]) when the preceding received data is valid, or an error code (upper 4 bits = F[h]) when the data is an error.

Error code types

F0h: Total number of valid communication bytes error

F1h: CAT number error

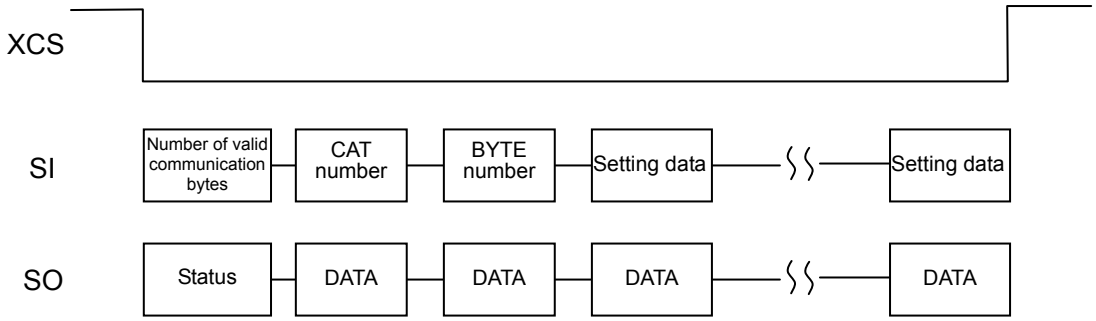
F2h: BYTE number error

F3h: Overrun error

F4h: Other error

<CAT1 to CAT7 and CAT9 communication>

Serial In



CAT1 to CAT7 and CAT9 are controlled by the external microcomputer. The clock wait status is established by the falling edge of XCS, and data communication starts synchronized with the external clock input.

The data output from the CXD3142R output pin SO is valid only when transmitting data corresponding to CAT8, so other data is processed as invalid data.

The status data indicates the status of the immediately preceding receive data.

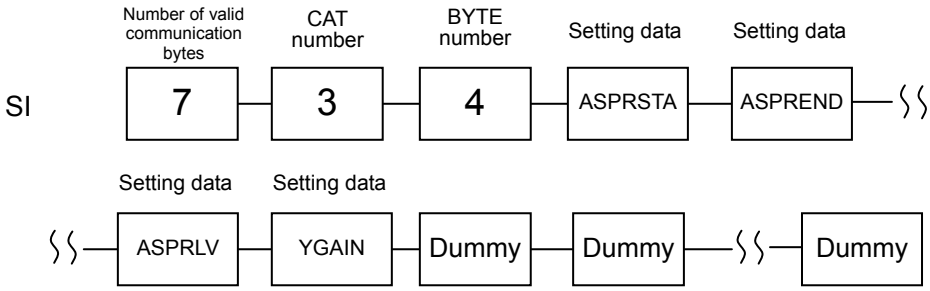
– The first byte sets the number of valid bytes within the total 16 bytes communicated while the XCS pin is low.

  Number of valid communication bytes = 3 bytes (Valid bytes + CAT number + BYTE number) + Number of valid data.

  Therefore, the number of valid communication bytes range is from 4 to 16.

Example: When transmitting the 4 bytes from CAT3 BYTE4 ASPRSTA to YGAIN

Transmit Number of valid communication bytes = 7, CAT number = 3, BYTE number = 4, and then the ASPRSTA, ASPREND, ASPRLV and YGAIN setting values.

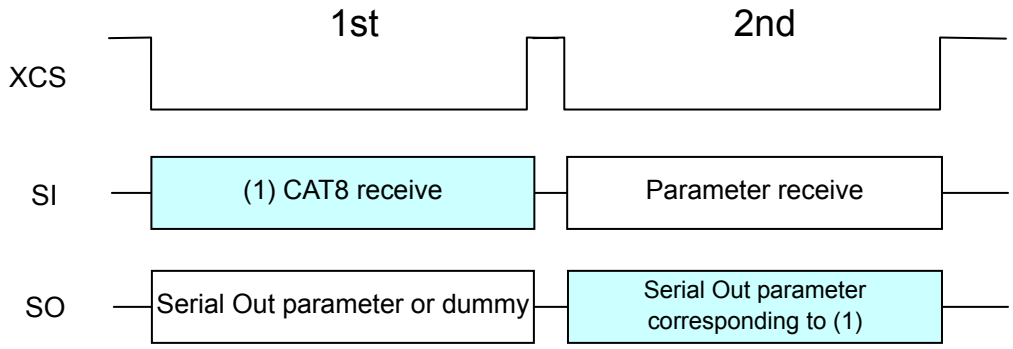


* Total 16-byte receive

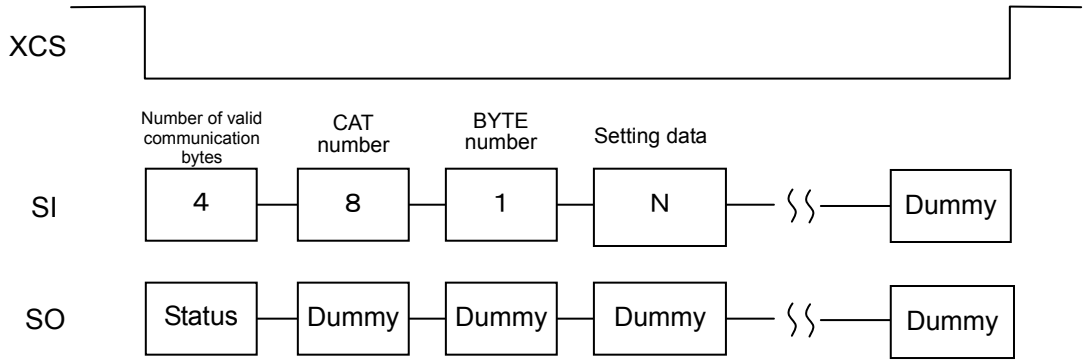
<CAT8 communication>

CAT8 communication consists of receiving CAT8 and then transmitting the optional serial parameter contents with the next communication.

Overview of CAT8 communication



Serial In (CAT8 parameter receive)

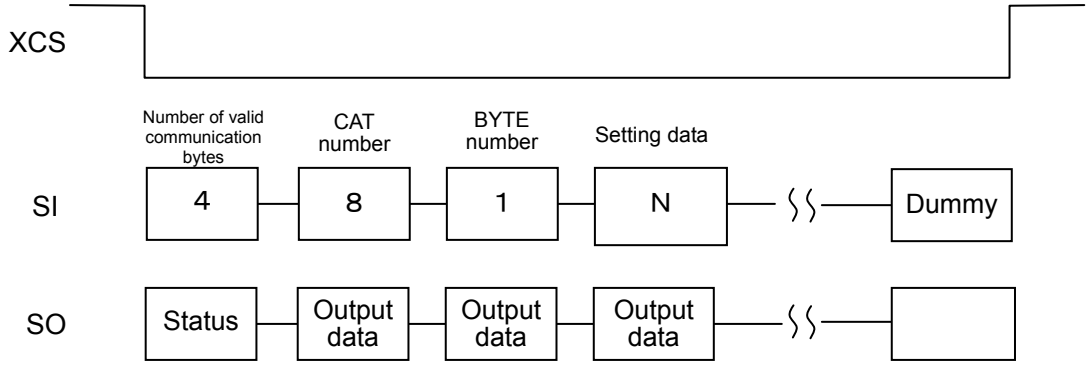


* N = 5 to 9: Serial Out parameter transmit start byte position

byte 5: AWOUT1
byte 6: AWOUT2
byte 7: AWOUT3
byte 8: AWOUT4
byte 9: E2RDATA

BYTE number = 1: Designates SOBYTE (CAT8)

Serial Out (Serial Out parameter transmit)



CAT1 to CAT7 and CAT9 are controlled by the external microcomputer. The clock wait status is established by the falling edge of XCS, and communication starts synchronized with the external clock input.

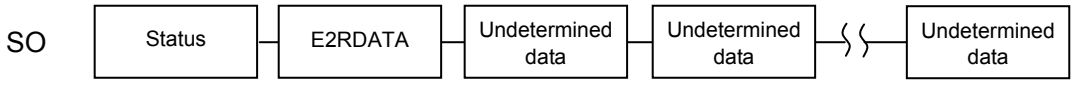
When CAT8 is received, the CXD3142R sets the output data and then outputs the data to SO with the next communication. When performing communication for the second time, set XCS high and then low again.

At this time, the data input to SI can be the same data as the preceding communication.

Note: The transmit data is always 16 bytes (output data 15 bytes), but the valid Serial Out parameters are 5 bytes, so the maximum valid output data is 5 bytes.
An error may not necessarily result when data other than 5 to 9 is set in the transmit start byte position. However, note that in this case the output data is undetermined.

The output data is transmitted from the Serial Out parameter start byte position set in CAT8 (SOUT) BYTE1 SOBYTE.

Example: When CAT8 BYTE1 SOBYTE is set to 9
The Serial Out parameter BYTE9 E2RDATA is output.



* Total 16-byte transmit

7.2.3. About the microcomputer for the communication

It is necessary to transfer between RS232C and 3 wires to communicate by using PC with SS-11RM. The microcomputer which is on our evaluation board does the above communication transfer.

And, even when the version of the control software changes, it doesn't need to change a micro computer for the communication.

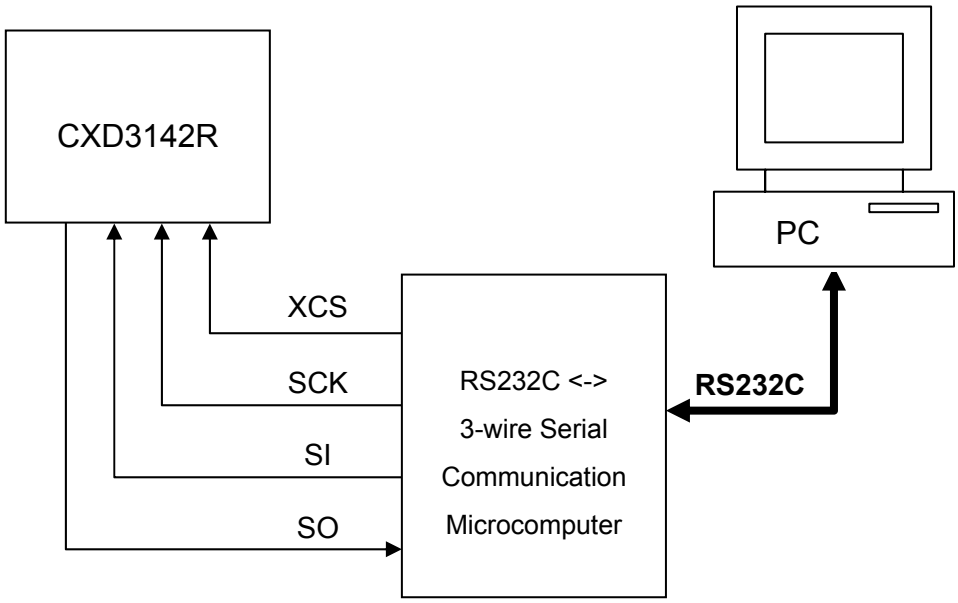


Fig. 7.2-4 Example Parameter Communication Settings when Using a PC

8. Description of Operation of Each Block

8.1. Port Driver Setting Method

This section describes CAT2-Bytes 8 to 23 PnCB and PnM (n: 0 to 7).

"n" indicates the port number (external pin).

<Cat/Byte> PnCB (n: 0 to 7)

D7	D6	D5	D4	D3	D2	D1	D0
CAT			BYTE				

CAT: Category number [h] to be set

BYTE: Byte number [h] to be set

<Mode> PnM (n: 0 to 7)

D7	D6	D5	D4	D3	D2	D1	D0
0	ADJ		PATTERN				

D7 = Fixed to 0

ADJ: 00 = ×0.0
01 = ×0.5
10 = ×1.5
11 = ×2.0

ADJ: Coefficient to be applied to that parameter

PATTERN: 0h = bit 0
1 = bit 1
2 = bit 2
3 = bit 3
4 = bit 4
5 = bit 5
6 = bit 6
7 = bit 7
8 = bit 1 to bit 0 (2 continuous bits)
9 = bit 3 to bit 2 (2 continuous bits)
A = bit 5 to bit 4 (2 continuous bits)
B = bit 7 to bit 6 (2 continuous bits)
C = bit 2 to bit 0 (3 continuous bits)
D = bit 6 to bit 4 (3 continuous bits)
E = bit 3 to bit 0 (4 continuous bits)

PATTERN: Bit string to be set

F = bit 7 to bit 4 (4 continuous bits)

10 = bit 7 to bit 0 (8 continuous bits)

See the parameter table in the specifications for a specific setting example.

The initial values of PnCB and PnM are the pins set by the default.

Port Driver Setting Procedure Examples

Example 1) Assigning the 1-bit data area ports

INT mode and LL mode are switched using switch (P0).

1. Set ESMODE (CAT1-Byte 6-bit 0) to 0.
2. Set the P0 pin (Pin 0) to off (low).
3. Set CPUCMD (CAT2-Byte 1) to 0.
4. Set CPUDIP (CAT2-Byte 4-bit 4) to 0.
   -> The control method changes from serial communication to DIP switch control.
5. Set P0CB (CAT2-Byte 8) to 26[h].
   -> Designate the ESMODE (CAT1-Byte 6-bit 0) category and byte position.
6. Set P0M (CAT2-Byte 9) to 0. (Input port setting and pattern setting)
7. Set CPUEXT (CAT2-Byte 4-bit 0) to 1.
8. Set CPUADRS (CAT2-Byte 2) to 2.
9. Set CPUCMD (CAT2-Byte 1) to 1.
10. Set CPUCMD (CAT2-Byte 1) to 0.
11. Write finishes after 4 to 5 seconds.
    When write finishes, return CPUEXT and CPUADRS to the original values.
    -> Data write to EEPROM processing
12. Turn the power off and then on again to reboot the system.
    -> When the system reboots, the port assignment processing is performed according to the EEPROM data.

When switch (P0) is OFF, the mode switches to INT mode; when ON, the mode switches to LL mode.

Example 2) Assigning the 8-bit data area ports

80 IRE (AEUSR = 4 value) and 100 IRE (AEUSR = 8 value) are switched using switch (P7).

1. Set AEREF (CAT2-Byte 6-bit 3) to 1.
   -> AEUSR data valid mode
2. Set AEUSR (CAT4-Byte 7) to 4.
   -> 80 IRE
3. Set the P7 pin (Pin 52) to off (low).
4. Set CPUCMD (CAT2-Byte 1) to 0.
5. Set CPUDIP (CAT2-Byte 4-bit 4) to 0.
   -> The control method changes from serial communication to DIP switch control.
6. Set P7CB (CAT2-Byte 22) to 87[h].
   -> This specifies the AEUSR (CAT4-Byte 7) category and byte position.
7. Set P7M (CAT2-Byte 9) to 70[h].
   -> Coefficient: x2, valid bits: 8 bits
8. Set CPUEXT (CAT2-Byte 4-bit 0) to 1.
9. Set CPUADRS (CAT2-Byte 2) to 2.
10. Set CPUCMD (CAT2-Byte 1) to 1.
11. Set CPUCMD (CAT2-Byte 1) to 0.
12. Write finishes after 4 to 5 seconds.
    When write finishes, return CPUEXT and CPUADRS to the original values.
    -> Data write to EEPROM processing
13. Turn the power off and then on again to reboot the system.
    -> When the system reboots, the port assignment processing is performed according to the EEPROM data.

When switch (P7) is OFF, the value switches to approximately 80 IRE (AEUSR = 4 value); when ON, the value switches to approximately 100 IRE (AEUSR = 8 value).

8.2. Sync Signal Output Setting Method

The tables below describe the parameters related to output switching for the sync signal output pins S0 (CXD3142R Pin 70), S1 (CXD3142R Pin 71) and S2 (CXD3142R Pin 72).

Note that when ESMODE (CAT1-Byte 6-bit 0) = 1 (External sync), the S1 pin functions as the external VD signal input pin (VRI IN).

Table. 8.2-1 SPINSW

SPINSW	Sx PIN SWitch
Parameter category	CAT1 SYSCON, byte 5, bit 7 (1 bit)
Outline	Selects S0, S1 and S2 pin active ON/OFF.
Setting range	0(b) to 1(b)
Initial value	0(b): S0, S1 and S2 pin active ON
Description	This selects active ON/OFF for each pin according to the following settings. 0(b): S0, S1 and S2 pins active, 1(b): Hi-Z
Note	

Table. 8.2-2 S0SEL

S0SEL	S0 pin SELect
Parameter category	CAT1 SYSCON, byte 7, bits 2 to 0 (3 bits)
Outline	Selects the S0 pin output signal.
Setting range	0[h] to 7[h]
Initial value	0[h]: FLD signal output
Description	Each signal is output according to the following settings. 0[h]: FLD, 1[h]: SYNC, 2[h]: BF, 3[h]: DISP, 4[h]: VD, 5[h]: HD, 6[h]: CBLK, 7[h]: DBLK The VD signal is shift –VD when SSHIFT = 1.
Note	When HD is selected, set SSHIFT to 0.

Table. 8.2-3 SSHIFT

SSHIFT	Sync SHIFT
Parameter category	CAT1 SYSCON, byte 7, bit 3 (1 bit)
Outline	Selects normal/shift signal output for S0, S1 and S2.
Setting range	0(b) to 1(b)
Initial value	0(b): Normal VD signal output
Description	0(b): Normal VD, 1(b) shift VD output
Note	

Table. 8.2-4 S1SEL

S1SEL	S1 pin SELect
Parameter category	CAT1 SYSCON, byte 7, bits 7 to 6 (2 bits)
Outline	Selects the S1 pin output signal. (Input port during external sync)
Setting range	0[h] to 3[h]
Initial value	0[h]: Normal HD/VD output
Description	Each signal is output according to the following settings. 0[h]: VD, 1[h]: FLD, 2[h]: HD, 3[h]: DISP The VD signal is shift –VD when SSHIFT = 1.
Note	When ESMODE = 01[h]: External sync mode, the S1 pin forcibly becomes the external VD signal input port. When HD is selected, set SSHIFT to 0.

Table. 8.2-5 S2SEL

S2SEL	S2 pin SELect
Parameter category	CAT1 SYSCON, byte 7, bits 7 to 6 (2 bits)
Outline	Selects the S2 pin output signal.
Setting range	0[h] to 3[h]
Initial value	0[h]: Normal HD/VD output
Description	Each signal is output according to the following settings. 0[h]: HD, 1[h]: FLD, 2[h]: VD, 3[h]: DISP The VD signal is shift –VD when SSHIFT = 1.
Note	When HD is selected, set SSHIFT to 0.

8.3. Picture Quality Adjustment

8.3.1. Aperture Correction Adjustment

Aperture correction processing performed by the SS-11RM includes H aperture correction processing, V aperture correction processing, and VH aperture correction processing which adds V and H aperture correction processing after GAMMA.

Table 8.3-1 Aperture Correction Related Parameters

CAT	Byte	bit	Parameter Name	Description	Default
3 PICT	1	0 to 1	HAPGL	Sets the horizontal aperture correction low frequency (about 2MHz) gain. 0:x0 1:x1 2:x2 3:x4	3
		2 to 3	HAPGH	Sets the horizontal aperture correction high frequency (about 3MHz) gain. 0:x0 1:x0.5 2:x1 3:x2	1
	2	0 to 3	VAPG	Sets the V aperture correction gain. The gain be set in 8 steps(0 to 7) from x0 to x2	A[h]
		4 to 6	VAPSL	Applies slice to V aperture correction. 0:slice level 0 -> 7:slice level max	2
	3	0 to 3	VHAPG	Sets the gain after adding V and H aperture correction. 0: x0 -> 15: x4	6
		4 to 7	VHAPSL	Applies slice after adding V and H aperture correction. 0: slice level 0 -> 15: slice level max	4

The procedure for adjusting the aperture correction is described below.

1. Set **CPUEXT** (CAT2-Byte 4-bit 0) to "1".
   Since the internal CPU overwrites the aperture correction gain, it is necessary to stop operations in order to make this adjustment.
2. Set the suppress start point and end point as follows.
   ASPRSTA (CAT3-Byte 4) = A0[h]
   ASPREND (CAT3-Byte 5) = D0[h]
3. Adjust **HAPGL** (CAT3-Byte 1-bits 0 and 1), **HAPGH** (CAT3-Byte 1-bits 2 and 3), **VAPG** (CAT3-Byte 2-bits 0 to 3), and **VHAPG** (CAT3-Byte 4-bits 0 to 3).
4. With CPUEXT = 1, write to the EEPROM.
   CPUADRS (CAT2-Byte 2) = 2
   CPUCMD (CAT2-Byte 1) = 0 -> 1 -> 0
5. The new EEPROM values are reflected when the power is turned on.

8.3.2. Y Suppress

Y suppress means the function that suppresses the signal level of high luminance sections of the screen in the Y gain immediately before D/A. This includes the two serial parameters YSPRLV (CAT3-Byte 18-bits 0 and 1) for setting the suppress level and YSPRTH (CAT3-Byte 18-bits 2 and 3) for setting the suppress threshold value.

Actually, the signal to be input to the Y gain multiplier is constantly monitored and if this value is greater than the setting value for YSPRTH, Y gain value is multiplied by 1, 1/2, 1/4, or 0 according to the setting value for YSPRLV. See “Fig. 8.3-1 Y Suppress Basic Diagram” for a basic diagram and “Table 8.3-2 Setting Parameters for Y-Suppress” for the parameters that can be set.

Note that Y suppress and Y gain function operate independently. Also note that since only the luminance signal level is suppressed, there is no effect on how chroma color is applied.

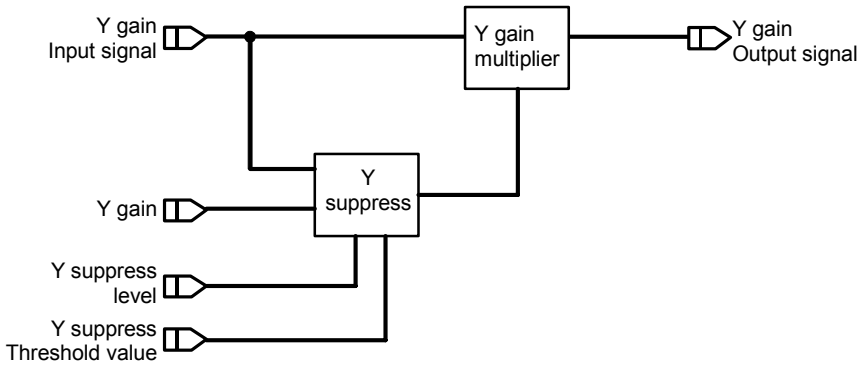


Fig. 8.3-1 Y Suppress Basic Diagram

8.3.3. Y-GAIN

Table 8.3-2 Setting Parameters for Y-Suppress

CAT	Byte	bit	Parameter name	Description
3 PICT	18	0 to 1	YSPRLV	Y Suppress Level Setting 0 to 3: 1, 1/2, 1/4, 0
	18	2 to 3	YSPRTH	Y Suppress Threshold Setting 0 to 3: 100, 105, 110, 115IRE

8.3.4. Y-LPF OFF Function

The 1HDL output signal (DL1) can be input directly to the gamma block by setting the Y-LPF (CCD color filter carrier trap) filter coefficient to zero and turning off the filter operation. The Y-LPF ON/OFF setting does not affect the clamp operation, signal level or system delay, and the Y signal path configuration is such that there is also no effect on VH aperture correction.

Table 8.3-3 YLPFOFF setting

CAT	Byte	bit	Parameter Name	Description
3 PICT	1	4	YLPFSW	0: ON 1:OFF

8.3.5. GAMMA-OFF Function

The CXD3141R has a GAMMA-OFF function, and can set Y/C Gain value at GAMMA-OFF.

Table 8.3-4 GAMSW

CAT	Byte	bit	Parameter Name	Description	Default
3 PICT	1	6	GAMSW	0: ON 1:OFF	0
	19	0 to 7	GOFGAIN	Y/C Gain setting at GAMMA-OFF 00[h] to FF[h]	00[h]

8.4. Chroma Signal Processing

8.4.1. Setting the Primary Color Separation Matrix Constants

1) When using an EEPROM

When an EEPROM is used, input the settings to the following parameters, send the data and then write these data to the EEPROM. The primary color separation matrix constants written in the EEPROM are reflected during power-on startup.

RMATY (CAT9-Byte 16)
RMATC (CAT9-Byte 17)
BMATY (CAT9-Byte 18)
BMATC (CAT9-Byte 19)

Note: Even if **OCCF** (CAT1-Byte 1-bit 1) is changed, the primary color separation matrix constants are not switched.

2) When not using an EEPROM

The primary color separation matrix constants can be switched to match the spectral characteristics of 1/4 type and 1/3 type CCD using **OCCF** (CAT1-Byte 1-bit 1).

Table. 8.4-1 Default primary color separation matrix

OCCF	0	1
	1/4 Type CCD	1/3 Type CCD
RMATY	2D[h]	32[h]
RMATC	00[h]	F8[h]
BMATY	45[h]	32[h]
BMATC	BB[h]	D3[h]

8.4.2. Color (Hue/Gain) Adjustment

The procedure for adjusting color (hue/gain) is described below.

1. Set **CPUEXT** (CAT2-Byte 4-bit 0) to "1".
   Since the internal CPU overwrites the Hue/Gain, it is necessary to stop oper ations in order to make this adjustment.
2. Set the suppress start point and end point as follows.
   CSPRSTA (CAT3-Byte 14) = A0[h]
   CSPREND (CAT3-Byte 15) = D0[h]
3. Adjust **RYGAIN** (CAT3-Byte 10), **BYGAIN** (CAT3-Byte 11), **RYHUE** (CAT3-Byte 12), and **BYHUE** (CAT3-Byte 13).
4. With CPUEXT = 1, write to the EEPROM.
   CPUADRS (CAT2-Byte 2) = 2
   CPUCMD (CAT2-Byte 1) = 0 -> 1 -> 0
5. The new EEPROM values are reflected when the power is turned on.

8.5. Weighted Integration

With the CXD3142R, the screen is split into four separate photometric windows. The integral function is used for both AE and AWB using a weighted average found by multiplying the quantity of light integral value for each section by a weight. The AE and AWB are suitable when the main subject is in a fixed location on the screen.

Weights can be independently set for AE and AWB for each of the windows 0 to 3. The setting range is 1, 1/4, 1/16, 0, For the 2 serial parameter bits to be set. The WIND3 position and size can be set on the 15x15 grid using the W3STAH, W3WIDH, W3STAV and W3WIDH (CAT7-Bytes 2 and 3) parameters. The positions and sizes of the other four detection windows are determined according to the set WIND3 position and size.

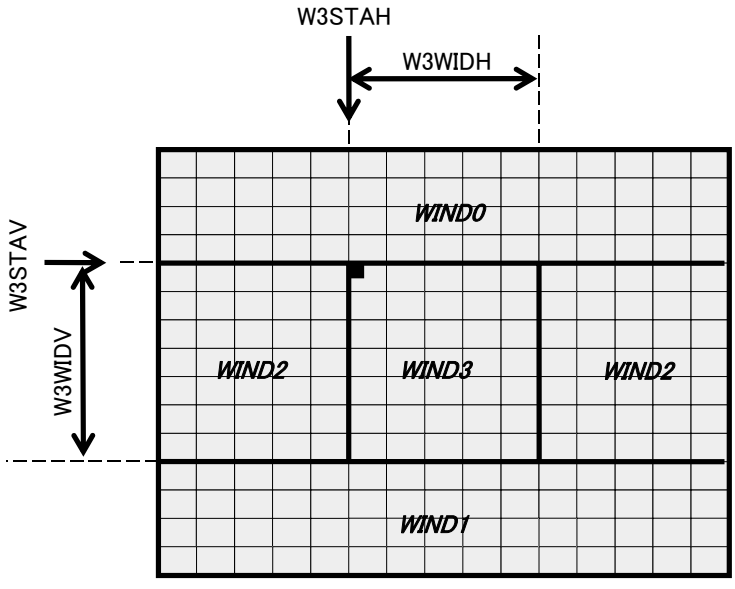


Fig. 8.5-1 OPD Detection Windows

(See “Fig. 8.5-1 OPD Detection Windows”.)

“Fig. 8.5-2” is a basic diagram that represents the OPD weighted integral function. Detection window values can be set independently for each of the AE/ABW windows 0 to 3.

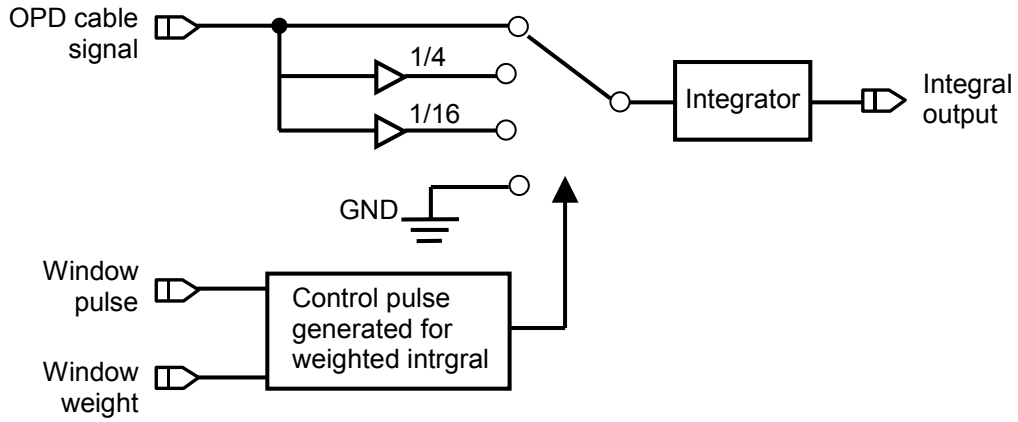


Fig. 8.5-2 Basic Diagram of OPD Weighted Integral

The parameters to be set are shown in “Table. 8.5-1 OPD Detection Window Related Setting Parameters”.

Table. 8.5-1 OPD Detection Window Related Setting Parameters

CAT	Byte	bit	Parameter name	Description
4 AE	1	0 to 1	AEW0	Weight of Window AE0 0 to 3: 1, 1/4, 1/16, 0
		2 to 3	AEW1	Weight of Window AE1 0 to 3: 1, 1/4, 1/16, 0
		4 to 5	AEW2	Weight of Window AE2 0 to 3: 1, 1/4, 1/16, 0
		6 to 7	AEW3	Weight of Window AE3 0 to 3: 1, 1/4, 1/16, 0
5 AWB	1	0 to 1	AWBW0	Weight of Window AWB0 0 to 3: 1, 1/4, 1/16, 0
		2 to 3	AWBW1	Weight of Window AWB1 0 to 3: 1, 1/4, 1/16, 0
		4 to 5	AWBW2	Weight of Window AWB2 0 to 3: 1, 1/4, 1/16, 0
		6 to 7	AWBW3	Weight of Window AWB3 0 to 3: 1, 1/4, 1/16, 0
7 TIMING	2	0 to 3	W3STAH	WIND3 horizontal start position setting data
		4 to 7	W3WIDH	WIND3 horizontal width setting data
	3	0 to 3	W3STAV	WIND3 vertical start position setting data
		4 to 7	W3WIDV	WIND3 vertical width setting data

8.6. AE Operation

8.6.1. Checking the Settings

Check the following settings in order to operate the AE.

1. NTSC/PAL

Check the used system and DIP switch settings. (When using an EEPROM, check the data written in the EEPROM; in the case of external microcomputer or RS232C control, check NTPAL (CAT1-Byte 1-bit 0).

2. CPUCMD（CAT2-Byte 1）

Be sure to set this to “0” other than during AE adjustment mode.

8.6.2. Mode

The operating mode can be selected and additional functions can be turned on and off by switching AEME, SHTFIX, BLCOFF, MIRIS, AEREF, AGCMAX and AESHUT. These items can be switched by the DIP switches or by serial communication.

1. When switching these items using the DIP switches, use AESHUT, AEME, SHTFIX, BLCOFF, MIRIS, AEREF and AGCMAX.
2. When switching these items by serial communication, set CPUDIP (CAT2-Byte 4-bit 4) to “1” and use AESHUT, AEME, SHTFIX, BLCOFF, MIRIS, AEREF and AGCMAX (CAT2-Byte 6-bits 0 to 6).

The DIP switch settings “Low” and “High” correspond to the serial settings “0” and “1”, respectively.

AE mode

AE operation is performed by the electronic iris and AGC control. AE operation basically sets AGC to the minimum necessary gain and controls the exposure with the electronic iris. However, when even the maximum exposure time results in insufficient exposure, AGC control is performed with the shutter speed set to the maximum exposure time. If exposure is excessive, first the AGC gain is lowered. Then, if exposure is still excessive even at the minimum gain, the electronic iris operates.
This mode has the following related parameters.

1. BLCOFF

This turns on and off backlight compensation.

2. AEREF

This switches and sets the AE convergence level.

When this is “0”, the level is set to 100 [IRE]; when “1”, the level can be set by the user in the range of 60 to 120 [IRE] by AEUSR (CAT4-Byte 7). The initial value is 80 [IRE].

3. AGCMAX

This switches the AGC maximum gain between two types.

When this is “0”, the maximum gain is the AGCMAXL (CAT4-Byte 8) setting value; when “1”, the maximum gain is switched to the AGCMAXH (CAT4-Byte 9) setting value.

4. AESPEED

This adjusts the AE response speed. The speed increases as the value becomes smaller and vice versa.

5. AGCMIN

This sets the AGC minimum gain. This is the AGC gain when shifting between electronic iris control and AGC gain control. The initial value is 10 [dB].

6. MSHTLIM

This sets the shutter limiter for the electronic iris. The initial value is 1/100,000 [s].

AE flickerless mode

Setting **NORMFL** (CAT2-Byte 5-bit 0) to “1” in AE mode results in flickerless mode. In this mode, control is performed by both AGC and the electronic shutter (except for shutter fixed mode).
Flickerless operation using either AGC or the electronic shutter can be turned off when NORMFL is 1. Setting **AGCFL** (CAT4-Byte 2-bit 0) = 1 turns off the AGC flickerless function. Setting **SHTFL** (CAT4-Byte 2-bit 1) = 1 turns off the electronic shutter flickerless function.

AE low speed shutter limiter mode

Setting **NORMFL** (CAT2-Byte 5-bit 0) to “1” in the AE mode results in flickerless mode. The contents of flickerless mode operation can be changed by **LSHTLIM** (CAT4-Byte 2-bit 2) to “1”.
LSHTLIM = 0 selects the flickerless mode.
LSHTLIM = 1 selects the low speed shutter limiter mode.
In the normal AE mode, the electronic iris and AGC operation is switched at 1/60 [s] during NTSC and 1/50 [s] during PAL, but in the shutter limiter mode these are switched at 1/100 [s] during NTSC and 1/120 [s] during PAL. Slower shutter speed cannot be obtained. Although dependent on the illumination of the subject, flicker should not occur when using a lens of F4 or higher under fluorescent lights as the limiter is activated at a shutter speed of 1/100 [s] during NTSC and 1/120 [s] during PAL.

AE shutter fixed flickerless mode

Setting **SFIXFL** (CAT2-Byte 5-bit 2) to “1” in AE mode results in shutter fixed flickerless mode. In this mode, the shutter speed is fixed to 1/100 [s] during NTSC and 1/120 [s] during PAL to reduce the flicker of fluorescent lights. AE operation is performed by only AGC control.

Flickerless Limiter

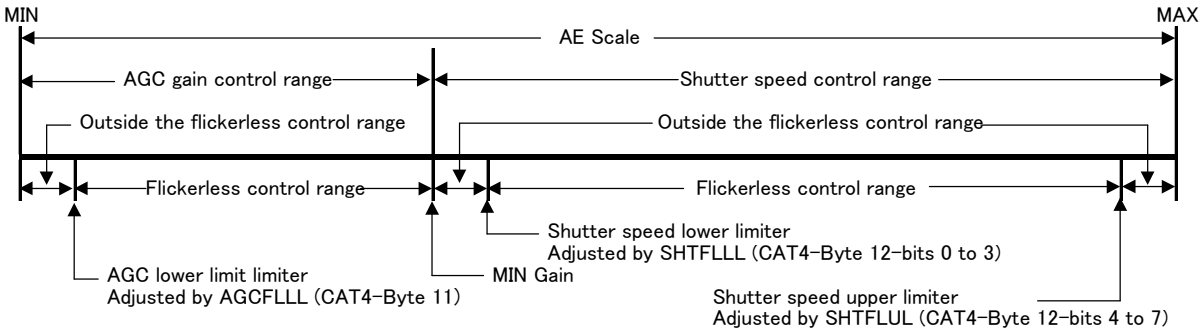


Fig. 8.6-1 Correlation between Flickerless Processing and AE Scale

Using AGCFLLL

This is set when limiting flickerless operation near the AGC MAX gain in flickerless mode. When changing the **AGCFLLL** (CAT4-Byte 11) value, set **SFIXFL**(CAT2-Byte 5-bit 2) to 0 and **LIMFL** (CAT2-Byte 5-bit 1) to 1 in AE mode.

Increasing the value widens the range near the AGC MAX gain over which flickerless control is not performed.

Using SHTFLLL

This is set when limiting flickerless operation in the low shutter speed range in flickerless mode. When changing the **SHTFLLL** (CAT4-Byte 12-bits 0 to 3) value, set **SFIXFL** (CAT2-Byte 5-bit 2) to 0 and **LIMFL** (CAT2-Byte 5-bit 1) to 1 in AE mode.

Increasing the value widens the low shutter speed range over which flickerless control is not performed.

Using SHTFLUL

This is set when limiting flickerless operation in the high shutter speed range in flickerless mode. When changing the **SHTFLUL** (CAT4-Byte 12-bits 4 to 7) value, set **SFIXFL** (CAT2-Byte 5-bit 2) to 0 and **LIMFL** (CAT2-Byte 5-bit 1) to 1 in AE mode.

Decreasing the value widens the high shutter speed range over which flickerless control is not performed.

The list of Flickerless control parameter

Table 8.6-1 The list of Flickerless Control Parameter

Mode	SFIXFL	LIM FL	NORM FL	LSHT LIM	AGC FL	SHT FL	AGC CNT	TG SHT	Shutter speed
AE flickerless off	0	0	0	-*	-*	-*	AGC*	SHUT*	SHUT*
AE flickerless	0	0	1	0	0	0	AGC*	SHUT*	SHUT*
AE flickerless	0	0	1	0	0	1	AGC*	SHUT*	SHUT*
AE flickerless	0	0	1	0	1	0	AGC*	SHUT*	SHUT*
AE flickerless	0	0	1	0	1	1	AGC*	SHUT*	SHUT*
AE flickerless	0	0	1	1	0	0	AGC*	SHUT*	SHUT* 1/100 (1/120)
AE flickerless	0	0	1	1	0	1	AGC*	SHUT*	SHUT*
AE flickerless	0	0	1	1	1	0	AGC*	SHUT*	SHUT*
AE flickerless	0	0	1	1	1	1	AGC*	SHUT*	SHUT*
AE flickerless (limit*)	0	1	-*	0	0	0	AGC* (limit*)	SHUT* (limit*)	SHUT*
AE flickerless (limit*)	0	1	-*	0	0	1	AGC* (limit*)	SHUT* (limit*)	SHUT*
AE flickerless (limit*)	0	1	-*	0	1	0	AGC* (limit*)	SHUT* (limit*)	SHUT*
AE flickerless (limit*)	0	1	-*	0	1	1	AGC* (limit*)	SHUT* (limit*)	SHUT*
AE flickerless (limit*)	0	1	-*	1	0	0	AGC* (limit*)	SHUT* (limit*)	SHUT* 1/100 (1/120)
AE flickerless (limit*)	0	1	-*	1	0	1	AGC* (limit*)	SHUT* (limit*)	SHUT*
AE flickerless (limit*)	0	1	-*	1	1	0	AGC* (limit*)	SHUT* (limit*)	SHUT*
AE flickerless (limit*)	0	1	-*	1	1	1	AGC* (limit*)	SHUT* (limit*)	SHUT*
Shutter speed fix	1	-*	-*	-*	-*	-*	AGC*	9B[h] (B5[h])	1/100 (1/120)

“AGC*”: Varies according to the subject.

“IRISV*”: Varies according to the subject.

“limit *”: Has limitter set by AGCFLLL or SHTFLUL.

“-*”: Don’t care.

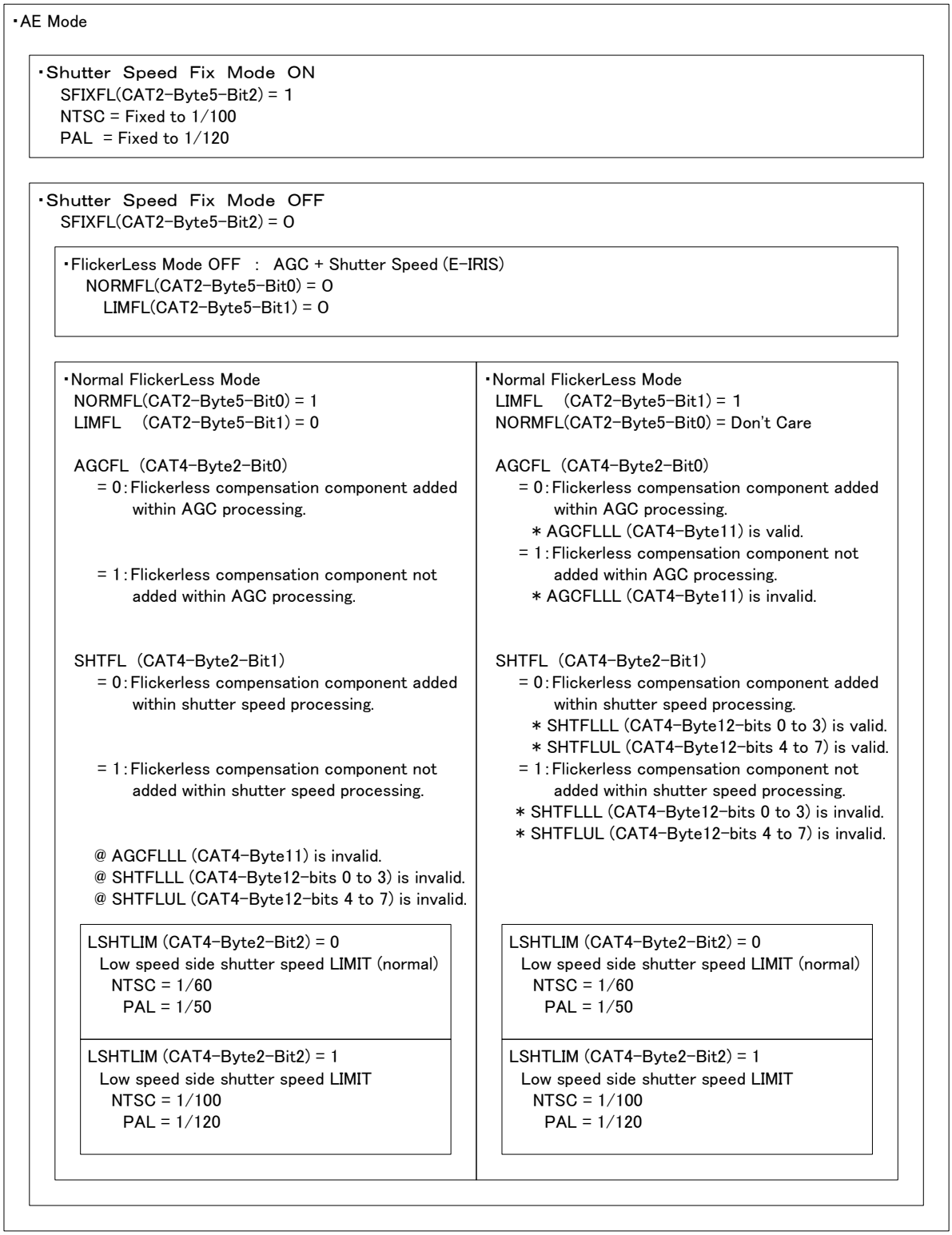


Fig. 8.6-1 Flickerless Transition Table

Video AE mode

Setting **VIDEOAE** (CAT1-Byte 3-bit 1) to 1 in AE mode results in video AE mode.

In this mode, the gain is increased up to approximately 2 times in the YGAIN immediately before the D/A after AGC has reached a maximum.

Only the luminance gain is increased, so the chroma noise is not amplified. Also, the S/N also does not change relative to the luminance.

This mode is linked with the normal AE operation, so gain-up operation is continuous from the AGC maximum state as shown in " Fig. 8.6-2 Video Out – Y Gain – AE Scale Correlation Drawing".

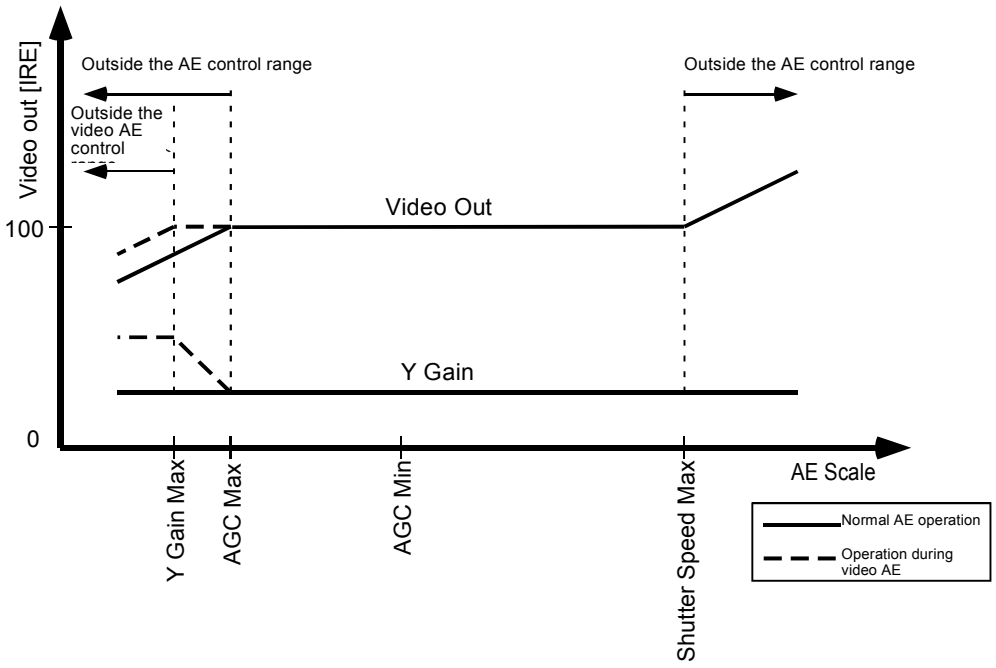


Fig. 8.6-2 Video Out – Y Gain – AE Scale Correlation Drawing

AE mechanical iris mode

Setting MIRIS (CAT2-Byte 6-bit 1) to “1” in the AE mode results in mechanical iris mode.
In this mode, the shutter speed is fixed to 1/60 [s] during NTSC and 1/50 [s] during PAL. AE operation is performed by AGC control and by the mechanical iris inside the external lens.
In this mode, AESPEED is multiplied internally by a factor of 8 times with respect to the setting value, thus slowing down AGC operation.

This mode has the following related parameters.

1. BLCOFF

This turns on and off backlight compensation.
When this is set to “0”, backlight compensation is on.
When this is set to “1”, backlight compensation is off.

2. AEREF

This switches and sets the AE convergence level.
When this is “0”, the level is set to 100 [IRE]; when “1”, the level can be set by the user in the range of 60 to 120 [IRE] by AEUSR.
AE operation in this mode is performed by the mechanical iris of the external lens and by AGC control. Care should be taken as operation may not be as specified by the setting value if the mechanical iris of the external lens is set improperly and the exposure exceeds the AGC control range. The initial value is 80 [IRE].

3. AGCMAX

This switches the AGC maximum gain between two types.
When this is “0”, the maximum gain is the AGCMAXL setting value; when “1”, the maximum gain is switched to the AGCMAXH setting value.

4. AESPEED

This adjusts the AGC control response speed. The speed increases as the value becomes smaller and vice versa.
In this mode, the AESPEED value is multiplied inside the microcontroller by a factor of 8 times.

5. AGCMIN

This sets the AGC minimum gain. The initial value is 10 [dB].

AE AESHUT mode

Setting AESHUT to “1” in AE mode results in AESHUT mode. This mode is the same as mechanical iris mode with the addition of a function allowing fixed shutter speeds to be selected by SHTFIX, BLCOFF and MIRIS. AE operation is performed by AGC control through the microcontroller AE and by the mechanical iris inside the external lens.

In this mode, AESPEED is multiplied internally by a factor of 8 times with respect to the setting value, thus slowing down AGC operation.

This mode has the following related parameters.

1. BLCOFF, MIRIS

These set one of eight different fixed shutter speeds. The shutter speeds that can be set are the same as the shutter speed settings during ME mode. (See “Table 8.6-2 ME Mode Shutter Speed”.)

2. AEREF

This switches and sets the AE convergence level.

When this is “0”, the level is set to 100 [IRE]; when “1”, the level can be set by the user in the range of 60 to 120 [IRE] by AEUSR.

AE operation in this mode is performed by the mechanical iris of the external lens and by AGC control. Care should be taken as operation may not be as specified by the setting value if the mechanical iris of the external lens is set improperly and the exposure exceeds the AGC control range. The initial value is 80 [IRE].

3. AGCMAX

This switches the AGC maximum gain between two types.

When this is “0”, the maximum gain is the AGCMAXL setting value; when “1”, the maximum gain is switched to the AGCMAXH setting value.

4. AESPEED

This adjusts the AGC control response speed. The speed increases as the value becomes smaller and vice versa.

In this mode, the AESPED value is multiplied inside the microcontroller by a factor of 8 times.

5. AGCMIN

This sets the AGC minimum gain. The initial value is 10 [dB].

ME shutter speed and AGC gain settings

In ME (Manual Exposure) mode, the shutter speed can be set by SHTFIX, BLCOFF and MIRIS. (See “Table 8.6-2 ME Mode Shutter Speed”.) In addition, the AGC gain can be set by AEREF and AGCMAX. (See “Table 8.6-3 ME Mode AGC Gain”.)

Table 8.6-2 ME Mode Shutter Speed

SHTFIX	BLCOFF	MIRIS	Shutter speed (NTSC) [s]	Shutter speed (PAL) [s]
0	0	0	1/60	1/50
1	0	0	1/100	1/120
0	1	0	1/250	1/250
1	1	0	1/500	1/500
0	0	1	1/1,000	1/1,000
1	0	1	1/2,000	1/2,000
0	1	1	1/4,000	1/4,000
1	1	1	1/10,000	1/10,000

Table 8.6-3 ME Mode AGC Gain

AEREF	AGCMAX	AGC gain
0	0	4 [dB]
1	0	10 [dB]
0	1	16 [dB]
1	1	22 [dB]

8.6.3. Coprocess Mode

The operating mode can be switched by CPUCMD (CAT2-Byte 1).

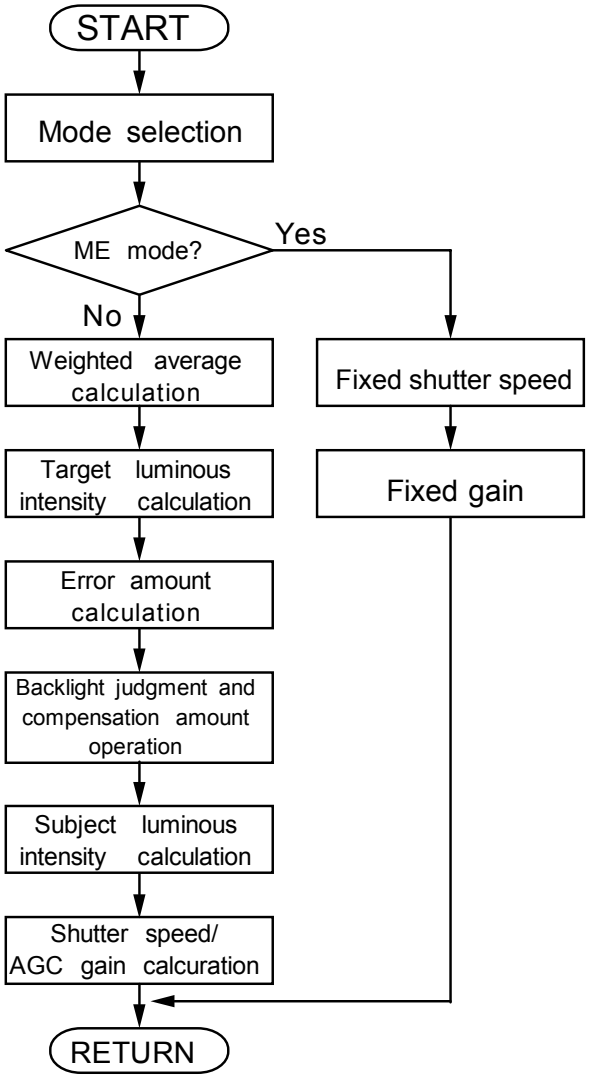
Coprocess mode off

Normal AE operation is performed. AE, flickerless (SHTFIX), backlight compensation (BLCOFF), ME based shutter and gain settings, and mechanical iris control can be performed by the DIP switches. AE operation can be arranged and customized by the parameters.

AE AGCMIN adjustment mode (CPUCMD = “21[h]”)

This mode is used to perform the AGCMIN adjustment. See “8.6.6. AE Related Adjustment Methods” for details.

8.6.4. AE Algorithm



Processing branches according to the mode input by the DIP switches or serial input.

In ME mode, the fixed shutter speed and fixed gain are selected and sent to the TG and AGC.

In AE mode, the subject luminous intensity is calcurlated from the integral values for each OPD window.

The backlight condition is determined from the data from the OPD and the compensation amount is calculated.

The shutter speed and AGC gain are obtained from the subject luminous intensity.

Fig. 8.6-3 AE Flow Chart

8.6.5. Backlight Compensation

Weighted average backlight compensation

Backlight compensation is performed by dividing the screen into five detection windows and multiplying the integrated luminous intensity values for each window by weighting values to obtain a weighted average. This method is suited for cases where the main subject is fixed within the screen.

The weighting for windows 0 to 3 can be set independently in a range from 0 to 3.

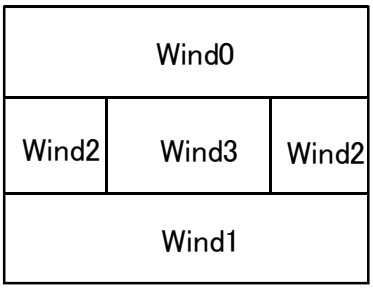


Fig. 8.6-4 OPD AE Detection Windows

Note

Compensation may be insufficient when the background is extremely bright.

Also, the backlight judgment may be difficult for some subjects with the result that AE operation appears to oscillate.

The weighted average backlight compensation function can be disabled by setting the same weighting values for all windows.

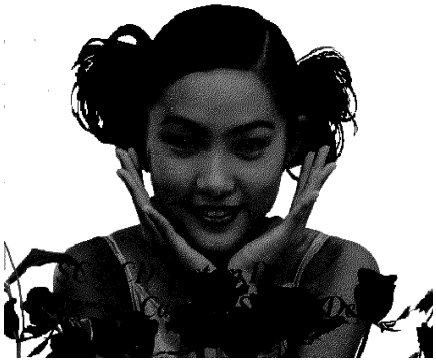


Fig. 8.6-5 Example Backlighted Subject

After backlight compensation

8.6.6. AE Related Adjustment Methods

Basic adjustments

AGCMIN adjustment

The SS-11RM system has a dynamic range of 250 [%], so A/D input of 400 [mVp-p] is necessary to obtain a video output of 100 [IRE]. A/D input of 400 [mVp-p] is necessary at the standard CCD output of 250 [mVp-p], but the AGC/SH gain characteristics vary somewhat between individual systems.
The AGCMIN adjustment absorbs the AGC/SH output and characteristic variance and sets the AGC minimum gain required to obtain A/D input of 400 [mVp-p] when the CCD output is 250 [mVp-p].

<Adjustment method>

1. Enter Min Gain adjustment mode.
   Set CPUCMD (CAT2-Byte 1) to “21 [hex]”.
2. Image an all-white subject (a subject which easily shows the white peak portions) with the light source turned on.
3. Adjust the exposure amount so that the video signal portion of the CCD-OUT signal is 250 [mVp-p].
   Adjust the exposure amount using ND filters and the lens iris, etc.
4. Adjust AGCMIN (CAT6-Byte 3) so that AGC-OUT (AD/IN) is 400 [mVp-p].
5. Once the adjustment value has been determined, write it to the EEPROM.
   (1) Set CPUCMD (CAT2-Byte 1) to 0 and CPUEXT(CAT2-Byte4-bit0) to 1 and CPUADRS (CAT2-Byte 2) to 2.
   (2) CPUCMD(CAT2-Byte 1) is set to 1 and is continuously set to 0.
   (Writing in EEPROM takes for 4 - 5 seconds.)
   (3) Finally, return CPUCEXT (CAT2-Byte4-bit0) to 0 and CPUADRS (CAT2-Byte 2) to 0.

AGCMAXL and AGCMAXH adjustment

These set the maximum AGC gain allowed under dim illumination conditions, and are set to compensate the minimum necessary subject illumination with respect to the CCD and AGC/SH characteristic variance.

Two types of minimum subject illumination can be set: AGCMAXL and AGCMAXH.

The setting is switched during AE operation by AGCMAX (CAT2-Byte 6-bit 4).

<Adjustment method>

1. Perform AE operation.
   Set CPUCMD (CAT2-Byte 1) to “00 [hex]”, NORMFL (CAT2-Byte 5-bit 0), LIMFL (CAT2-Byte 5-bit 1), SFIXFL (CAT2-Byte 5-bit 2) to “0”, and BLCOFF (CAT2-Byte 6-bit 2) to “1”.
2. Set AGCMAX (CAT2-Byte 6-bit 4) to “0” to set AGCMAXL (CAT4-Byte 8) or to “1” to set AGCMAXH (CAT4-Byte 9).
3. Set the subject illumination to the minimum subject illumination.
4. Adjust AGCMAXL (CAT4-Byte 8) or AGCMAXH (CAT4-Byte 9) using a screen or waveform monitor, etc.
5. Once the adjustment value has been determined, write it to the EEPROM.
   (1) Set CPUCMD (CAT2-Byte 1) to 0 and CPUADRS (CAT2-Byte 2) to 2.
   (2) Set CPUCMD (CAT2-Byte 1) to 1. This writes all the parameters to the EEPROM.
   (3) Finally, return CPUCMD (CAT2-Byte 1) to 0 and CPUADRS (CAT2-Byte 2) to 0.

Function adjustments

SHTLIM adjustment

This sets the maximum shutter speed allowed under high illumination conditions. The shutter speed is determined in consideration of the dynamic range, picture quality and smear, etc.

<Adjustment method>

1. Perform AE operation.
   Set NORMFL (CAT2-Byte 5-bit 0) to “0” and AGCMAX (CAT2-Byte 6-bit 4) to “0”.
2. Increase the subject illumination.
3. Adjust SHTLIM using a screen or waveform monitor, etc.
4. Once the adjustment value has been determined, write it to the EEPROM.

8.6.7. Parameter Reference

Category 2

CPUAE (CAT2-Byte 4-bit 1)

This bit controls the on (0)/off (1) status for all AE operation functions.

CPUCMD (CAT2-Byte 1)

When CPUAE is “0” (AE operation is on), this bit select the operating mode. (See “Table 8.6-4 CPUCMD and Operating Mode”.)

Table 8.6-4 CPUCMD and Operating Mode

CPUCMD	Operation contents
20[h]	AE/ME operation mode
21[h]	AE AGCMIN adjustment mode

AESPEED

Table 8.6-5 AESPEED

AESPEED	AESPEED
Parameter category	CAT4 AE, byte 6, bits 7 to 0 (8 bits)
Outline	Sets the AE responsiveness.
Conditions	AE/ME = 0
Setting range	00[h] to FF[h]
Initial value	08
Description	01: Maximum speed, FF: Minimum speed
Notes	Setting to “00” may stop AE operation or result in misoperation.

AEUSR

Table 8.6-6 AEUSR

AEUSR	AE USeR level set
Parameter category	CAT4 AE, byte 7, bits 7 to 0 (8 bits)
Outline	Sets the AE convergence luminous intensity (AE reference). Valid when AEREF = 1 (USR).
Conditions	AE/ME = 0
Setting range	00[h] to 0C[h]
Initial value	04 (80 [IRE])
Description	Allows the white video level to be set as shown in “Table 8.6-7 AEUSR and AE Convergence Values” when imaging a gray scale chart with BLCOFF = 1.
Notes	

Table 8.6-7 AEUSR and AE Convergence Values

AEUSR	IRE
00[h]	approximately 60
01[h]	approximately 65
02[h]	approximately 70
03[h]	approximately 75
04[h]	approximately 80
05[h]	approximately 85
06[h]	approximately 90
07[h]	approximately 95
08[h]	approximately 100
09[h]	approximately 105
0A[h]	approximately 110
0B[h]	approximately 115
0C[h]	approximately 120

AGCMAXL

Table 8.6-8 AGCMAXL

AGCMAXL	ae AGC MAXimum gain Low
Parameter category	CAT4 AE, byte 8, bits 7 to 0 (8 bits)
Outline	Sets the AGC maximum gain during AE operation.
Conditions	AE/ME = 0, AGCMAX = 0
Setting range	00[h] to FF[h]
Initial value	CC[h] 21 ([dB])
Description	Allows the maximum value limiter for the AGC gain when AGCMAX = 0 to be set as shown in “Fig. 8.6-6 Correspondence between AGCMIN, AGCMAXL,”.
Notes	Valid when AGCMAX = 0. Set a value equal to or greater than AGCMIN.

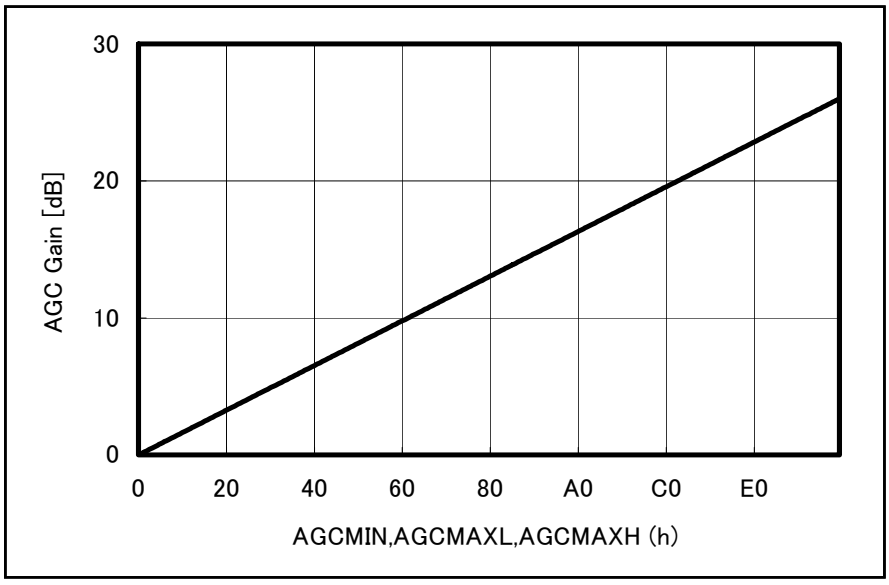


Fig. 8.6-6 Correspondence between AGCMIN, AGCMAXL,

AGCMIN

Table 8.6-9 AGCMIN

AGCMIN	ae AGC MINimum gain
Parameter category	CAT6 ADJUST, byte 3, bits 7 to 0 (8 bits)
Outline	Sets the AGC minimum gain during AE operation.
Conditions	CPUCMD = 21[h] (during the adjustment), AE/ME = 0
Setting range	00[h] to FF[h]
Initial value	11[h] (2[dB])
Description	Allows the minimum limiter for AGC to be set as shown in “Fig. 8.6-6 Correspondence between AGCMIN, AGCMAXL,”.
Notes	This is the transition point where AE control shifts between the AGC control and electronic iris control range. Set a value equal to or less than AGCMAXL and AGCMAXH.

MSHTLIM

Table 8.6-10 MSHTLIM

MSHTLIM	Maximum ae SHuTter LIMit
Parameter category	CAT4 AE, byte 10, bits 7 to 0 (8 bits)
Outline	Sets shutter speed limitter when using the electronic iris during AE operation.
Conditions	AE/ME = 0
Setting range	00[h] to 07[h]
Initial value	07[h] (1/100,000[s])
Description	Allows the shutter limiter to be set as shown in “Table 8.6-11 Correspondence between MSHTLIM and Shutter Limitter”.
Notes	

Table 8.6-11 Correspondence between MSHTLIM and Shutter Limitter

MSHTLIM	Shutter-Speed[s]
0	1/500
1	1/1,000
2	1/2,000
3	1/5,000
4	1/10,000
5	1/20,000
6	1/50,000
7	1/100,000

AGCMAXH

Table 8.6-12 AGCMAXH

AGCMAXH	ae AGC MAXimum gain High
Parameter category	CAT 4 AE, byte 9, bits 7 to 0 (8 bits)
Outline	Sets the AGC maximum gain during AE operation.
Conditions	AGCMAX = 1
Setting range	00[h] to FF[h]
Initial value	FF[h] (26 [dB])
Description	Allows the maximum value limiter for the AGC gain when AGCMAX = 1 to be set as shown in “Fig. 8.6-6 Correspondence between AGCMIN, AGCMAXL,”.
Notes	Valid when AGCMAX = 1. Set a value equal to or greater than AGCMIN.

LSHTLIM

Table 8.6-13 LSHTLIM

LSHTLIM	Lower SHuTter LIMitter
Parameter category	CAT4 AE, byte 2, bit 2 (1bit)
Outline	Switches between the flickerless mode and low-speed shutter limiter mode during flickerless mode.
Conditions	NORMFL = 1, LIMFL = 1
Setting range	0[h] to 1[h]
Initial value	0 (flickerless mode)
Description	The flickerless mode and low-speed shutter limiter mode can be switched as follows. Flickerless mode 1: low-speed shutter limiter mode
Notes	

AEW0, AEW1, AEW2, AEW3

Table 8.6-14 AEW0, AEW1, AEW2, AEW3

AEW0, AEW1, AEW2, AEW3	AE Window 0 weight, AE Window 1 weight , AE Window 2 weight, AE Window 3 weight
Parameter category	CAT4 AE, byte 1 (8 bits) AEW0, bits 1 and 0 / AEW1, bits 3 and 2 AEW2, bits 5 and 4 / AEW3, bits 7 and 6
Outline	Sets the photometry window weighting values for backlight compensation by weighted average photometry.
Conditions	AE/ME = 0, BLCOFF = 0
Setting range	0[h] to 3[h]
Initial value	0, 0, 0, 0 (windows 0, 1, 2 and 3)
Description	Allows the photometry window weighting values for backlight compensation by weighted average photometry during AE operation to be set.
Notes	

AESTAB

Table 8.6-15 AESTAB

AESTAB	AE STABility
Outline	Dead band width when the luminance level entered the hysteresis area
Category	CAT4 Byte3 (8bit)
Conditions	There are some objects which may still be difficult to shoot with this effect, such as when the subject is backlight.
Available settings range	00[h]-FF[h]
Initial value	00[h]
Description	00[h] (no dead band) to FF[h] (dead band maximum) If the setting value is too small, AE tracks even minimal fluctuations in the brightness and the hysteresis function is less effective. Contrarily, excessive values make the differences in the brightness level obvious when convergence is reached in AE.

AEHYST

Table 8.6-16 AEHYST

AEHYST	AE HYSTeresis
Outline	Dead band width when the luminance level moved outside the hysteresis area.
Category	CAT4 Byte4 (8bit)
Conditions	There are some objects which may still be difficult to shoot with this effect, such as when the subject is backlight.
Available settings range	00[h]-FF[h]
Initial value	00[h]
Description	00[h] (no dead band) to FF[h] (dead band maximum) If the setting value is too small, AE tracks even minimal fluctuations in the brightness and the hysteresis function is less effective. Contrarily, excessive values make the differences in the brightness level obvious when convergence is reached in AE.

AEWAIT

Table 8.6-17 AEWAIT

AEWAIT	AE WAIT
Outline	Counter value outside the hysteresis area.
Category	CAT4 Byte5 (8bit)
Conditions	There are some objects which may still be difficult to shoot with this effect, such as when the subject is backlight.
Available settings range	00[h]-FF[h]
Initial value	00[h]
Description	00[h] (no dead band) to FF[h] (dead band maximum) The time of hysteresis on to off becomes late as the setting value becomes large.

8.6.8. List of AE output states

There are two output destinations for the control data from the microcontroller AE: AGC gain (EVR) and shutter speed (TG). The microcontroller output states to these destinations for each operating mode are shown in the table below.

AE mode

Table 8.6-18 List of Output States during AE Mode

Name	AE SHUT	MIRIS	BLC OFF	SHT FIX	AEME	AGC CNT	TGSHT	SHUTTER SPEED
AE	0	0	0	0	0	AGC*	SHUT*	SHUT*
AE flickerless	0	0	0	1	0	AGC*	9B[h] (B5[h])	1/100 (1/120)
AE BLC off	0	0	1	0	0	AGC*	SHUT*	SHUT*
AE flickerless, BLC off	0	0	1	1	0	AGC*	9B[h] (B5[h])	1/100 (1/120)
AE mechanical iris	0	1	0	0	0	AGC*	32[h] (00[h])	1/60 (1/50)
AE mechanical iris, flickerless	0	1	0	1	0	AGC*	9B[h] (B5[h])	1/100 (120)
AE mechanical iris, BLC off	0	1	1	0	0	AGC*	32[h] (00[h])	1/60 (1/50)
AE mechanical iris, flickerless, BLC off	0	1	1	1	0	AGC*	9B[h] (B5[h])	1/100 (1/120)

AESHUT mode

Table 8.6-19 List of Output States during AESHUT Mode

Name	AE SHUT	MIRIS	BLC OFF	SHT FIX	AEME	AGC CNT	TG SHT	SHUTTER SPEED
AE-SHUT, 1/60(50)	1	0	0	0	0	AGC*	32[h] (00[h])	1/60 (1/50)
AE-SHUT, 1/100(120)	1	0	0	1	0	AGC*	9B[h] (B5[h])	1/100 (1/120)
AE-SHUT, 1/250	1	0	1	0	0	AGC*	F9[h]	1/250
AE-SHUT, 1/500	1	0	1	1	0	AGC*	118[h]	1/500
AE-SHUT, 1/1,000	1	1	0	0	0	AGC*	128[h]	1/1,000
AE-SHUT, 1/2,000	1	1	0	1	0	AGC*	134[h]	1/2,000
AE-SHUT, 1/4,000	1	1	1	0	0	AGC*	16A[h]	1/4,000
AE-SHUT, 1/10,000	1	1	1	1	0	AGC*	197[h]	1/10,000

“AGC*”: Varies according to the subject.

ME mode (shutter speed)

Table 8.6-20 List of ME Mode Shutter Speed Settings

AE SHUT	MIRIS	BLCOFF	SHTFIX	AEME	TGSHT	SHUTTER SPEED
0	0	0	0	1	32[h] (00[h])	1/60 (1/50)
0	0	0	1	1	9B[h] (B5[h])	1/100 (1/120)
0	0	1	0	1	F9	1/250
0	0	1	1	1	118	1/500
0	1	0	0	1	128	1/1,000
0	1	0	1	1	134	1/2,000
0	1	1	0	1	16A	1/4,000
0	1	1	1	1	197	1/10,000

ME mode (gain)

Table 8.6-21 List of ME Mode Gain Settings

AGCMAX	AEREF	AEME	AGCCNT 5V(3.3V)	AGC GAIN
0	0	1	64C[h] (98A[h])	4[dB]
0	1	1	7A6[h] (B97[h])	10[dB]
1	0	1	84A[h] (C8F[h])	16[dB]
1	1	1	8D8[h] (D67[h])	22[dB]

8.6.9. Other

When using a mechanical iris lens

-> The SS-11RM is not equipped with an IRISV function (present on the SS-1M (CXD2163BR)).

When backlight compensation control is needed for a mechanical iris lens, the OPD center window must be output from CXD3140R **S0**, **S1** or **S2** (Pin 70, 71 or 72), and an external circuit capable of weighting the iris detection signal using this Windw signal is also necessary. The setting method is as follows.

When **S0SEL** (CAT1-Byte 7-bits 0 to 2) is set to 3, the center Window signal is output to **S0** (Pin 70).

The flickerless function NORMFL cannot be turned on and off.

-> When changing the **NORMFL** (CAT2-Byte 5-bit 0) bit value, be sure to set **LIMFL** (CAT2-Byte 5-bit 1) and **SFIXFL** (CAT2-Byte 5-bit 2) to 0.

Vibration appears in flickerless mode

-> Vibration can be resolved by the following methods.

1. Near AGC MAX

   Vibration can be avoided by setting **AGCFL** (CAT4-Byte 2-bit 0) to 1 while **NORMFL** (CAT2-Byte 5-bit 0) is 1. However, this turns flickerless control off for AGC.

2. Near 0 dB

   Vibration can be avoided by setting **AGCFL** (CAT4-Byte 2-bit 0) to 1 while **NORMFL** (CAT2-Byte 5-bit 0) is 1. However, this turns flickerless control off for AGC.

3. Near SHUTTER MAX

   Vibration can be avoided by setting **SHTFL** (CAT4-Byte 2-bit 1) to 1 while **NORMFL** (CAT2-Byte 5-bit 0) is 1. However, this turns flickerless control off for the electronic shutter.

4. Other cases (using LIMFL)

   See "Using LIMFL".

Flickerless accuracy

-> Flickerless mode checks the integration results between three fields. Luminance variation in excess of a certain level is judged to be flicker and control is performed.

Therefore, even if flickerless is on, if the above judgment is incorrect, flicker cannot be suppressed or over-correction may occur.

Using LIMFL

-> In flickerless mode there is a mode where the electronic shutter upper and lower limits and the AGC gain lower limit for flickerless are determined. The parameter that activates this mode is **LIMFL** (CAT2-Byte 5-bit 1).

- The electronic shutter upper limit is determined by **SHTFLUL** (CAT4-Byte 12-bits 4 to 7).
- The electronic shutter lower limit is determined by **SHTFLLL** (CAT4-Byte 12-bits 0 to 3).
- The AGC gain lower limit is determined by **AGCFLLL** (CAT4-Byte 11).

Note that when changing the **SHTFLUL** (CAT4-Byte 12-bits 4 to 7), **SHTFLLL** (CAT4-Byte 12-bits 0 to 3) and **AGCFLLL** (CAT4-Byte 11) values, **SFIXFL** (CAT2-Byte 5-bit 2) should be set to 0 and **LIMFL** (CAT2-Byte 5-bit 1) should be set to 1.

When high luminance subjects for which the electronic shutter speed is approximately 1/2000 [s] have flicker, it may not be possible to suppress hunting if the flickerless function operates. In these cases, picture Vibration can be suppressed by setting **LIMFL** to 1 and adjusting **SHTFLUL**.

8.6.10. Flickerless Function

NORMFL (CAT2-Byte 5-bit 0)

Flickerless function off.

1: Flickerless function on.

This flickerless is controlled independently for AGC and the electronic shutter.

When NORMFL = 1, flickerless can be turned off for AGC or the electronic shutter.

AGCFL (CAT4-Byte 2-bit 0) = 1: Flickerless function is off for AGC.

SHTFL (CAT4-Byte 2-bit 1) = 1: Flickerless function is off for the electronic shutter.

8.6.11. AE flickerless mode

Setting NORMFL (CAT2-Byte 5-bit 0) to 1 in AE mode results in flickerless mode.

In this mode, control is performed for both AGC and the electronic shutter.

8.6.12. AE low speed shutter limiter mode

Setting NORMFL (CAT2-Byte 5-bit 0) to 1 in AE mode results in flickerless mode. The contents of flickerless mode operation can be changed by setting LSHTLIM (CAT4-Byte 2-bit 2) to 1.

LSHTLIM = 0 selects the normal flickerless mode.

LSHTLIM = 1 selects the low speed shutter limiter mode. In the normal AE mode, the electronic iris and AGC operation are switched at 1/60 [s] during NTSC and 1/50 [s] during PAL, but in the low speed shutter limiter mode, these are switched at 1/100 [s] during NTSC and 1/120 [s] during PAL. Slower shutter speeds cannot be obtained.

Although dependent on the illumination of the subject, flicker should not occur when using a lens of F4 or higher under fluorescent lights as the limiter is activated at a shutter speed of 1/100 [s] during NTSC and 1/120 [s] during PAL.

8.6.13. AE shutter fixed flickerless mode

Setting SFIXFL (CAT2-Byte 5-bit 2) to 1 in AE mode results in shutter fixed flickerless mode.
In this mode, the shutter speed is fixed to 1/100 [s] during NTSC and 1/120 [s] during PAL to reduce the flicker of fluorescent lights. AE operation is performed by only AGC control.

8.6.14. Video AE mode

Setting VIDEOAE (CAT1-Byte 3-bit 1) to 1 in AE mode results in video AE mode.
In this mode, the gain is increased up to approximately 2 times in the YGAIN immediately before the D/A after AGC has reached a maximum.
Only the luminance gain is increased, so the chroma noise is not amplified. Also, the S/N also does not change relative to the luminance.
This mode is linked with the normal AE, so operation is continuous and natural from the AGCMAX state.

8.6.15. IR cutless mode

Setting IRLESS (CAT1-Byte 3-bit 0) to 1 results in IR cutless mode.
This mode is for use when the IR cut filter is removed, and performs processing so that color reproduction does not break down even if the filter is removed.
First, the primary color separation matrix constants are changed. In addition, the hue and gain are also automatically adjusted with respect to the color temperature to achieve the optimum color reproduction.
The primary color separation matrix constants are changed, so AWB pre-white balance adjustment should be performed again when using this mode. If pre-white balance adjustment is not performed, the AWB may not operate properly.

8.6.16. AE-AWB link mode

LAEFL1 (CAT2-Byte 5-bit 3)

Setting LAEFL1 to 1 loads information that AWB judged shooting to be under fluorescent lights to AE and shifts to flickerless mode (mode equivalent to NORMFL: 1).

LAEFL2 (CAT2-Byte 5-bit 4)

Setting LAEFL2 to 1 loads information that AWB judged shooting to be under fluorescent lights to AE and shifts to flickerless mode (mode equivalent to LIMFL: 1).

LAWBFL (CAT2-Byte 5-bit 6)

Setting LAWBFL to 1 loads information that AE detected flicker under fluorescent lights to AWB and shifts to high speed pull-in mode.

8.7. WB Operation

8.7.1. Introduction

The SS-11RM mode, SS-11 and SS-1M mode are compared in the following table.

Table. 8.7-1 Comparison of the SS-11RM, SS-11 and SS-1M Modes

Mode	SS-11RM	SS-11	SS-1M
Anti-clolr rolling	○	○	×
Triggered push	○	○	○
Convergence shift	○	○	○
Luminance specific integration ON/OFF	○	○	○
Luminance specific integration slice level setting	Fixed (changeable)	Fixed (changeable)	Fixed (changeable)
Selection of minimum high lumination area	○	○	○
ATW operation frame	2 types	2 types	3 types
Adjustment method (adjustment points)	3 point	3 point	3 point
Manual white balance	—	—	○

8.7.2. Modes

The seven modes shown in “Table 8.7-2 WB Modes” can be selected by switching **AWB1, 2 and 3**.

1. When switching the mode using the DIP switches (default)
   Switch the mode using **AWB1, 2 and 3** (CXD3142R Pins 50, 51 and 52).
2. When switching the mode by serial communication
   Set **CPU** (CAT2-Byte 4-bit 4) to “1” and then switch the mode using **AWB, 2 and 1** (CAT2-Byte 7-bits 2, 1 and 0).

Table. 8.7-2 WB Modes

Mode	AWB1	AWB2	AWB3	Set color temperature (K)
ATW	0	0	0	—
Push	0	1	0	—
Hold	0	1	1	—
Indoor fixed value	1	0	0	approximately 3200
Fluorescent light fixed value	1	0	1	approximately 4200
User	1	1	0	approximately 4700
Outdoor fixed value	1	1	1	approximately 6300

ATW

ATW is the Auto Trace White balance mode.

ATW is a feedback system that automatically aligns the white balance by detecting the R, G and B before gamma correction processing.

The convergence point can be shifted by **AWBRSFT (CAT5-Byte 7)** and **AWBBSFT (CAT5-Byte 8)**.

In addition, the following items can also be switched.

- Luminance specific integration ON/OFF selection (**AWBSEPOF (CAT5-Byte 2-bit 0)**)
- Luminance specific integration minimum high luminance area selection (**AWBHLCUT (CAT5-Byte 2- bits 2 and 3)**)

Push

Operation is performed at a faster operating speed than ATW without an operation frame or other limitations.

However, the response time, an operation frame and other factors cannot be selected.

The conventional system or trigger system can be selected. (See the Hold mode for a detailed description below.)

This switch is made by means of **AWBTRIG (CAT5-Byte 2-bit 1)**.

Hold

Pull-in operation stops when the mode shifts from push mode to hold mode, and the R and B gains at that point are written to the EEPROM.

Push mode and hold mode can be combined to realize the push lock mode.

1. Conventional push lock mode (**AWBTRIG** = 0)

   Operation is performed in push mode while the button is pressed and shifts to hold mode when the button is released, allowing the white balance gain at that point to be written to the EEPROM.

2. Trigger system push lock mode (**AWBTRIG** = 1)

   Operation shifts to push mode when the button is pressed and convergence operation continues even if the button is released. When convergence is automatically judged to be completed, the white balance gain at that point is written to the EEPROM.

User

In user mode, when an EEPROM is present, the gain set by **WBUSRR (CAT5-Byte 11)** and **WBUSRB (CAT5-Byte 12)** is written to the EEPROM, and this gain is read and reflected the next time the system is started up.

Fixed values

There are three fixed value modes: indoor, fluorescent light and outdoor fixed value.

The fixed value modes can be shifted by **WBRSFT (CAT5-Byte 13)** and **WBBSFT (CAT5-Byte 14)**. However, this shift affects all four modes including user mode. A mode cannot be shifted separately.

Table. 8.7-3 Difference between ATW and Push

	ATW (with frame)	ATW (without frame)	Push
OPD integration	Luminance specific integration	Luminance specific integration	No luminance specific integration
Speed	×1	×1	×30 to 40
Operation color temperature range	Limited	Unlimited	Unlimited
High luminance area	Limited	Limited	Unlimited

8.7.3. AWB Arithm

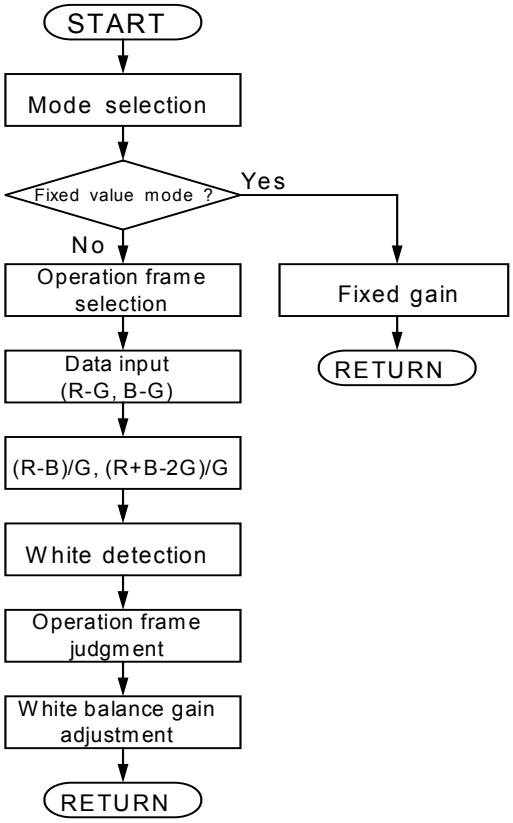


Fig. 8.7-1 AWB Flow Chart

Processing branches according to the mode input by the DIP switches or serial input.

In fixed value mode, the fixed gain is selected, shift processing is performed, and the signal is sent to the WB gain amplifier.

In ATW mode, the operation frame is selected.
The operation frame is not selected for push mode.

Next, operations are performed using the data from the OPD.

The detection data from the OPD is converted to (R-B)/G and (R+B–2G)/G format.

In ATW mode, after performing white detection, the operation frame is judged and operation shifts to convergence processing.

8.7.4. Pre-White Balance Adjustment

Pre-white balance consists of aligning the operation color temperature range of the built-in ATW with two reference color temperatures for each CCD to be used.

The pre-white balance alignment procedures are as follows. (This adjustment is reflected during power-on.)

1. Image a light source of the reference color temperature (**approximately 3200 K**) onto the entire screen.
2. Set **WBRSFT** and **WBBSFT** to 0[h].
3. Enter user mode (AWB1 = 1, AWB2 = 1, AWB3 = 0).
4. Adjust **WBUSRR** and **WBUSRB** to align the point with white (the center of the vector scope).
5. Transfer the **WBUSRR** and **WBUSRB** values at that point to **AWBPRER** and **AWBPREB**.
6. Apply a color temperature conversion filter to the light source (approximately 3200 K) to obtain a color temperature of **approximately 2500 K**.
7. Adjust **WBUSRR** and **WBUSRB** to align the point with white (the center of the vector scope).
8. Transfer the **WBUSRB** value at that point to **BLOGAIN**.
9. Apply a color temperature conversion filter to the light source (approximately 3200 K) to obtain a color temperature of **approximately 9500 K**.
10. Set the AWB coprocess mode (CPUCMD (CAT2-Byte 1)) to 32[h].
11. Set the **WBR** and **WBB** to the same values as **AWBPRER** and **AWBPREB** described above, and set **WBYREFH** to D0[h] and **WBYREFL** to 04[h] and transmit the data.
12. At this point, the **AWOUT1** and **AWOUT2** values are transferred to the **PRERB**. And the **AWOUT3** and **AWOUT4** values are transferred to the **PRERBG**.
13. Exit the coprocess mode (CPUCMD (CAT2-Byte 1): 00[h]) and adjust **WBUSRR** and **WBUSRB** to align the point with white (the center of the vector scope). (Same operation as step 4.)
14. Transfer the **WBUSRR** and **WBUSRB** values at that point to **PRE2R** and **PRE2B**.
15. Return **WBRSFT**, **WBBSFT**, **WBUSRR** and **WBUSRB** to their initial values (03[h], 01[h], 49[h] and 2D[h], respectively).
16. Write the values to the EEPROM.

The white balance operation range is determined by the above adjustment as shown in the figure below.

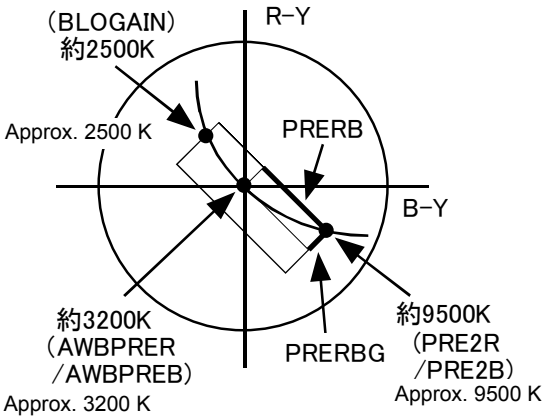


Fig. 8.7-2 Adjusting the Operation Frame for the Pre-White Balance

8.7.5. Gain Limiter Adjustment

The gain limiter is adjusted by **AWBAJST1 (CAT6-Byte 16)** and **AWBAJST2 (CAT6-Byte 17),** which set maximum and minimum range as the sum of R gain and B gain**.**

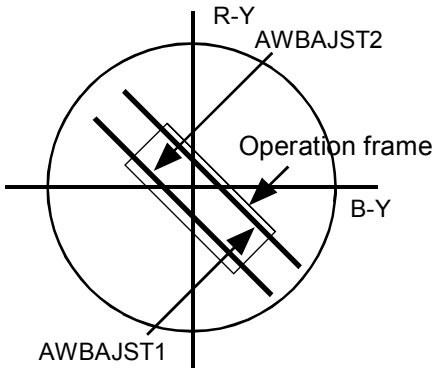


Fig. 8.7-3 Gain Limiter Position

AWBAJST1 limits convergence from the **G** direction.

AWBAJST2 limits convergence from the **Mg** direction.

AWBAJST1

AWBAJST1 is the value obtained by subtracting the sum of the R gain and B gain at approximately 3200 K from the larger value of either the sum of the R gain and B gain at approximately 9500 K or the sum of the R gain and B gain at approximately 2500 K.

AWBAJST2

AWBAJST2 is the fixed value 1C[h].

8.7.6. ATW Operation Range

ATW sets an operation frame that follows the black body radiation curve.

The operation color temperature range (R-B axis direction) for the standard operation frame is from approximately 2500 K to approximately 9500 K.

The Mg-G axis direction has a width of approximately 1/2 that of the operation frame in the R-B axis direction, and the ratio between the widths in the Mg and G directions is approximately 8:7.

The operation color temperature ranges for each operation frame are as shown in the table below.

The frame is selected by **AWBFRAM (CAT5-Byte 6)** described hereafter.

Table. 8.7-4 Operation Color Temperature Ranges for Different Operation Frame

Frame	Minimum operation color temperature	Maximum operation color temperature
Standard frame	approximately 2500 K	approximately 9500 K
frame canceled	less than approximately 2000 K	more than approximately 18000 K

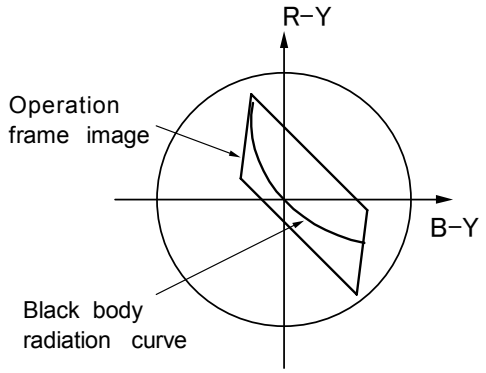


Fig. 8.7-4 Operation Frame Image

The operation frame axes are (R-B)/G and (R+B–2G)/G.

During push mode, this frame is canceled.

In addition, the frame is also canceled during ATW operation if **AWBFRAM** is set to 1[h].

When the frame is canceled, convergence operation is performed for any subject. However, push and white balance may differ for some subjects. This is due to a difference in the algorithms for ATW and push.

Note that the convergence accuracy during ATW and push modes is **approximately 4%** with respect to the size of the burst flag.

8.7.7. ATW Related Parameters

［Serial input］

WBR Red Gain : 8 bits, initial value 37[h]
[CAT9-Byte 5-bits 7 to 0]

WBG Green Gain : 8 bits, 26[h] fixed at standard
[CAT9-Byte 6-bits 7 to 0]

WBB Blue Gain : 8 bits, initial value 39[h]
[CAT9-Byte 7-bits 7 to 0]

WBYREFH Luminance specific integration slice level setting (upper level): initial value D0[h]
[CAT9-Byte 8-bits 7 to 0]

WBYREFL Luminance specific integration slice level setting (lower level): initial value 4[h]
[CAT9-Byte 9-bits 7 to 0]

The above gains are automatically written to the EEPROM when operation shifts to hold mode.
In addition, the EEPROM write addresses are not **WBR, WBG** and **WBB**, but **RGAIN** 45[h], **GGAIN** 3F[h] and **BGAIN** 46[h].
The white balance gains (**WBR, WBG** and **WBB**) and the integral range (**WBYREFH** and **WBYREFL**) cannot normally be manipulated. However, these values can be changed by stopping the built-in AWB (setting **CPUAWB** (CAT2-Byte 4-bit 2) to “1”).

AWBLLCUT AWB Low Light Cut : 1 bit, initial value 0: **WBYREFH** = 04[h]
[CAT5-Byte 2-bit 4]

WBYREFH is switched by **AWBLLCUT** = 0: 04[h], 1: 00[h].
The **WBYREFH** and **WBYREFL** values in the ATW and push modes are shown in "Table. 8.7-5 Integral Threshold Value Settings by Luminance" below.

Table. 8.7-5 Integral Threshold Value Settings by Luminance

Mode	AWBLLCUT = 0		AWBLLCUT = 1	
ATW	Medium luminance	High luminance	Medium luminance	High luminance
WBYREFH	80[h]	D0[h]	80[h]	D0[h]
WBYREFL	04[h]	80[h]	00[h]	80[h]
Push				
WBYREFH	D0[h]		D0[h]	
WBYREFL	04[h]		00[h]	

[Serial output]

AWBCNTL Integral pixel counter output: (16 bits) lower 8 bits: 8 bits
[SERIALOUT-Byte 14-bits 7 to 0]
AWBCNTM Integral pixel counter output: (16 bits) upper 8 bits: 8 bits
[SERIALOUT-Byte 15-bits 7 to 0]

INTGRL R integral data output (16 bits) lower 8 bits: 8 bits, R output as standard
[SERIALOUT-Byte 16-bits 7 to 0]
INTGRM R integral data output (16 bits) upper 8 bits: 8 bits
[SERIALOUT-Byte 17-bits 7 to 0]

INTGGL G integral data output (16 bits) lower 8 bits: 8 bits, G output as standard
[SERIALOUT-Byte 18-bits 7 to 0]
INTGGM G integral data output (16 bits) upper 8 bits: 8 bits
[SERIALOUT-Byte 19-bits 7 to 0]

INTGBL R integral data output (16 bits) lower 8 bits: 8 bits, B output as standard
[SERIALOUT-Byte 20-bits 7 to 0]
INTGBM R integral data output (16 bits) upper 8 bits: 8 bits
[SERIALOUT-Byte 20-bits 7 to 0]

CAT2 CPU (CPUCMD: Byte1, CPUAWB: Byte4-bits 2)

For details on **CPUCMD**, see "8.7.9. AWB Coprocess Mode".

CPUAWB can be switched to operate the internal AWB program or so that AWB is completely stopped.

Table. 8.7-6 CPUCMD Mode Setting

Parameter name	Control	0 (Standard)	31	32
CPUCMD	Coprocess mode switching	Normal operation	Monitor	Average

Table. 8.7-7 CPUAWB AWB Operation Status

Parameter name	Control	0 (Standard)	1
CPUAWB	Internal AWB on/off	ON	OFF

8.7.8. WB Parameter Reference

AWBSPED:

This determines the ATW operation speed. The speed decreases as the value becomes larger.

Table. 8.7-8 AWBSPED

AWBSPED	AWB SPEeD
Parameter category	CAT5 AWB, byte 5, bits 3 to 0 (4 bits)
Outline	Sets the ATW responsiveness.
Conditions	AWB1, 2, 3 = Low or 0
Setting range	1[h] to F[h]
Initial value	1[h]
Description	1[h]: Maximum speed, F[h]: Minimum speed
Notes	The upper 4 bits correspond to AWBAJST5 and AWBAJST6. Setting 0[h] results in high-speed pull-in.

Changing from 2500 K to 9500 K takes approximately 10 seconds under standard conditions.

AWBFRAM:

This selects the ATW operation frame.

Table. 8.7-9 AWBFRAM

AWBFRAM	AWB vector FRAMe
Parameter category	CAT5 AWB, byte 6, bits 7 to 0 (8 bits)
Outline	Selects ATW operation frame.
Conditions	AWB1, 2, 3 = Low or 0
Setting range	00[h] to 01[h]
Initial value	00[h] (standard frame)
Description	00[h]: standard frame, 1[h]: frame canceled
Notes	This parameter is only valid in ATW mode.

WBRSFT/WBBSFT:

Increasing the WBRSFT value shifts toward the plus side of the R-Y axis.

Increasing the WBBSFT value shifts toward the minus side of the B-Y axis.

Table. 8.7-10 WBRSFT/WBBSFT

WBRSFT/WBBSFT	WB R Shift/WB B Shift
Parameter category	CAT5 AWB, byte 13, bits 7 to 0 (8 bits) CAT5 AWB, byte 14, bits 7 to 0 (8 bits)
Outline	Shift gain for fixed value mode
Conditions	AWB1 = High or 1
Setting range	00[h] to FF[h]
Initial value	03[h] (WBRSFT), 01[h] (WBBSFT)
Description	The same shift amount is applied simultaneously to all fixed value modes.
Notes	This parameter is not valid in ATW, push, manual or hold modes.

WBUSRR/WBUSRB

Table. 8.7-11 WBUSRR/WBUSRB

WBUSRR/WBUSRB	WB USeR preset R gain/WB USeR preset B gain
Parameter category	CAT5 AWB, byte 11, bits 7 to 0 (8 bits) CAT5 AWB, byte 12, bits 7 to 0 (8 bits)
Outline	Adjustment gain for user mode
Conditions	AWB1 and 2 = High or 1, AWB3 = Low or 0
Setting range	00[h] to FF[h]
Initial value	49[h] (WBUSRR), 2C[h] (WBUSRB)
Description	
Notes	This parameter is only valid in user mode.

AWBPRER/AWBPREB

This is the pre-white balance gain. The adjustment method was described previously.

Table. 8.7-12 AWBPRER/AWBPREB

AWBPRER/ AWBPREB	AWB PRE white balance R AWB PRE white balance B
Parameter category	CAT6 ADJUST, byte 8, bits 7 to 0 (8 bits)
Outline	Adjustment gain for pre-white balance
Conditions	
Setting range	00[h] to FF[h]
Initial value	37[h] (AWBPRER), 39[h] (AWBPREB)
Description	Gain when white balance is aligned for approximately 3200 K.
Notes	This parameter is valid after writing to the EEPROM and resetting.

AWBRSFT/AWBBSFT: Initial value 00[h]/00[h]

Table. 8.7-13 AWBRSFT/AWBBSFT

AWBRSFT/ AWBBSFT	AWB white point R ShiFT AWB white point B ShiFT
Parameter category	CAT5 AWB, byte 7, bits 7 to 0 (8 bits) CAT5 AWB, byte 8, bits 7 to 0 (8 bits)
Outline	This shifts the convergence point during ATW.
Conditions	AWB1, 2, 3 = Low or 0 and More than AWBSPED = 1[h].
Setting range	80[h] to 00[h] to 7F[h]
Initial value	00[h] (AWBRSFT), 00[h] (AWBBSFT)
Description	This shifts the convergent point in a desired direction during ATW and push modes.
Notes	If the value becomes too large, convergence operation is not performed.

PRERBL/PRERBH

Table. 8.7-14 PRERBL/PRERBH

PRERBL/PRERBH	PRE R-B L/H
Parameter category	CAT6 ADJUST, byte 10, bits 7 to 0 (8 bits) CAT6 ADJUST, byte 11, bits 7 to 0 (8 bits)
Outline	Adjustment data for ATW operation frame (R–B)/G
Conditions	AWB1, 2, 3 = Low or 1
Setting range	80[h] to 00[h] to 7F[h]
Initial value	0A[h] (PRERBH), 00[h] (PRERBL)
Description	Value at approximately 9500 K after white balance was aligned at approximately 3200 K.
Notes	If the color temperature is different at the time of setting, the operation color temperature range will also be different.

PRERBGL/PRERBGH

Table. 8.7-15 PRERBGL/PRERBGH

PRERBGL/ PRERGBH	PRE R+B-2G L/H
Parameter category	CAT6 ADJUST, byte 12, bits 7 to 0 (8 bits) CAT6 ADJUST, byte 13, bits 7 to 0 (8 bits)
Outline	Adjustment data for ATW operation frame (R+B–2G)/G
Conditions	AWB1, 2 and 3 = Low or 0
Setting range	80[h] to 00[h] to 7F[h]
Initial value	23[h] (PRERBGM), 00[h] (PRERBGL)
Description	Value at approximately 9500 K after white balance was aligned at approximately 3200 K.
Notes	If the color temperature is different at the time of setting, the operation color temperature range will also be different.

PRE2R/PRE2B

Table. 8.7-16 PRE2R/PRE2B

PRE2R/PRE2B	AWB PRE white balance 2 R/AWB PRE white balance 2 B
Parameter category	CAT6 ADJUST, byte 14, bits 7 to 0 (8 bits) CAT6 ADJUST, byte 15, bits 7 to 0 (8 bits)
Outline	ATW gain for high color temperature (approximately 9500 K)
Conditions	AWB1, 2 and 3 = Low or 0
Setting range	00[h] to FF[h]
Initial value	60[h] (PRE2R), 20[h] (PRE2B)
Description	Gain when white balance is aligned at approximately 9500 K.
Notes	If the color temperature is different at the time of measurement, the operation color temperature range will also be different.

AWBAJST1

Table. 8.7-17 AWBAJST1

AWBAJST1	AWB AdJuST1
Parameter category	CAT6 ADJUST, byte 16, bits 7 to 0 (8 bits)
Outline	ATW gain limiter Upper limit offset
Conditions	AWB1, 2 and 3 = Low or 0
Setting range	00[h] to FF[h]
Initial value	18[h]
Description	Parameter to control convergence from the G direction.
Notes	If the value is too small, convergence operation stops.

AWBAJST2

Table. 8.7-18 AWBAJST2

AWBAJST2	AWB AdJuST2
Parameter category	CAT6 ADJUST, byte17, bits 7 to 0 (8 bits)
Outline	ATW gain limiter Lower limit offset
Conditions	AWB 1, 2 and 3 = Low or 0
Setting range	00[h] to FF[h]
Initial value	1C[h]
Description	Parameter to control convergence from the Mg direction.
Notes	If the value is too small, convergence operation stops.

BLOGAIN

Table. 8.7-19 BLOGAIN

BLOGAIN	BLOwGAIN
Parameter category	CAT6 ADJUST, byte 20, bits 7 to 0 (8 bits)
Outline	Lower limit B gain for manual white balance
Conditions	AWB 1 and 2 = Low or 0
Setting range	00[h] to FF[h]
Initial value	46[h]
Description	This determines lower limit color temperature for ATW operation.
Notes	If the color temperature is different at the time of setting, the operation color temperature range will also be different.

INTSLICE

Table. 8.7-20 INTSLICE

INTSLICE	INTegral SLICE level
Parameter category	CAT6 ADJUST, byte 21, bits 7 to 0 (8 bits)
Outline	Luminance specific integration slice level
Conditions	AWB 1, 2 and 3 = Low or 0
Setting range	00[h] to FF[h]
Initial value	80[h]
Description	This changes the luminance specific integral slice level in ATW.
Notes	Enter within the 04[h] to D0[h] range.

AWBAJST3

Table. 8.7-21 AWBAJST3

AWBAJST3	AWB AdJuST3
Parameter category	CAT6 ADJUST, byte 18, bits 7 to 0 (8 bits)
Outline	Operation frame ((R-B)/G axis direction) offset
Conditions	AWB 1, 2 and 3 = Low or 0
Setting range	80[h] to 00[h] to 7F[h]
Initial value	00[h]
Description	This adds offset to the operation frame ((R-B)/G axis direction).
Notes	If the value is too large, the operation color temperature range becomes larger.

AWBAJST4

Table. 8.7-22 AWBAJST4

AWBAJST4	AWB AdJuST4
Parameter category	CAT6 ADJUST, byte 19, bits 7 to 0 (8 bits)
Outline	Operation frame ((R+B-2G)/G axis direction) offset
Conditions	AWB 1, 2 and 3 = Low or 0
Setting range	80[h] to 00[h] to 7F[h]
Initial value	00[h]
Description	This adds offset to the operation frame ((R+B-2G)/G axis direction).
Notes	If the value is too large, the operation color temperature range becomes larger.

AWBAJST5

Table. 8.7-23 AWBAJST5

AWBAJST5	AWB AdJuST5
Parameter category	CAT5 AWB, byte 5, bits 5 to 4 (2 bits)
Outline	Gain limit ((R+B-2G)/G axis direction) offset
Conditions	AWB 1, 2 and 3 = Low or 0
Setting range	0[h] to 3[h]
Initial value	0[h]
Description	This determines width of the frame region in (R+B-2G)/G axis direction.
Notes	

AWBAJST6

Table. 8.7-24 AWBAJST6

AWBAJST6	AWB AdJuST6
Parameter category	CAT5 AWB, byte 5, bits 7 to 6 (2 bits)
Outline	Gain limit ((R-B)/G axis direction) offset
Conditions	AWB 1, 2 and 3 = Low or 0
Setting range	0[h] to 3[h]
Initial value	0[h]
Description	This determines width of the frame region in (R-B)/G axis direction.
Notes	

8.7.9. AWB Coprocess Mode

CPUCMD（CAT2-Byte1）

00[h]: AWB coprocess mode off (normal AWB operation)

31[h]: Monitor mode

32[h]: Average mode (AWB operation stopped)

31[h]: In the monitor mode, the white balance gain during AWB operation is output.
WBR is output to AWOUT1, WBG to AWOUT2, and WBB to AWOUT3.

32[h]: In the average mode, the AWB integral data is output.
R/G is output to AWOUT1 and 2, and B/G is output to AWOUT3 and 4. (The built-in AWB is stopped.)

Table. 8.7-25 Output during Coprocess Mode

Parameter	Normal operation (0[h])	Monitor (31[h])	Average (32[h])
AWOUT1	Undetermined	R gain	(R-B)/G (lower)
AWOUT2	Undetermined	G gain	(R-B)/G (upper)
AWOUT3	Undetermined	B gain	(R+B-2G)/G (lower)
AWOUT4	Undetermined	Undetermined	(R+B-2G)/G (upper)

8.7.10. AE-AWB link mode

* See “8.6.16. AE-AWB link mode”.

8.7.11. AWB anti-color rolling mode

Cyclic color changes with a long period appear when shooting with a NTSC (59.94 [Hz]) camera under fluorescent lights with a 60 [Hz] power supply. This is called color rolling.

Setting AWBSPED (CAT5-Byte5) to 00 [h] in ATW mode or setting push mode (AWB (CAT2-Byte7-bits 0 to 2) = 2) results in anti-color rolling mode.

In this mode, the convergence speed is set to high speed to suppress color rolling under fluorescent lights. Whereas conventional white balance required several tens of fields for convergence, this mode achieves it in 2 or 3 fields.

8.7.12. Other

Effect on the built-in AWB when the primary color separation matrix constants are changed

-> These constants affect ATW convergence operation and the operation color temperature range. Operation is not assured when the primary color separation matrix constants are changed.

Effect on the built-in AWB when the linear matrix constants are changed

-> Hue and gain linear matrix processing is performed after passing through AWB processing, so there is no effect on AWB operation.

Difference between push and ATW (without operation frame)

-> In push mode, white balance processing is performed by integrating the information for the entire screen and luminance.

In ATW (without frame) mode, the integral range is divided into two parts according to differences in luminance and white balance processing is performed using the data from either of these parts.

Therefore, the white balance may differ between the two modes even when shooting the same subject.

The screen becomes black and white during push (or push lock) and ATW operation

-> **GGAIN** (CAT5-Byte 3) may be set to “0”.

In this case, write the initial value of **26**[h] for **GGAIN** (address 26[h]) to the EEPROM.

Users wish to align the white balance under the desired subject conditions

-> Use user mode. Adjust the gain using **WBUSRR** and **WBUSRB**.Users wish to shift the ATW convergence point from white

-> This can be accomplished by using **AWBRSFT** and **AWBBSFT**.

White balance cannot be obtained under fluorescent light

-> The fluorescent light may be judged as outside the operation range. Switch to a larger operation frame (**AWBFRAM**:01[h]).

Using AWBAJST3 and AWBAJST4

-> AWBAJST3 is the operation frame offset in the R-B axis direction, and AWBAJST4 in R+B-2G axis direction. The plus direction (00[h] to 7F[h]) widens the operation frame.

8.8. Suppress

8.8.1. Chroma Suppress

The related parameters are as follows.

Table 8.8-1 Chroma Suppress Related Parameter

CAT	Byte	bit	Parameter Name	Description	Default
3 PICT	17	0 to 1	CSVLV	Chroma suppression amount when the V aperture correction level is detected 0: 0% 1: 25% 2: 50% 3: 100%	0
		2 to 3	CSVTH	V aperture correction level at which chroma suppress starts 0: 25% 1: 43.7% 2: 62.5% 3: 81.2%	1
		4 to 5	CSHLV	Chroma suppress amount when the luminance level is detected 0: 0% 1: 25% 2: 50% 3: 100%	0
		6 to 7	CSHTH	Luminance level at which chroma suppress starts 0: 75% 1: 81.2% 2: 87.5% 3: 93.7%	2
	3	0 to 3	VHAPG	Sets the gain after adding V and H aperture correction. 0: x0 -> 15: x4	6
		4 to 7	VHAPSL	Applies slice after adding V and H aperture correction. 0:sloce level 0 -> 15:slice level max	4

The following 3 parameters suppress the chroma signal level in accordance with the AGC gain.

When changing the settings by serial input, set CPU (CAT2-Byte 4-bit 3) to “1”.

Also, the changed settings must be written to the EEPROM before use. The new values are reflected the next time the system is booted.

The settings (start AGC CONT, end AGC CONT, end level) are changed using the SPEC CODE.

- CSPRSTA (CAT3-Byte 14) : Suppress start AGC CONT
- CSPREND (CAT3-Byte 15): Suppress end AGC CONT
- CSPRLV (CAT3-Byte 16) : Suppress end level

Table 8.8-2 CSPRSTA

CSPRSTA	Chroma SuPpReSs STArt level
Parameter category	CAT3 PICT, byte 14, bits 7 to0 (8 bits)
Outline	Chroma suppress start AGC CONT
Setting range	00[h] to FF[h]
Initial value	A0[h]
Description	
Notes	Do not set a value larger than CSPREND.

Table 8.8-3 CSPREND

CSPREND	Chroma SuPpReSs END level
Parameter category	CAT3 PICT, byte 15, bits 7 to 0 (8 bits)
Outline	Chroma suppress end AGC CONT
Setting range	00[h] to FF[h]
Initial value	D0[h]
Description	
Notes	Do not set a value smaller than CSPRSSTA.

Table 8.8-4 CSPRLV

CSPRLV	Chroma SuPpRess LeVel
Parameter category	CAT3 PICT, byte 16, bits 7 to 0 (8 bits)
Outline	Chroma suppress end suppress level
Setting range	00[h] to FF[h]
Initial value	8A[h]
Description	00[h]: Complete suppress, FF[h]: No suppress
Notes	

8.8.2. Aperture Correction Suppress

This suppresses the aperture correction level in accordance with the AGC gain.

When changing the settings by serial input, set CPU (CAT2-Byte 4-bit 1) to “1”.

Also, the changed settings must be written to the EEPROM before use. The new values are reflected the next time the system is booted.

The settings (start AGC CONT, end AGC CONT, end level) are changed using the SPEC CODE.

- ASPRSTA (CAT3-Byte 4) : Suppress start AGC CONT
- ASPREND (CAT3-Byte 5) : Suppress end AGC CONT
- ASPRLV (CAT3-Byte 6) : Suppress end level

Table 8.8-5 ASPRSTA

ASPRSTA	Apcon SuPpRess STArt level
Parameter category	CAT3 PICT, byte 4, bits 7 to 0 (8 bits)
Outline	Aperture correction suppress start AGC CONT
Setting range	00[h] to FF[h]
Initial value	AD[h]
Description	
Notes	Do not set a value larger than ASPREND.

Table 8.8-6 ASPRLV

ASPRLV	Apcon SuPpRess LeVel
Parameter category	CAT3 PICT, byte 6, bits 7 to 0 (8 bits)
Outline	Aperture correction suppress end suppress level
Conditions	
Setting range	00[h] to FF[h]
Initial value	00[h]
Description	00[h]: Complete suppress, FF[h]: No suppress
Notes	

Table 8.8-7 ASPREND

ASPREND	Apcon SuPpRess END level
Parameter category	CAT3 PICT, byte 5, bits 7 to 0 (8 bits)
Outline	Aperture correction suppress end AGC CONT
Setting range	00[h] to FF[h]
Initial value	D0[h]
Description	
Notes	Do not set a value smaller than ASPRSTA.

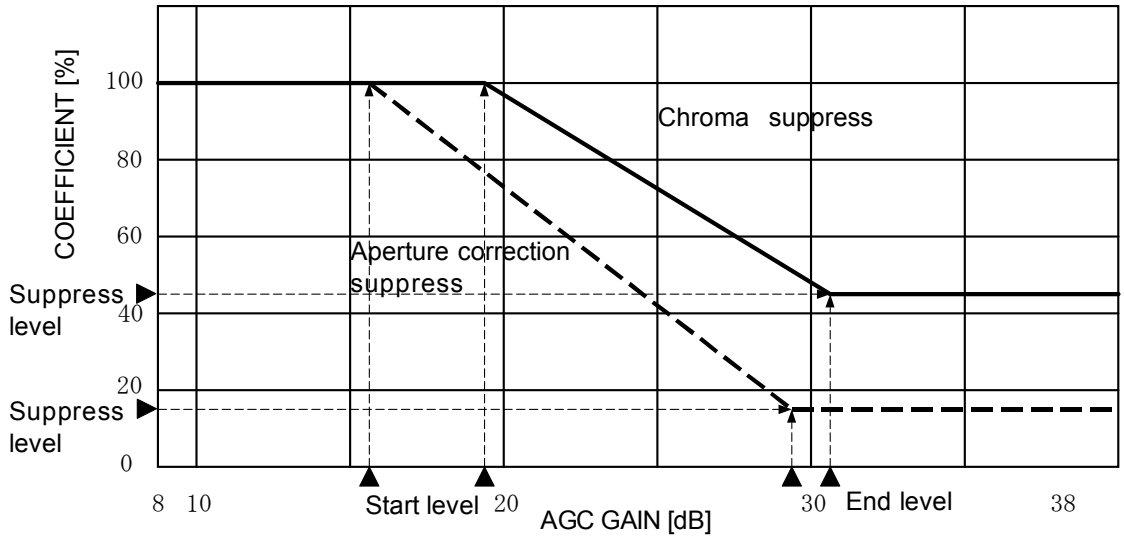


Fig. 8.8-1 Suppress Characteristics Diagram

8.8.3. The correlation figure of AGC and AGCCNT

When you set up a suppress start value and a suppress end value, please set up according to the following figure.

If it does not set up as follows, correlation of AGC and suppress cannot be taken. Consequently, suppression always operates and a suppression coefficient does not become 100%.

By the case when EVR5V is "0" and AGCMIN is "33[h]", since AGCCNT is set to "AA[h]", a suppress start value should be set up in a larger value than "AA[h]".

Suppress processing will be started when a value smaller than a suppress start value is set up.

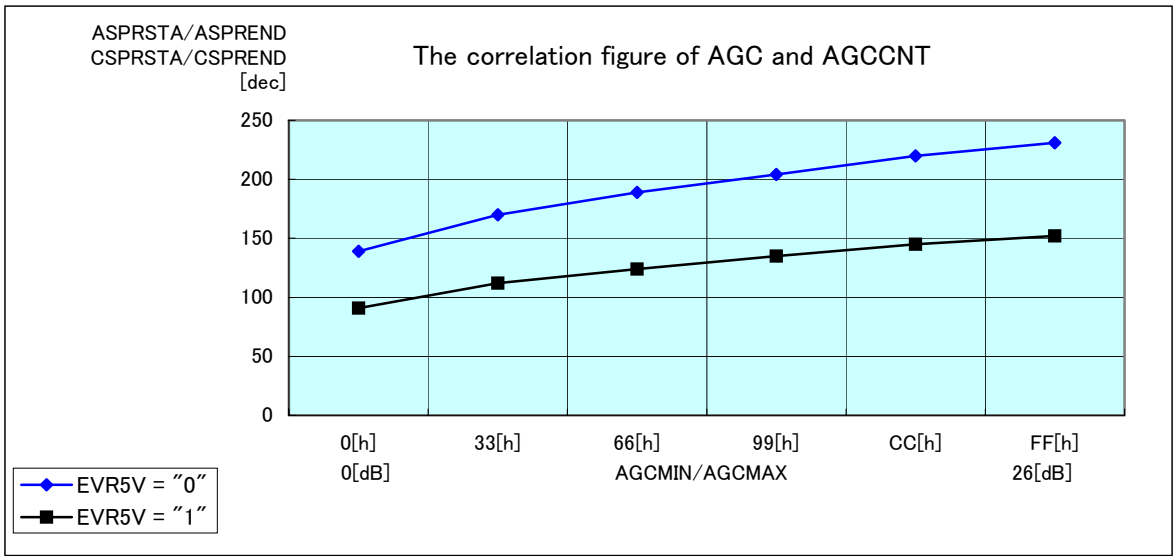


Fig. 8.8-2 The correlation figure of Suppress

9. Supporting Functions for Applications

9.1. External Sync (Line Lock Mode)

Line lock mode synchronizes the camera's vertical phase with the external VD signal input.

The external VD signal frequency is 60 [Hz] for NTSC and 50 [Hz] for PAL.

Table. 9.1-1 TV System and Power Supply Frequency

TV system	Line Lock Power Supply Frequency
NTSC	60 [Hz]
PAL	50 [Hz]

9.1.1. System Configuration

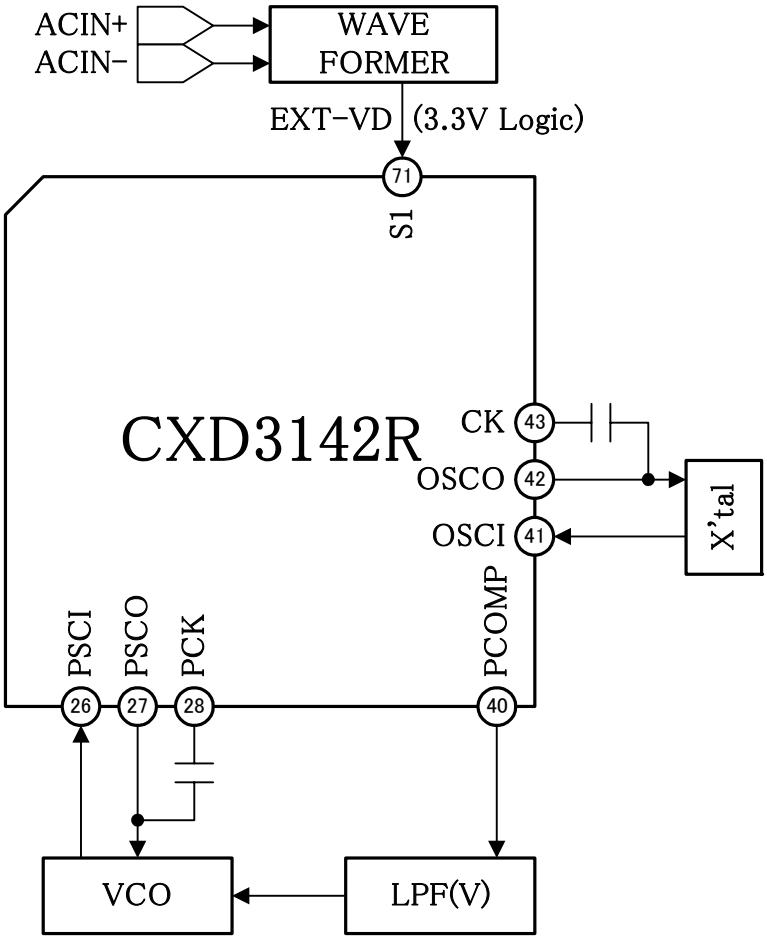


Fig. 9.1-1 LL Mode System configuration

In addition to the external VD signal, the following two clocks are necessary.

(1) CK (Pin 43): This clock is crystal oscillation, and is a fixed frequency with the same circuit as INT mode. (See "Fig. 3.1-1 Oscillator Circuit Configuration in Internal Sync Mode".)

NTSC: 19.06993 [MHz], PAL: 18.9375 [MHz]

(2) PCK (Pin 28): This clock is generated by the PLL and has a center frequency of 19 [MHz]. It should be synchronized to the external VD signal fluctuation of approximately +/- 1 [Hz].

An external LPF and VCO are required to configure the PLL. Note that the CXD3142R also includes a VCO oscillation cell (input PSCI (Pin 26), output PSCO (Pin 27)).

See "Fig. 9.1-5 Example of Ext-VD Wave-former" under " 9.1.6. Application Circuits" for the LPF and VCO configurations.

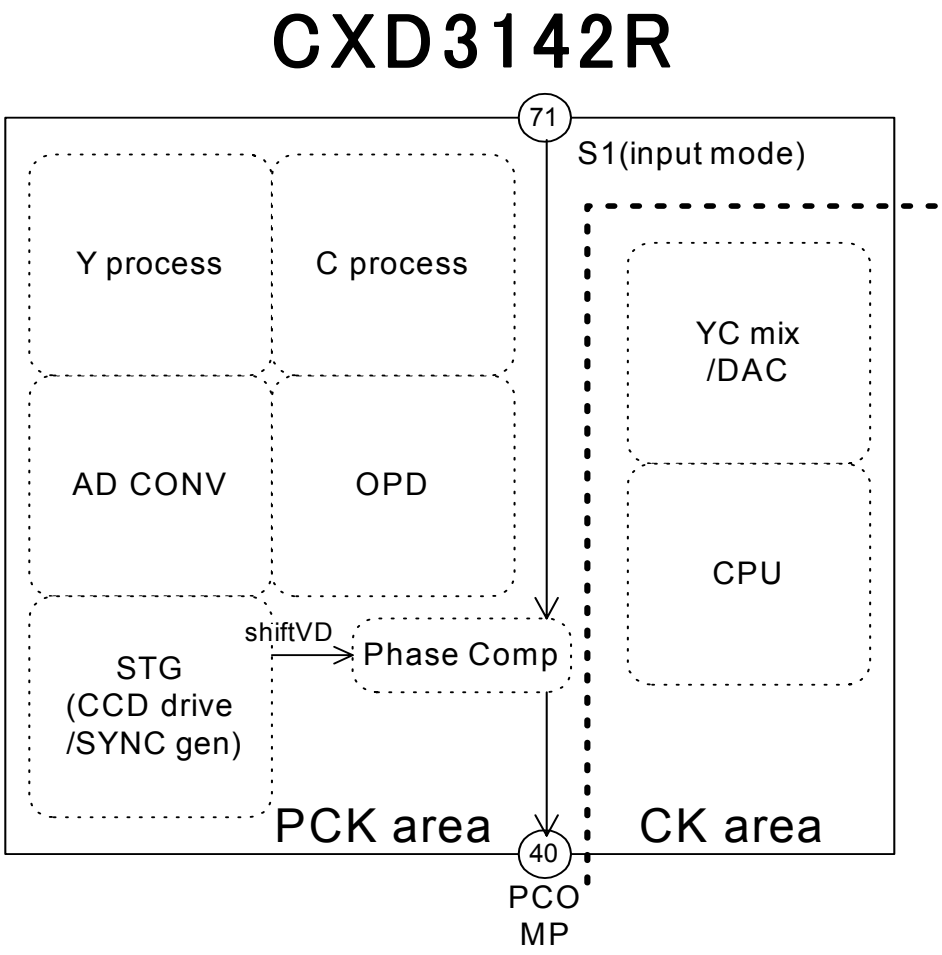


Fig. 9.1-2 LL Mode 2Clocks Block Diagram

9.1.2. System Description

CK (crystal oscillation) is used in the YCmix and CPU blocks, and maintains both a stable subcarrier frequency and the serial communication speed.

Other blocks operate at PCK (PLL generation) to ensure synchronization with the external VD signal.

The PLL master signal is the external VD signal (3.3 V rectangular waveform). PCK is generated by phase comparing the internally frequency-divided VD signal (shift VD) and the external VD signal inside the CXD3142R, and the results are output on PCOMP (CXD3142R Pin 40). The V direction PLL is configured by applying the PCOMP signal to the LPF(V) and applying feedback to the VCO for PCK generation.

A VCO incorporating a LC oscillator and varicap (variable capacitance diode) is generally used to ensure a wide PCK modulation range.

Also, the system parameters must be set by EEPROM write or serial communication as described hereafter.

The SS-11RM system does not have an external sync auto identification function.

9.1.3. External Input Signal

The external VD signal must be input to S1 (CXD3142R Pin 71).

S1 (Pin 71) can be switched to an input port by setting ESMODE (CAT1-Byte 6-bit 0) to 1 (Line lock mode).

The external VD signal should be a 3.3 [Vp-p] pulse wave (digital signal).

There are no restrictions concerning the duty, but the low period should be 4 x 105 [ns] (min.).

Also, when using an analog AC sine wave as the input signal, form a pulse before input.

(See "9.1.6. Application Circuits (Peripheral Circuits for External Sync)".)

9.1.4. Internal Phase Comparator

Edge trigger phase comparator (PCOMP output)

This phase comparator is an edge trigger-type device which performs phase comparison at the falling edges of the external VD and shift VD signals. This comparator is used for phase comparison in the V direction.

The result of the phase comparison is output from PCOMP (CXD3142R Pin 40).

The LPF including a PLL supports both a passive filter and active filter.

Select the LPF, and then use the serial communication data CMPINV (CAT1-Byte 4-bit 4) setting to switch the polarity of the PCOMP signal.

The initial setting value during power-on for the CXD3142R is:

CMPINV = 0 [Active filter setting].

Table. 9.1-2 LPF Type and PCOMP Output Polarity Settings

LFP type	Serial communication data settings CMPINV (CAT1-Byte 4-bit 4)	PCOMP (CXD3142R 40pin) output Shift VD signal phase relative to external VD signal	
		Forward	Backward
Passive filter	0	L (GND)	H (3.3V)
Active filter	1	H (3.3V)	L (GND)

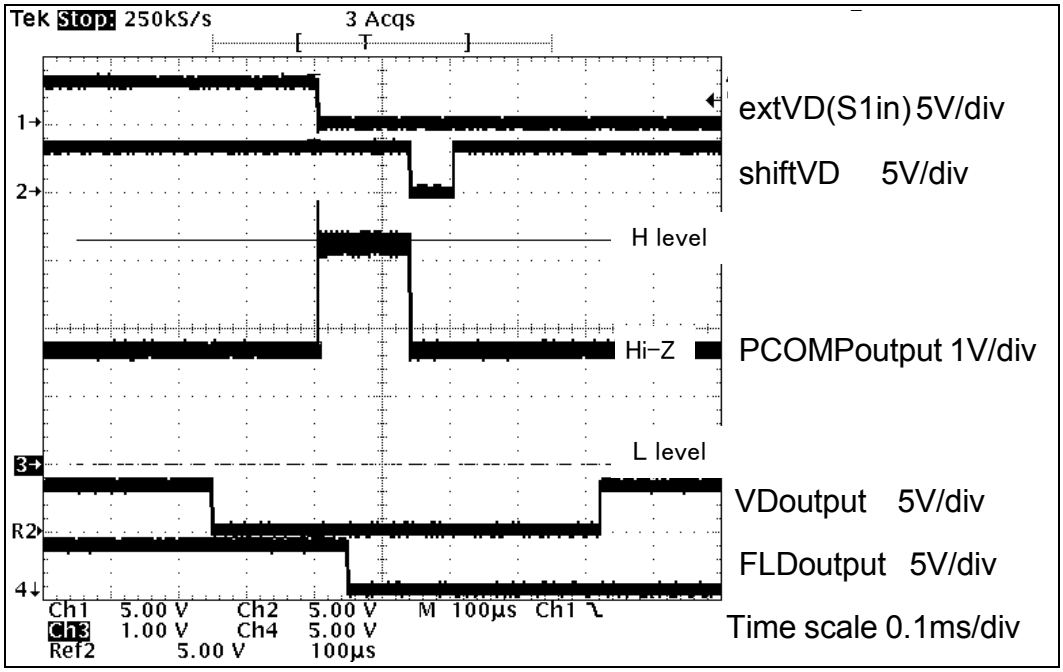


Fig. 9.1-3 PCOMP waveforms (zoom up) CMPINV = 0

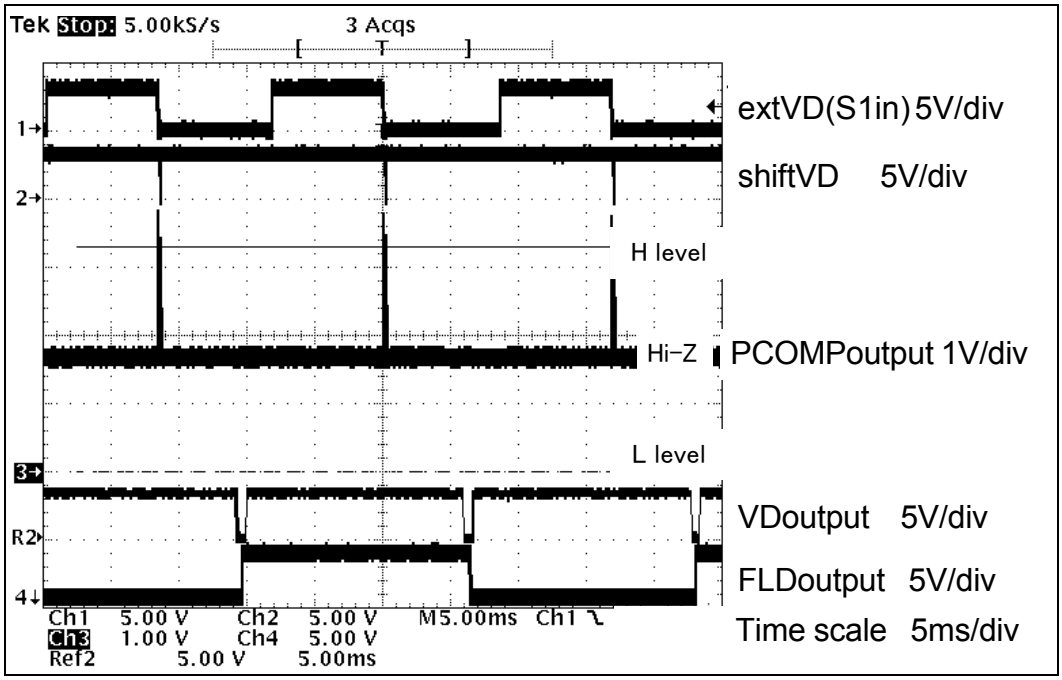


Fig. 9.1-4 PCOMP waveforms with PLL lock-on

9.1.5. Line Lock Mode Settings

An example of the line lock mode settings is given below.

For a detailed description of each parameter, see "9.1.8. External Sync Parameter Reference".

1. Set the following parameters in the CXD3142R by EEPROM write or serial communication, etc.
   <Related parameter settings>
   ESMODE (CAT1-Byte 6-bit 0) = 1 (Line Lock)
   CMPMODE (CAT1-Byte 6-bit 2) = 1 (VCOMP mode)
   * The above settings switch S1 (Pin 71) to an input port.
   Note that S1 (Pin 71) is an output port in internal mode.
   Passive filter/active filter (inverted) switching is performed by **CMPINV** (CAT1-Byte 6-bit 4) = 0 or 1, respectively.

2. Input the 3.3 [Vp-p] pulse-formed external VD signal to S1 (Pin 71).
3. This sets the line lock mode, and operation is synchronized with the external VD signal.

<Reference> Shift VD signal

When a shift VD signal is required inside the CXD3142R to check phase comparison operation, this signal can be output from S0 (Pin 70) or S2 (Pin 72). Set the parameters as follows.

SSHIFT (CAT1-Byte 7-bit 3) = 1 (shift-VD selected)

S2SEL (CAT1-Byte 7-bits 7 and 6) = 10b (S2 set to shift-VD output)

* The shift VD signal output when SSHIFT = 1 is in-phase with the internal counter, and also has the same phase as the PCOMP (Pin 40) output.
  Also, note that the shift-VD pulse width is narrow at approximately 1 HD interval.
  When SSHIFT = 0, the normal VD signal having the same phase as the video output is output. This signal has a phase difference from the PCOMP output signal.

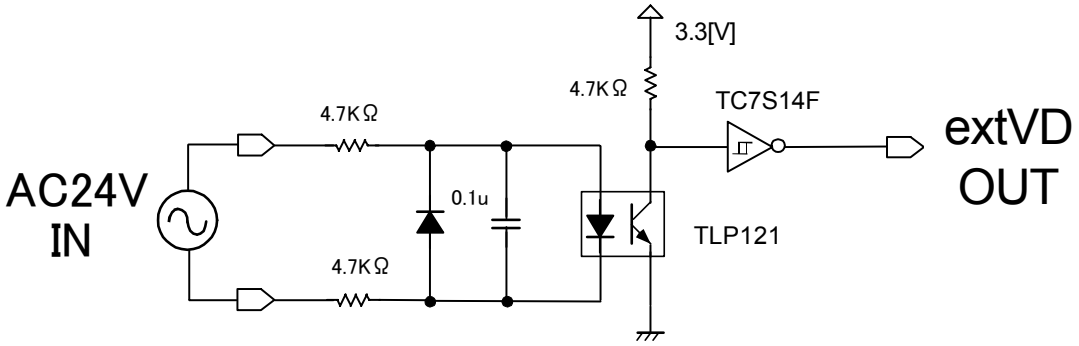
9.1.6. Application Circuits (Peripheral Circuits for External Sync)

Example application circuits are shown below for the external VD pulse forming circuit (wave-former), LPF(V) and VCO that are required when configuring external sync (line lock) in the SS-11RM system.

<Note>

Operation with these circuits has been confirmed on a Sony evaluation board. However, note that the PLL stability and the lock range differ significantly according to the electrical and temperature characteristics of the parts used and the layout on the board, so circuits noted herein are for reference purposes only, and Sony does not guarantee operation for these circuits.

When applying these circuits to an actual set, users are requested to confirm PLL stability (jitter), supply voltage fluctuation and temperature fluctuation.



NTSC 60[Hz]
PAL 50[Hz]

Fig. 9.1-5 Example of Ext-VD Wave-former

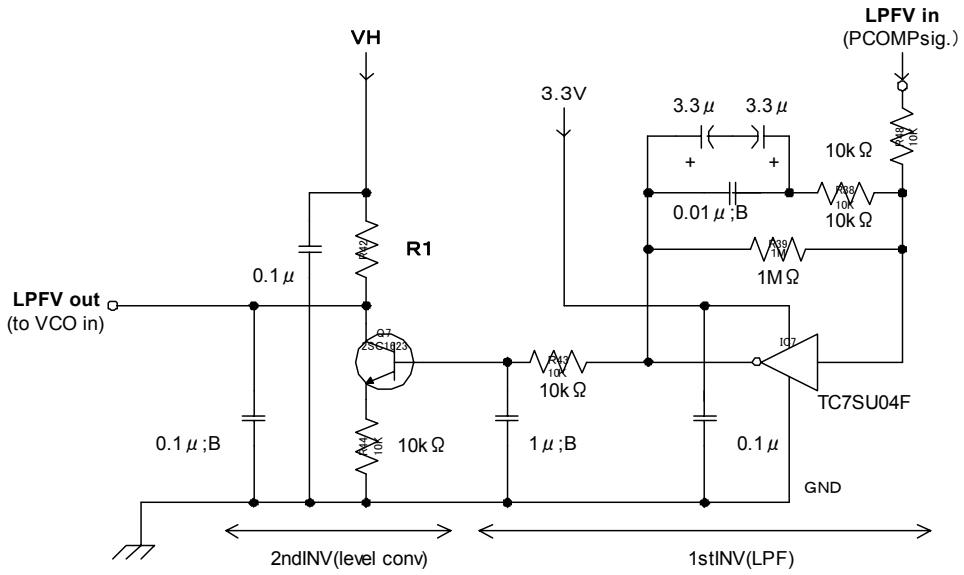


Fig. 9.1-6 Example of LPFV (CXD3142REVB/Double-inverter amplifier)

*These circuits are for both NTSC (60 [Hz]) and PAL (50 [Hz]). However, the system power supply VH differs according to the CCD type, so the R1 resistance value should be adjusted as follows.

Table. 9.1-3 CCD Type, VH Voltage, LPFV R1 Constant and Output Voltage Range

CCD type	VH supply voltage	R1 resistance value	LPFV output range
ICX404/405	15 [V]	56 [k ohm]	+2 to 15 [V]
ICX226/227	12 [V]	47 [k ohm]	+2 to 12 [V]

The static characteristics when DC voltage is applied to the LPFV in of the discrete LPFV (with the PCOMP signal separated from the LPFV) are as shown in “” Double-inversion is performed using an active filer and the rear-end inverter for DC level conversion.

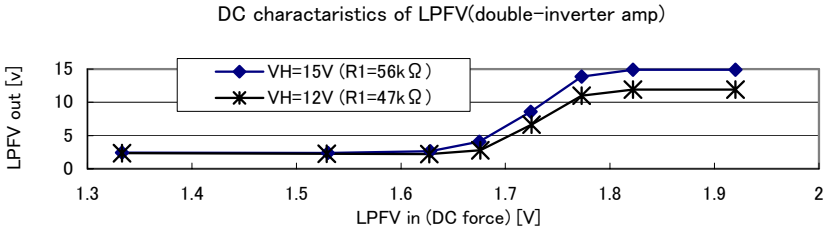


Fig. 9.1-7 Static DCin-out Characteristics of LPFV

“”shows the VCO applied to the Sony evaluation board CXD3142REVB (SS-140B board).

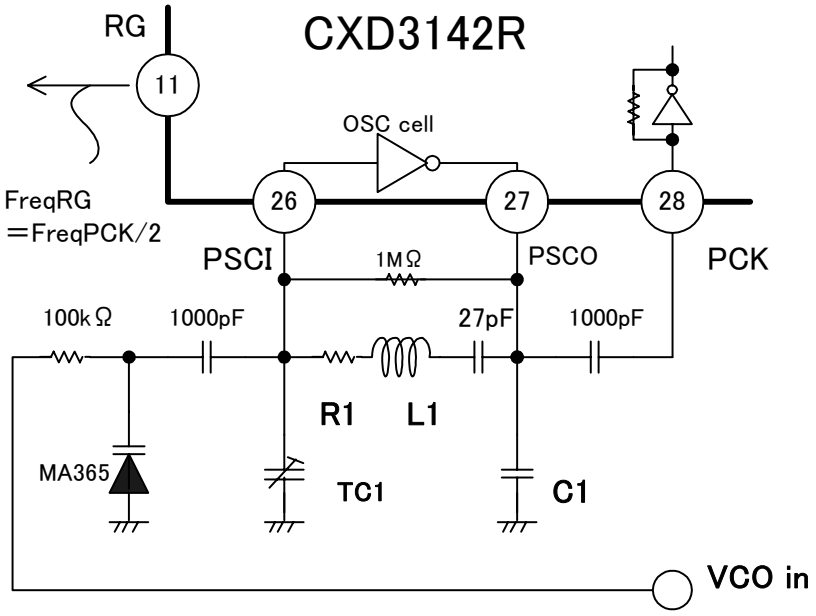


Fig. 9.1-8 Example of VCO (CXD3142REVB)

The VCO center frequency is 19 [MHz] for both NTSC and PAL, but VCOin (= LPFVout) differs according to the CCD type, so the part constants in the following table should be adjusted accordingly. TC1 adjusts the VCO variable range (= PLL lock range) with a semi-fixed trimmer.

Table. 9.1-4 CCD Type, VH Voltage and VCO Part Constants

CCD type	VH voltage	VCOin range	TC1	R1	L1	C1
ICX404/405	15 [V]	+2 to 15[V]	20 [pF] trimmer	10 [ohm]	5.6 [uH]	6 [pF]
ICX226/227	12 [V]	+2 to 12[V]	10 [pF] trimmer	47 [ohm]	6.8 [uH]	4 [pF]

The electrical characteristics of the parts used also have a significant effect on the VCO performance. The Sony evaluation board used the high-frequency inductor shown in the table below for L1.

Table. 9.1-5 Parts Used on the Sony Evaluation Board (Inductor L1)

L1 constant	Manufacturer	Part model name	Shape	Self Q	Self resonance frequency
5.6 [uH]	Taiyo Yuden Inc.	LAL03NA5R6K	axial lead	50	48 [MHz]
6.8 [uH]	Taiyo Yuden Inc.	LAL03NA6R8K	axial lead	50	37 [MHz]

"Fig. 9.1-9" shows the measurement values of the discrete VCO characteristics (output frequency variation with LPFVout separated from VCOin and DV applied) when testing the PLL on the Sony evaluation board. However, note that in order to avoid the effects of the probe capacitance, VCOout was not measured directly, and instead the RG (Pin 11) output pulse frequency which corresponds to 1/2 the VCOout frequency was measured.

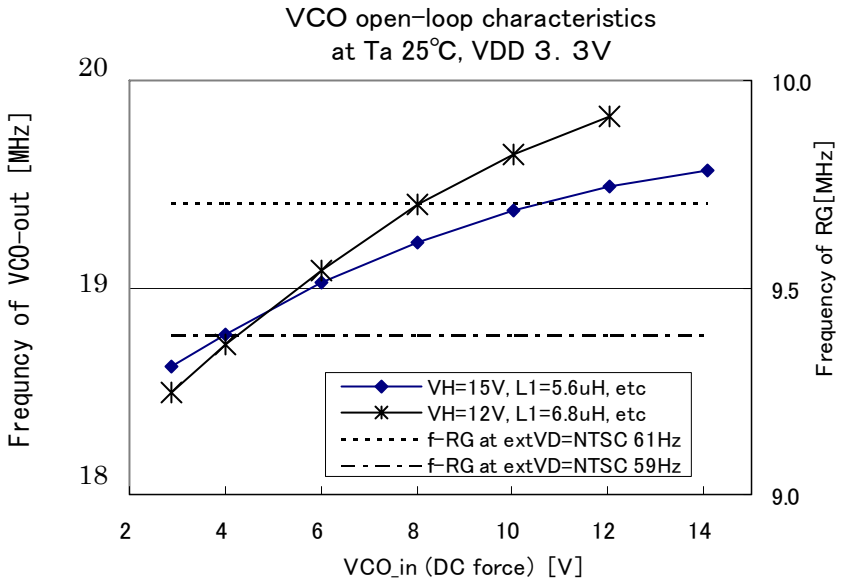


Fig. 9.1-9 Measured values of VCO (CXD3142REVB/Open-loop)

9.1.7. Shift Function

In external sync mode, the V phase can be changed by **SFTUP** (CAT2-Byte 7-bit 5) and **SFTDWN** (CAT2-Byte 7-bit 6). Also, the phase shift speed can be adjusted by **SFTSPED** (CAT7-Byte 10-bits 4 to 6).

Shift function related parameters

1. Shifter value

   The V phase is shifted by setting data in **SFTVM** and **SFTVL** (total 9 bits) below.

   SFTVM (CAT7-Byte 10-bit 2): shift-V MSB, 1 bit

   SFTVL (CAT7-Byte 9-bits 7 to 0): shift-V LSB, 8 bits

   Note: The setting range for these parameters are as follows.

   Operation is not guaranteed for data settings outside this range.

   NTSC: 1[h] to 105[h]

   PAL: 1[h] to 137[h]

2. Shift up/down

   The respective shift operations are performed by setting SFTUP (CAT2-Byte 7-bit 5) and SFTDWN (CAT2-Byte 7-bit 6) as shown in "Table. 9.1-6 Shift Up/Down Parameters".

Table. 9.1-6 Shift Up/Down Parameters

Shift operation	SFTDWN	SFTUP
No shift operation (stop)	0	0
SHIFT UP	0	1
SHIFT DOWN	1	0
Shifter value reset to 1	1	1

<Shift operations>

・ No shift operation (stop)

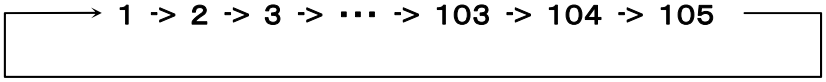
Shift up/down operation stops when this mode is set.

No other operation is performed.

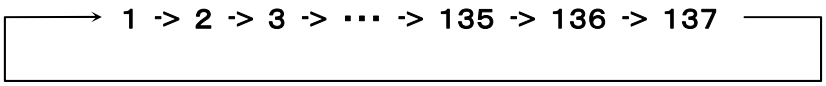
・ SHIFT UP

SFTVM and **SFTVL** (total 9 bits) change as shown in the figure below (hexadecimal notation).

NTSC:



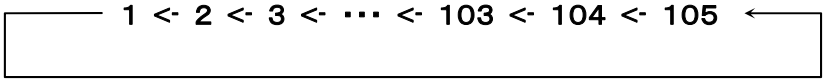
PAL:



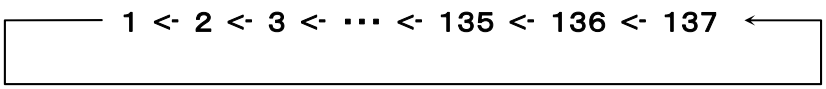
・ SHIFT DOWN

SFTVM and **SFTVL** (total 9 bits) change as shown in the figure below (hexadecimal notation).

NTSC:



PAL:



・ Shifter value reset to 1

SFTVM and **SFTVL** (total 9 bits) are forcibly reset to 1.

3. Shift speed

   The up/down speed when performing continuous shift up/down operation can be adjusted by **SFTSPED** (CAT7-Byte 10-bits 6 to 4).

   0: Up/down at 1-field intervals
   1: Up/down at 2-field intervals
   to
   7: Up/down at 8-field intervals

Shifter value data setting method

1. Setting by DIP switches

   Optional DIP switches can be assigned to **SFTUP** (CAT2-Byte 7-bit 5) and **SFTDWN** (CAT2-Byte 7-bit 6), and shift up/down operation can be performed by setting the parameters using these DIP switches.

2. Setting by PC control software

   Shift up/down can be performed by setting data in **SFTUP** (CAT2-Byte 7-bit 5) and **SFTDWN** (CAT2-Byte 7-bit 6) using SS-11RM compatible PC control software, or by setting data directly in **SFTVM** (CAT7-Byte 10-bit 2) and **SFTVL** (CAT7-Byte 9-bits 7 to 0).

   At this time, care should be taken for the following point.

   Note: The setting range for these parameters are as follows.
   Operation is not guaranteed for data settings outside this range.
   NTSC: 1[h] to 105[h]
   PAL: 1[h] to 137[h]

9.1.8. External Sync Parameter Reference

Table. 9.1-7 ESMODE

ESMODE	External Sync MODE
Category/Byte	CAT1 SYSCON, byte 6, bit 0 (1 bit)
Outline	Selects internal or external sync.
Setting range	0(b) to 1 (b)
Initial value	0[h]: Internal sync
Description	Each mode is selected by the following settings. 0: Internal sync, 1: External sync
Notes	

Table. 9.1-8 CMPMODE

CMPMODE	CoMParator Mode
Category/Byte	CAT1 SYSCON, byte 6, bit 2（1 bit）
Outline	Selects the phase comparator operating mode.
Setting range	0(b) to 1 (b)
Initial value	0(b): PCOMP output not used
Description	Each mode is selected by the following settings. 0: PCOMP output not used, 1: PCOMP output used
Notes	Set to 1(b) when using external sync.

Table. 9.1-9 CMPINV

CMPINV	PCOMP ref/var INVerse
Category/Byte	CAT1 SYSCON, byte 6, bit 4（1 bit）
Outline	Selects the LPF and phase comparison signal (PCOMP output polarity.
Setting range	0(b) to 1 (b)
Initial value	0(b): Passive filter
Description	This switches between 0(b): Passive filter and 1(b): Active filter (inverted).
Notes	

Table. 9.1-10 SFTVM

SFTVM	ShiFTer V Msb
Category/Byte	CAT7 TIMING, byte 10, bit 2（1 bit）
Outline	Shifter V data (9 bits), MSB 1 bit
Setting range	0[h] to 1[h] * See note
Initial value	0[h]
Description	This represents the upper 1 bit of the shifter V data (9 bits).
Notes	Operation is not guaranteed outside the following shifter V data (9 bits) range. NTSC: 1[h] to 105[h] PAL: 1[h] to 137[h]

Table. 9.1-11 SFTVL

SFTVL	ShiFTer V Lsb
Category/Byte	CAT7 TIMING, byte 9, bits 7 to 0（8 bits）
Outline	Shifter V data (9 bits), LSB 8 bit
Setting range	00[h] to FF[h] * See note
Initial value	00[h]
Description	This represents the lower 8 bits of the shifter V data (9 bits).
Notes	Operation is not guaranteed outside the following shifter V data (9 bits) range. NTSC: 1[h] to 105[h] PAL: 1[h] to 137[h] Therefore, note that when SFTVM is 0[h], setting SFTVL to 0[h] results in a value outside the setting range.

Table. 9.1-12 SFTUP

SFTUP	ShiFTer UP
Category/Byte	CAT2 CPU, byte 7, bit 5 (1 bit)
Outline	Changes (up) the shifter V data.
Setting range	0(b) to 1 (b)
Initial value	0[h]
Description	Operation is performed in combination with SFTDWN as shown in "Table. 9.1-6 Shift Up/Down Parameters".
Notes	

Table. 9.1-13 SFTDWN

SFTDWN	ShiFTer DoWN
Category/Byte	CAT2 CPU, byte 7, bit 6 (1 bit)
Outline	Changes (down) the shifter V data.
Setting range	0[h] to 1 [h]
Initial value	0[h]
Description	Operation is performed in combination with SFTUPas shown in "Table. 9.1-6 Shift Up/Down Parameters".
Notes	

9.2. Digital Out

9.2.1. Setting Method

Table. 9.2-1 OUTMODE

CAT	Byte	bit	Parameter name	Description
1 SYSCON	1	4, 5	OUTMODE	0x : Analog 1x : Analog and Digital

9.2.2. Format

A digital signal is output from CXD3142R Pins 61 to 68 by setting OUTMODE = 1x[b] (“Table. 9.2-1 OUTMODE”).

This signal is output synchronized to the CK clock (Pin 43) with the YUV signals multiplexed. The Y signal is binary data, and the UV signal is Offset Binary data.

9.2.3. Timing Chart – NTSC

*The CCD active pixel area output timing relative to VD and HD is shown below.

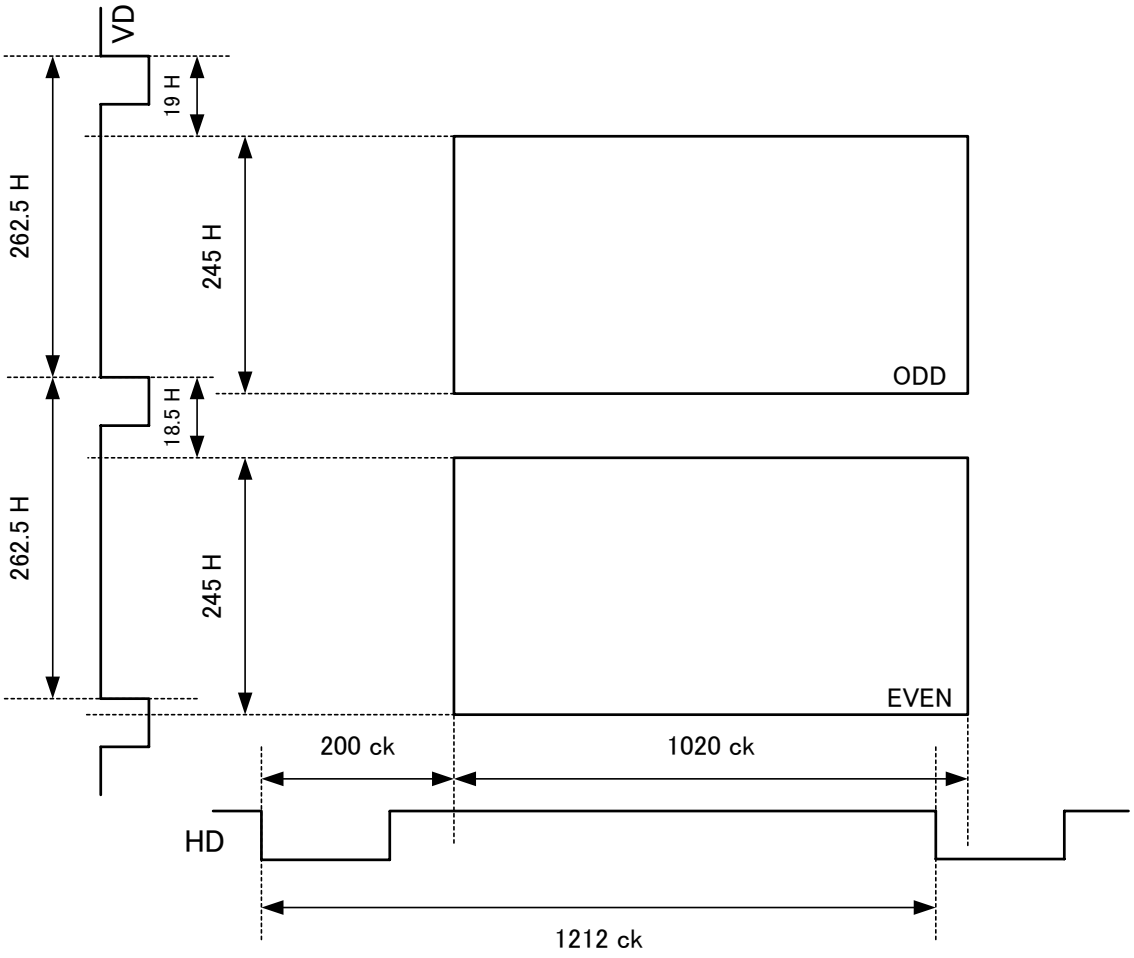


Fig. 9.2-1 Output timing of a CCD effective pixel domain to DV and HD –NTSC-

*The CCD active pixel area output timing relative to each sync signal is shown below.

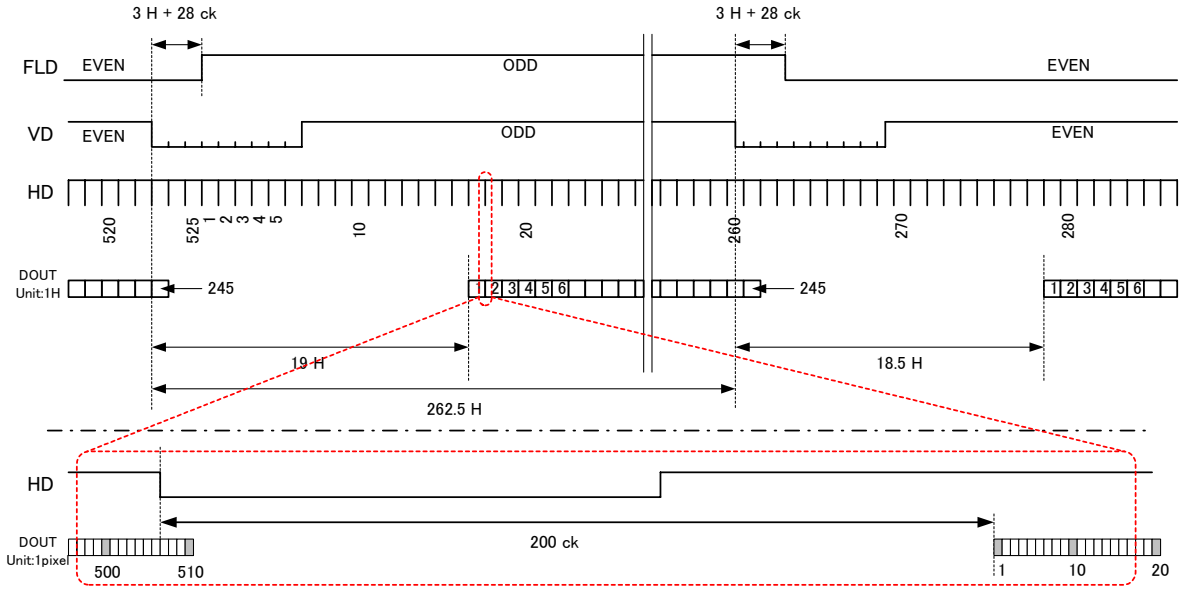


Fig. 9.2-2 Output timing of a CCD effective pixel domain to each synchronized signal -NTSC-

*The Digital Out sequence output timing relative to each sync signal is shown below.

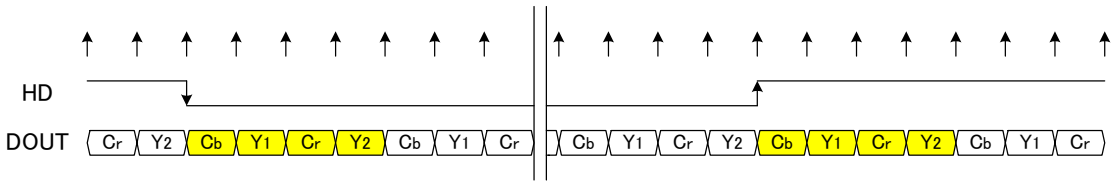


Fig. 9.2-3 Output timing of the digital out sequence to each synchronized signal -NTSC-

9.2.4. Timing Chart – PAL

*The CCD active pixel area output timing relative to VD and HD is shown below.

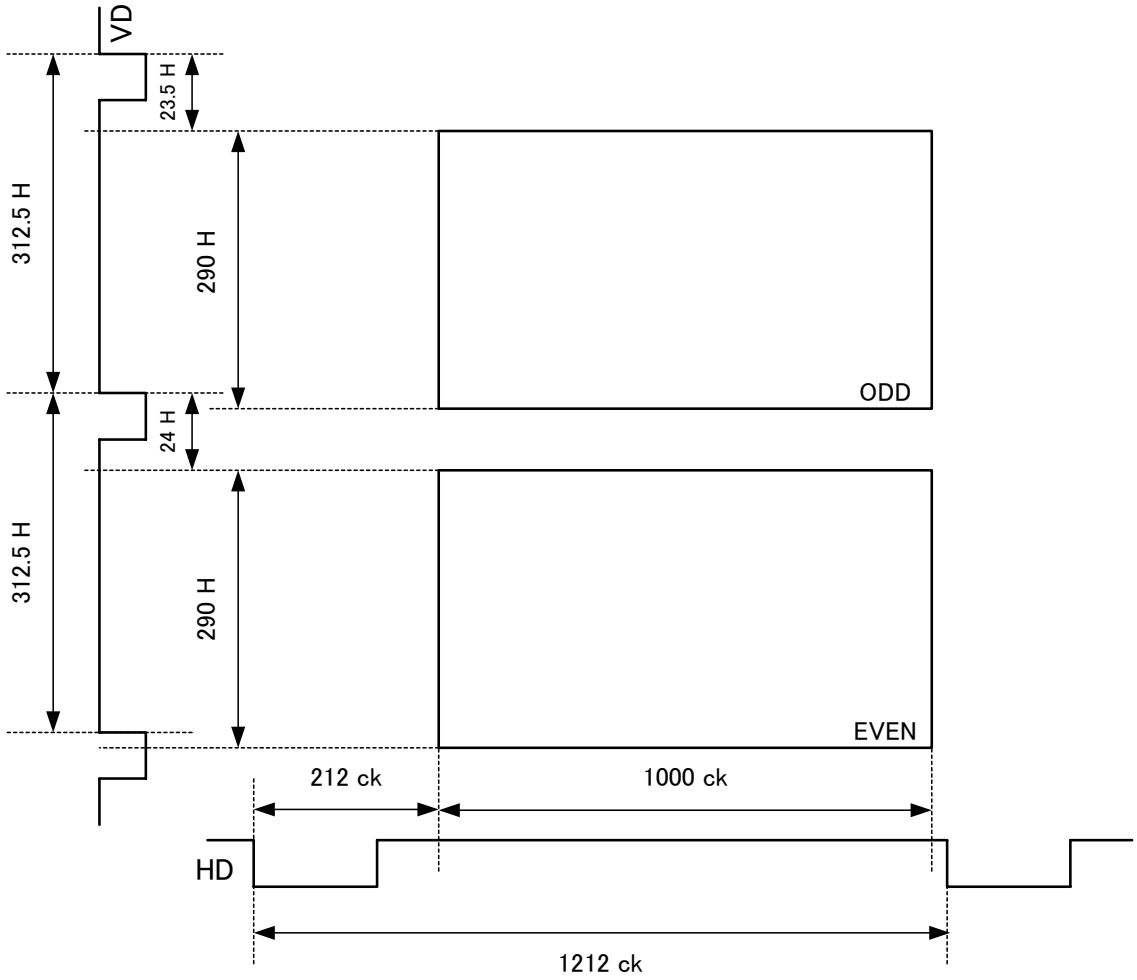


Fig. 9.2-4 Output timing of a CCD effective pixel domain to DV and HD –PAL-

*The CCD active pixel area output timing relative to each sync signal is shown below.

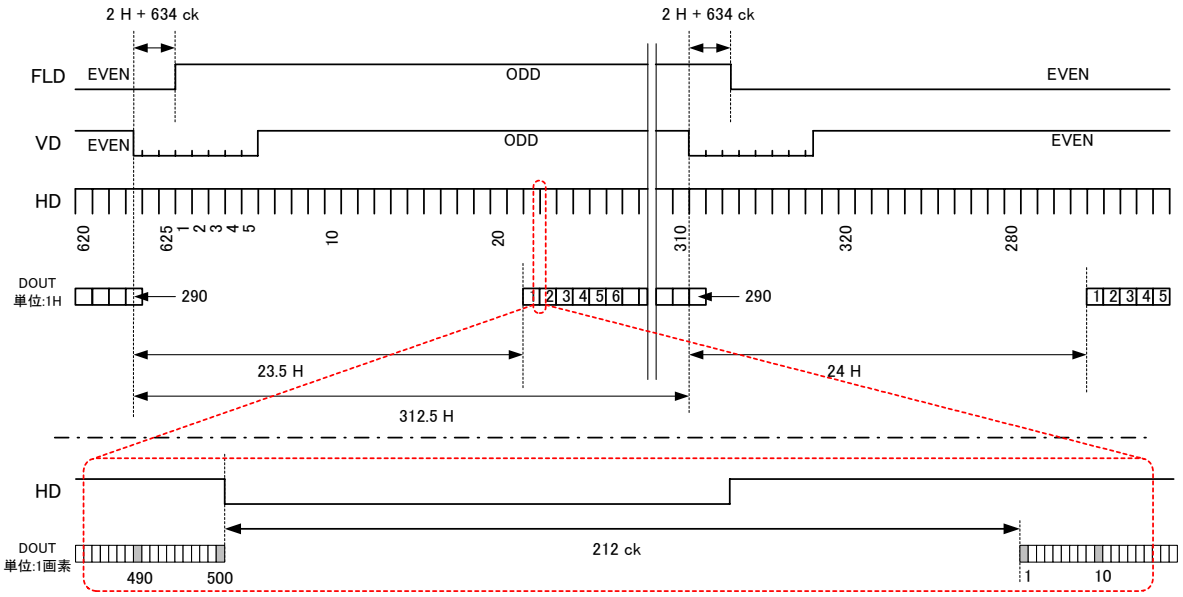


Fig. 9.2-5 Output timing of a CCD effective pixel domain to each synchronized signal -PAL-

*The Digital Out sequence output timing relative to each sync signal is shown below.

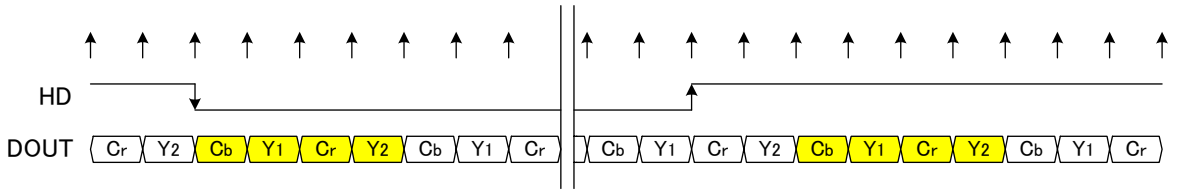


Fig. 9.2-6 Output timing of the digital out sequence to each synchronized signal -PAL-

9.2.5. Output signal D range

*Y signal D range

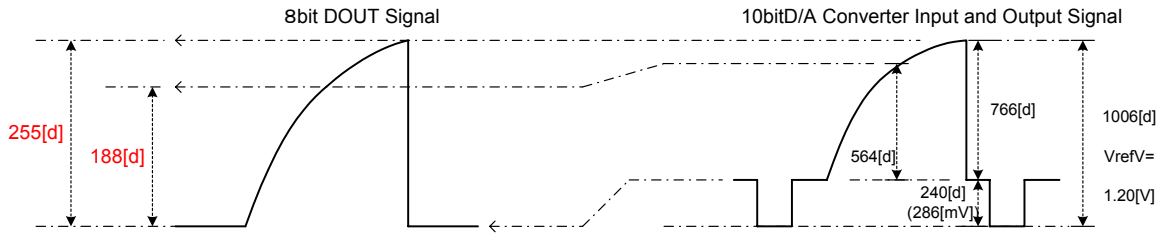


Fig. 9.2-7 Y signal D range

*C signal D range

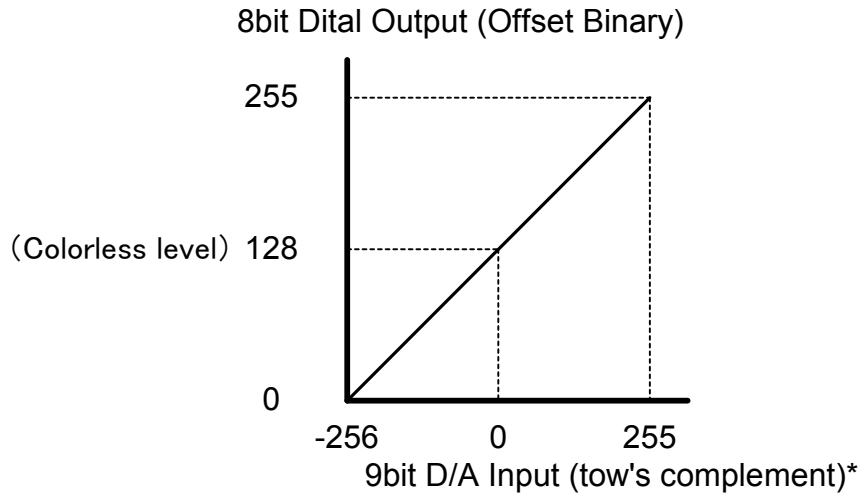


Fig. 9.2-8 C signal D range

10. Useful Functions for Line Adjustment

10.1. Blemish Compensation

Spot blemishes are one type of pixel blemish. Spot blemish standards have been implemented for Sony CCDs, and CCDs are sorted according to these standards during the production stage. However, in the case of white spot blemishes, which are one type of spot blemish, the blemish level differs in proportion to the temperature, and these blemishes sometimes become observable due to external causes and particularly in case of high temperatures. This blemish compensation function makes it possible to maintain the picture quality by performing a simple operation.

The CXD3142R has a blemish compensation function that compensates for blemish CCD pixels by means of the average value of two adjacent pixels of the same color in the horizontal direction. The horizontal/vertical direction address data of the blemish (marker) can be set using the marker function described below. By writing the address data for the blemish position to the EEPROM, this address data is automatically loaded and blemish compensation operation performed when the system is reset thereafter.

10.1.1. Compensation

Compensation is possible for up to 2 points. The compensation position is set by serial communication data for both the horizontal and the vertical directions. 1-pixel compensation or 2-pixel continuous compensation can be performed for each of the points to be compensated.

When this function is not used, all the parameters in the table should be set to 0[h].

10.1.2. Setting method

Table. 10.1-1 Compensation Address Setting Method

	Serial communication data	Setting value
Horizontal position of compensation 1	DEF1H (CAT7-Byte 11, Byte 13-bits 0 and 1)	See “Table. 10.1-2”
Vertical position of compensation 1	DEF1V (CAT7-Byte 12, Byte 13-bits 2 and 3)	See “Table. 10.1-2”
Continuous 2-pixel compensation of compensation 1	DEF1L (CAT7-Byte 13-bit 4)	0: 1-pixel compensation 1: 2-pixel compensation
Horizontal position of compensation 2	DEF2H (CAT7-Byte 14, Byte 16-bits 0 and 1)	See “Table. 10.1-2”
Vertical position of compensation 2	DEF2V (CAT7-Byte 15, Byte 16-bits 2 and 3)	See “Table. 10.1-2”
Continuous 2-pixel compensation of compensation 2	DEF2L (CAT7-Byte 16-bit 4)	0: 1-pixel compensation 1: 2-pixel compensation

Table. 10.1-2 Setting Range in Horizontal/Vertical Directions

TV system	CCD mode	Setting range	
		Horizontal direction	Vertical direction
NTSC	510H	6F[h] to 25D[h]	11[h] to 101[h]
PAL	510H	77[h] to 25D[h]	16[h] to 134[h]

10.1.3. Marker function

Indicates the position for compensation on the screen. This function can be used to confirm the position for compensation on the screen. Display the marker, change the horizontal direction/vertical direction setting values and confirm the position for compensation.

Table. 10.1-3 Marker Display Function

	Serial communication data	Setting value
Marker display	DEFMK (CAT7-Byte 1-bit 3)	0: Compensation 1: Marker display

Note on blemish compensation!

When using this blemish compensation function, it should be used as the final adjustment item. Blemish compensation operation is performed by writing the parameters to the EEPROM.

11. Appendix

11.1. EEPROM Address and Read Address

11.1.1. CAT1(SYSTEM)

Name	CAT	Byte	Bit	Initial	Address	
					EEPROM	Reg.
NTPAL	1	1	0	0	01h	290h
OCCF			1	0		
OUTMODE			4, 5	1		
DLYH		2	0, 1	0	02h	291h
DTYH			2, 3	0		
DLRYG			4, 5	0		
DTYRG			6, 7	0		
IRLESS		3	0	0	03h	292h
VIDEOAE			1	1		
ADCKSEL			2, 3	0		
OPBCKINV			6	0		
S2DLY		4	5, 6	0	04h	293h
SPINSW		5	7	0	05h	294h
ESMODE		6	0	0	06h	295h
CMPMODE			2	0		
CMPINV			4	0		
S0SEL		7	0, 1, 2	0	07h	296h
SSHIFT			3	0		
S1SEL			4, 5	0		
S2SEL			6, 7	0		

11.1.2. CAT2 (CPU)

Name	CAT	Byte	Bit	Initial	Address	
					EEPROM	Reg.
NORMFL	2	5	0	1	08h	224h
LIMFL			1	0		
SFIXFL			2	0		
LAEFL1			3	0		
LAEFL2			4	0		
LAWBFL			6	0		
AEME		6	0	0	09h	225h
MIRIS			1	0		
BLCOFF			2	0		
AEREF			3	0		
AGCMAX			4	0		
SHTFIX			5	0		
AESHUT			6	0		
AWB		7	0, 1, 2	0	0Ah	226h
SFTUP			5	0		
SFTDWN			6	0		
P0CB		8	0 to 7	46h	0Bh	227h
P0M		9	0 to 7	00h	0Ch	228h
P1CB		10	0 to 7	46h	0Dh	229h
P1M		11	0 to 7	01h	0Eh	22Ah
P2CB		12	0 to 7	46h	Fh	22Bh
P2M		13	0 to 7	20h	10h	22Ch
P3CB		14	0 to 7	46h	11h	22Dh
P3M		15	0 to 7	04h	12h	22Eh
P4CB		16	0 to 7	46h	13h	22Fh
P4M		17	0 to 7	05h	14h	230h
P5CB		18	0 to 7	47h	15h	231h
P5M		19	0 to 7	00h	16h	232h
P6CB		20	0 to 7	47h	17h	233h
P6M		21	0 to 7	01h	18h	234h
P7CB		22	0 to 7	47h	19h	235h
P7M		23	0 to 7	02h	1Ah	236h

11.1.3. CAT3 (PICT)

Name	CAT	Byte	Bit	Initial	Address	
					EEPROM	Reg.
HAPGL	3	1	0, 1	3	1Bh	297h
HAPGH			2, 3	1		
YLPFSW			4	0		
GAMSW			6	0		
VAPG		2	0 to 3	0Ah	1Ch	298h
VAPSL			4, 5, 6	2		
VHAPG		3	0 to 3	6	1Dh	299h
VHAPSL			4 to 7	4		
ASPRSTA		4	0 to 7	A0h	1Eh	29Ah
ASPREND		5	0 to 7	D0h	1Fh	29Bh
ASPRLV		6	0 to 7	0	20h	29Ch
YGAIN		7	0 to 7	5Ah	21h	29Dh
SETUP		8	0～3	Dh	22h	29Eh
WCLIP			4, 5, 6	5		
BSTLV		9	0 to 4	NT=12h / PAL=13h	23h	29Fh
BSTINV			5	1		
MIRROR			7	0		
RYGAIN		10	0 to 7	2Fh	24h	2A0h
BYGAIN		11	0 to 7	1Ch	25h	2A1h
RYHUE		12	0 to 7	FFh	26h	2A2h
BYHUE		13	0 to 7	FEh	27h	2A3h
CSPRSTA		14	0 to 7	A0h	28h	2A4h
CSPREND		15	0 to 7	D0h	29h	2A5h
CSPRLV		16	0 to 7	8Ah	2Ah	2A6h
CSVLV		17	0, 1	0	2Bh	2A7h
CSVTH			2, 3	1		
CSHLV			4, 5	0		
CSHTH			6, 7	2		
YSPRLV		18	0, 1	0	2Ch	2A8h
YSPRTH			2, 3	0		
HLLIM			4, 5	0		
PEDLIM			6, 7	0		
GOFGAIN		19	0 to 7	00h	2Dh	2A9h

11.1.4. CAT4 (AE)

Name	CAT	Byte	Bit	Initial	Address	
					EEPROM	Reg.
AEW0	4	1	0, 1	0	2Fh	237h
AEW1			2, 3	0		
AEW2			4, 5	0		
AEW3			6, 7	0		
AGCFL		2	0	0	30h	238h
SHTFL			1	0		
LSHTLIM			2	0		
EVR5V			4	0		
AESCEV			7	0		
AESTAB		3	0 to 7	0	31h	239h
AEHYST		4	0 to 7	0	32h	23Ah
AEWAIT		5	0 to 7	0	33h	23Bh
AESPEED		6	0 to 7	8	34h	23Ch
AEUSR		7	0 to 7	4	35h	23Dh
AGCMAXL		8	0 to 7	CCh	36h	23Eh
AGCMAXH		9	0 to 7	FFh	37h	23Fh
MSHTLIM		10	0 to 7	7	38h	240h
AGCFLLL		11	0 to 7	20h	39h	241h
SHTFLLL		12	0 to 3	01h	3Ah	242h
SHTFLUL			4 to 7	0Bh		
AETHL		13	0 to 7	10h	3Bh	243h
AETHH		14	0 to 7	20h	3Ch	244h

11.1.5. CAT5 (AWB)

Name	CAT	Byte	Bit	Initial	Address	
					EEPROM	Reg.
AWBW0	5	1	0, 1	0	3Dh	245h
AWBW1			2, 3	0		
AWBW2			4, 5	0		
AWBW3			6, 7	0		
AWBSEPOF		2	0	0	3Eh	246h
AWBTRIG			1	0		
AWBHLCUT			2, 3	0		
AWBLLCUT			4	0		
GGAIN		3	0 to 7	26h	3Fh	247h
AWBSPED		5	0 to 3	1	41h	249h
AWBAJST5			4, 5	0		
AWBAJST6			6, 7	0		
AWBFRAM		6	0 to 7	0	42h	24Ah
AWBRSFT		7	0 to 7	0	43h	24Bh
AWBBSFT		8	0 to 7	0	44h	24Ch
WBUSRR		11	0 to 7	49h	47h	24Fh
WBUSRB		12	0 to 7	2Ch	48h	250h
WBRSFT		13	0 to 7	3	49h	251h
WBBSFT		14	0 to 7	1	4Ah	252h

11.1.6. CAT6 (ADJUST)

Name	CAT	Byte	Bit	Initial	Address	
					EEPROM	Reg.
VSUB	6	1	0 to 7	00h	4Bh	253h
RGL		2	0 to 7	00h	4Ch	254h
AGCMIN		3	0 to 7	11h	4Dh	255h
SHOFST		4	0 to 7	A0h	4Eh	256h
DAVRF		5	0 to 7	58h	4Fh	257h
EVRUSR7		6	0 to 7	00h	50h	258h
EVRUSR8		7	0 to 7	00h	51h	259h
AWBPRER		8	0 to 7	37h	52h	25Ah
AWBPREB		9	0 to 7	39h	53h	25Bh
PRERBL		10	0 to 7	00h	54h	25Ch
PRERBH		11	0 to 7	0Ah	55h	25Dh
PRERBGL		12	0 to 7	00h	56h	25Eh
PRERBGH		13	0 to 7	23h	57h	25Fh
PRE2R		14	0 to 7	60h	58h	260h
PRE2B		15	0 to 7	20h	59h	261h
AWBAJST1		16	0 to 7	18h	5Ah	262h
AWBAJST2		17	0 to 7	1Ch	5Bh	263h
AWBAJST3		18	0 to 7	00h	5Ch	264h
AWBAJST4		19	0 to 7	00h	5Dh	265h
BLOGAIN		20	0 to 7	46h	5Eh	266h
INTSLICE		21	0 to 7	80h	5Fh	267h

11.1.7. CAT7 (TIMING)

Name	CAT	Byte	Bit	Initial	Address	
					EEPROM	Reg.
WINDSEL	7	1	0,1	0	61h	269h
WINDMK			2	0		
DEFMK			3	0		
SVHMK			4	0		
W3STAH		2	0 to 3	05h	62h	26Ah
W3WIDH			4 to 7	05h		
W3STAV		3	0 to 3	04h	63h	26Bh
W3WIDV			4 to 7	07h		
ADCKDLY		4	4, 5	2	64h	26Ch
OFFSET25			7	0		
DLYXSH		5	0, 1	0	65h	26Dh
DTYXSH			2, 3	0		
DLYXRS			4, 5	0		
DTYXRS			6, 7	0		
SFTVL		9	0 to 7	01h	69h	271h
SFTVM		10	2	0	6Ah	272h
SFTSPED			4, 5, 6	0		
DEF1HL		11	0 to 7	00h	6Bh	273h
DEF1VL		12	0 to 7	00h	6Ch	274h
DEF1HM		13	0, 1	0	2Eh	2AAh
DEF1VM			2, 3	0		
DEF1L			4	0		
DEF2HL		14	0 to 7	00h	6Eh (bit 0 to 4)	276h
DEF2VL		15	0 to 7	00h	6Fh	277h
DEF2HM		16	0, 1	0	60h (bit 0 to 4)	268h
DEF2VM			2, 3	0		
DEF2L			4	0		

11.1.8. CAT9 (EXTCON)

Name	CAT	Byte	Bit	Initial	Address	
					EEPROM	Reg.
DRSL1	9	12	4, 5, 6	1	72h	2B6h
IDINV		13	7	NT=0 / PAL=1	73h	2B7h
PLLSW		14	4	0	74h	2B8h
DRSL2			5, 6, 7	1		
YDLY		15	0, 1	0	75h	2B9h
CDLY			2, 3	0		
YDDLY			4, 5	0		
CDDLY			6, 7	0		
RMATY		16	0 to 7	2Dh	76h	2BAh
RMATC		17	0 to 7	00h	77h	2BBh
BMATY		18	0 to 7	45h	78h	2BCh
BMATC		19	0 to 7	BBh	79h	2BDh
DRSL3		20	2, 3, 4	1	7Ah	2BEh
DRSL4			5, 6, 7	1		

SS-11RM Application Notes

Not for sale

June / 2005 Ver. 1.1.4

Editor and Publisher:
Sony Corporation
Semiconductor Solutions Network Company