UBA2036TS

Full-bridge control IC for HID automotive lighting

Rev. 06 — May 2007 | Preliminary data sheet

1. General description

The UBA2036 is a high voltage monolithic integrated circuit manufactured in a High Voltage Silicon On Insulator process. This circuit is designed for driving MOSFETs in a full bridge configuration. In addition, it features a disable function, an internal adjustable oscillator and an external clock input function with a high-voltage level shifter for driving the bridge. To guarantee an accurate 50% duty cycle, the oscillator signal can be passed through a divider before being fed to the output drivers.

The UBA2036 is especially suitable for High Intensity Discharge lamp drivers for automotive car headlights, beamers and general lighting applications.

2. Features

- Full bridge driver circuit
- Integrated bootstrap diodes
- 464V integrated high voltage level shift function to drive HID lamps below ground level
- 550V series regulator input to make the internal supply
- 550 V maximum bridge voltage
- Accurate bridge disable function
- Input for start-up delay
- Adjustable oscillator frequency
- Selectable frequency divider
- Predefined bridge position during start-up
- Adaptive non-overlap

3. Applications

- The UBA2036 can drive (via the power MOSFETs) any kind of load in a full bridge configuration.
- The circuit is especially designed as a commutator for High Intensity Discharge (HID) lamps in automotive car headlight, beamer and general lighting applications.

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4. Ordering information

Table 1: Ordering information

	Package		
	Name	Description	Version
UBA2036TS	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

5. Block diagram

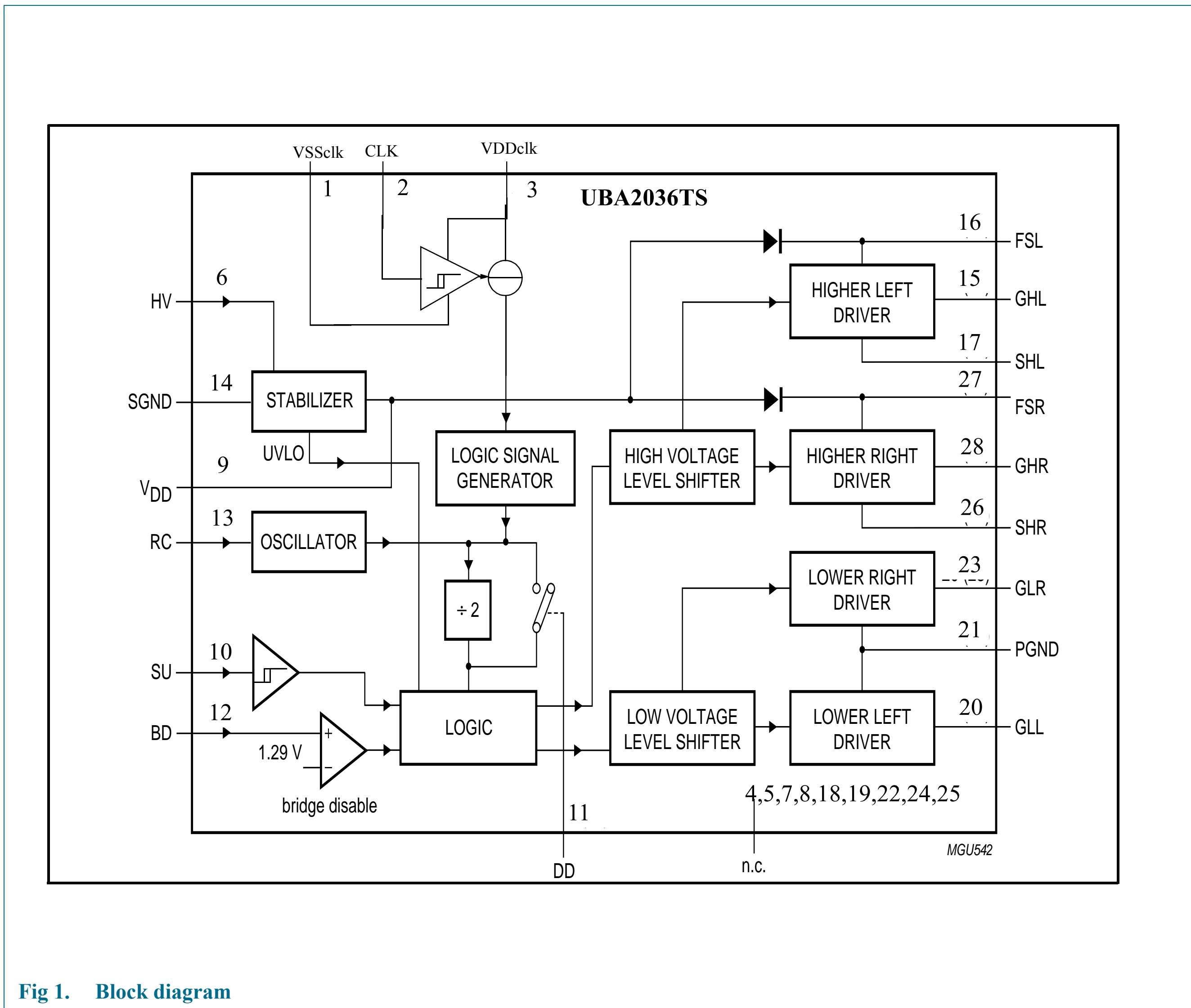

Fig 1. Block diagram

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6. Pinning information

6.1 Pinning

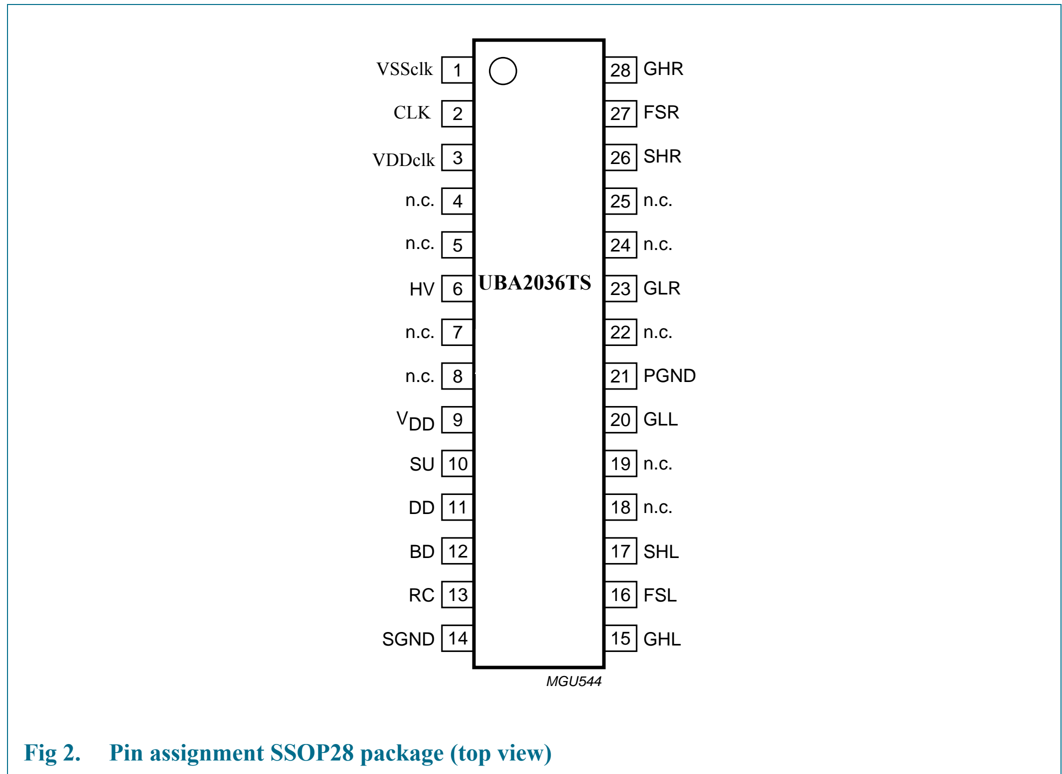

Fig 2. Pin assignment SSOP28 package (top view)

6.2 Pin description

Table 2: Pin description

Symbol	Pin	Description
VSS_{CLK}	1	negative supply voltage for logic oscillator input
CLK	2	oscillator input
VDD_{CLK}	3	positive supply voltage for logic oscillator input
n.c.	4	not connected
n.c.	5	not connected
HV	6	high voltage supply input for internal series regulator
n.c.	7	not connected
n.c.	8	not connected
VDD	9	internal low voltage supply
SU	10	input for startup delay
DD	11	input for divider disable
BD	12	input for bridge disable
RC	13	RC input for internal oscillator
SGND	14	signal ground
GHL	15	gate driver output for upper left MOSFET

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Table 2: Pin description ...continued

Symbol	Pin	Description
FSL	16	floating supply left
SHL	17	source upper left MOSFET
n.c.	18	not connected
n.c.	19	not connected
GLL	20	gate driver output for lower left MOSFET
PGND	21	power ground
n.c.	22	not connected
GLR	23	gate driver output for lower left MOSFET
n.c.	24	not connected
n.c.	25	not connected
SHR	26	source upper right MOSFET
FSR	27	floating supply right
GHR	28	gate driver upper right MOSFET

7. Functional description

7.1 Supply voltage

The UBA2036 is powered by a supply voltage applied to pin HV, for instance the supply voltage of the full bridge. The IC generates its own low supply voltage for its internal circuitry. Therefore an additional low voltage supply is not required. A capacitor has to be connected to pin V_{DD} to obtain a ripple-free internal supply voltage. The circuit can also be powered by a low voltage supply directly applied to pin V_{DD}. In this case pin HV should be connected to pin V_{DD} or pin SGND. The maximum current which the internal series regulator can deliver, is temperature dependent. This is depicted in Figure 3.

7.2 Start up

With an increasing supply voltage the IC enters the start-up state i.e. the upper power transistors are set in off-state and the lower power transistors are switched on. During the start-up state the bootstrap capacitors are charged. The start-up state is defined until $V_{DD} = V_{DD(start)}$ or $V_{HV} = V_{HV(start)}$. The state of the outputs during the start-up phase is overruled by the bridge disable function.

7.3 Oscillation state

At the moment the supply voltage on pin V_{DD} exceeds $V_{DD(start)}$ or the supply voltage on pin V_{HV} exceeds $V_{HV(start)}$, the output voltage of the fullbridge depends on the control signal on pin CLK, SU, DD and BD. This is listed in Table 3

As soon as the supply voltage on pin V_{DD} becomes lower than $V_{DD(stop)}$ or the supply voltage on pin V_{HV} becomes lower than $V_{HV(stop)}$, the IC enters the start-up state again.

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Table 3: Driver

Gate driver output voltages as function of the logical levels at the pins BD, SU, DD and EXTDR

Device state	BD	SU	DD	CLK	GHL	GHR	GLL	GLR
Start up state	1				0 (=V_{SHL})	0 (=V_{SHR})	0 (=V_{PGND})	0 (=V_{PGND})
	0				0 (=V_{SHL})	0 (=V_{SHR})	1 (=V_{VDD})	1 (=V_{VDD})
Oscillation state	1				0 (=V_{SHL})	0 (=V_{SHR})	0 (=V_{PGND})	0 (=V_{PGND})
	0	0			0 (=V_{SHL})	0 (=V_{SHR})	1 (=V_{VDD})	1 (=V_{VDD})
	0	1	1	1	0 (=V_{SHL})	1 (=V_{FSR})	1 (=V_{VDD})	0 (=V_{PGND})
	0	1	1	0	1 (=V_{FSL})	0 (=V_{SHR})	0 (=V_{PGND})	1 (=V_{VDD})
	0	1	0 [1]	1 --> 0 [2]	$\overline{GHL}$	$\overline{GHR}$	$\overline{GLL}$	$\overline{GLR}$

[1] If pin DD = 0 the bridge enters the state (oscillation state and pin BD = 0 and pin SU = 1) in the pre-defined position : $V_{GHL} = V_{FSL}$, pin $V_{GLR} = V_{VDD}$, pin $V_{GLL} = V_{PGND}$ and pin $V_{GHR} = V_{SHR}$.

[2] Only if the level of pin CLK changes from logical 1 to 0, the level of outputs GHL, GHR, GLL and GLR changes.

In case that there is no external clock available, the internal oscillator can be used. The design equation for the bridge oscillator frequency is :

$$f_{bridge} = \frac{1}{k_{osc} \times R_{osc} \times C_{osc}}$$

R_{osc} and C_{osc} are external components connected to the RC pin (R_{osc} connected to pin VDD and C_{osc} connected to pin SGND). In this situation the pins VDDclk, CLK and VSSclk can be connected to SGND.

The clock signal, either coming from pin RC or pin CLK, can be divided by two in order to obtain a 50% dutycycle gate drive signal. This can be achieved by apply a voltage to the DD input lower than $V_{DD(L)}$ (for instance connect pin DD to pin SGND).

7.4 Non overlap time

In the full bridge configuration the non overlap time is defined as the time between turning off the two conducting MOSFETs and turning on the two other MOSFETs. The non overlap time is realized by means of an adaptive non overlap circuit. With an adaptive non overlap, the application determines the duration of the non overlap and makes the non overlap time optimal for each frequency. The non overlap time is determined by the duration of the falling slope of the relevant half bridge voltage. The occurrence of a slope is sensed internally. The minimum non-overlap time is internally fixed.

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7.5 Start up delay

A simple RC filter (R between pin V_{DD} and pin SU; C between pin SU and pin SGND) or a control signal from a processor can be used to make a start up delay. This can be beneficial for those applications in which building up the high voltage takes a larger amount of time : A start up delay will ensure that the HID system will not start up before this high voltage has settled.

7.6 Bridge disable

The bridge disable function can be used to switch off all the MOSFETs as soon as the voltage on pin BD exceeds the bridge disable voltage V_{BD}. The bridge disable function overrules all the other states.

8. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to signal ground (pin 14); positive currents flow into the chip. The voltage ratings are valid provided other ratings are not violated.

Symbol	Parameter	Conditions	Min	Max	Unit
General					
T_{amb}	ambient temperature		–40	+125	°C
T_j	junction temperature		–40	+150	°C
T_{stg}	storage temperature		–55	+150	°C
Voltages					
V_{VDD}	supply voltage (low voltage)	DC $tpulse_{max}$ = 100ns	0 0	14 17	V
V_{HV}	supply voltage (high voltage)		0	550	V
V_{SHL}	source voltage for higher left MOSFET	with resepect to PGND and SGND	-3	550	V
V_{SHL}	pulsed source voltage for higher left MOSFET	with resepect to SGND $tpulse_{max}$ = 1us	-14	550	V
V_{SHR}	source voltage for higher right MOSFET	with resepect to PGND and SGND	-3	550	V
V_{SHR}	pulsed source voltage for higher right MOSFET	with resepect to SGND $tpulse_{max}$ = 1us	-14	550	V
V_{FSL}	floating supply voltage left	with resepect SHL	0	14	V
V_{FSR}	floating supply voltage right	with resepect SHR	0	14	V
V_{GHL}	gate output voltage upper left		V_{SHL}	V_{FSL}	V
V_{GHR}	gate output voltage upper right		V_{SHR}	V_{FSR}	V
V_{GLL}	gate output voltage lower left		V_{PGND}	V_{VDD}	V
V_{GLR}	gate output voltage lower right		V_{PGND}	V_{VDD}	V
V_{PGND}	power ground voltage		0	+5	V
V_{VSSclk}	negative supply for CLK input	t<1s	0	464	V
V_{VDDclk}	positive supply for CLK input	t<1s	0	464	V
V_{VDDclk}	positive supply for CLK input	with respect to VSSclk, DC $tpulse_{max}$ = 100ns	0 0	14 17	V
$V_{i(CLK)}$	input voltage on pin CLK	with respect to VSSclk, DC $tpulse_{max}$ = 100ns	0 0	V_{VDD} 17	V

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Table 4: Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to signal ground (pin 14); positive currents flow into the chip. The voltage ratings are valid provided other ratings are not violated.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{i(RC)}$	input voltage on pin RC	$tpulse_{max}$ = 100ns	0	17	V
$V_{i(SU)}$	input voltage on pin SU	DC $tpulse_{max}$ = 100ns	0 0	V_{VDD} 17	V
$V_{i(BD)}$	input voltage on pin BD	DC $tpulse_{max}$ = 100ns	0 0	V_{VDD} 17	V
$V_{i(DD)}$	input voltage on pin DD	DC $tpulse_{max}$ = 100ns	0 0	V_{VDD} 17	V
SRbridge	slewrate on pins SHL, SHR			6	V/ns
SRclk	slewrate on pin VSSclk			0.5	V/us
Currents					
R_{RC}	resistor connected between pins VDD and RC		100		kOhm
ESD					
V_{ESD}	electrostatic discharge voltage				
	human body model	HV, VSSclk, VDDclk,CLK, FSL, FSR, GHL, GHR, SHL, SHR	-	900	V
		other pins	-	2kV	kV
	machine model	all pins	-	200	V
	charged device model	all pins	-	500	V

9. Thermal characteristics

Table 5: Thermal characteristics

	Parameter	Conditions		Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	100	K/W

10. Characteristics

Table 6: Characteristics

T_j = -40 °C to 125 °C; all voltages are measured with respect to signal ground (pin 14); currents are positive when flowing into the IC, Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High voltage						
$I_{leakage(HV)}$	leakage current HV pin	$I_{HV}(V_{HV}$=565V) - $I_{HV}(V_{HV}$=500V)		0	5	µA
$I_{leakage(FSL)}$	leakage current FSL pin	$V_{FSL} = V_{SHL} = V_{GHL}$ = 564V		0	5	µA
$I_{leakage(FSR)}$	leakage current FSR pin	$V_{FSR} = V_{SHR} = V_{GHR}$ = 564V		0	5	µA
$I_{leakage(VSSclk)}$	leakage current VSSclk pin	$V_{VSSclk} = V_{clk}$ = 450V		0	10	µA
$I_{leakage(VDDclk)}$	leakage current VDDclk pin	$V_{VDDclk} = V_{clk}$ = 464V		0	10	µA
Start-up via HV pin						
$I_{i(HV)}$	HV input current	V_{HV}= 80V		590	825	uA
$V_{VHV(start)}$	start up voltage		11.3	13.2	14.7	V

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Table 6: Characteristics *...continued*

T_j = -40°C to 125 °C; all voltages are measured with respect to signal ground (pin 14); currents are positive when flowing into the IC, Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{VHV(stop)}$	undervoltage lockout voltage		8.6	10.7	12.2	V
$V_{VHV(hyst)}$	HV hysteresis voltage		2	2.5	3	V
V_{VDD}	internal supply voltage	V_{HV}= 20V	10.5	12	13.5	V
Start-up via VDD pin						
$I_{i(VDD)}$	VDD input current	V_{VDD}= 8.25V		500	800	uA
$V_{VDD(start)}$	start up voltage		8.25	9.0	9.75	V
$V_{VDD(stop)}$	undervoltage lockout voltage		5.75	6.5	7.25	V
$V_{VDD(hyst)}$	VDD hysteresis voltage	V_{FSL} =V_{FSR} = 12V	2	2.5	3	V
gate drivers						
$R_{on(H)}$	on resistance GHR and GHL driver	V_{FSL} = V_{FSR} = 12V V_{SHL} = V_{SHR} = 0V I_{GHL} = I_{GHR} = -50mA		20	42	Ohm
$R_{on(L)}$	on resistance GLR and GLL driver	V_{VDD}= 12V V_{PGND}= 0V I_{GLL} = I_{GLR} = -50mA		20	42	Ohm
$R_{off(H)}$	off resistance GHR and GHL driver	V_{FSL} = V_{FSR} = 12V V_{SHL} = V_{SHR} = 0V I_{GHL} = I_{GHR} = 50mA		12	26	Ohm
$R_{off(L)}$	off resistance GLR and GLL driver	V_{VDD}= 12V V_{PGND}= 0V I_{GLL} = I_{GLR} = 50mA		12	26	Ohm
$I_{o(source)}$	source current drivers	V_{FSL} = V_{FSR} = V_{VDD} = 12V V_{SHL} = V_{SHR} = 0V V_{GHL} = V_{GHR} = V_{GLL} = V_{GLR} = 4V		200		mA
$I_{o(sink)}$	sink current drivers	V_{FSL} = V_{FSR} = V_{VDD} = 12V V_{SHL} = V_{SHR} = 0V V_{GHL} = V_{GHR} = V_{GLL} = V_{GLR} = 4V		200		mA
V_{diode}	bootstrap diode voltage	I_{diode} = 1mA	0.8	1.0	1.2	V
t_{slope}	minimum dv/dt for adaptive non-overlap	absolute values	5	15	25	V/us
$t_{no(min)}$	minimum non-overlap time		600	900	1300	ns
$V_{HSlockout}$	HS lockout voltage			4.0	5	V
I_{FS}	floating supply current	V_{FSL}= V_{FSR} = 12V V_{SHL}= V_{SHR} = 0V	2	4	6	uA
I_{FS} ratio	floating supply current ratio	I_{FSL} / I_{FSR}	0.8		1.2	
DD input						
$V_{DD(h)}$	high level input voltage	V_{VDD}= 12V	6	4.5		V
$V_{DD(l)}$	low level input voltage	V_{VDD}= 12V			3	V
$I_{i(DD)}$	input current into pin DD	V_{VDD}= 12V		0	1	uA
SU input						
V_{SU}	start-up input level	V_{VDD}= 12V	1	1.3	1.5	V
$V_{SU(hyst)}$	hysteresis on input level	V_{VDD}= 12V		100		mV
$I_{i(SU)}$	input current into pin SU	V_{VDD}= 12V		0	1	uA

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Table 6: Characteristics *...continued*

T_j = -40 ℃ to 125 ℃; all voltages are measured with respect to signal ground (pin 14); currents are positive when flowing into the IC, Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CLK input						
V_{CLK}	CLK input level	V_{VSSCLK}= 0V V_{VDDCLK}= 12V	0.9	1.6	2.7	V
$V_{CLK(hyst)}$	hysteresis on input level	V_{VSSCLK}= 0V V_{VDDCLK}= 12V		100		mV
$I_{i(CLK)}$	input current into pin CLK			0	1	uA
$f_{bridge,CLK}$	maximum bridge oscillating frequency	V_{RC}= 0V			200	kHz
supply for CLK						
I_{VDDclk}	supply current for CLK	V_{VSSCLK}= 0V V_{VDDCLK}= 14V		420	625	uA
$V_{VDDclk(range)}$	supply voltage range	V_{VSSCLK}= 0V	5.75		14	V
BD input						
V_{BD}	BD input level		1.23	1.29	1.35	V
$I_{i(BD)}$	input current into pin BD			0	1	uA
Internal Oscillator						
$f_{bridge,RC}$	maximum bridge oscillating frequency	V_{CLK}= 0V V_{VSSCLK}= 0V			100	kHz
k_{osc}	oscillator constant	f_{bridge} = 500Hz	0.94	1.02	1.1	

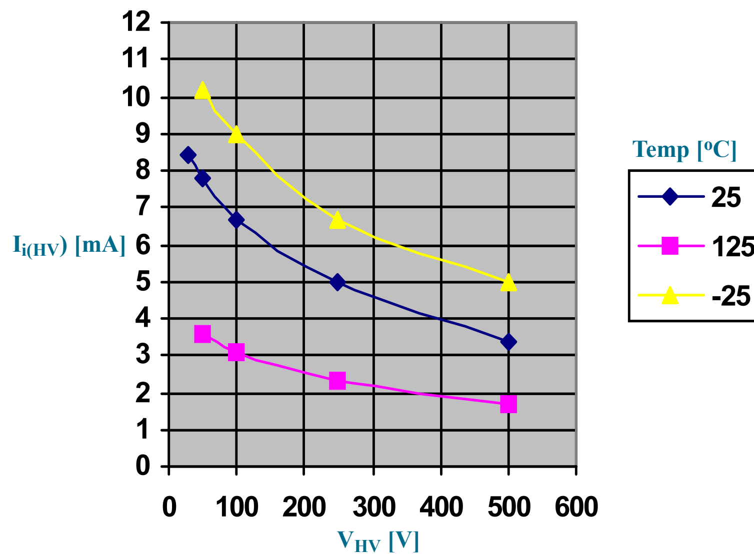

Fig 3. Typical $I_{i(HV)}$ when VDD shorted to SGND, as function of V_{HV} and temperature

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11. Application information

12. Test information

12.1 Quality information

This product has been qualified to the appropriate Automotive Electronics Council (AEC) standard Q100 or Q101 and is suitable for use in automotive critical applications.

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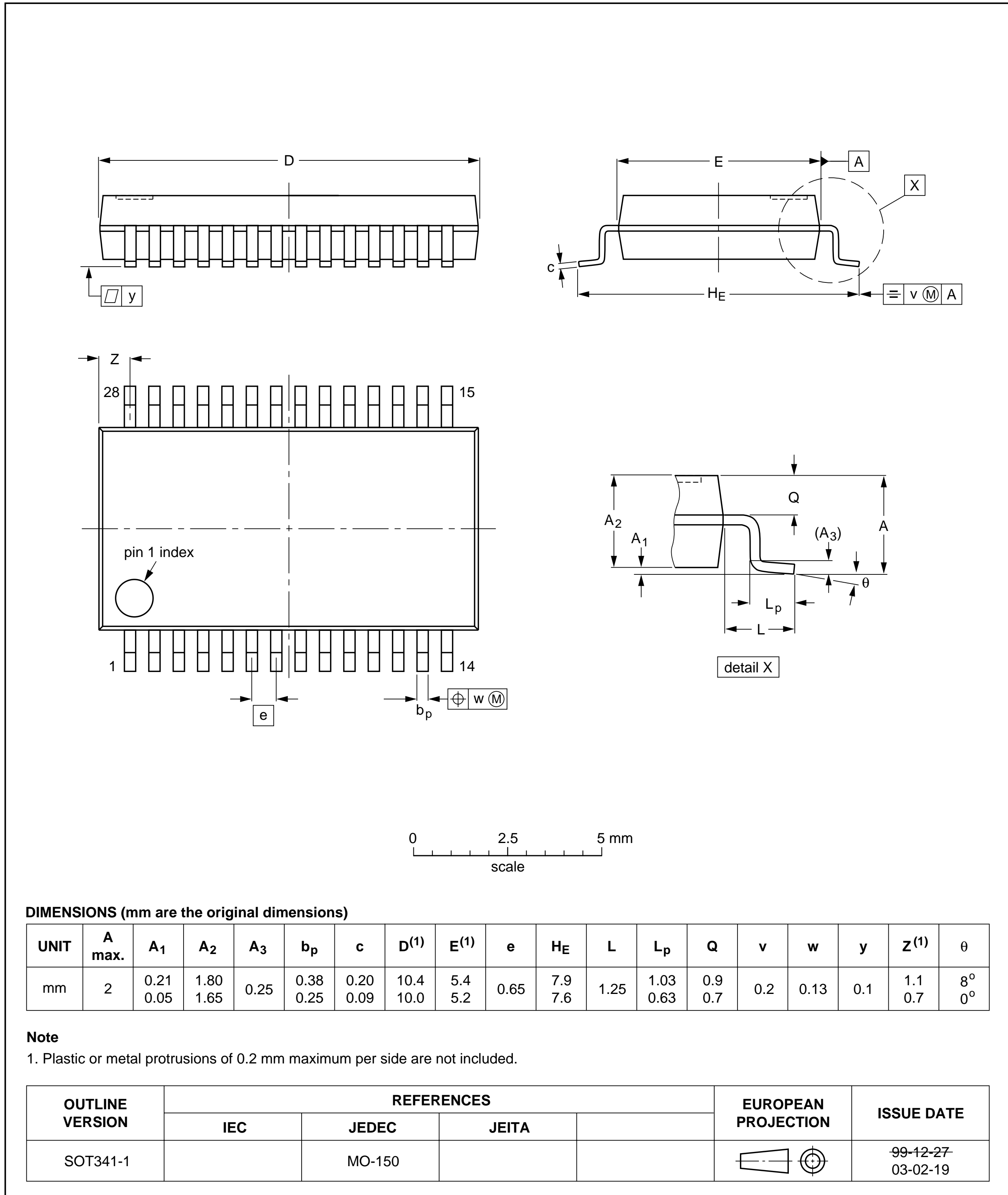
13. Package outline

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8° 0°

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT341-1		MO-150				~~99-12-27~~ 03-02-19

Fig 4. Package outline SSOP28 (SOT134-1)

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14. Soldering

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

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  – smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

14.5 Package related soldering information

Table 7: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

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[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

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15. Revision history

Table 8: Revision history

	Release date	Data sheet status	Change notice	Order number	Supersedes
		Preliminary data	-	xxxx xxx xxxxx	

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16. Data sheet status

	Data sheet status [1]		
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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