TEA1750

GreenChip™III SMPS control IC

Rev. 0.10 — June 16, 2006 Objective data sheet

1. General description

The GreenChip™III is the third generation of green Switched Mode Power Supply (SMPS) controller ICs. The TEA1750 integrates a controller for power factor correction and a flyback controller. Its high level of integration allows the design of a cost effective power supply with a very low number of external components.

The special built-in green functions allow a high efficiency at all power levels. This holds for quasi-resonant operation at high power levels, quasi-resonant operation with valley skipping, as well as in reduced frequency operation at lower power levels. At low power (standby) levels, the power factor controller switches over to burst mode control to maintain high efficiency. In burst mode soft-start and soft-stop is added to eliminate audible noise. Highly efficient and reliable supplies can easily be designed using the GreenChipIII control IC.

The proprietary high voltage BCD800 process makes direct start-up possible from the rectified universal mains voltage in an effective and green way. A second low voltage SOI IC is used for accurate, high speed protection functions and control.

The TEA1750 enables highly efficient and reliable supplies for powers above 75W to be designed easily and with a minimum number of components.

2. Features

2.1 Distinctive features

- Integrated PFC and flyback controller
- Universal mains supply operation (70 V to 276 V AC)
- High level of integration, resulting in a very low external component count

2.2 Green features

- On-chip start-up current source.

2.3 Green features PFC part

- Valley/zero voltage switching for minimum switching losses
- Frequency limitation to reduce switching losses
- Burst mode operation if a low load is detected at the flyback output

2.4 Green features flyback part

- Valley switching for minimum switching losses
- Frequency reduction with fixed minimum peak current at low power operation to maintain high efficiency at low output power levels

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2.5 Protection features

- Safe restart mode for system fault conditions
- Continuous mode protection by means of demagnetization detection for both converters
- Undervoltage protection (foldback during overload)
- Accurate over-voltage protection for both converters (adjustable for flyback converter)
- Open control loop protection for both converters
- IC over-temperature protection
- Low and adjustable over-current protection trip level for both converters
- Soft (re)start for both converters
- Mains undervoltage protection/ brown out protection
- General purpose input for latched protection, e.g. to be used for system over-temperature protection

3. Applications

- The device can be used in all applications that demand an efficient and cost-effective power supply solution from 75W up to 250 W. Notebook adapters can especially benefit from the high integration level.

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
TEA1750T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5. Block diagram

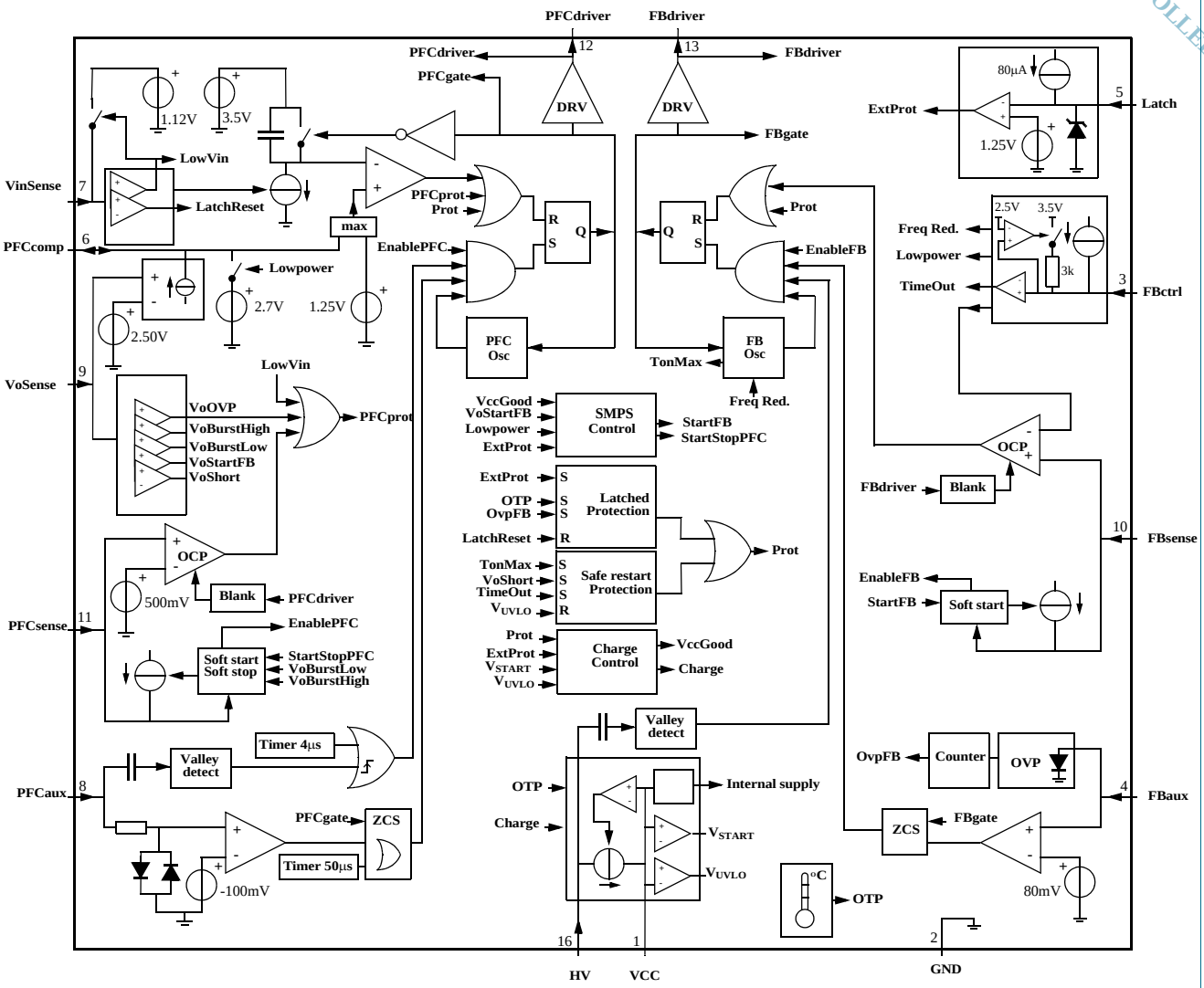


Fig 1. Block diagram.

6. Pinning information

6.1 Pinning

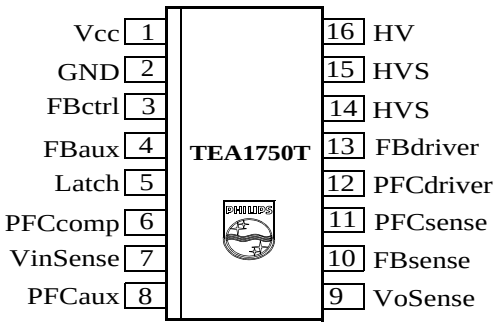


Fig 2. Pin configuration: TEA1750T (SOT109-1).

6.2 Pin description

Table 2: Pin description

Symbol	Pin	Description
Vcc	1	supply voltage
GND	2	ground
FBctrl	3	control input for flyback
FBaux	4	input from auxiliary winding for demagnetization timing and over-voltage protection for flyback
Latch	5	general purpose protection input
PFCcomp	6	frequency compensation pin for PFC
VinSense	7	sense input for mains voltage
PFCaux	8	input from auxiliary winding for demagnetization timing for PFC
VoSense	9	sense input for PFC output voltage
FBsense	10	programmable current sense input for flyback
PFCsense	11	programmable current sense input for PFC
PFCdriver	12	gate driver output for PFC
FBdriver	13	gate driver output for flyback
HVS	14, 15	high voltage safety spacer, not connected
HV	16	high voltage start-up and valley sensing of flyback part.

7. Functional description

7.1 General control

The TEA1750 contains a controller for a power factor correction circuit as well as a controller for a flyback circuit. A typical configuration is drawn in Figure 3.

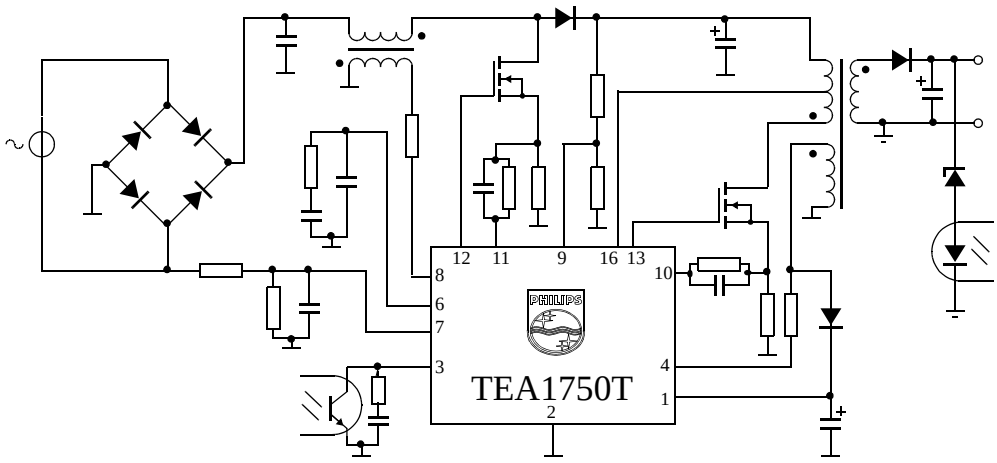


Fig 3. Typical configuration.

7.1.1 Start-up and undervoltage lock-out

The IC will initially charge the capacitor on the VCC pin from the high voltage mains via the HV pin. The charge current will switch to the high level as soon as Vcc passes the V_{trip} level. As soon as the V_{UVLO} level is reached, the current is switched back to the low level. The control logic will activate the internal circuitry and switch off the charge current as soon as the voltage on pin Vcc passes the V_{start} level. First the Latch pin output will be activated. As soon as the Latch pin voltage is above the $V_{enable(Latch)}$ voltage, the power factor correction circuit will be activated and the supply current from the HV pin is switched on again. After charging the soft-start capacitor on the PfcSense pin, the PFC will start switching and charge the Cbus capacitor. As soon as the voltage on pin VoSense reaches the $V_{startFB}$ level, the charge current will be switched off and the flyback converter will be activated. The flyback converter will first charge the soft start capacitor connected to the FbSense pin and subsequently starts switching. The output voltage of the flyback converter will than be controlled to its intended level. See Figure 4.

If during start-up the Latch pin does not reach the $V_{enable(Latch)}$ level before Vcc reaches V_{UVLO}, the Latch pin output will be de-activated and the charge current will be switched on again.

As soon as the flyback converter is started, the voltage on the FbCtrl pin is monitored. If the output voltage of the flyback converter does not reach its intended regulation level in a predefined time, the voltage on the FbCtrl pin will reach the $V_{TimeOut}$ level and an error is assumed. The TEA1750 will than preform a safe restart.

The IC supply from the high voltage pin is stopped as soon as the flyback converter is activated. The IC supply will be taken over by the auxiliary winding of the flyback converter.

When a protection is activated, both converters will stop switching and the Vcc voltage will drop to V_{UVLO}. A latched protection will recharge the Vcc capacitor via the HV pin, but will not restart the converters. In case of a safe-restart protection the Vcc capacitor will be recharged via the HV pin and a restart will be made. (see also the block diagram in Figure 1)

In case of an over-voltage protection of the PFC part, sensed via the VoSense pin ($V_{VoSense}>V_{OVP(VoSense)}$), only the PFC controller will stop switching until the VoSense pin voltage drops below the $V_{OVP(VoSense)}$ voltage again. Also if a mains undervoltage is detected via the VinSense pin ($V_{VinSense}<V_{stop(VinSense)}$), only the PFC controller will stop switching until the voltage on pin VinSense is above the VinSense start level again. ($V_{VinSense}>V_{start(VinSense)}$)

When the voltage on pin Vcc drops below the undervoltage lock-out level, both controllers stop switching and will re-enter the safe restart mode. In the safe restart mode the driver outputs are disabled and the Vcc pin voltage is recharged via the HV pin.

If Vcc is below V_{trip}, the charge current is low. This will protect the IC in case the Vcc pin is shorted to ground. For a short start-up time the charge current is increased until Vcc reaches V_{UVLO}. If, during start-up, Vcc is between V_{UVLO} and V_{start}, the charge current will be low, ensuring a low duty cycle during fault conditions. When the PFC is started, there is initially no supply take-over from the auxiliary winding. To make a small Vcc capacitor possible, the Vcc voltage is regulated to the V_{start} level as long as the flyback converter has not started yet. Regulation is done by hysteretic control with a limited (high level) charge current.

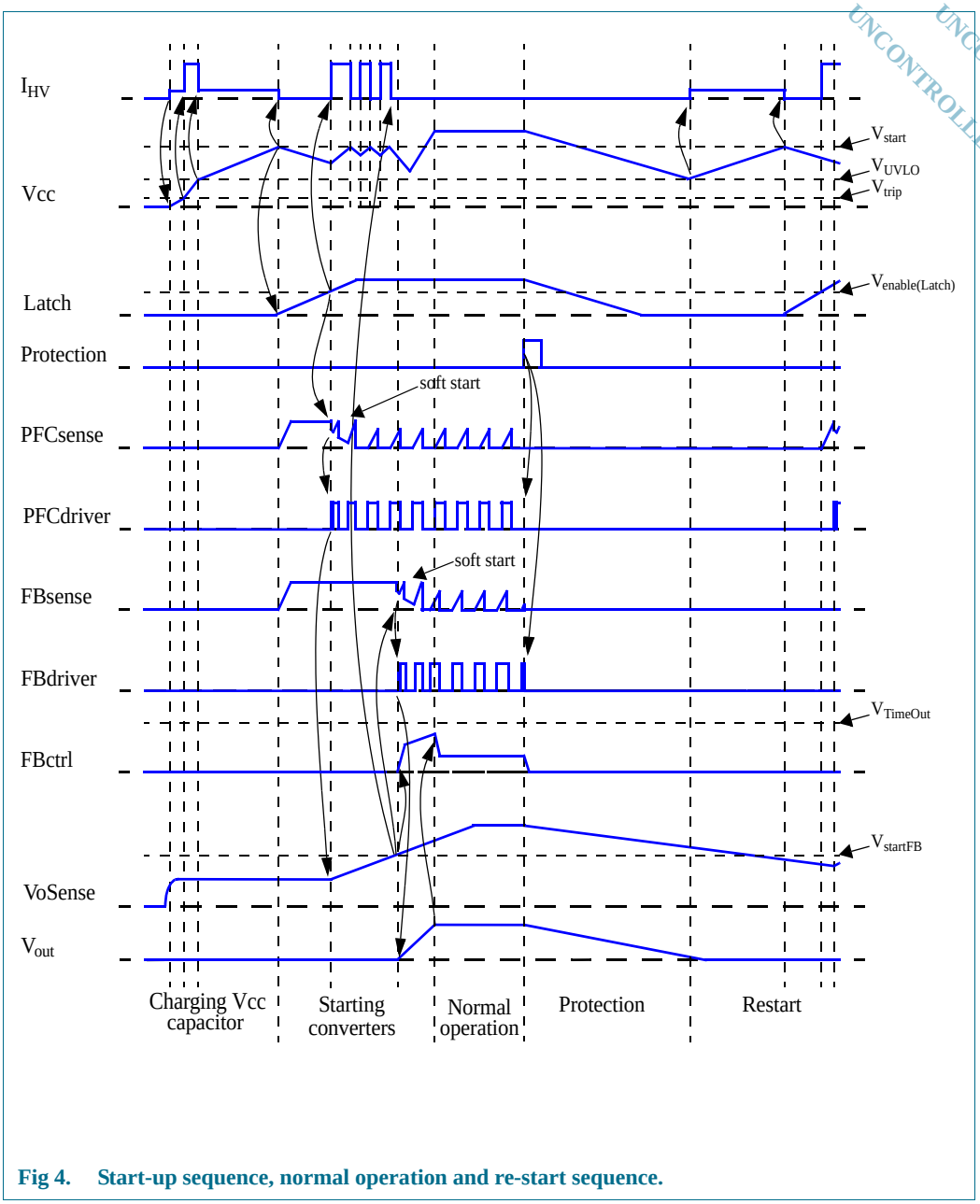


Fig 4. Start-up sequence, normal operation and re-start sequence.

7.1.2 Supply management

All internal reference voltages are derived from a temperature compensated and trimmed, on-chip band gap circuit. Internal reference currents are derived from a temperature compensated and trimmed on-chip current reference circuit.

7.1.3 Latch input

Pin Latch is a general purpose input pin, which can be used to switch off both converters. The pin sources a current I_{LATCH} (typ. 80uA). As soon as the voltage on this pin is below 1.25 volts switching of both converters will be stopped immediately.

At initial start-up the switching is inhibited until the voltage on the Latch pin is above 1.35 volts (typ). No internal filtering is done on this pin. An internal zener clamp of 2.7 volts (typ.) will protect this pin from excessive voltages.

7.1.4 Fast latch reset

The latched protection will be reset when the Vcc voltage of the IC drops below 6V (typ.). Typically the PFC bus capacitor, Cbus, has to discharge for the Vcc to drop to this reset level. Also when the latched protection is set, the clamping circuit of the VinSense circuit is disabled. (see also Section 7.2.8) As soon as the VinSense voltage drops below 110mV (typ.) and after that is raised to 225mV (typ.), the latched protection is reset.

In a typical application the mains can be interrupted shortly to reset the latched protection. The PFC bus capacitor, Cbus, does not have to discharge for this latched protection to reset.

7.1.5 OverTemperature Protection (OTP)

An accurate internal temperature protection is provided in the circuit. When the junction temperature exceeds the thermal shutdown temperature, the IC will stop switching and enter the safe restart mode. As long as OTP is active, the Vcc capacitor will not be recharged from the HV mains. The OTP circuit is supplied from the HV pin if the Vcc supply voltage is not sufficient.

7.2 Functional description power factor correction circuit

The power factor correction circuit operates in quasi resonant or discontinuous conduction mode with valley switching. A next primary stroke is only started as soon as the previous secondary stroke has ended and the voltage across the PFC MOSFET has reached a minimum value. The voltage on the PfcAux pin is used to detect transformer demagnetization and the minimum voltage across the external PFC MOSFET switch.

7.2.1 Ton control

The power factor correction circuit is operated in Ton control. The resulting mains harmonic reduction of a typical application will be well within the class-D requirements.

7.2.2 Valley switching and demagnetization (PFCaux pin)

The PFC MOSFET is switched on after the transformer is demagnetized. Internal circuitry connected to the PFCaux pin detects the end of the secondary stroke. Also it detects the voltage across the PFC MOSFET. The next stroke will be started if the voltage across the PFC MOSFET is at its minimum. (valley switching)

If no demagnetization signal is detected on the PFCaux pin, the controller generates a zero current signal 50µsec. (typ) after the last PFCgate signal.

If no valley signal is detected on the PFCaux pin, the controller generates a valley signal 4µsec. (typ) after demagnetization was detected.

To protect the internal circuitry, for example during lightning events, it is advised to add an 5kΩ series resistor to this pin. To prevent incorrect switching due to external disturbance, the resistor should be placed closed to the IC on the printed circuit board.

7.2.3 Frequency limitation

For optimizing the transformer and minimizing the switching losses, the switching frequency is limited to $f_{osc,max,PFC}$. If the frequency for quasi resonant operation is above the $f_{osc,max,PFC}$ limit, the system will switch over to discontinuous conduction mode. Also here, the PFC MOSFET is only switched on at a minimum voltage across the switch. (valley switching)

7.2.4 Mains voltage compensation (VinSense pin)

The mathematical equation for the transfer function of a power factor corrector contains the square of the mains input voltage. In a typical application this will result in a low bandwidth for low mains input voltages, while at high mains input voltages the MHR requirements may be hard to meet.

To compensate the mains input voltage influence, the TEA1750 contains a correction circuit. Via the VinSense pin the average input voltage is measured and the information is fed to an internal compensation circuit. With this compensation it is possible to keep the regulation loop bandwidth constant over the full mains input range, yielding a fast transient response on load steps, while still complying with class-D MHR requirements.

The bandwidth of the regulation loop is set by a resistor and two capacitors on the PFCcomp pin in a typical application.

7.2.5 Soft start-up (pin PFCsense)

To prevent transformer rattle at start-up or during hiccup, the transformer peak current, $I_{DM,PFC}$, is slowly increased by the soft start function. This can be achieved by inserting a resistor R_{SS1} and a capacitor C_{SS1} between pin PFCsense and current sense resistor R_{sense1}. An internal current source charges the capacitor to $V_{PFCsense} = I_{startup(soft),PFC} \times R_{ss1}$. The voltage is limited to $V_{SoftStart,PFC}$.

The start level and the time constant of the increasing primary current level can be adjusted externally by changing the values of R_{ss1} and C_{ss1}.

$$I_{DM,PFC} = \frac{V_{sense(max),PFC} - (I_{startup(soft),PFC} \times R_{ss1})}{R_{sense1}}$$

$$\tau = R_{ss1} \times C_{ss1}$$

The charging current $I_{startup(soft),PFC}$ will flow as long as the voltage on pin PFCsense is below 0.5 V (typ). If the voltage on pin PFCsense exceeds 0.5 V, the soft start current source will start limiting current $I_{startup(soft),PFC}$. As soon as the PFC starts switching the $I_{startup(soft),PFC}$ current source is switched off; see Figure 5.

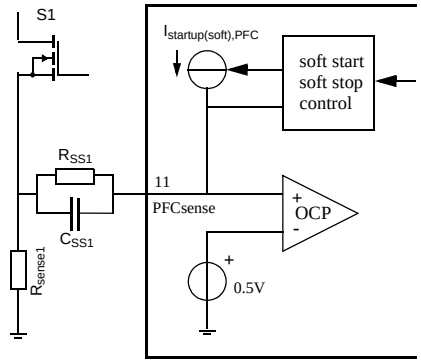


Fig 5. Soft start-up and soft stop of PFC.

7.2.6 Burst mode control

When the output power of the flyback converter (see Section 7.3) is low, the flyback converter switches over to VCO mode. When VCO mode is entered by the flyback controller, the power factor correction circuit switches to burst mode control.

In burst mode control, switching of the power factor correction circuit is inhibited until the voltage on the VoSense pin has dropped to $V_{burst,low}$. Switching than restarts with a soft-start to avoid audible noise. As soon as the voltage on the VoSense pin reaches $V_{burst,high}$ the soft-stop circuit will be activated, again to avoid audible noise. During the soft-stop time the output voltage of the power factor correction circuit will overshoot dependent on the soft-start resistor and capacitor R_{SS1} and C_{SS1} on the PFCsense pin. As the $V_{burst,high}$ voltage is well below the $V_{reg(VoSense)}$ voltage, the PFC output voltage will not reach the normal operation output voltage of the power factor correction circuit in a typical application due to this overshoot.

The burst mode frequency is defined by the output power, the value of the bus capacitor C_{bus} and the $V_{burst,low}$ and $V_{burst,high}$ levels.

During burst mode operation the PFCcomp pin is clamped to a minimal voltage of 2.7V (typ). This will limit the maximum power that is delivered during burst mode operation and will yield a more sinusodial input current during the burst pulse.

As soon as the flyback converter leaves the VCO mode, the power factor correction circuit restores normal operation immediately.

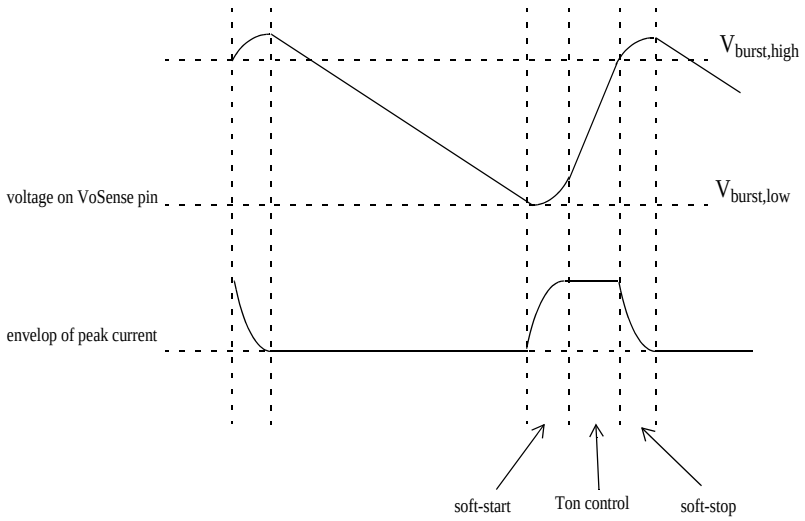


Fig 6. Burst mode control

7.2.7 Over-current protection (PFCsense pin)

The maximum peak current is limited cycle-by-cycle by sensing the voltage across an external sense resistor (R_{sense1}) on the source of the external MOSFET. The voltage is measured via the PFCsense pin.

7.2.8 Mains undervoltage lock-out / Brown out protection (VinSense pin)

To prevent the PFC to operate at very low mains input voltages, the voltage on the VinSense pin is sensed continuously. As soon as the voltage on this pin drops below the $V_{stop(VinSense)}$ level, switching of the PFC is stopped. When the low mains situation continues the PFC bus voltage will eventually drop. The voltage on the VoSense pin will than drop below the $V_{start,FB}$ level and the flyback converter will also be disabled.

The voltage in the VinSense pin is clamped to a minimum value ($V_{start(VinSense)}$-$V_{delta(VinSense)}$) for fast restart as soon as the mains input voltage returns after a mains-dropout.

7.2.9 Over voltage protection (VoSense pin)

To prevent output over-voltage during load steps and mains transients, an over voltage protection circuit is build in.

As soon as the voltage on the VoSense pin exceeds the $V_{OVP(VoSense)}$ level, switching of the power factor correction circuit is inhibited. Switching of the PFC recommences as soon as the VoSense pin voltage drops below the $V_{OVP(VoSense)}$ level again.

When the resistor between pin VoSense and ground is open, the over voltage protection will also trigger.

7.2.10 PFC open loop protection (VoSense pin)

The power factor correction circuit will not start switching until the voltage on the VoSense pin is above the $V_{short(VoSense)}$ level. This will protect the circuit from open loop situations. As the VoSense pin draws a small input current, switching is also inhibited when the pin is left open.

As long as the voltage on the VoSense pin is below the $V_{short(VoSense)}$ level, the voltage on the PFCcomp pin will be clamped to the $V_{clamp,PFC}$ level 2.7V (typ.)

7.2.11 Driver (pin PFCdriver)

The driver circuit to the gate of the power MOSFET has a current sourcing capability of typically -500 mA and a current sink capability of typically 1.2 A. This permits fast turn-on and turn-off of the power MOSFET for efficient operation.

7.3 Functional description flyback controller

The TEA1750 includes a controller for a flyback converter. The flyback converter operates in quasi resonant or discontinuous conduction mode with valley switching. The auxiliary winding of the flyback transformer provides demagnetization detection and powers the IC after start-up.

7.3.1 Multi mode operation

The TEA1750 flyback controller can operate in multi modes; see Figure 7

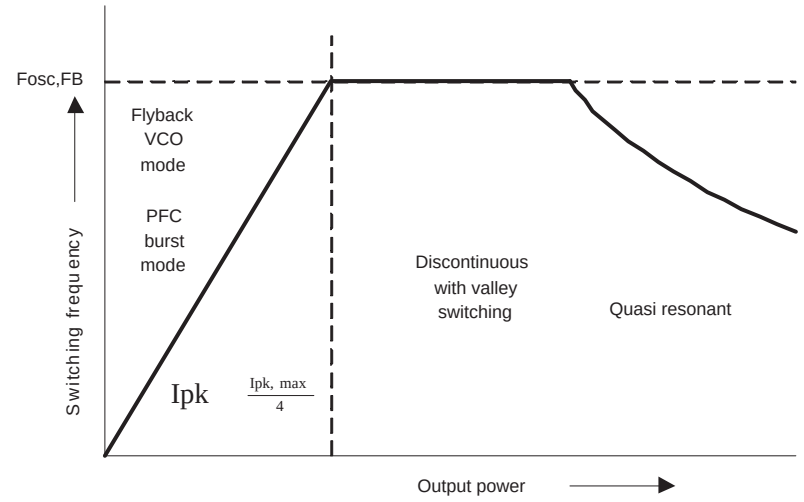


Fig 7. Multi mode operation flyback

At high output power the converter will switch in quasi resonant mode. The next converter stroke is started after demagnetization of the transformer current. In quasi resonant mode switching losses are minimized as the converter only switches on when the voltage across the external MOSFET is at its minimum (valley switching, see also Section 7.3.2).

To prevent high frequency operation at lower loads, the quasi-resonant operation changes in discontinuous mode operation with valley skipping in which the switching frequency is limited to $F_{osc,FB}$ (125kHz typ.). Again the external MOSFET is only switched on when the voltage across the MOSFET is at its minimum.

At very low power and standby levels the frequency is controlled down by a voltage controlled oscillator (VCO). The minimum frequency can be reduced to zero. During VCO mode, the primary peak current is kept at a minimal level of Ipkmax/4 to maintain a high efficiency. (Ipkmax is the maximum primary peak current set by the sense resistor and the maximum sense voltage) As the primary peak current is low in VCO operation (Ipk=Ipkmax/4), no audible noise will be noticeable at switching frequencies in the audible range. Also here valley switching is active.

In VCO mode the PFC controller is switched to burst mode operation and the flyback maximum frequency changes linearly with the control voltage on the FBctrl pin (see Figure 8). At no load operation the switching frequency can be reduced to (almost) zero.

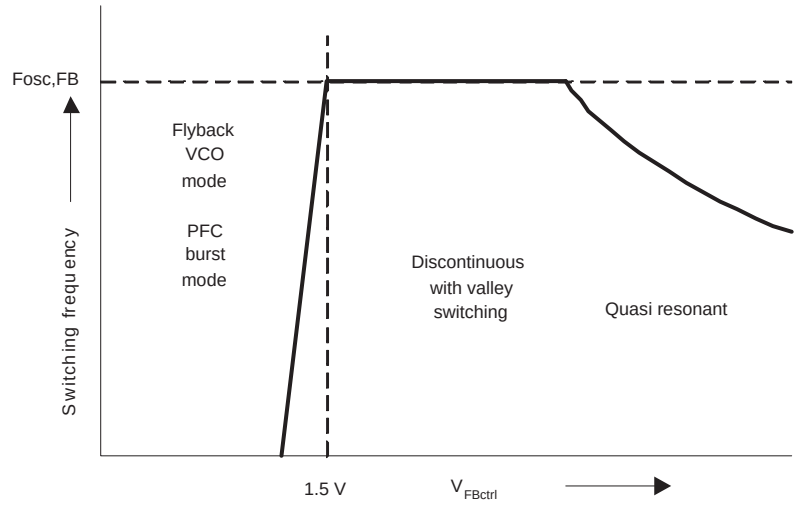


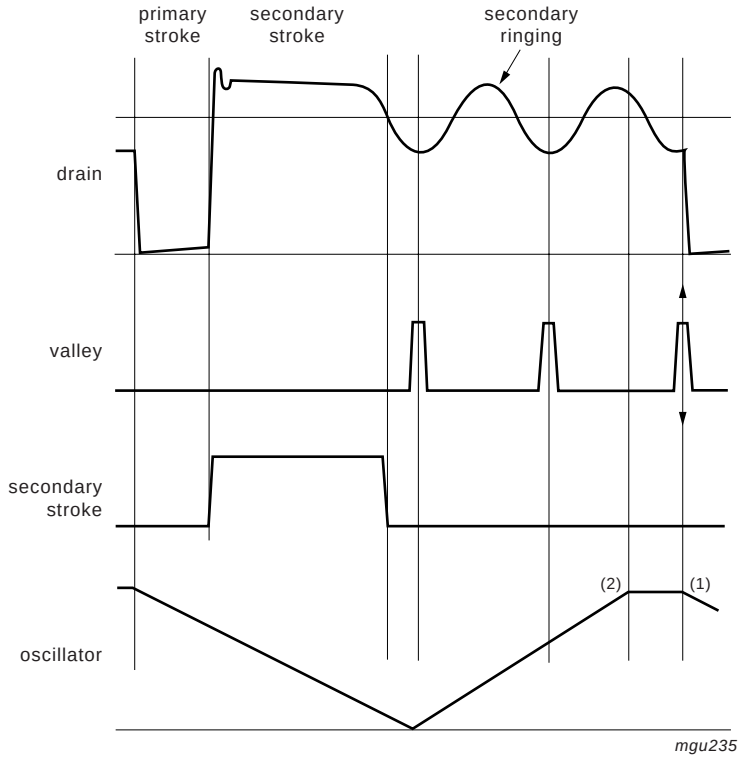
Fig 8. Frequency control of flyback part

7.3.2 Valley switching (HV pin)

Refer to Figure 9. A new cycle starts when the external MOSFET is activated. After the on-time (determined by the FbSense voltage and the FbCtrl voltage), the MOSFET is switched off and the secondary stroke starts. After the secondary stroke, the drain voltage shows an oscillation with a frequency of approximately $\frac{1}{(2 \times \pi \times \sqrt{(L_p \times C_d)}}$ where L_p is the primary self inductance of the flyback transformer and C_d is the capacitance on the drain node.

As soon as the internal oscillator voltage is high again and the secondary stroke has ended, the circuit waits for the lowest drain voltage before starting a new primary stroke. This method is called valley detection. Figure 9 shows the drain voltage, valley signal, secondary stroke signal and the internal oscillator signal.

Valley switching will allow high frequency operation as capacitive switching losses $\left(P = \frac{1}{2} \times C_d \times V^2 \times f\right)$ are reduced. High frequency operation makes small and cost effective magnetics possible.



(1) Start of new cycle at lowest drain voltage.

(2) Start of new cycle in a classical PWM system without valley detection.

Fig 9. Signals for valley switching.

7.3.3 Current mode control (FBsense pin)

Current mode control is used for the flyback converter for its good line regulation.

The primary current is sensed by the FBsense pin across an external resistor and compared with an internal control voltage.The internal control voltage is proportional to the FBctrl pin voltage.

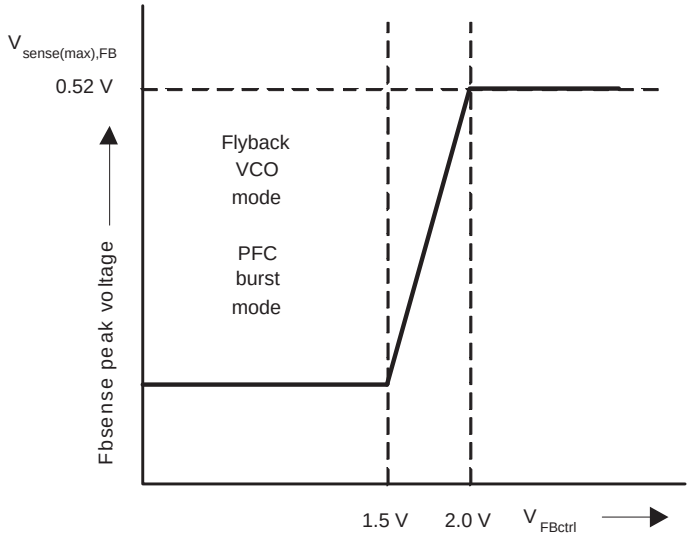


Fig 10. Frequency control of flyback part

The driver output is latched in the logic, preventing multiple switch-on.

7.3.4 Demagnetization (FBaux pin)

The system will be in quasi resonant or discontinuous conduction mode all the time. The internal oscillator will not start a new primary stroke until the previous secondary stroke has ended.

Demagnetization features a cycle-by-cycle output short-circuit protection by immediately lowering the frequency (longer off-time), thereby reducing the power level.

Demagnetization recognition is suppressed during the first t_{supp} time (2µsec. typ). This suppression may be necessary at low output voltages and at start-up and in applications where the transformer has a large leakage inductance.

If pin FbAux is open-circuit or not connected, a fault condition is assumed and the converter will stop operating immediately. Operation will recommence as soon as the fault condition is removed.

7.3.5 Flyback Control / time out (FBctrl pin)

The pin FBctrl is connected to an internal voltage source of 3.5V via an internal resistor. (typical resistance is 3kΩ). As soon as the voltage on this pin is above 2.5V (typ), this connection is disabled. Above 2.5V the pin is biased with a small current. When the voltage on this pin rises above 4.7V (typ), a fault is assumed and switching is inhibited.

When a small capacitor is connected to this pin, a time-out function can be realized to protect for an open control loop situation. The time-out function can be disabled by placing a resistor (100kΩ) to ground on the FBctrl pin.

If the pin is shorted to ground, switching of the flyback controller is inhibited.

In normal operating conditions, when the converter is regulating the output voltage, the voltage on the FBctrl pin will be between 1.4V and 2.0V (typical values) from minimum to maximum output power.

7.3.6 Soft start-up (pin FbSense)

To prevent transformer rattle during start-up, the transformer peak current, $I_{DM,FB}$ is slowly increased by the soft start function. This can be achieved by inserting a resistor and a capacitor between pin FbSense and the current sense resistor.

An internal current source charges the capacitor to $V = I_{startup(soft),FB} \times R_{SS2}$, with a maximum of approximately 0.5 V.

The start level and the time constant of the increasing primary current level can be adjusted externally by changing the values of R_{SS2} and C_{SS2}.

$$I_{DM,FB} = \frac{V_{sense(max),FB} - (I_{startup(soft)),FB} \times R_{SS2})}{R_{sense2}}$$

$$\tau = R_{SS2} \times C_{SS2}$$

The soft start current $I_{startup(soft),FB}$ is switched on as soon as Vcc reaches V_{start}. As soon as the voltage on the VoSense pin reaches the $V_{start,FB}$ level and the voltage on pin FBsense has reached 0.5V, the flyback converter will start switching.

The soft start current will flow as long as the voltage on pin FBsense is below approximately 0.5 V. If the voltage on pin FBsense exceeds 0.5 V, the soft start current source will start limiting the current. After the flyback converter has started, the soft start current source is switched off.

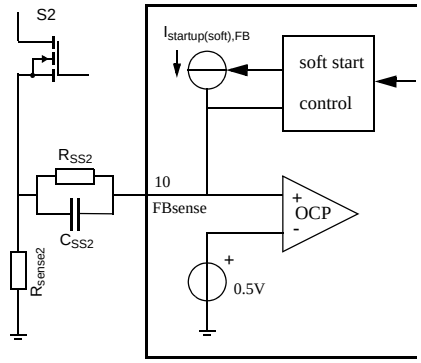


Fig 11. Soft start-up of flyback.

7.3.7 Maximum on-time

The flyback controller limits the ‘on-time’ of the external MOSFET to 25 µs (typ.). When the ‘on-time’ is longer than 25 µs, the IC will stop switching and enter the safe restart mode.

7.3.8 Over-voltage protection (FBaux pin)

An output over-voltage protection is implemented in the GreenChip III series. This works for the TEA1750 by sensing the auxiliary voltage via the current flowing into pin FbAux during the secondary stroke. The auxiliary winding voltage is a well-defined replica of the output voltage. Voltage spikes are averaged by an internal filter.

If the output voltage exceeds the OVP trip level, an internal counter starts counting subsequent OVP event. The counter has been added to prevent incorrect OVP detection which might occur during ESD or lightning events. If the output voltage exceeds the OVP trip level a few times and not again in a subsequent cycle, the internal counter will count down with twice the speed

compared with counting-up. However, when typical 10 cycles of subsequent OVP events are detected, the IC assumes a true OVP and the OVP circuit switches the power MOSFET off. As the protection is latched, the converter will only restart after the internal latch is reset. In a typical application the mains should be interrupted to reset the internal latch.

The output voltage $V_{o(OVP)}$ at which the OVP function trips, can be set by the demagnetization resistor, R_{FbAux}:

$$V_{o(OVP)} = \frac{N_s}{Naux}\{I_{OVP(FBaux)} \times R_{FBaux} + V_{clamp(pos)}\}$$

where N_s is the number of secondary turns and N_{aux} is the number of auxiliary turns of the transformer.

Current $I_{OVP(FBaux)}$ is internally trimmed.

The value of R_{FBaux} can be adjusted to the turns ratio of the transformer, thus making an accurate OVP possible.

7.3.9 Over-current Protection (FBsense pin)

The primary peak-current in the transformer is measured accurately cycle-by-cycle using the external sense resistor R_{sense2}. The OCP circuit limits the voltage on pin FBsense to an internal level (see also Section 7.3.3). The OCP detection is suppressed during the leading edge blanking period t_{leb} to prevent false triggering caused by switch-on spikes.

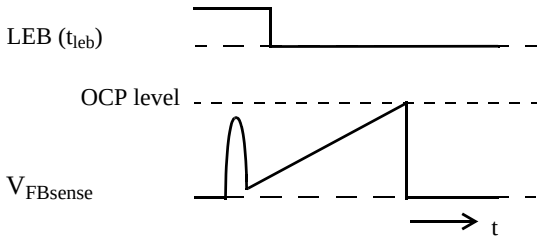


Fig 12. OCP leading edge blanking

7.3.10 Driver (pin FBdriver)

The driver circuit to the gate of the external power MOSFET have a current sourcing capability of -500 mA typical and a current sink capability of 1.2 A typical. This permits fast turn-on and turn-off of the power MOSFET for efficient operation.

8. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground (pin 2); positive currents flow into the chip; pin V_{CC} may not be current driven. The voltage ratings are valid provided other ratings are not violated; current ratings are valid provided the maximum power rating is not violated.

Symbol	Parameter	Conditions		Min	Max	Unit
Voltages						
V_{CC}	supply voltage	continuous		–0.4	+38	V
V_{Latch}	voltage on pin Latch	continuous		–0.4	+5	V
V_{FBctrl}	voltage on pin FBctrl			–0.4	+5	V
$V_{PFCcomp}$	voltage on pin PFCcomp			–0.4	+5	V
$V_{VinSense}$	voltage on pin VinSense			–0.4	+5	V
$V_{VoSense}$	voltage on pin VoSense			–0.4	+5	V
V_{PFCaux}	voltage on pin PFCaux			–25	+25	V
$V_{FBsense}$	voltage on pin FBsense	current limited		–0.4	+5	V
$V_{PFCsense}$	voltage on pin PFCsense	current limited		–0.4	+5	V
V_{HV}	voltage on pin HV			–0.4	+650	V
Currents						
I_{FBctrl}	current on pin FBctrl			-3	0	mA
I_{FBaux}	current on pin FBaux			–1	+1	mA
$I_{PFCsense}$	current on pin PFCsense			–1	+10	mA
$I_{FBsense}$	current on pin FBsense			–1	+10	mA
$I_{FBdriver}$	current on pin FBdriver	d < 10 %		–0.8	+2	A
$I_{PFCdriver}$	current on pin PFCdriver	d < 10 %		–0.8	+2	A
I_{HV}	current on pin HV			-	5	mA
General						
P_{tot}	total power dissipation	T_{amb} < 75 °C				
		SO16 package		-	0.6	W
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–20	+150	°C
ESD						
V_{ESD}	electrostatic discharge voltage	class 1				
	human body model	pins 1 to 13	[1]	-	2000	V
		pin 16 (HV)	[1]	-	1500	V
	machine model		[2]	-	200	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] Equivalent to discharging a 200 pF capacitor through a 0.75 µH coil and a 10 Ω resistor.

9. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; JEDEC test board	124	K/W

10. Characteristics

Table 5: Characteristics

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Start-up current source (pin HV)						
I_{HV}	supply current drawn from pin HV	V_{HV} > 80 V;				
		$V_{CC} < V_{trip}$, $V_{UVLO}<Vcc<V_{startup}$		0.9		mA
		$V_{trip}< V_{CC} < V_{UVLO}$		5.4		mA
		with auxiliary supply	8	20	40	µA
V_{BR}	breakdown voltage		650	-	-	V
Supply voltage management (pin V_{CC})						
V_{trip}	VCC supply current trip point		0.55	0.65	0.75	V
$V_{startup}$	start-up voltage		21	22	23	V
$V_{th(UVLO)}$	undervoltage lockout threshold voltage		14	15	16	V
$V_{hys, start}$	hysteresis voltage on start level	during start-up phase		0.3		V
V_{hys}	hysteresis voltage	$V_{start} - V_{UVLO}$	6.3	7	7.7	V
$I_{ch(low)}$	low charging current	V_{HV} > 80 V; $V_{CC} < V_{trip}$ or $V_{UVLO}<Vcc<V_{start}$		–0.9		mA
$I_{ch(high)}$	high charging current	V_{HV} > 80 V; $V_{trip} < V_{CC} < V_{UVLO}$	–4.6	–5.4	–6.3	mA
$I_{CC(oper)}$	operating supply current	no load on pin FBdriver and PFCdriver	2.25	3	3.75	mA
Input Voltage Sensing PFC (pin VinSense)						
$V_{stop(VinSense)}$	Low input voltage detection level		0.87	0.9	0.93	V
$V_{start(VinSense)}$	Input voltage detection level		1.11	1.15	1.19	V
$V_{delta(VinSense)}$	Input voltage pull-up under $V_{start(VinSense)}$	active after $V_{stop(VinSense)}$ is detected		–100		mV
$I_{delta(VinSense)}$	Maximum input voltage pull-up current	active after $V_{stop(VinSense)}$ is detected	–55	–47	–40	µA
$V_{mult(VinSense)}$	Maximal input voltage for mains voltage compensation		4.0			V
$V_{reset(VinSense)}$	Fast latch reset level	active after V_{UVLO} is detected	60	110	160	mV
$V_{hyst,reset(VinSense)}$	Hysteresis on fast latch reset level		80	115	150	mV
$I_{in(VinSense)}$	Input current	$V_{VinSense}$>0.9V	10	33	100	nA
Loop compensation PFC(pin PFCcomp)						
g_m	Transconductance $V_{VoSense}$ to $I_{PFCcomp}$		60	80	100	µA/V

Table 5: Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{out,\ postive}$	Output current	$V_{VoSense}$=3.3V	33	39	45	µA
$I_{out,\ negative}$	Output current	$V_{VoSense}$=2.0V	-45	-39	-33	µA
$V_{clamp,PFC}$	Clamp level	Low power mode, PFC in burst mode [3]	2.5	2.7	2.9	V
$V_{zeroduty,PFC}$	Zero duty cycle voltage		3.4	3.5	3.6	V
$V_{maxduty,PFC}$	Maximum duty cycle voltage		1.20	1.25	1.30	V
Pulse width modulator PFC						
$t_{on(min,PFC)}$	minimum on-time	$V_{VinSense}$=3.3V	3.6	4.5	5.0	µs
$t_{on(max,PFC)}$	maximum on-time	$V_{VinSense}$=0.9V	30	40	53	µs
Output Voltage Sensing PFC (pin VoSense)						
$V_{short(VoSense)}$	Short pin detection level		0.35	0.40	0.45	V
$V_{start,FB}$	Start level for flyback converter			1.72 [2]		V
$V_{stop,FB}$	Stop level for flyback converter		1.55	1.60	1.65	V
$V_{burst,low}$	Low level during burst mode operation		1.87	1.92	1.97	V
$V_{burst,high}$	High level during burst mode operation		2.19	2.24	2.29	V
$V_{reg(VoSense)}$	regulation level for PFC, output current pin PFCcomp=0		2.475	2.500	2.525	V
$V_{OVPlow(VoSense)}$	OVP detection level (PFC disabled)		2.60	2.63	2.67	V
$I_{in(VoSense)}$	Input current	$V_{VoSense}$=2.5V	10	45	100	nA
Over-current protection PFC (pin PFCsense)						
$V_{sense(max),PFC}$	maximum sense voltage for PFC	ΔV/Δt = 50mV/µs	0.49	0.52	0.55	V
		ΔV/Δt = 200mV/µs	0.51	0.54	0.57	V
$t_{leb,PFC}$	leading edge blanking time		250	310	370	ns
$I_{prot(PFCsense)}$	pin protection current		–50	-	–10	nA
Soft start, soft stop PFC (pin PFCsense)						
$I_{startup(soft),PFC}$	soft startup current		45	60	75	µA
$V_{SoftStart,PFC}$	soft start maximum pin voltage		0.46	0.50	0.54	V
$V_{SoftStop,PFC}$	soft stop voltage		0.42	0.45	0.48	V
$R_{SoftStart,PFC}$	minimum required external soft start resistor		12			kΩ
Oscillator PFC						
$f_{osc,max,PFC}$	maximum oscillator frequency		100	125	150	kHz
$t_{off,minimum}$	minimum off time		1.1	1.4	1.7	µs
Valley switching PFC (pin PFCaux)						
$\Delta V/\Delta t_{valley}$	valley recognition voltage change			-	1.7	V/µs
$\Delta V/\Delta t_{valley}$	voltage change no valley recognized		0.36	-		V/µs
$t_{time\text{-}out,valley}$	time-out valley detection		3	4	6	µs

Table 5: Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Demagnetization management PFC(pin PFCaux)						
$V_{th(PFCaux)}$	demagnetization comparator threshold voltage		-150	-100	-50	mV
$t_{time-out,demag}$	time-out demag detection		40	50	60	µs
$I_{prot(PFCaux)}$	open pin protection current	V_{PFCaux} = 50 mV	–50	-	–10	nA
Over Voltage Protection flyback (pin FBaux)						
$I_{OVP(FBaux)}$	OVP current on pin FBaux		279	300	321	µA
N_{OVP}	number of over voltage cycles before protection is triggered		6	8	12	
Demagnetization management flyback (pin FBaux)						
$V_{th(FBaux)}$	demagnetization comparator threshold voltage		60	80	110	mV
$I_{prot(FBaux)}$	open pin protection current	V_{FBaux} = 50 mV	–50	-	–10	nA
$V_{clamp(neg)}$	negative clamp voltage	I_{FBaux} = –500 µA	–1.0	–0.8	–0.6	V
$V_{clamp(pos)}$	positive clamp voltage	I_{FBaux} = 500 µA	0.5	0.7	0.9	V
t_{supp}	suppression of transformer ringing at start of secondary stroke		1.5	2	2.5	µs
Pulse width modulator flyback						
$t_{on(min,flyback)}$	minimum on-time		-	t_{leb}	-	ns
$t_{on(max,flyback)}$	maximum on-time		20	25	30	µs
Oscillator flyback						
$f_{osc,high,FB}$	high oscillator frequency		100	125	150	kHz
$V_{FBctrl,VCO\ start}$	Voltage on pin FBctrl for start frequency reduction		1.3	1.5	1.7	V
$V_{Delta,FBctrl}$	Delta voltage on pin FBctrl from start frequency reduction to frequency is zero			-0.1		V
Duty cycle control flyback (pin FBctrl)						
$V_{FBctrl,max}$	voltage for maximum duty cycle		1.85	2.0	2.15	V
V_{FBctrl}	Internal voltage for FBctrl			3.5		V
$V_{FBctrl,off}$	Internal resistor switch off level			2.5		V
R_{FBctrl}	Internal resistance between the V_{FBctrl} voltage source and the FBctrl pin			3		kΩ
I_{FBctrl}	FBctrl pin current	V_{FBctrl}=0V	–1.4	–1.17	–0.93	mA
I_{FBctrl}	FBctrl pin current	V_{FBctrl}=2V	–0.6	–0.5	–0.4	mA
$V_{TimeOut}$	Time out voltage level		4.1	4.5	4.9	V
$I_{TimeOut}$	Time out current	V_{FBctrl}>$V_{FBctrl,off}$	–36	–30	–24	µA
Valley switching flyback (pin HV)						
$\Delta V/\Delta t_{valley}$	valley recognition voltage change		–75	-	+75	V/µs
$t_{valley-swon}$	delay from valley recognition to switch-on	[1]	-	150	-	ns

Table 5: Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Soft start flyback (pin FBsense)						
$I_{startup(soft),FB}$	soft start current		45	60	75	µA
$U_{SoftStart,FB}$	soft start maximum pin voltage		0.46	0.5	0.54	V
$R_{SoftStart,FB}$	minimum required external soft start resistor		12			kΩ
Over-current protection flyback (pin FBsense)						
$V_{sense(max),FB}$	maximum sense voltage for FB	ΔV/Δt = 50mV/µs	0.49	0.52	0.55	V
		ΔV/Δt = 200 mV/µs	0.51	0.54	0.58	V
$t_{leb,FB}$	leading edge blanking time		255	305	355	ns
Driver (pin FBdriver and PFCdriver)						
I_{source}	source current	V_{driver} = 2 V	-	−0.5		A
I_{sink}	sink current	V_{driver} = 2 V		0.7		A
		V_{driver} = 10 V	-	1.2	-	A
$V_{o(max)}$	maximum driver output voltage		-	11	12	V
Latch input (pin Latch)						
$V_{prot(Latch)}$	Latch pin protection level		1.23	1.25	1.27	V
I_{Latch}	Latch pin current	$V_{prot(Latch)} < V_{Latch} < V_{open(Latch)}$	−85	−80	−75	µA
$V_{enable(Latch)}$	Latch pin enabling level	at start-up	1.30	1.35	1.40	V
$V_{hys(Latch)}$	Latch pin hysteresis	$V_{enable(Latch)}$-$V_{prot(Latch)}$	80	100	120	mV
$V_{open(Latch)}$	Latch pin voltage	Latch pin open	2.5	2.75	3	V
Temperature protection						
$T_{prot(max)}$	maximum temperature protection level		130	140	150	°C
$T_{prot(hyst)}$	hysteresis for the temperature protection level		-	10	-	°C

[1] Guaranteed by design.

[2] Typically 120mV above $V_{stop,FB}$.

[3] For a typical application with a compensation network on pin PFCcomp like in Figure 3

11. Application information

A power supply with the TEA1750 consists of a power factor correction circuit followed by a flyback converter. See Figure 13

Capacitor C_{VCC} buffers the IC supply voltage, which is powered via the high voltage rectified mains during start-up and via the auxiliary winding of the flyback converter during operation. Sense resistor R_{sense1} and R_{sense2} convert the current through the MOSFET S1 and S2 into a voltage at pin PFCsense and FBsense. The values of $R_{sense1}$and R_{sense2} define the maximum primary peak current in MOSFETS S1 and S2. In the example given, the Latch pin is connected to a NTC resistor. When the resistance drops below $V_{prot(Latch)}/I_{latch}$=15.6kΩ (typ.) the protection will be

activated. A capacitor $C_{TimeOut}$ is connected to the FBctrl pin. For a 120nF capacitor, typically after 10 msec the time-out protection is activated. A resistor R_{loop} is added such that the time-out capacitor does not interfere with the normal regulation loop.

Resistors R_{S1} and RS2 are added to prevent that the soft-start capacitors are charged during normal operation due to negative voltage spikes across the sense resistors.

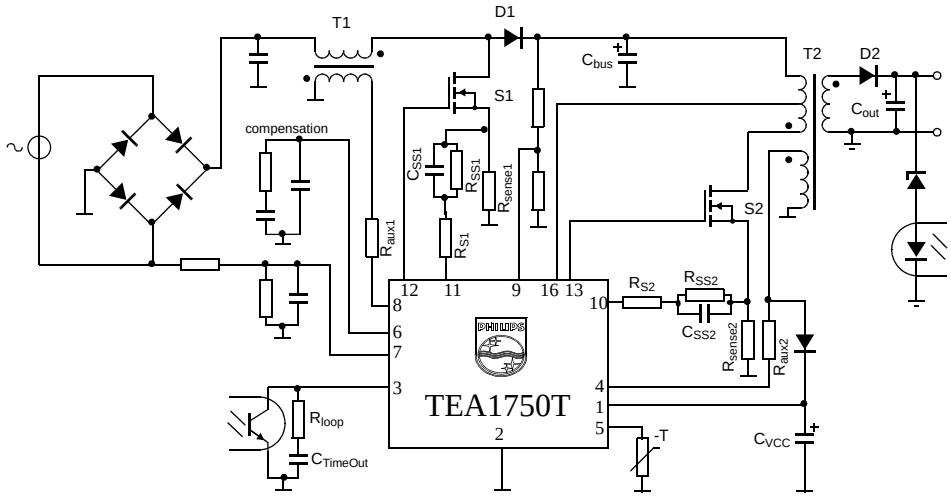


Fig 13. Typical application diagram.

12. Test information

12.1 Quality information

The *General Quality Specification for Integrated Circuits, SNW-FQ-611* is applicable.

13. Package outline

14. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
TEA1750_v0.10	not released	Objective data	-	xxxx xxx xxxx0	TEA1750_v0.9

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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20. Figures

21. Contents

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