GENERAL DESCRIPTION

XN1042 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications. PWM switching frequency at normal operation is externally programmable and trimmed to tight range. At no load or light load condition, the IC operates in extended 'burst mode' to minimize switching loss. Lower standby power and higher conversion efficiency is thus achieved. VDD low startup current and low operating current contribute to a reliable power on startup design with XN1042. A large value resistor could thus be used in the startup circuit to minimize the standby power. The internal slope compensation improves system large signal stability and reduces the possible subharmonic oscillation at high PWM duty cycle output. Leading-edge blanking on current sense input removes the signal glitch due to snubber circuit diode reverse recovery. This greatly helps to reduce the external component count and system cost in application.

XN1042 offers complete protection coverage with automatic self-recovery feature including Cycle by Cycle current limiting (OCP), over load protection (OLP), over temperature protection (OTP), VDD over voltage protection (OVP) and under voltage lockout (UVLO). The Gate-drive output is clamped at 18V to protect the power MOSFET. In XN1042, OCP threshold slope is internally optimized for 50KHz switching frequency application to reach constant output power limit over universal AC input range. Excellent EMI performance is achieved with soft switching control at the totem pole gate drive output.

TYPICAL APPLICATION

The tone energy at below 20KHZ is minimized in operation. Consequently, audio noise performance is greatly improved. XN1042 is offered in both SOP-8 and DIP-8 packages.

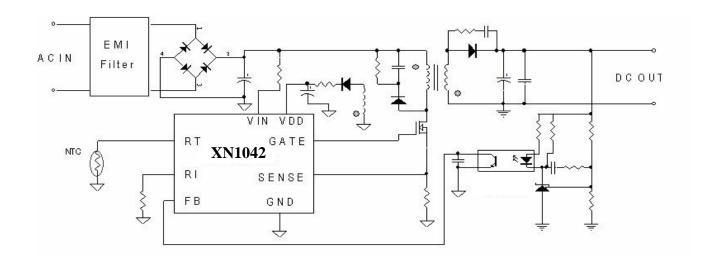
FEATURES

- Extended Burst Mode Control For Improved
- ■Efficiency and Minimum Standby Power Design
- Audio Noise Free Operation
- ■External Programmable PWM Switching Frequency
- ■Internal Synchronized Slope Compensation
- ■Low VIN/VDD Startup Current(6.5uA) and Low Operating Current (2.3mA)
- ■Leading Edge Blanking on Current Sense Input
- ■Complete Protection Coverage With Auto Self-Recovery
- ExternalProgrammable Over Temperature Protection (OTP)
- ■With or Without Built in VDD OVP for System OVP
- ■Under Voltage Lockout with Hysteresis (UVLO)
- ■Gate Output Maximum Voltage Clamp (18V)
- ■Line Compensated Cycle-by-Cycle Over current Threshold Setting For Constant Output Current Limiting Over Universal Input Voltage Range (OCP)
- ■Over Load Protection. (OLP)

APPLICATIONS

Offline AC/DC flyback converter for

- ■Laptop Power Adaptor
- ■PC/TV/Set-Top Box Power Supplies
- ■Open-frame SMPS
- ■Battery Charger



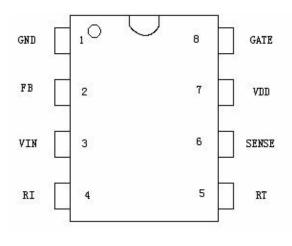
GENERAL INFORMATION

Absolute Maximum Ratings

Parameter	Value
VDD/VIN DC Supply Voltage	30 V
VDD Clamp Voltage	35 V
VDD Clamp Continuous Current	10 mA
V _{FB} Input Voltage	-0.3 to 7V
Vsense Input Voltage to Sense Pin	-0.3 to 7V
VRT Input Voltage to RT Pin	-0.3 to 7V
V _{RI} Input Voltage to RI Pin	-0.3 to 7V
Min/Max Operating Junction	
Temperature T _J	-20 to 150°C
Min/Max Storage Temperature T _{stg}	-55 to 160°C
Lead Temperature (Soldering, 10 secs)	260°C

Pin Assignment

The XN1042 is offered in DIP and SOP Packages shown as below.



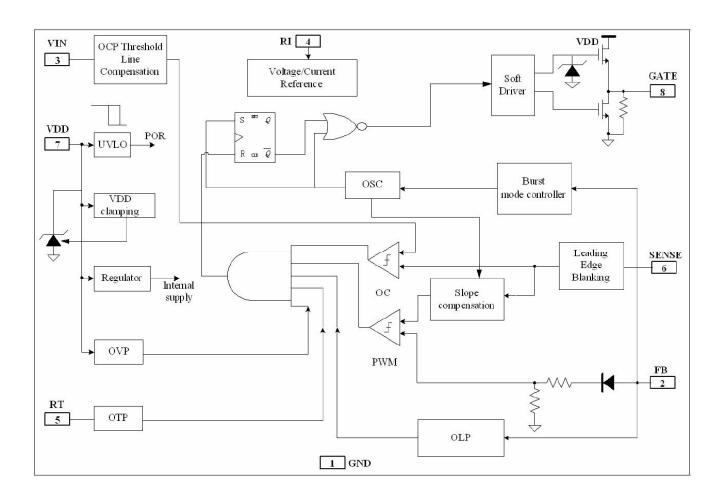
Terminal Definition

Pin Num	Pin Name	I/O	Description .
1	GND	P	Ground
2	FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin 6.
3	VIN	I	Connected through a large value resistor to rectified line input for Startup IC supply and line voltage sensing.
4	RI	I	Internal Oscillator frequency setting pin. A resistor connected between RI and GND sets the PWM frequency.
5	RT	I	Temperature sensing input pin. Connected through a NTC resistor to GND
6	SENSE	I	Current sense input pin. Connected to MOSFET current sensing resistor node.
7	VDD	P	IC DC power supply pin.
8	GATE	О	Totem-pole gate drive output for the power MOSFET

RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min/Max	Unit
VDD	VDD Supply Voltage	12 to 23	V
RI	RI Resistor Value	24	Kohm
TA	Operating Ambient Temperature	-20 to 85	οС

Block Diagram



ESD INFORMATION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
HBM ^{Note}	Human Body Model	MIL-STD		3		KV
	on All Pins Except					
	VIN and VDD					
MM	Machine Model on	JEDEC-STD		250		V
	All Pins					

Note: HBM all pins pass 3KV except High Voltage Input pin. The details are VIN passes 1kV, VDD passes 1.5KV, all other I/Os pass 3KV. In system application, High Voltage Input pin is either a high impedance input or connected to a cap. The lower rating has minimum impacts on system ESD performance.

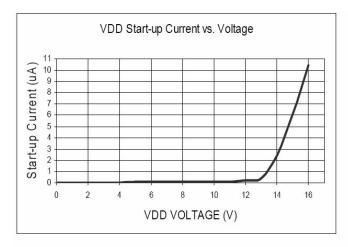
ELECTRICAL CHARACTERISTICS

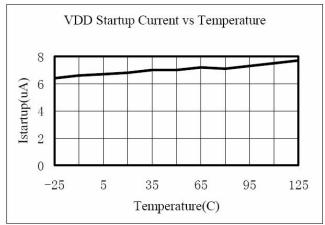
(Γ_{A}	$= 25^{\circ}C$, VDD=16V	√, RI=24Kohm	if not ot	herwise noted)

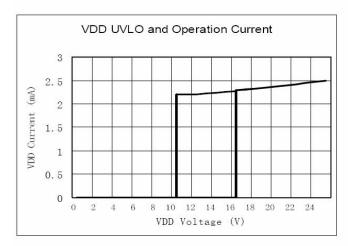
Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Supply Voltage (V.	DD)	3	W.	3.000		19
I_VDD_Startup	VDD Start up	VDD=15V, Measure		6.5	20	uA
	Current	current into VDD				
I_VDD_Operation	Operation Current	$V_{FB}=3V$		2.3		mA
UVLO(Enter)	VDD Under		9.5	10.5	11.5	V
	Voltage Lockout					
	Enter					
UVLO(Exit)	VDD Under		15.5	16.5	17.5	V
	Voltage Lockout					
	Exit (Startup)					
OVP(ON)*Optional	VDD Over Voltage		23.5	25	26.5	V
	Protection Enter					
OVP(OFF)*Optional	VDD Over Voltage		21.5	23	24.5	V
	Protection Exit					
	(Recovery)					
OVP Hys*Optional	OVP Hysteresis	OVP(ON)-OVP(OFF)		2		V
T _D OVP	VDD OVP			80		uSec
	Debounce time			Section		50.400.0000000000
V _{DD} Clamp	V _{DD} Zener Clamp	$I(V_{DD}) = 5 \text{ mA}$		35		V
	Voltage	, /				
Feedback Input Se	ection(FB Pin)	*		-22		
A _{VCS}	PWM Input Gain	$\Delta\mathrm{V_{FB}}/\Delta\mathrm{V_{cs}}$		2.8		V/V
V _{FB} Open	V _{FB} Open Voltage	12 63		5.9		V
· 1D I	15 - 17 - 17 - 18 - 18 - 18 - 18 - 18 - 18					
I _{FB} Short	FB pin short circuit	Short FB pin to GND,	1	0.80		mA
-1 <u>D_</u>	current	measure current)F8858-5
V_{TH}_0D	Zero Duty Cycle				0.95	V
111	FB Threshold				7.1.7.07.0	
	Voltage					
V _{TH} BM	Burst Mode FB			1.7		V
111	Threshold Voltage					
V _{TH} PL	Power Limiting FB			4.4		V
111	Threshold Voltage					
T _D _PL	Power limiting		ES .	80		mSec
- D_* -	Debounce Time					
Z _{FB} IN	Input Impedance		2	9.0		Kohm
Current Sense Inp			7,0	1 0	1	
T blanking	Sense Input		Ť	250		nS

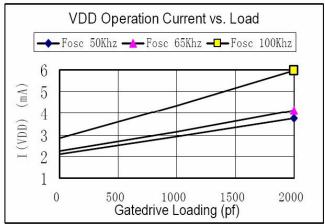
	Leading Edge					
	Blanking Time					
Z _{SENSE} _IN	Sense Input Impedance			30		Kohm
T _D OC	Over Current Detection and Control Delay	CL=1nf at GATE,		120		nSec
V _{TH} _OC_0	Current Limiting Threshold at No Compensation	I(VIN) = 0uA	0.85	0.90	0.95	V
V _{TH} _OC_1	Current Limiting Threshold at Compensation	I(VIN) = 150uA		0.81		V
Oscillator	<u> </u>	I.	Lis.	L	th:	1
Fosc	Normal Oscillation Frequency		61	65	69	KHZ
Δf _Temp	Frequency Temperature Stability	-20°C to 100 °C		2		%
Δf_{VDD}	Frequency Voltage Stability	VDD = 12-25V		2		%
RI range	Operating RI Range		12	24	60	Kohm
V RI open	RI open voltage		0 000	2.0		V
F_BM	Burst Mode Base Frequency			22		KHZ
DC_max	Maxmum Duty Cycle		75	80	85	%
DC_min	Minimum Duty Cycle		-	-	0	%
Gate Drive Outpu	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1			W/	,	1.0
VOL	Output Low Level	Io = -20 mA		Î	0.3	V
VOH	Output High Level	Io = +20 mA	11			V
VG_Clamp	Output Clamp Voltage Level	VDD =20V		18		V
Tr	Output Rising Time	CL = 1nf		120		nSec
<u></u>	Output Falling Time	CL = 1nf		50		nSec
Over Temperatur		1	T.	1	1	1
I_RT	Output Current of RT pin			70		uA
V _{TH} _OTP	OTP Threshold Voltage		1.015	1.065	1.115	V
V _{TH} _OTP_off	OTP Recovery Threshold Voltage			1.165		V
T _D OTP	OTP De-bounce			100		uSec
	Time					

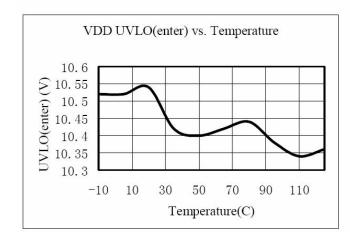
CHARACTERIZATION PLOTS

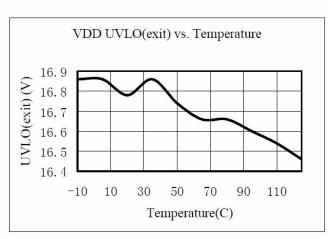


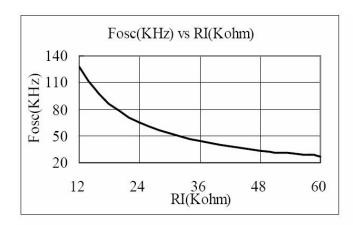


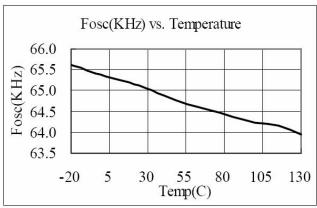


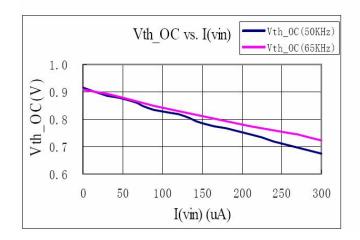


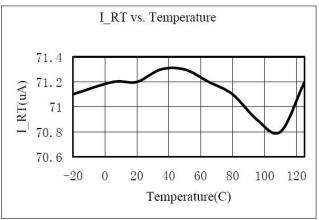












OPERATION DESCRIPTION

The XN1042 is a highly integrated PWM controller IC optimized for offline flyback converter applications. The extended burst mode control greatly reduces the standby power consumption and helps the design easily meet the international power conservation requirements.

Startup Current and Start up Control

Startup current of XN1042 is designed to be very low So that VDD could be charged up above UVLO(exit) threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application. For a typical AC/DC adaptor with universal input range design, a 2 M Ω , 1/8 W startup resistor could be used together with a VDD capacitor to provide a fast startup and yet low power dissipation design solution.

Operating Current

The Operating current of XN1042 is low at 2.3mA. Good efficiency is achieved with XN1042 low operating current together with extended burst mode control schemes.

Burst Mode Operation

At zero load or light load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy. XN1042 self adjusts the switching mode according to the loading condition. At from no load to light/medium load condition, the FB input drops below burst mode threshold level (1.8V). Device enters Burst Mode control. RT pin becomes lower at high temperature. The internal The Gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss thus reduce the standby power consumption to the greatest extend. The nature of high frequency switching also reduces the audio noise at any loading conditions.

Oscillator Operation

A resistor connected between RI and GND sets the constant current source to charge/discharge the internal cap and thus the PWM oscillator frequency is determined. The relationship between RI and switching frequency follows the below equation within the specified RI in Kohm range at nominal loading operational condition.

Fosc
$$\frac{1560}{RI(Kohm)}$$
 (KHZ)

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in XN1042 current mode PWM controller. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to snubber diode reverse recovery so that the external RC filtering on sense input is no longer required. The current limit comparator is disabled and thus cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Over Temperature Protection

A NTC resistor in series with a regular resistor should connect between RT and GND for temperature sensing and protection. NTC resistor value becomes lower when the ambient temperature rises. With the fixed internal current IRT flowing through the resistors, the voltage at OTP circuit is triggered and shutdown the MOSFET when the sensed input voltage is lower than V_{TH} OTP.

Gate Drive

XN1042 Gate is connected to the Gate of an external MOSFET for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI.

Good tradeoff is achieved through the built-in totem

pole gate drive design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 18V clamp is added for MOSFET gate protection at higher than expected VDD input.

Protection Controls

Good system reliability is achieved with XN1042's rich protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP), over temperature protection (OTP), on-chip VDD over voltage protection (OVP, optional) and under voltage lockout (UVLO). The OCP threshold value is self adjusted lower at higher current into VIN pin. This OCP threshold slope adjustment helps to compensate the increased output power limit at higher AC voltage caused by inherent Over-Current sensing and control delay. A constant output power limit is achieved with recommended OCP compensation scheme on XN1042. At output overload condition, FB voltage is biased higher. When FB input exceeds power limit threshold value for more than 80mS, control circuit reacts to turnoff the power MOSFET. Similarly, control circuit shutdowns the power MOSFET when an Over Temperature condition is detected. XN1042 resumes the operation when temperature drops below the hysteresis value. VDD is supplied with transformer auxiliary winding output. It is clamped when VDD is higher than 35V. MOSFET is shut down when VDD drops below UVLO(enter) limit and device enters power on start-up sequence thereafter.