ICB1FL02G
Smart Ballast Control IC for Fluorescent Lamp Ballasts

Power Management & Supply

Never stop thinking

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ICB1FL02G

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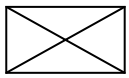

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Smart Ballast Control IC for Fluorescent Lamp Ballasts

Product Highlights

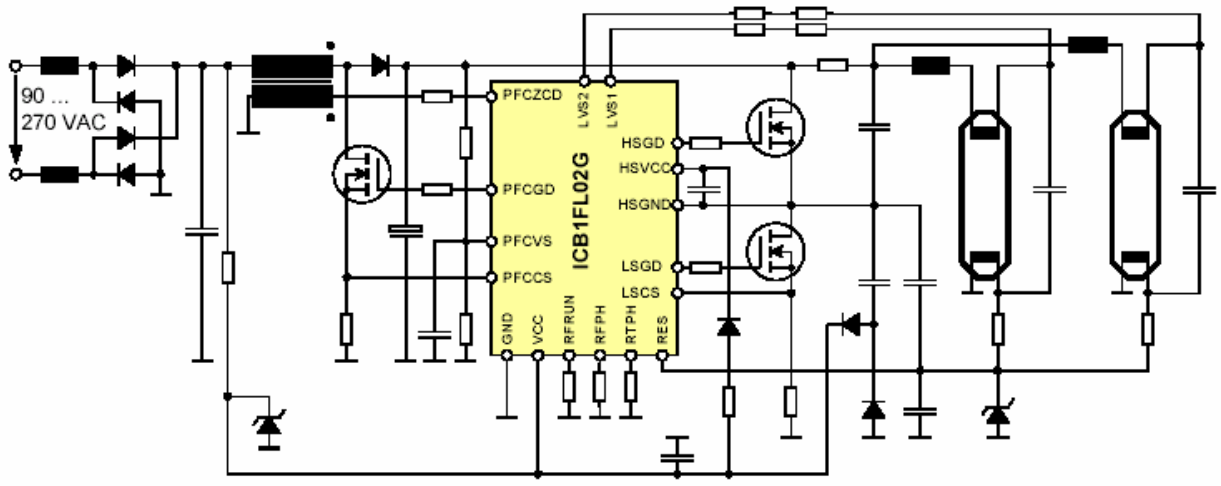
- **Lowest Count of external Components optimizes System Costs**
- **600V-Half-Bridge driver with coreless Transformer Technology**
- **Highest Ballast Reliability and minimized Parameter Spread**
- **Numerous Monitoring and Protection Features**
- **Minimum Start-Up- and Operation-Current**
- **Supports Multi-Lamp Designs**

Features PFC

- Discontinuous Mode PFC for Load Range 0 to 100%
- Integrated Compensation of PFC Control Loop
- Adjustable PFC Current Limitation
- Adjustable PFC Bus Voltage

Features Lamp Ballast Inverter

- Supports Restart after Lamp Removal and End-of-Life-Detection in Multi-Lamp Topologies
- End-of-Life (EOL) detected by adjustable +/- thresholds of sensed lamp voltage
- Rectifier Effect detected by ratio of +/- amplitude of lamp voltage
- Adjustable Detection of Overload and Rectifier Effect
- Detection of operation modes with Capacitive Load
- Self adaption of ignition time from 40ms to 235ms
- Parameters adjustable by Resistors only
- Pb-free Lead Plating; RoHS compliant



Description

The ICB1FL02G is designed to control a fluorescent lamp ballast including a discontinuous mode Power Factor Correction (PFC), a lamp inverter control and a high voltage level shift half-bridge driver.

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1 Introduction

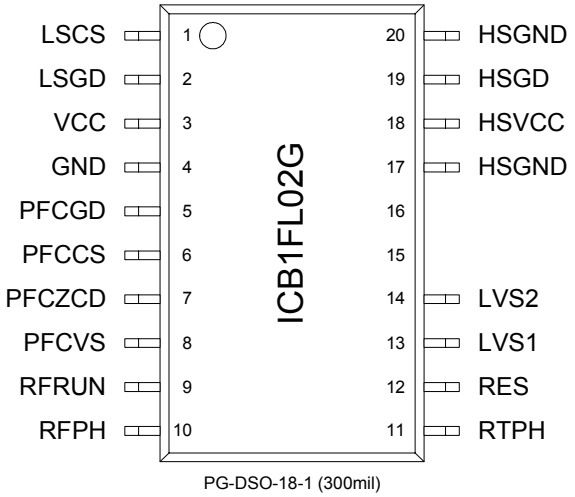


Fig. 1 Package PG-DSO-18-1 (300mil)

Pin	Symbol	Function
1	LSCS	Low side current sense (inverter)
2	LSGD	Low side Gate drive (inverter)
3	Vcc	Supply voltage
4	GND	Controller ground
5	PFCGD	PFC Gate drive
6	PFCCS	PFC current sense
7	PFCZCD	PFC zero current detector
8	PFCVS	PFC voltage sense
9	RFRUN	Set R for run frequency
10	RFPH	Set R for preheat frequency
11	RTPH	Set R for preheating time
12	RES	Restart after lamp removal
13	LVS1	Lamp voltage sense 1
14	LVS2	Lamp voltage sense 2
15	n.e.	Not existing
16	n.e	Not existing
17	HSGND	High side ground
18	HSVCC	High side supply voltage
19	HSGD	High side Gate drive (inverter)
20	HSGND	High side ground

Ballast Controller ICB1FL02G sets a new Benchmark

Infineon Technologies has introduced a new controller ICB1FL01G to control electronic lamp ballast for fluorescent lamps to the market. The control concept offers a unique set of features and a comprehensive functionality to operate single and multiple lamps at a minimum effort of external components.

The new generation of fluorescent lamps of the T4 and T5 type are optimized for high efficacy. In order to achieve long lifetimes they require a specific, more complex start-up procedure and an intensive monitoring of the operating behaviour compared to the older lamp T8 and T12 types. For these new generation lamps the IC offers an optimized functionality.

The ballast controller ICB1FL02G controls in a first functional block a boost converter as an active harmonic filter for the power factor correction. A second block of the IC controls a half-bridge inverter according to the level-shift method. The driver for the floating high-side MOSFET makes use of the new Coreless Transformer technology. The inverter feeds the lamp via a resonant circuit. Different operating modes such as softstart, preheating ignition and run mode according to a fixed and adjustable timing sequence are controlled by the operating frequency of the inverter. The device detects a lamp removal as well as the dangerous rectifier effect at the lamp's end of life in configurations of one, two and 4 lamps.

The device processes analogue as well as digital signals offering a more precise control of the operation flow and monitoring criteria by adjustable and defined time periods. The adjustment of the parameters determining time and frequency is done solely by resistors, completely avoiding any capacitors for this task. The ballast controller ICB1FL02G is manufactured in a 20V BICMOS technology with a minimum feature size of 0.6µm and 3 metal layers.

2 Functional IC Description

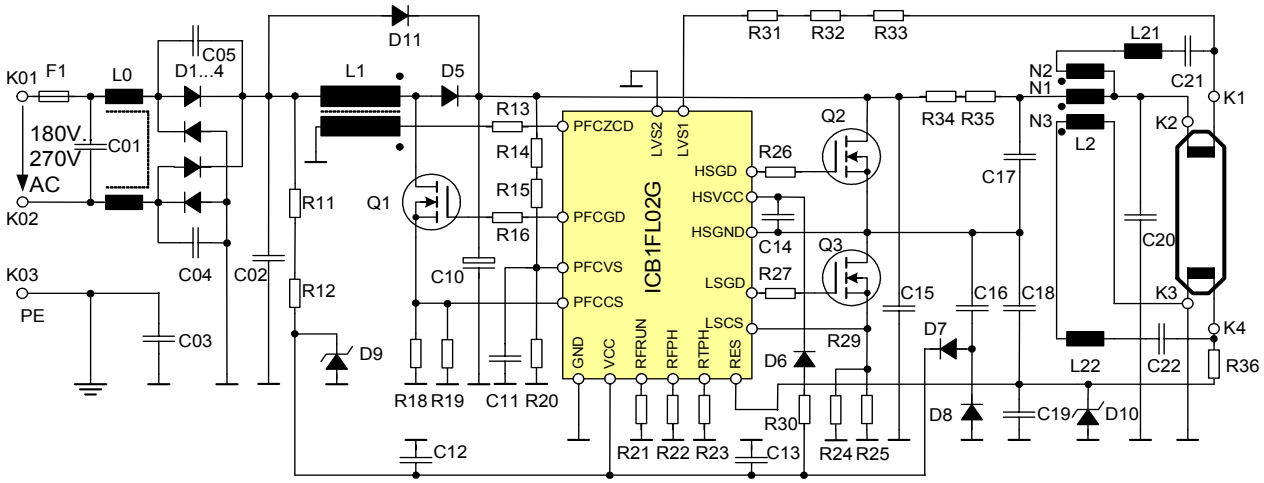


Fig. 2 T5-FL-Ballast Circuit Diagram

Operating behaviour

The functional description shall be performed using the circuit diagram of a lamp ballast for the T5 fluorescent lamp (Fig. 2). After switching on the mains the filter capacitor C2 and the bulk capacitor C10 are charged to the peak voltage of the mains supply. The capacitors C12 and C13 which support the IC supply voltage Vcc are charged via the start-up resistors R11 and R12. The current consumption of the IC at this stage is typically below 100µA until the supply voltage has reached Vcc = 10V. Above this level a current source of typically 20µA at the RES pin is activated which can detect the existence of the low-side filament. As long as the voltage level at the RES pin is below 1.6V the filament is assumed to be undamaged. In the path of the measured current a resistor R36 is placed which adjusts the voltage drop and - in conjunction with the capacitor C19 - filters the alternating voltage on the filament during run mode. In addition a zener diode D10 is placed between the RES pin and ground to protect the pin against over voltages that can occur when the lamp is removed during operation.

Via the resistors R34 and R35 a current is fed to the high-side filament and via the resistors R31, R32, R33 to the LVS1 pin. A filament is detected if the current is above 15µA. For multi lamp operation a second detection pin LVS2 is available, which can be deactivated by a ground connection in the same way as LVS1. The measured current at the LVS pin is clamped on the supply voltage Vcc and by this means supports the start-up. If the measured current at LVS pin is too small this fault generates a higher current level of typically 41µA at the RES pin. This causes the voltage drop at R36 to exceed the 1.6V level preventing the start-up of the IC.
In other words if the existence of the filaments is detected and the voltage at the PFCVS pin has reached at least 0.375V, which is interpreted as closed regulation loop for the boost converter, the IC can activate its driver outputs as long as the supply voltage Vcc exceeds the turn-on threshold of 14V.

Inverter to feed the fluorescent lamp

With the first pulse the low side MOSFET Q3 of the half-bridge is turned on. Then the floating capacitor C14, which supplies the high-side control logic like a battery, is charged from capacitor C13 via R30 and the diode D6. The resistor R30 prevents the activation of the over current protection at the LSCS pin. Thus already with the next half cycle the high-side MOSFET Q2 can be turned on. At the output of the half-bridge inverter the capacitor C16 together with the diodes D7 and D8 acts as a charge pump.

The continuous recharging of C16 with the inverter frequency shifts energy for the supply voltage Vcc of the IC to C13. A surplus of energy is dissipated by the zener diode D9. In addition C16 is used to limit the voltage slew rate and to produce zero voltage switching conditions.

During operation C16 is recharged without losses in the dead time periods of MOSFET Q2 and Q3 by the inductive driven current of the load circuit. So the succeeding turn on of the MOSFET occurs at zero voltage. At turn-off C16 limits the voltage slew rate in such a way, that the MOSFET channel is already turned off before the Drain to Source voltage has reached considerable levels. Therefore the inverter creates negligible switching losses at normal operation.

The load circuit of the inverter consists of a series resonant circuit with the resonance inductor L2 and the resonance capacitor C20. The lamp is connected in parallel to the resonance capacitor. In the shown example the preheating of the lamp is done voltage controlled. This means that the resonance inductor L2 has two additional windings. Each of those windings drives a current in the filament via the band pass consisting of L21/C21 and L22/C22. The band pass filter ensures that the current in the filaments is only flowing during the preheat phase. By reducing the frequency during run mode the heating current is almost completely blocked by the band pass. The load circuit also contains a capacitor C17. This capacitor is charged to half the value of the bus voltage thus operating the lamp symmetrically to the ground potential of the rectified mains supply.

Preconverter for power factor correction

Simultaneously with the inverter the MOSFET Q1 of the PFC boost converter starts the operation. This circuit consists of the inductor L1, diode D5, MOSFET Q1 together with the bulk capacitor C10. Such a boost converter can transform the input voltage to any arbitrary higher output voltage. Using a suitable control method this converter is used as an active harmonic filter and for the correction of the power factor. The input current follows the same sinusoidal wave form as the AC mains supply voltage.

On the output of the PFC preconverter a feedback controlled DC voltage is available at capacitor C10 for the application. The PFC stage is operated with a controlled turn-on time without input voltage sense. A turn-on time set by the control unit is followed by a turn-off time which is detemined by the duration until the current in the inductor and hence in the diode too has reached the level zero. This point of time is detected by the voltage level at the zero current detector winding on the inductor L1 and feed to the IC via the resistor R13 and the PFCZCD pin. The result is a gapless triangular shaped current through inductor L1 (so called critical conduction mode) which is sustained for a turn-on time in the range of 23µs down to 2.3µs. A further reduction of the energy flow reduces the turn-on time down to 0.4µs while at the same time the turn-off time is extended causing triangular shaped currents with gaps (discontinuous conduction mode). Such a control method allows a stable operation of the boost converter over a large range of the input voltage as well as the output power.

Of course the IC includes a couple of protection features for the PFC preconverter. The overcurrent is sensed at the PFCCS pin. The bus voltage, overvoltage and undervoltage are monitored at the PFCVS pin as well as the open loop detection. The ICB1FL02G includes the error amplifier with entire compensation build up by a digital PI regulator and a digital filter to suppress the 100Hz ripple.

Operating procedure during start-up

The inverter starts at a frequency of 125 kHz. Within 10ms the frequency is reduced in 16 steps to the preheat frequency adjustable by the resistor R22. The duration of preheating can be selected between zero and 2000ms by the resistor R23. Subsequently the frequency is further reduced in 128 steps and a time period of 40ms to the run frequency f_RUN adjustable by the resistor R21. The ballast should be designed in such a way that during the preheating phase the voltage across the lamp is low and at the same time the current in the filaments is large. In the ignition phase following to the preheating period the frequency of the inverter should be at - or at least close to - the resonance frequency of the resonant circuit in order to reach a sufficient voltage for the ignition of the lamp.

After successful ignition and frequency reduction to the run frequency the current in the lamp should reach its nominal value and the current in the filaments should become a minimum. During the ignition period a high voltage at the lamp and a large current in the resonant circuit is generated due to the unloaded resonant circuit. The current in the resonant circuit is monitored by the resistors R24 and R25. As soon as the voltage at pin LSCS exceeds a level of 0,8V, the operating frequency of the inverter is increased by a couple of frequency steps in order to prevent a further increase of the current and in the same way of the voltage at the lamp. If the level of 0,8V at pin LSCS is not crossed any more, the operating frequency of the inverter decreases with the typical step width of the ignition phase towards the run frequency. As a result of this measure the ignition phase is enlarged from 40ms up to 235ms with a lamp not willing to ignite, while the voltage at the lamp keeps on the level of the ignition voltage with a certain ripple. If the run frequency is not achieved within 235ms after finishing the preheating period the IC changes over into the failure mode. In such a situation the Gate drives will be shut down, the current consumption of the IC will be reduced to 150µA typically and the detection of the filaments will be activated. A restart is initiated either by lamp removal or after a new cycle of turn-off and turn-on of the mains voltage.

Protection features

Numerous protection functions complement the basic functions of the ICB1FL02G. As soon as the level at pin LSCS exceeds the voltage threshold of 1,6V for longer than 400ns, it is recognized as a risky operating condition as it can occur during lamp removal in a running device or during transients of mains voltage, and the IC changes over into the failure mode.

During run mode of the inverter a deviation from the typical zero voltage switching is recognized as an operation with capacitive load. In such an operating condition peak currents occur during turn-on of the MOSFETs due to switched charging of the charge pump capacitor C16. The IC distinguishes between two different natures of capacitive load. In a first situation there is in part a change of the charge of capacitor C16. Such an operating condition is less risky. So the IC changes over into the failure mode, when the situation happens for longer than 500ms. In a second situation capacitor C16 is completely charged and discharged by the MOSFETs switching. Possibly there is a commutation of the body diode of the MOSFETs during flowing forward current. In such a critical operating condition with high power dissipation the IC changes into failure mode already after 610µs (Fig. 35).

Finally dangerous operating conditions can happen, when the fluorescent lamp reaches the end of lifetime or at operating conditions leading to thermal instability of the lamp. As a consequence the lamp voltage becomes unsymmetrical or increases. For detecting such operating conditions the resistors R31, R32, R33 measure the lamp voltage by evaluating the current through these resistors at pin LVS. The turn-off threshold because of exceeding the maximum lamp voltage is detected when the current through the resistors R31, R32, R33 crosses +/- 215µA. This failure condition is called EOL1 (end-of-life 1) in the datasheet. The rectifier effect with unsymmetrical lamp voltage is called EOL2 in the datasheet. If the ratio of measured positive and negative peak value at pin LVS is higher than 1,15 or lower than 0,85 the IC detects a rectifier effect.
The failure events EOL1 and EOL2 are summarized in time periods of about 40µs and 4ms respectively. A counter adds up periods with failure events and adds down periods without failure events. There is a change over into failure mode only when the counter has reached 15 or 128 periods with failure events respectively. By this method is guaranteed, that the ballast is turned-off only when a significant number of failure events in sequence has happened. Therefore a continuous rectifier effect results in a change over into the failure mode after 500ms. The IC controls the operating frequency of the inverter during the different operating sequences such as softstart, preheat, ignition, pre-run and run mode. During the different operating sequences there are only some of the protection features active first. All the protection features are active during run mode only.The integrated circuit ICB1FL02G has a unique combination of features that make a design of high-quality lamp ballast with a low number of external components possible.
Further information and datasheet can be found on the subsequent link to Infineon Technologies.

http://www.infineon.com/smartlighting

3 Ballast Design

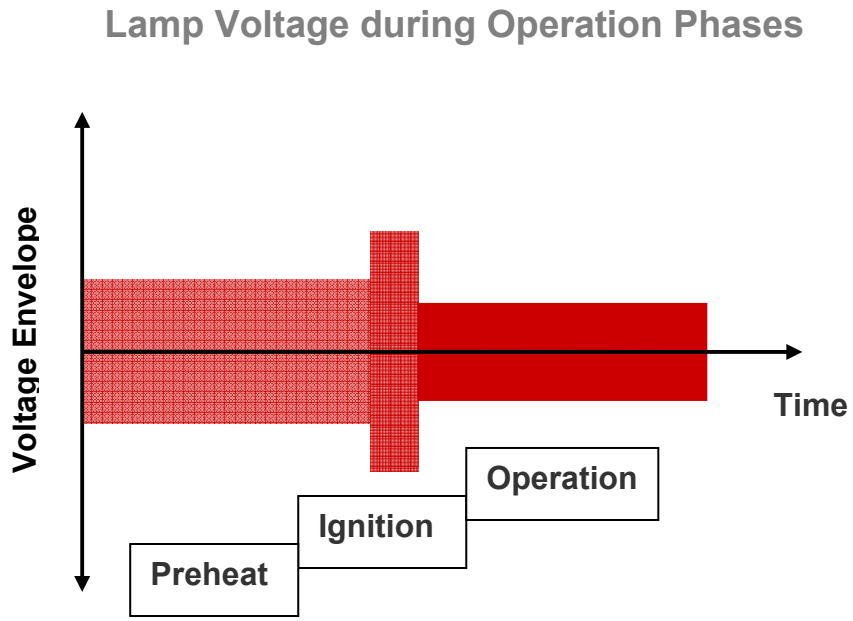


Fig. 3

Principles of Lamp Operation

For operating the FL it is necessary to provide at least a sufficiently high voltage for generating the needed amount of free charge carriers during the discharge ignition process. In most cases it is wishful to include an additional Preheat Phase for a sufficient thermalization of the lamp filaments which increases the number of maximum starting cycles during the lamp lifetime significantly.

After ignition of the discharge the negative U(I) – curve of the FL requires a current source behaviour of the supplying lamp circuit. The periodic ac signal should also offer an appropriate crest factor of the lamp voltage.

In addition to these pure physical requirements of lamp operation it is necessary to provide safe operation employing adequate protection functionality respecting all operational states and lifetimes phases of the discharge lamps. The supply unit shall also show Immunity against external signals and emission signal levels below the limits given in the Electro Magnetic Compliance (EMC) - Standardization. These demands lead to the inclusion of a substantial control and protection functionality into High-Performance-FL-Ballasts and the associated Control-IC's. So the block diagram of an Electronic Ballast will posses typically the following function blocks:

Electronic Ballast - Functions

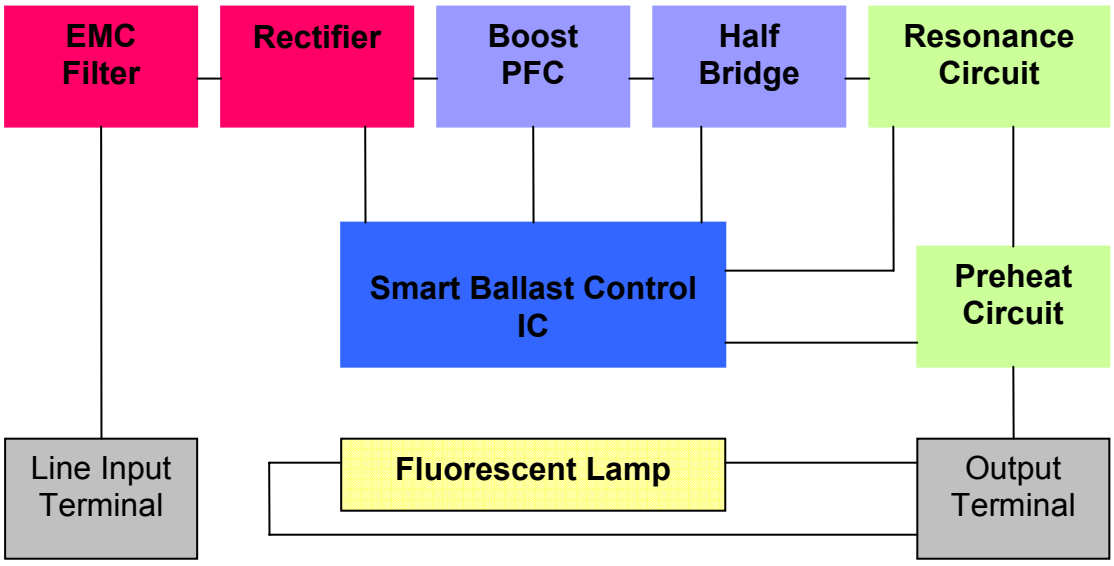


Fig. 4

States of Lamp Operation

Preheating of the lamp filament

The lifetime of fluorescent lamps can be increased significantly by thermalizing the lamp filaments to an appropriate temperature of emission which is $T_e \geq 900$ K. This means that the ratio of thermalized to cold filament resistance should be

$$\frac{R}{R_c} \cong 4$$

For preheating of the lamp filament different modes of energy transfer can be applied. In the following the pure cases of preheating by constant current respectively constant voltage are depicted.

Constant current mode I_F = const.

Starting with cold filaments the constant current I_F is applied to the cold filaments with the resistance $R(0) = R_c$. In this case the temporal increase shows an approximate exponential behaviour according

$$R_I(t) = R_c \, e^{\frac{\alpha R_c}{c_v} I_F^2 t}$$

Where α denotes the temperature coefficient of the resistance and c_v the heat capacity of the filament. It can be seen that increasing α, R_c and I_F accelerates preheating while increasing c_v will lead to a prolongation of the filament thermalization (Fig. 5).

Constant voltage mode U_F = const.

The application of constant voltage to the lamp filaments will rise its resistance according the temporal square root law

$$R_U(t) = \sqrt{R_c^{\,2} + 2\frac{\alpha R_c}{c_v} U_F^{\,2} \cdot t}$$

Where the parameters α , R_c and U_F accelerate preheating while increasing c_v will again lead to a prolongated filament preheating (Fig. 5).

In the lamp data sheets of the manufacturers the parameters for sufficient preheating are listed. The essential magnitude is the minimum cathode preheat energy

$$E_{\min} = Q + P\, t_e$$

Where Q indicates the specific heat and P an average power transformed into heat losses of the filament when thermalizing the filament to emission temperature. The data sheets also indicate the maximum energy which may not be exceeded to prevent overheating of the filament. Preheat current and –time t_e should be chosen accordingly using the denoted substitution resistor.

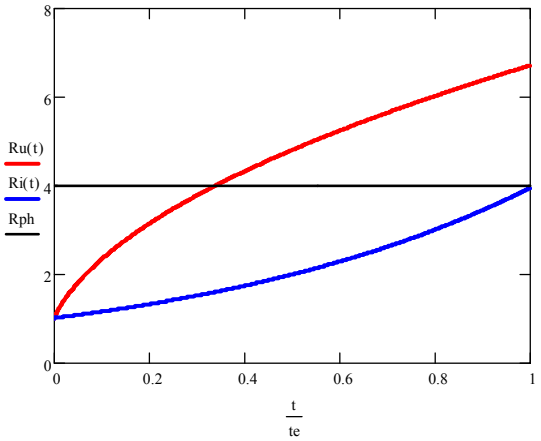


Fig. 5 Lamp-Filament Resistance Ratios for preheating with constant Voltage (Ru) and constant Current Mode (Ri) show a faster thermalization to an approximate end value Rph = 4 when Voltage Mode Preheating is applied.

Generation of Lamp Voltages

With preheated filament the lamp is prepared for igniting the discharge. For this the voltage is increased by lowering the inverter frequency until the lamp resistance breaks down abruptly and the resonant circuit shows strong damping.

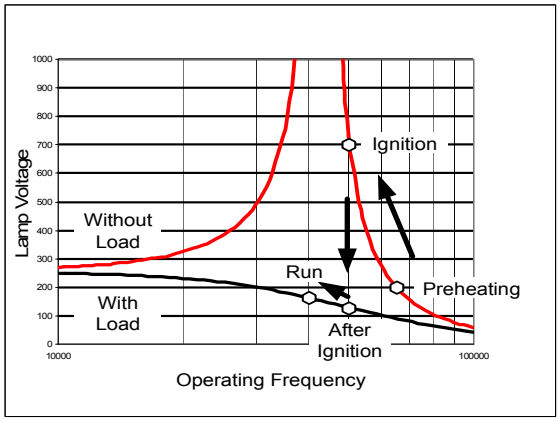


Fig. 6 Lamp Voltage in different resonant states

From Softstart to normal operation

Preceding the required filament preheating a softstart phase is traversed. The ignition phase with the sufficiently increased lamp voltage is followed by a normal operation which starts with the abrupt appearance of the lamp current (Fig. 7). In the timing diagrams of Fig. 8 and 9 current and voltage controlled preheating can be observed.

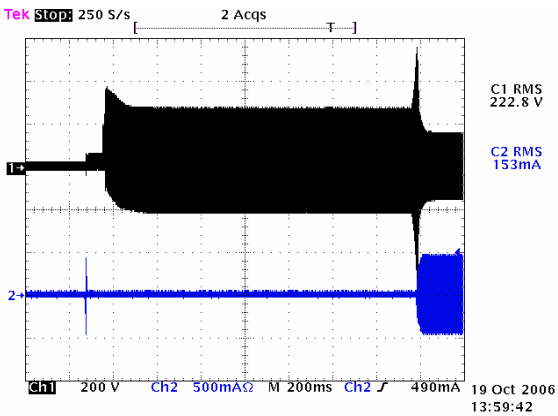


Fig. 7 Softstart, Preheating, Ignition and normal operation of FL T8 36W

Lamp Voltage (black, 200 V / div.)
Lamp Current (blue, 500 mA / div.)

4 Illustration of ballast signals

Preheating

The temporal resistance curves calculated as approximation from the filament voltage and – current slopes show the typical exponential (Fig. 8) for current controlled preheating and square root behaviour (Fig. 9) for voltage controlled preheating respectively. In the case of voltage controlled preheating a limitation of filament current takes place during the temporal phase with low resistant filaments owing to the limits of the preheat circuit energized by the transformer.

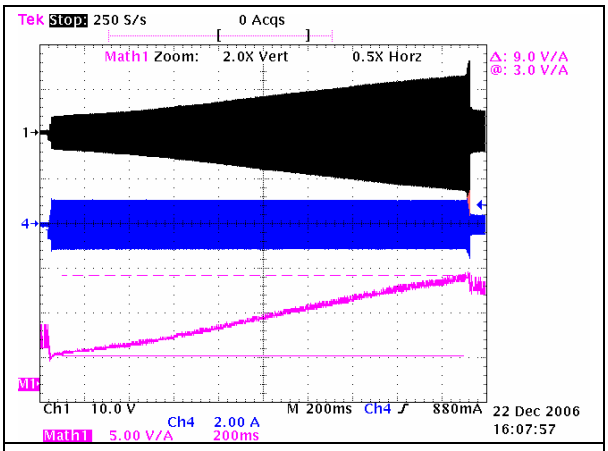


Fig. 8 Current controlled preheating of the 36W Lamp, R_C = 3 Ω

Filament Voltage (black, 10V / div.)

Filament Current (blue, 2A / div.)

Filament Resistance (pink, 5Ω / div.)

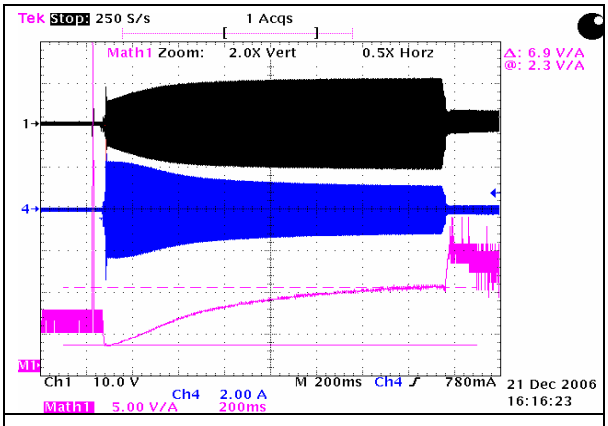


Fig. 9 Voltage Controlled Preheating of the T5 54W Lamp, R_C = 2.3 Ω

Filament Voltage (black, 10 V / div.)

Filament Current (blue, 2 A / div.)

Filament Resistance (pink, 5 Ω /div.)

Ignition Control

After preheating the operating frequency of the inverter is shifted downwards in 40 milliseconds typically to the run frequency (Fig. 10). During this frequency shifting the voltage and current in the resonant circuit will rise when it operates close to the resonant frequency with increasing voltage across the lamp. As soon as the lower current sense level (0,8V) is reached, the frequency shift downwards is stopped and if necessary it is increased by eight steps in order to limit the current and the ignition voltage as well. The procedure of shifting the operating frequency up and down in order to stay within the max ignition level is limited to a time frame of 235ms. If there is no ignition within this time the control is disabled and the status is latched as a fault mode. While the softstart proceeds in 15 steps of 650us with

$$\Delta f_{ss} = \frac{120\,\text{kHz} - f_{PH}}{15\,\text{Steps}}$$

The ignition proceeds in 127 steps of 162 us each having the frequency change

$$\Delta f_{ss} = \frac{f_{PH} - f_{RUN}}{127\,\text{Steps}}$$

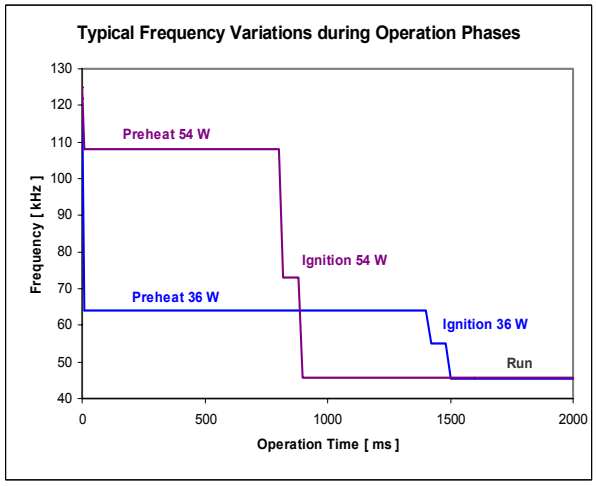


Fig. 10 Temporal frequency profiles of the inverter during the main Operation phases

During the process of lamp ignition it is useful to control also the current in the half bridge. An increase of the corresponding voltage detected at pin LSCS (Fig. 11) is used to control saturation effects arising in the lamp choke.

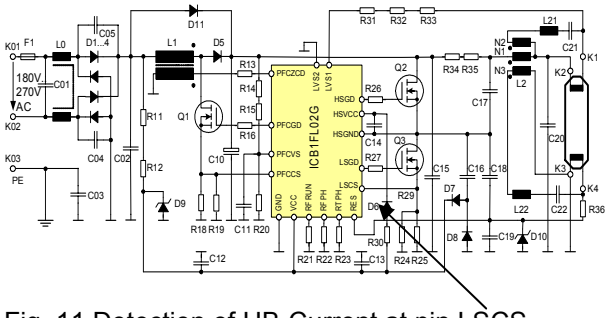


Fig. 11 Detection of HB-Current at pin LSCS

The function of the ignition control is displayed in Fig. 12. The increment of the ignition frequency by eight steps can be observed at the RFPH-Voltage displayed in Fig. 13. So the control function is able to keep the ignition voltage in a sufficiently small voltage window if the ferrite material of the lamp choke begins to saturate.

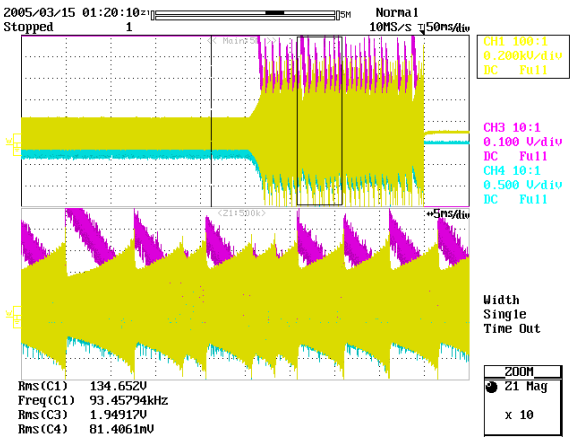


Fig. 12 Effect of ICB ignition control

Ignition voltage (yellow, 500V / div.)

Ignition Voltage = 489,5V_{RMS}

Voltage at RFPH (magenta)

Adjustment of RFPH-Voltage-Offset = 1,32V

Voltage at pin LSCS (blue)

$R_{LSCS-PIN}$ = 0,56Ω

By means of the ignition control function it is possible to provide stable conditions even at essential variation of the values arising with the onset of saturation effects. These influences owing to temperature and tolerances of the lamp choke on ballast functions can be respected smartly.

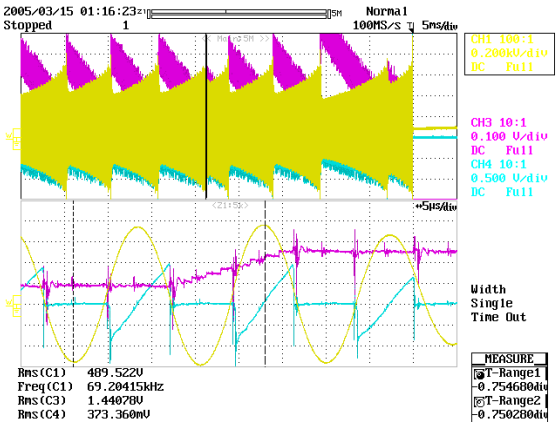


Fig. 13 Limitation of Ignition voltage and lamp choke saturation

Ignition voltage (yellow, 500V / div.)

Ignition Voltage = 489,5V_{RMS}

Voltage at the RFPH (magenta)

Adjustment of RFPH-Voltage-Offset = 1,32V

Voltage at the LSCS-PIN (blue)

$R_{LSCS-PIN}$ = 0,56Ω

Normal mode phase control

As the I-U-Characteristic of fluorescent lamps is negative it is necessary to operate fluorescent lamps with current sources. The appropriate realization is a resonant circuit controlled by the ICB1 generating high frequency lamp voltage and –current slopes. At this time scale the resulting I-U- characteristic is positive. In Fig. 14 the case of normal lamp operation of the T8 36W –Lamp in the Run Mode of the ICB1 is represented.

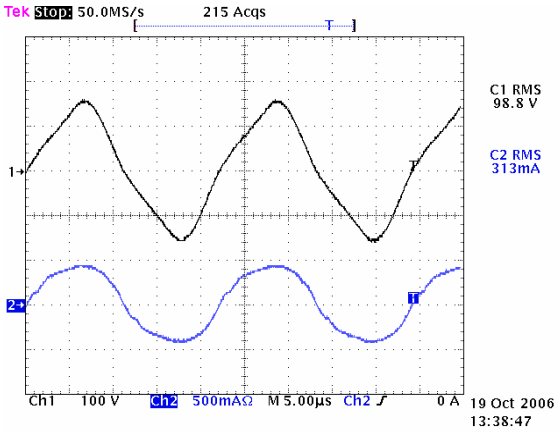


Fig. 14 High frequency operation of the lamp

Lamp Voltage (black, 200 V / div.)
Lamp Current (blue, 500 mA / div.)

The operation phases are realized by varying the operation frequencies of the HALF BRIDGE (HB) in a controlled manner. The impedance of the connected resonant circuit allows an appropriate variation of voltage and current at the discharge and the lamp-filaments.

For the ballasts of the T5 54W respective T8 36W Lamps the temporal sequences of the inverter frequencies in the single phases are shown with their falling characteristic in Fig. 10. For the Softstart the highest frequencies arise, followed by a phase with decreased constant frequency leading to the described preheating of the lamp filaments.

After the correct filament thermalization is reached the frequency is decreased in a short time interval, which will result in the ignition of the fluorescent lamp. After performing a successful ignition of the discharge the inverter frequency is lowered further to the operation frequency connected with the appropriate lamp power. The functionality associated with the different operation phases shall be revealed with the timing diagrams described below.

Preparing a controlled Softstart the operation phases Under Voltage Lock Out (UVLO) and Monitoring are traversed (Fig. 15). Switching on the supply voltage to the ballast the voltage at the Pin VCC rises to the turn-on threshold of 14V. In the Softstart phase the HB drivers are activated with a frequency of 125 kHz. The inverter supplies the load circuit and leads to voltage oscillations at PIN RES and current oscillations in the lamp inductor (Fig. 16).

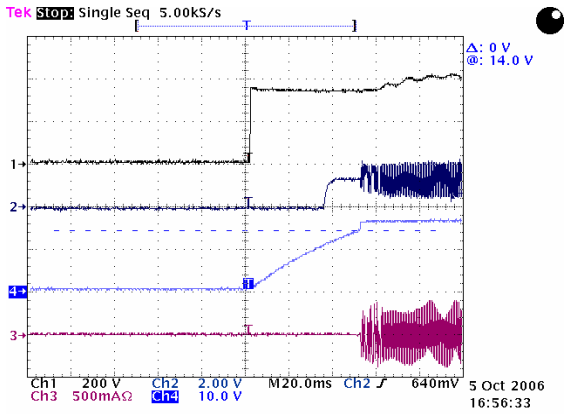


Fig. 15 UVLO, Monitoring and transition to Softstart

Bus Voltage (black, 200 V / div.)
VRES (dark blue, 2 V / div.)
VCC (blue, 10 V / div.)
Lamp Inductor Cur.(violet,500mA/div.)

Monitoring and Softstart

The high frequency oscillations zoomed in Fig. 16 show the trapez form of VRES and the sinusoidal current curve of the lamp choke. With the first gate signals of the Softstart generated by the IC temporary hard switching behaviour with elevated current peaks can arise due to charging of the coupling- and charge-pump- capacitors (Fig. 17).

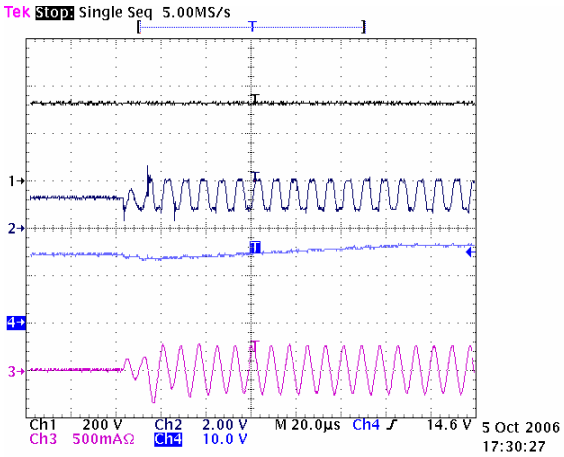


Fig. 16 Monitoring and transition to Softstart

Bus Voltage (black, 200 V / div.)
VRES (dark blue, 2 V / div.)
VCC (blue, 10 V / div.)
Lamp Inductor Current (pink, 0,5 A / div.)

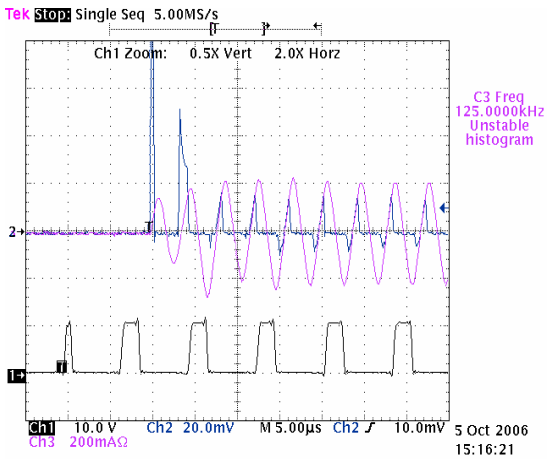


Fig. 17 Softstart

Drain-Current of Q3 (blue, 0,2A / div.)
Lamp-Inductor-Current (pink, 0,2 A / div.)
Gate-Voltage of Q3 (black, 10 V / div.)

Preheating

From the Drain Current curve of the low side half bridge MOSFET it can be seen (Fig. 18) that in the steady state of preheating the transistor performs inductive switching of the resonant circuit and that it carries the inductor current during its turn-on-phase. The programming of the relevant magnitudes preheat time and –frequency can be performed

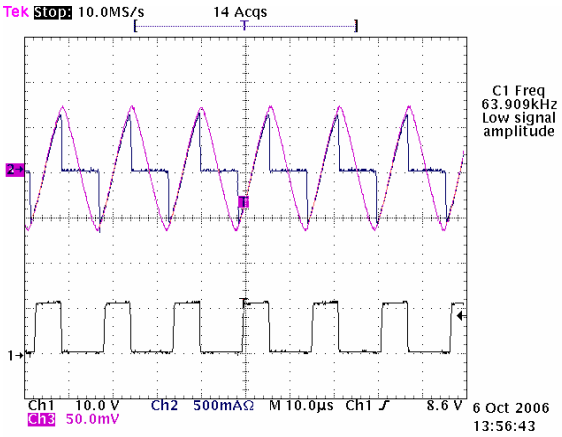


Fig. 18 Preheating

Drain-Current of Q3 (blue, 0,5 A / div.)
Lamp-Inductor-Current (pink, 0,5 A / div.)
Gate-Voltage of Q3 (black, 10 V / div.)

by means of the resistors at the pins RTPH and RFPH respectively.

Ignition

During the ignition phase where the currents in the half bridge are extensively higher (Fig. 19) than in the preceding phases. In all states these states before completed ignition of the lamp the high-Q character of the load circuit can be observed.

The application of high voltage initiates the free charge carrier generation process in the lamp and hence ignites the discharge with abrupt lowering of the infinite resistance to values fastly approximating the specified lamp voltage. With a load circuit impedance fulfilling the standard requirements the ignition process is short enough to cause no damage at the lamp electrodes.

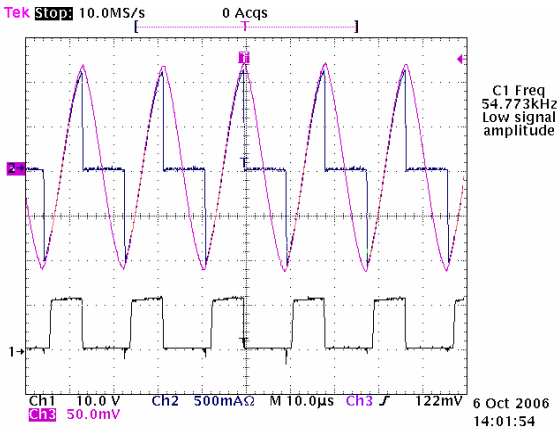


Fig. 19 Lamp Ignition

Drain-Current of Q3 (blue, 500 mA /div.)
Lamp-Inductor-Current (pink, 500 mA / div.)
Gate-Voltage of Q3 (black, 10 V / div.)

In Ignition Mode of the ICB1 the detection of Bus-Voltage, voltages at Pins PFCCS, LSCS and VCC are active. Also if the Run frequency can not be achieved Driver turn off and Power Down respectively are performed.

Pre-Run and Normal Run Mode

With completion of the lamp ignition process the lamp resistance lowers dramatically. The ICB1FL02G changes to the Pre-Run-Mode in which already the normal operation frequency is applied but only a selected set of protection functions active.

In the normal run mode the operation frequency keeps unchanged and is connected with the desired lamp-current and –power via the defined dimensioning of the resonant circuit. In the ballast board designed for the T5 54W lamp at frun = 45 kHz inductive switching occurs in interaction with the damped resonant circuit as can be derived from (Fig. 20).

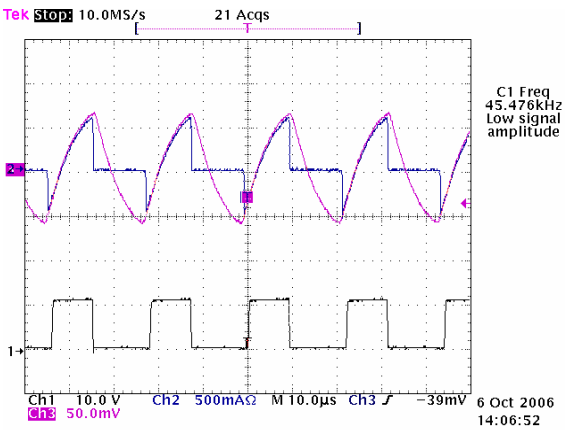


Fig. 20 Run – Normal Operation

Drain-Current of Q3 (blue, 500 mA / div.)
Lamp-Inductor-Current (pink, 500 mA / div.)
Gate-Voltage of Q3 (black, 10 V / div.)

In Run-Mode all protection functions needed are activated.

Protection Functions

Under Voltage Lock Out - UVLO

The intermediate circuit voltage (Bus Voltage) is sensed by a resistive divider at the pin PFCVS so that the cases open control loop, undervoltage and overvoltage can be detected. In Fig. 21 the case of repeating UVLO as consequence of ballast operation near line undervoltage can be observed. The connected detection limit of 1.83 V is 73% of the reference voltage of 2.5 V.

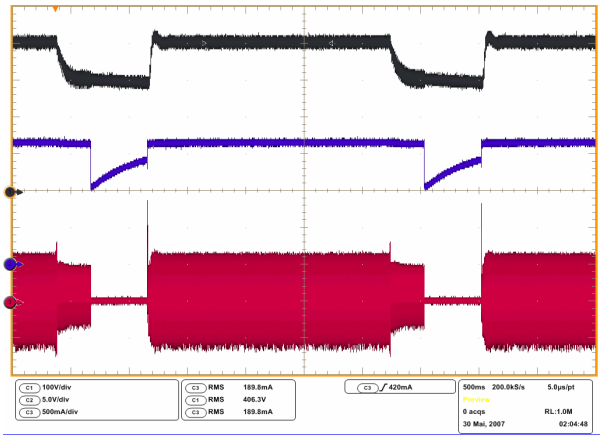


Fig. 21 Repeating UVLO at U_{Line} ~ 100V_{ac}

Phases: Bus Voltage decrease after lamp ignition in Run-Mode with adjacent IC power down, Vcc-increase and IC-startup. In preheat mode the reduced U_{Line} is sufficient to increase U_{Bus} again.

Bus Voltage (black, 100V / div)

VCC (blue, 5V / div) , (500ms / div)

Low Side Drain-Current (red, 500mA / div)

End of Lamp Life Protection - EOL

Reaching the Normal Run Mode the EOL-Monitoring is enabled. This protection function is necessary as at the end of the fluorescent lamp life often broken filaments or at least regions with used up electrode pasts arise which will lead to elevated work functions for the electrons leaving the cathode. This effect can arise almost symmetrical on both lamp electrodes or with significant difference at each electrode. An appropriate EOL-protection hence includes the detection of symmetrical lamp voltage enhancement as well as the processing of signal ratios reflecting asymmetric material consumption.

The safety of lamp operation is influenced by a dangerous thermalization of the lamp regions which are surrounding the electrodes especially of low diameter lamps as the power densities arising in this cases are high. Another damaging effect is given if high pulse powers are heating up the HB-MOSFETS. So the EOL-events are detected by measuring the positive and negative peak level of the lamp voltage by a current fed into the LVS pin. The relevant lamp-voltage-levels are indicated in Fig. 22 . During Run Mode slow and abrupt increases of Lamp Voltage can be detected at pins LVS1 and LVS2. Exceeding one of the two thresholds of either +215µA or -215µA cycle by cycle for longer than 610µs, the interpretation of this event is a failure due to EOL1.

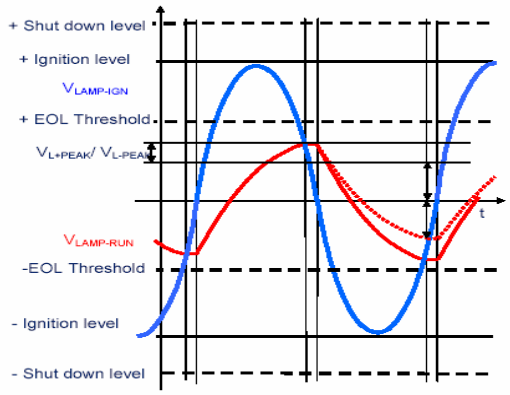


Fig. 22 EOL-Detection with lamp voltage levels

EOL2 is detected when ratio of the positive and negative amplitude of the lamp voltage is above of the ratio of Fig. 23 for longer than 500ms . The voltage ratio is dependent of the sensed current. If the end-of-life conditions are detected, the control is disabled and the status is latched as a failure mode. If the EOL conditions are interrupted for some cycles, a counter counts down the number of events and counts up if the events appear again.

According the standard of EN 61347-2-3 one of three tests (asymmetric pulse test, asymmetric power dissipation test, open filament test) may be used to qualify electronic ballast. The ballast manufacturer determines which test will be used to given ballast based on the design of that particular ballast circuit. The chosen test has to be passed and the manufacturer has to refer to it in the ballast description.

Asymmetric power dissipation

The EOL2-test applying asymmetric power dissipation shows for the negative rectifier effect the following results:

Positive Lamp voltage = 116V
Negative Lamp Voltage = 158V
I (LVS, pos) = 116V / R (LVS) = 76 µA
Amplitude ratio 158V /116V = 1,36 > 1,27
Asymmetric power losses P_{R1} at R1= 4,8W

For this effect the experimental setup provides the ratios illustrated in Fig. 23. The belonging timing diagram (Fig. 24) shows lamp voltage and the negative signals measured at resistor R1 as defined in the standard EN 61347-2-3.

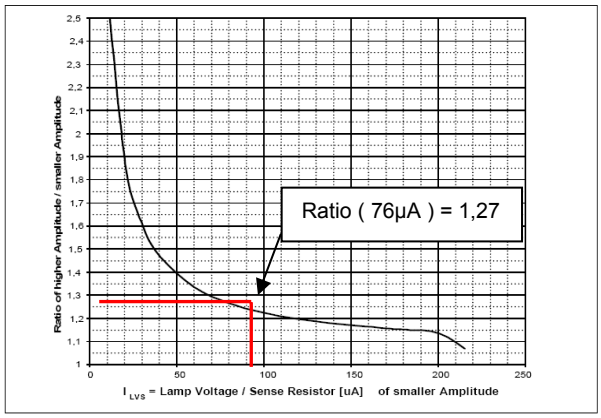


Fig. 23 Negative rectifier effect
High to low Amplitude ratio versus signal derived from the low amplitude

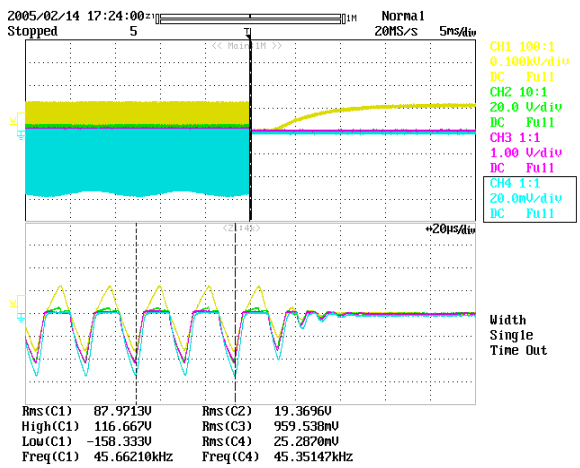


Fig. 24 Negative rectifier effect
Lamp voltage (yellow, 100 V / div.)
Voltage at R1 (magenta, 20 V / div.)
Current at R1 (blue, 200 mA / div.)

The EOL2-test applying asymmetric power dissipation exhibits for the positive rectifier effect the following results:

Positive Lamp voltage = 179V
Negative Lamp Voltage = 133V
I (LVS, neg) = 133V / R (LVS) = 87 µA
Amplitude ratio 179V / 133V = 1,35 > 1,25
Asymmetric power losses P_{R1} = 5,6W

The belonging ratio- and timing -diagram shows lamp voltage and the negative signals in Fig. 25 and Fig. 26 measured at resistor R1 according EN 61347-2-3. For both directions EOL2 is detected with t (EOL2) > 500 ms.

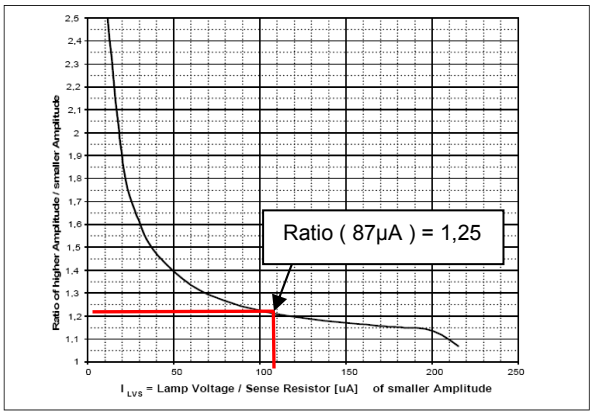


Fig. 25 Positive rectifier effect
High to low Amplitude ratio versus signal derived from the low amplitude

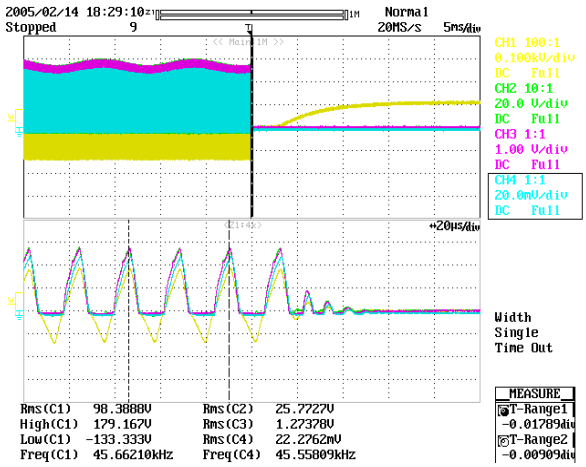


Fig. 26 Positive rectifier effect
Lamp voltage (yellow, 100V / div.)
Voltage at R1 (magenta, 20V / div.)
Current at R1 (blue, 200mA / div.)

Signals at Pin RES and RFPH in case of deactivated fluorescent lamp

The sequence from Softstart, Preheat, Ignition and direct transition to power-down due to high-ohmic lamp is displayed in the following timing-diagram on a long time scale (Fig. 27) and as detailed representation (Fig. 28 – Fig. 30) for the pins RES and RFPH respectively. It can be seen that the state of normal Run Mode will not be reached when starting a deactivated lamp. The phase of triangle voltage form (Fig. 28) at Pin RES during power down with low current consumption of I_{VCC} < 170µA is generated to prevent that voltage transient are interpreted as lamp removal.

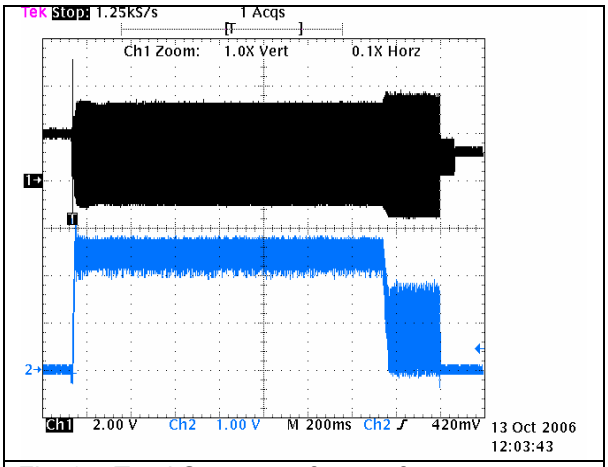


Fig. 27 Total Sequence from soft start to power down due to increased lamp resistance

Curves in envelope mode
Voltage on Pin RES (black, 2 V / div.)
Voltage on Pin RFPH (blue, 1 V / div.)

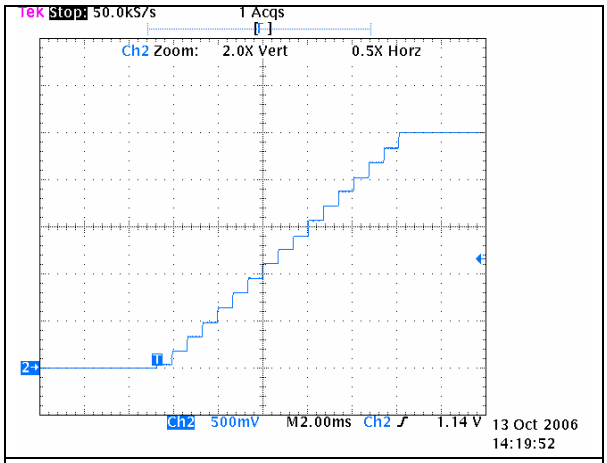


Fig. 29 Transition from soft start to preheating RFPH-Voltage-Steps reflecting the decrease of operation frequency

Curve in high resolution
Voltage on Pin RFPH (blue, 0.5 V / div.)

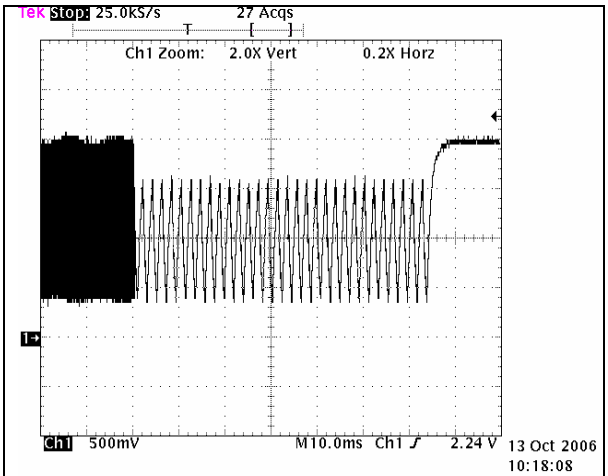


Fig. 28 Transition to power down
Voltage-Signal on Pin RES changes from 45kHz Signal to triangle curve

Curve with reduced time scale
Voltage on Pin RES (0.5 V / div.)

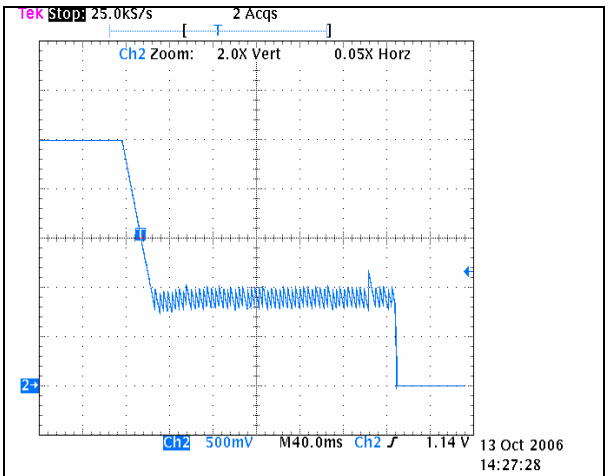


Fig. 30 Transition to power down Voltage-Signal on Pin RFPH changes from DC over triangle to zero voltage

Curve in high resolution
Voltage on Pin RFPH (blue, 0.5 V / div.)

Protection against Capacitive Load

a) Normal Operation

In normal operation of the half bridge inductive or near resonant switching on the inductive side of the resonant curve takes place which can be observed at the timing diagrams of the Drain-Source-Voltage and the Drain-Current of the Low-Side Switch (Fig. 31).

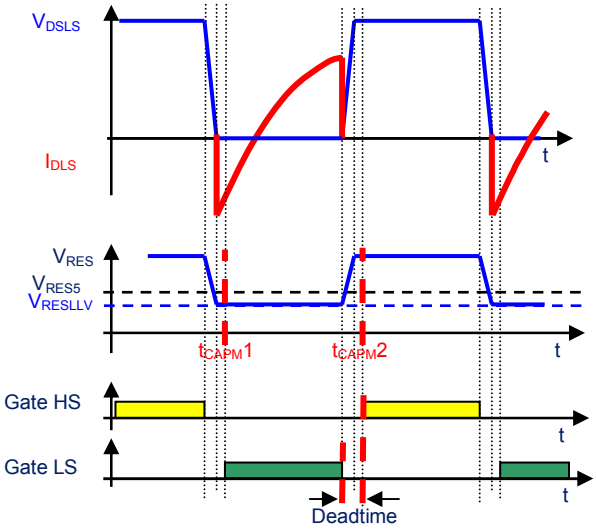


Fig. 31 ZVS at Normal Operation of the Lamp

b) Capacitive Load 1

A first criterion detects low deviations from ZVS (CapLoad 1, Fig. 32) and changes operation into fault mode, if this operation lasts longer than 500ms. For CapLoad1 the same counter is used as for the end-of-life evaluation.

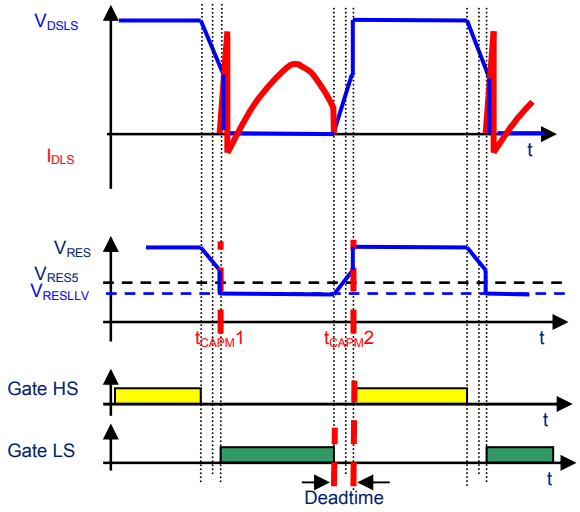


Fig. 32 Current Spikes at Capacitive Load 1

In the case of an open resonant circuit which appears e.g. at sudden break of the tube the voltage across the resonant capacitor and current through the shunt of the low-side inverter MOSFET rises quickly. This event is detected by inverter current limitation (1,6V threshold or EOL1 detection) and results in shut down of the control. This status is latched as a failure mode. In another kind of failure the operation of the inverter may leave the zero voltage switching (ZVS) and move into capacitive mode operation or into operation below resonance. There are two different levels for capacitive mode detection implemented in the IC.

c) Capacitive Load 2

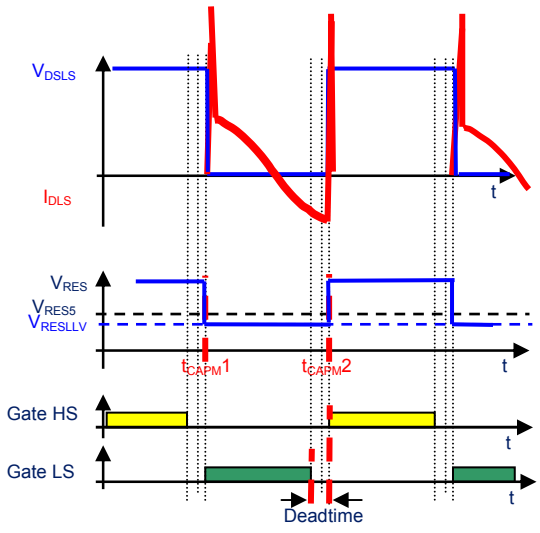


Fig. 33 Current Spikes at Capacitive Load 2

Detection of Capacitive Load

At the pin RES the detection of Capacitive Load takes place. If the Drain-Voltage of the lower MOSFET is already zero when its Gate Voltage is turned on (Fig. 34) , no capacitive switching occurs. The detection relates to cases in which only low deviation from ZVS (Cap. Load 1) as well as the more severe case of operation below resonance (Cap. Load 2) occurs.

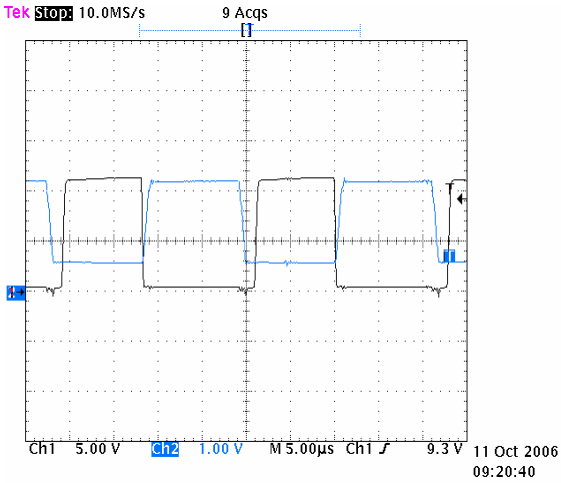


Fig. 34 Normal Run Mode - no Power Down:
Gate Voltage of Low Side MOSFET rises when voltage at PIN RES has already declined

Gate Voltage (black, 5 V / div.)
Voltage at PIN RES (blue, 1V / div.)

In the first case the fault mode is acquired if the Cap Load1 operation lasts longer than 500ms. In the second case of Cap Load2 the inverter is turned off after the shorter time interval of 610µs and the IC changes over into fault mode. Capacitive Modes may arise when the lamp voltage increases which will lead to a shift of the resonant frequency to higher values.

The evaluation of the failure condition is done by an up and down counter. In the second case of Cap Load2 the inverter is turned off this conditions lasts longer than 610µs and the IC changes over into fault mode. The evaluation of the failure condition is done by an up and down counter which samples the status every 40µs.
CapLoad 1 is sensed in the moment when the low-side gate is drived on. If the voltage level at pin RES is above the V_{REScap} threshold (typ. 0.24 V) related to the level V_{RESLLV} conditions of CapLoad1 are assumed.

CapLoad2 is sensed in the moment when the high-side Gate drive is turned on. If the voltage level at pin RES is below the V_{REScap} threshold related to the level V_{RESLLV} , conditions of CapLoad2 (Fig. 35) are assumed. As the reference level V_{RESLLV} is a floating level, it is updated every on-time of the low-side MOSFET. Dramatic changes of the load circuit

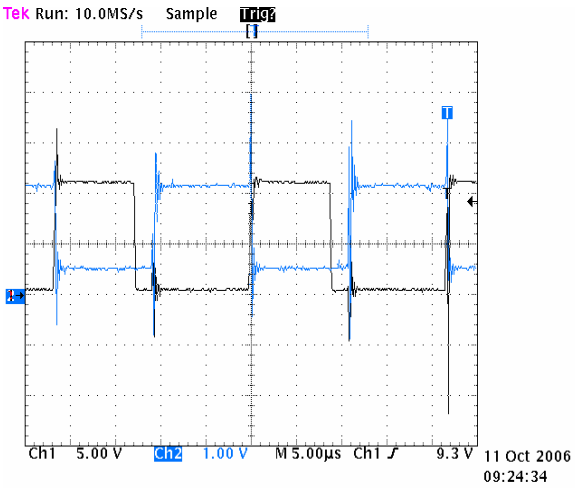


Fig. 35 Capacitive Load / Cap.Load 2:
Gate Voltage of Low Side MOSFET rises when Voltage at PIN RES is still in the high-state

Gate Voltage (black, 5 V / div.)
Voltage at PIN RES (blue, 1 V / div.)

like sudden break of the lamp tube will cause a quick rise of the low side MOSFET. This event is detected by inverter current limitation (1,6 V threshold or EOL1 detection) and results in shut down of the control. This status is latched as a failure mode.

Filament Detection at start up

A source current out of pin RES via resistor and filament to ground monitors the existence of the low-side filament of the fluorescent lamp for restart after lamp removal. During typical start-up with connected filaments of the lamp a current source (20µA) is active as long as Vcc > 10,5V and VRES < 1,6V. An open Lowside filament is detected, when VRES > 1,6V. Such a condition will prevent the start-up of the IC. An open high-side filament is detected when there is no sink current ILVSsink (15µA) into both of the LVS-Pins before the VCC start-up threshold is reached.

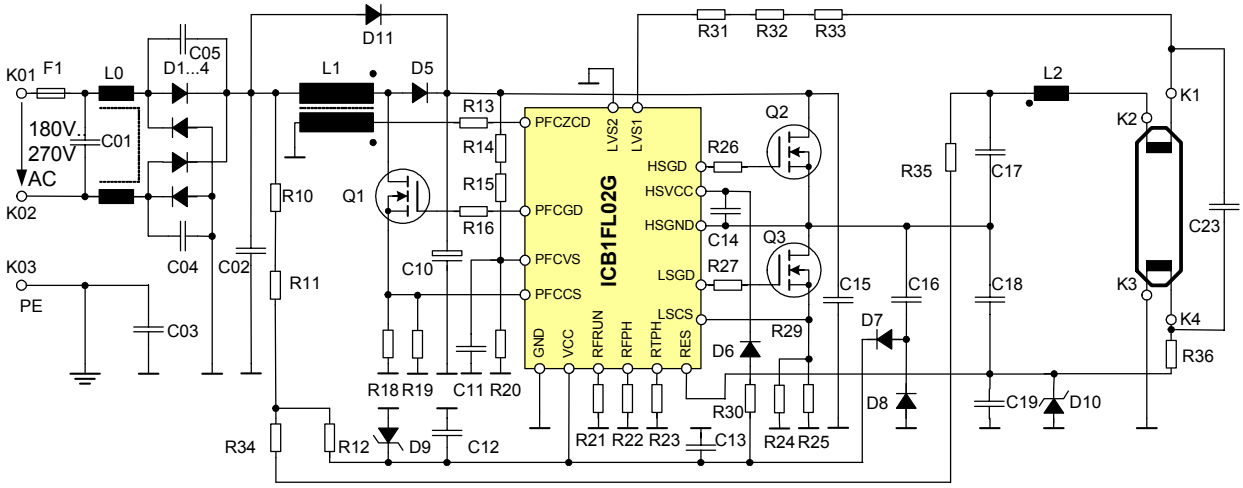


Fig. 36 Ballast with varied Filament detection

While T5 and CFL lamps have additives to ignite only at a rather high and constant level with lower influence by temperature, T8 lamps have a significant change of ignition level versus temperature. The shifting of the lamp voltage is a result of the DC level on the resonant capacitor. So it is a good choice, to bring this level down in order to avoid early ignition during the preheating phase. This can be done either by a higher ohmic resistor R34, R35 (Fig. 36) to a value up to 10M. However this results in a long time constant. R34, R35 can be kept in a range of 1M, when feeding them from a lower input voltage and not from the bus voltage. As the bus voltage increases during start-up from peak input voltage to the 400V, while the rectified input voltage stays on an average AC voltage it is obvious, to use this voltage as a source for the sensing of the high-side filaments.

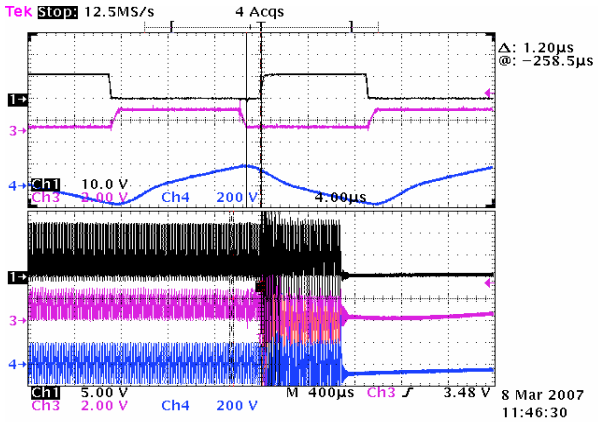


Fig. 37 Normal Mode before Lamp Removal
Gate Voltage (black, 5 V / div.)
Voltage at PIN RES (magenta, 2 V / div.)
Lamp-Voltage (blue, 200 V / div.)

Lamp Removal during Run Mode

Removing the Lamp during Run Mode changes the load conditions dramatically and normally will cause a transition to capacitive operation (Fig. 37 and Fig. 38) with strong lamp voltage increase at the output capacitor. The inverter is turned off as this condition will last longer than 610µs and the IC changes over into fault mode. In special configurations it is possible that the Vcc block is influenced via the RES PIN. This effect can be prevented by means of a resistor e.g. R = 330Ω in series from the high side of capacitor C19 to the RES PIN.

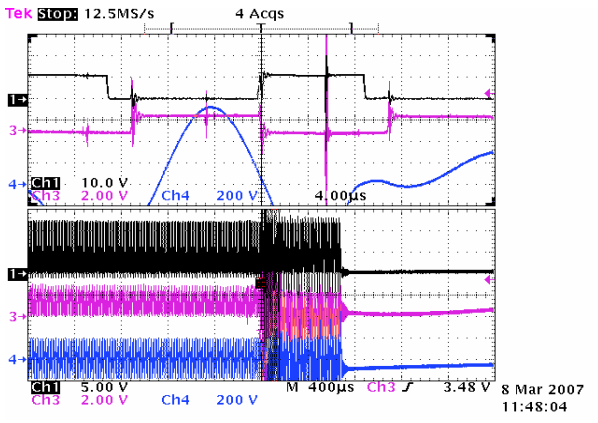


Fig. 38 Cap Mode 2 after Lamp Removal
Gate Voltage (black, 5 V / div.)
Voltage at PIN RES (magenta, 2 V / div.)
Lamp-Voltage (blue, 200 V / div.)

Power Factor Correction (PFC)

Principal Behaviour

The standards for the suppression of line current harmonics (EN61000-3-2 , IEC61000-3-2) require certain limits for the generation of the single current harmonics. Providing an extensive approximation to a resistive load behaviour of the ballast will lead to a high power factor, low harmonic generation and minimum THD. For this an appropriate drive control of the MOSFET-Switch in the Boost Converter used as power factor correction circuit is provided. It is based on the detection and processing of the signals at the pins PFCVS (Bus Voltage Sense), PFCZCD (Zero Current Detection) and PFCCS (Current Sense for Over-Current-Detection). Base on this the On-Time of the switch can be varied in frequency and duration of the Gate Signal. The PFC starts with fixed frequency operation and switches over into critical conduction mode operation as soon as a sufficient ZCD signal is available.

The control depends on the effective value and phase of the line voltage and on the bus voltage. The timing diagram of the negative voltage at pin PFCCS for U_{line} = 230 V in the phase I_{line} = I_{max} is shown in Fig. 39. The positive value of U(pin PFCCS)(-1) correlates with the T_{on} -Time of the Boost-Switch.

The rising slope of the inductor current belongs to the phase in which the energy in the inductor increases. During the blocking phase of the Boost Transistor the Boost-Diode is conducting and carries the discharging current of the Inductor (Fig. 40). The falling slope of the timing diagram Integral [U(pin PFCCS) (-1)] corresponds to the Diode-Current as expected. With the chosen scaling the induction curve has the same amplitude as the diode-current-curve. So it is obvious that both curves can differ only by an additive integration constant.

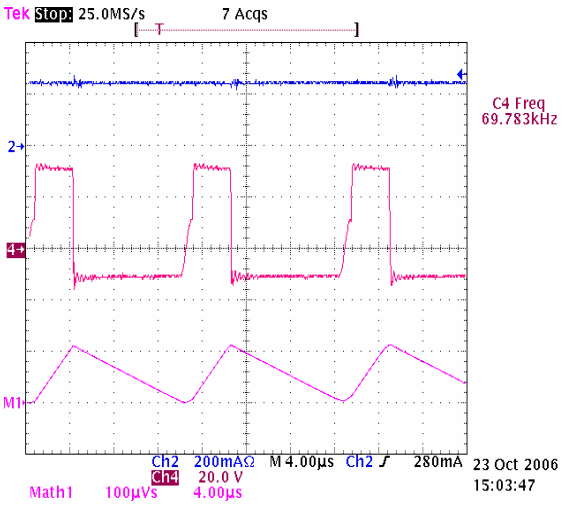


Fig. 39 Voltage Signal at pin PFCZCD at I_{line} (t) = I_{max} for U_{line} = 230V

Line Current as reference (blue, 200 mA / div)
U (Pin PFCZCD) * (-1) (red, 20 V / div)
Boost-L-Induction (pink, 100 µVs / div.)

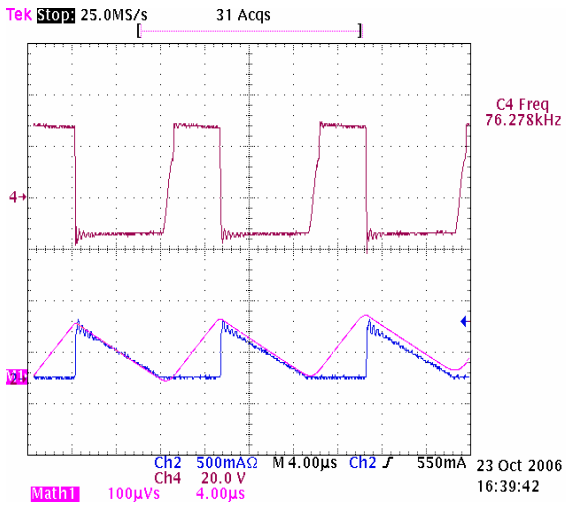


Fig. 40 Voltage Signal at pin PFCZCD at I_{line} (t) = I_{max} for U_{line} = 230 V

Voltage at Pin PFCZCD (red, 20 V / div.)
Boost Diode current (blue, 500 mA / div.)
Boost-L-Induction (pink, 100µVs / div.)

PFC – Line Voltage Dependence

For $U_{line,peak} = U_{Bus} / 2$ the conducting and blocking durations of the Boost-Transistor are equal with $T_{on} = T_{off}$. With the effective line voltage decreasing from U_{line} = 230 V to U_{line} = 130 V the pfc-operation frequency reduces from about 70 kHz to about 35 kHz measured at the phase of peak line voltage. The duty cycle increase from $\tau = 0.3$ to $\tau = 0.85$ raises the line current and hence keeping the line power approximately constant.

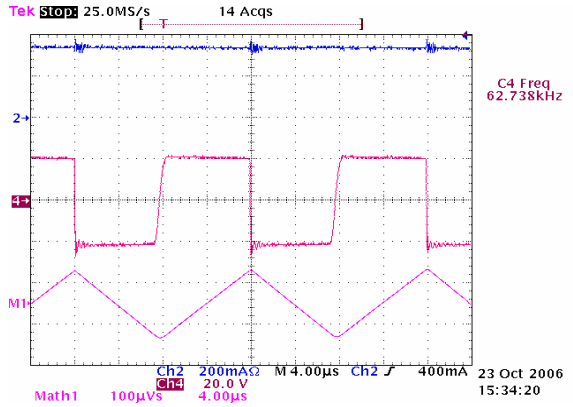


Fig. 41 Voltage Signal at Pin PFCZCD at $I_{line}(t) = I_{line,max}$ for $U_{line,max} \sim U_{Bus} / 2$

Line Current as reference (blue, 200 mA / div.)
U (Pin PFCZCD)*(-1) (red, 20 V / div.)
Boost-L-Induction (pink, 100µVs / div.)

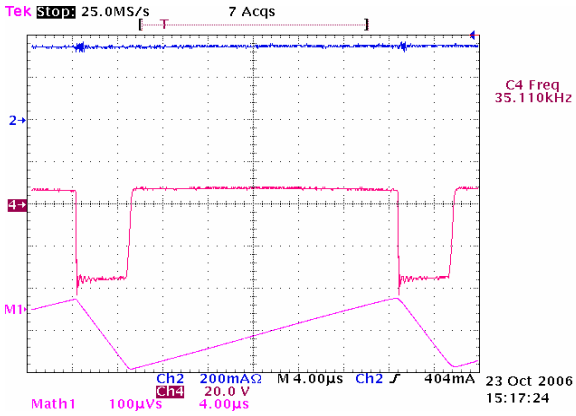


Fig. 42 Voltage Signal at Pin PFCZCD at $I_{line}(t) = I_{line,max}$ for U_{line} = 130V

Line Current as reference (blue, 200 mA / div.)
U (Pin PFCZCD) * (-1) (red, 20 V / div.)
Boost-L-Induction (pink, 100 µVs / div.)

PFC - Protection

There is an overvoltage threshold at 109% of rated Bus voltage that stops PFC Gate Drive as long as the Bus voltage has reached a level of 105% of rated Bus voltage again. The compensation of the voltage control loop is completely integrated. The internal reference level of the Bus voltage sense (PFCVS) is 2,5V with high accuracy.

The PFC control operates in CritCM in the range of 23µs > on-time > 2,3µs. For lower loads the control operates in discontinuous conduction mode (DCM) with an on-time down to 0,5µs and an increasing off-time. With this control method the PFC preconverter covers a stable operation from 100% of load to 0,1% .

Overvoltage, undervoltage and open loop detection at pin PFCVS are sensed by analog comparators. The BUS voltage loop control is provided by a 8bit sigma-delta A/D-Converter with a sampling rate of 400µs and a resolution of 4mV/bit. So a range of +/- 0,5V from the reference level of 2,50V is covered. The digital error signal has to pass a digital notch filter in order to suppress the AC voltage ripple of twice of the mains frequency. A subsequent error amplifier with PI characteristic cares for stable operation of the PFC preconverter. During ignition and pre-run
mode the notch filter is bypassed in order to increase control loop reaction.

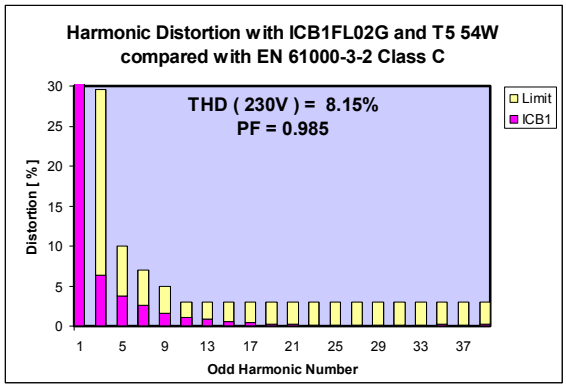
The zero current detection is sensed by a separate pin PFCZCD. The information of finished current flow during demagnetization is required in CritCM and in DCM as well. The input is equipped with a special filtering including a blanking of typically 500ns and is combined with a large hysteresis between the thresholds of typically 0,5V and 1,5V. In case of bad coupling between primary inductor winding and secondary ZCD-winding an additional filtering by a capacitor at ZCD pin might be necessary in order to avoid mistriggering by long lasting oscillations during
switching slopes of the PFC MOSFET.

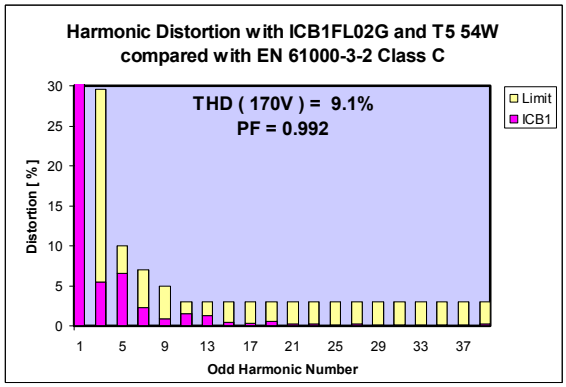
The diode D11 (Fig. 36) has the function of increasing the circuit robustness against Surge-Signal-Impacts.

PFC – Input Voltage dependence with T5 54W

The line current harmonics were analysed in the application of a ballast board for the operation of a T5 54W fluorescent lamp. For the nominal line voltage and the extreme values of the voltage range from 170V to 270V the harmonics distortions relating to the fundamental mode lead to low THD < 9.2 % and high power factors exceeding PF > 0.975.

The dependence of THD and power versus line voltage is week. Analysing the single harmonic distortions sufficient distances to the limit values set by the EN 61000-3-2 Class C-Standard arise in the displayed range of line voltages. These performance of the PFC can be achieved using a constant design and dimensioning of the EMI-Filter.





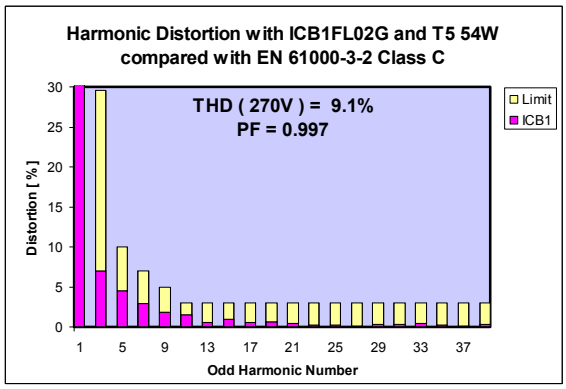
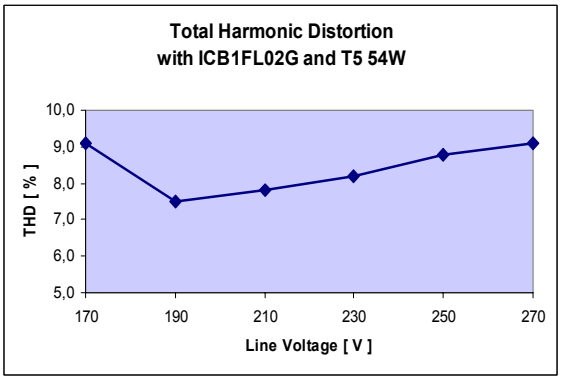


Fig. 43 – 45 Harmonic Distortions with ICB1 compared to EN 61000-3-2 at increased input voltages



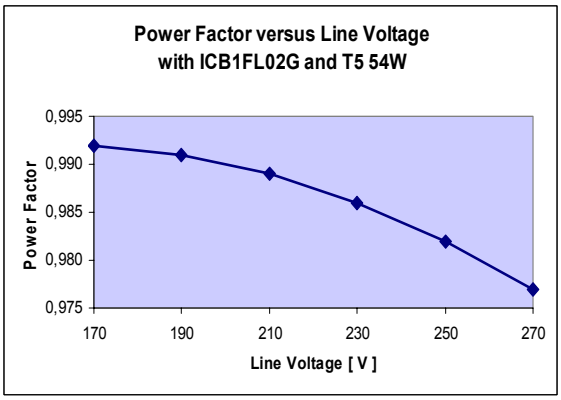


Fig. 46 - 47 Line Voltage Dependences of THD and Power Factor with ICB1- PFC in T5 FL Ballast

PFC – Load behaviour for different EMC-Filter

The line current harmonics were analysed with PFC controlled by the ICB1FL02G at variable input powers with enhanced filter topology. Using an EMC Filter (e.g. Fig. 36) without capacitance between L1 and Rectifier D1..D4 a clear THD increase for reduced input power is observed. For a Filter (Fig. 48) with additional capacitor C2 = 220 nF placed between L1 and rectifier and C3 = 10nF at medium and high input voltages a weaker increase of THD at low input powers exists. It is shown that the power quality can be varied strongly by filter design.

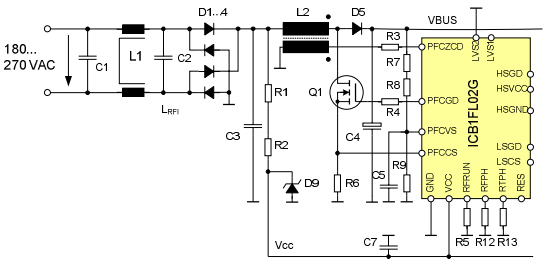


Fig. 48 Enhanced Filter-Configuration with additional C between L1 and Rectifier C1, C2, C3 variable and fixed values C4 = 10µF/450V, L1 = 2×68mH

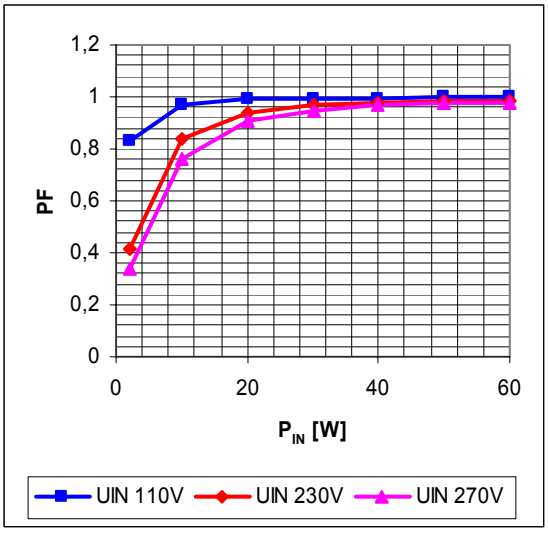


Fig. 49 Input Power dependences at different line voltages for C1 = C3 = 220 nF and C2 = 0 nF

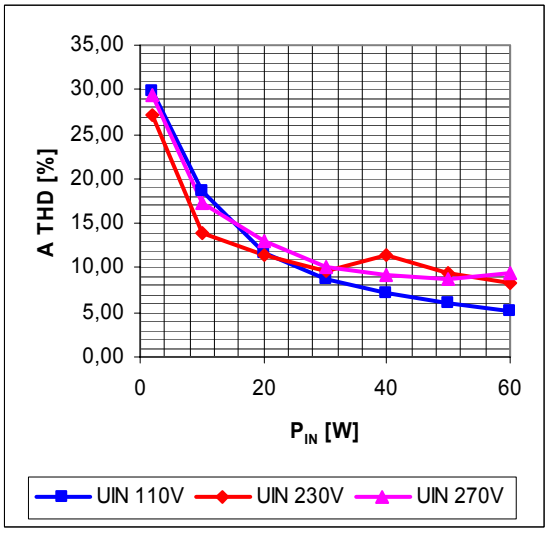


Fig. 51 THD dependences at different line voltages for C1 = C3 = 220 nF and C2 = 0 nF

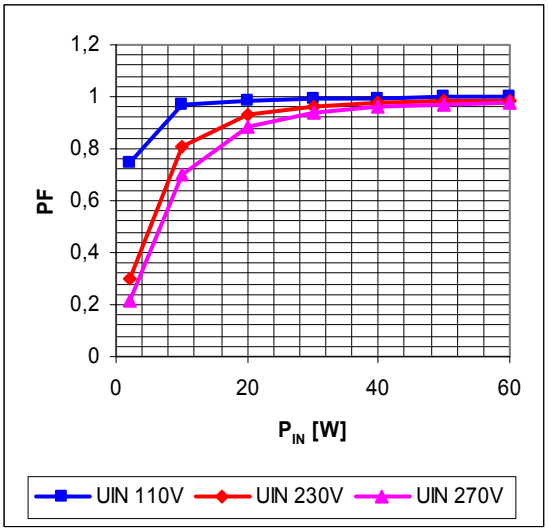


Fig. 50 Input Power dependences at different line voltages for C1 = C2 = 220 nF and C3 = 10 nF

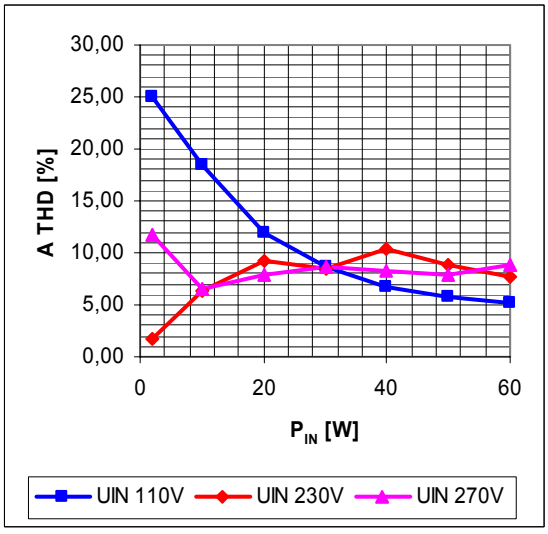


Fig. 52 THD dependences at different line voltages for C1 = C2 = 220 nF and C3 = 10 nF

5 Application Examples

Ballast Application for a single Fluorescent Lamp with current mode preheating

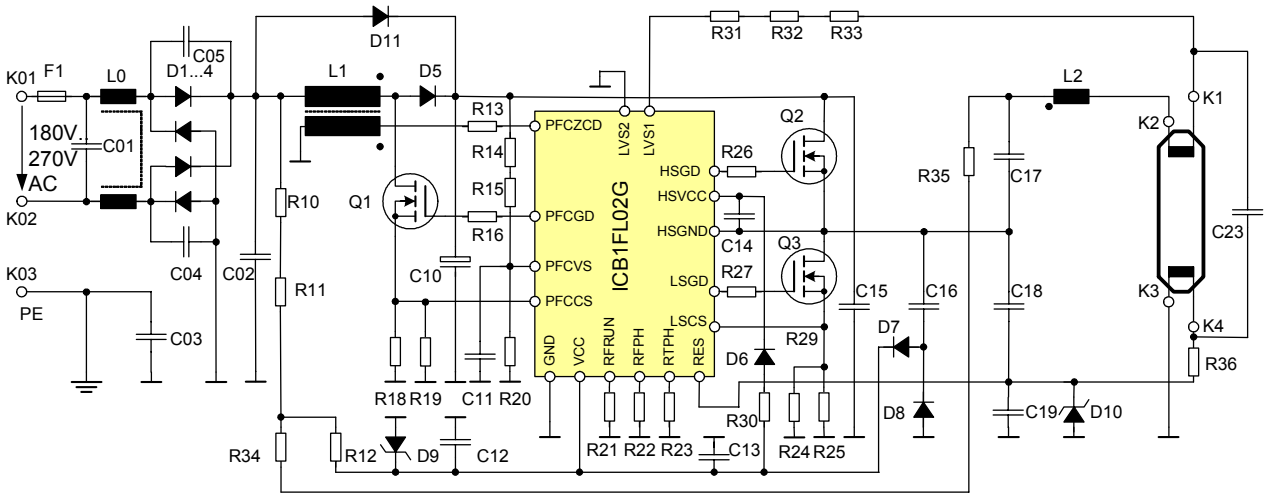


Fig. 53 Single FL Ballast Application with ICB1 for current mode preheating

Application for a single Fluorescent Lamp Ballast with voltage mode preheating

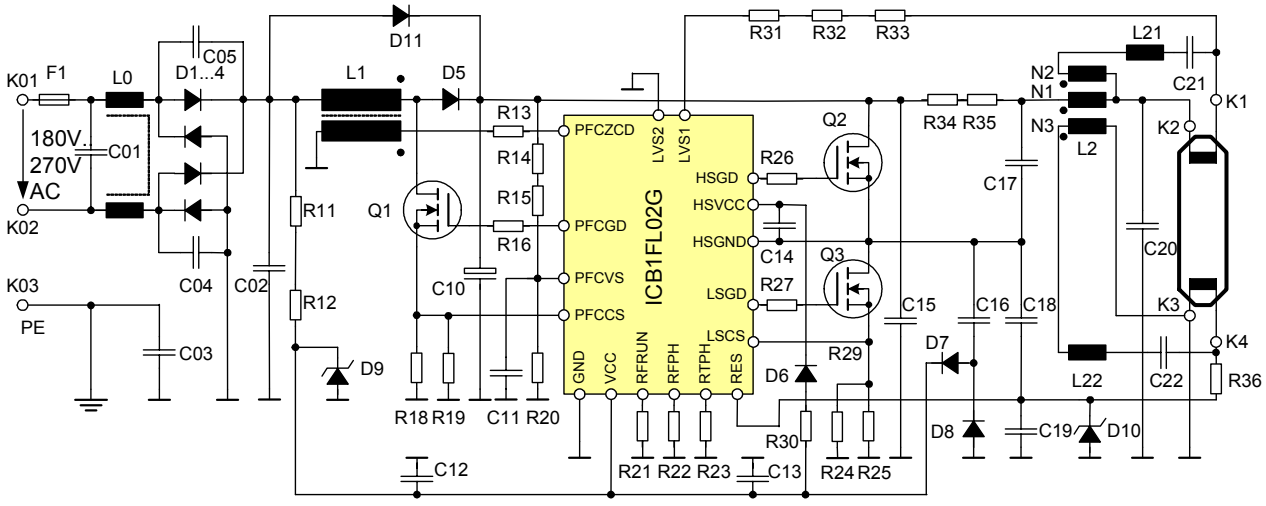


Fig. 54 Single FL Ballast Application with ICB1 for voltage mode preheating

Bill of Material for Single Lamp Ballast with current mode preheating in Fig. 53

	36W T8, single lamp, current mode preheat						**ICB1FL02G**	
	Input Voltage 180VAC...270V AC							
				Package				Package
F1	Fuse 1A slow	Wickmann	type 360					
K1	Filament1, side A					R10	390kΩ	.1206
K2	Filament1, side B	WAGO	B-Nr: 250-403			R11	330kΩ	.1206
K3	not connected					R12	330kΩ	.1206
K4	not connected					R13	33kΩ	.1206
K5	Filament2, side 1	WAGO	B-Nr: 250-403			R14	820kΩ	.1206
K6	Filament2, side 2					R15	820kΩ	.1206
K11	AC Input					R16	22Ω	.0805
K12	AC Input	WAGO	B-Nr: 250-403					
K13	PE					R18	4,7Ω	.1206
IC1	ICB1FL02G	Infineon	Q67045-A5088	SO-20		R19	2,2Ω	.1206
Q1	SPD03N60C3	Infineon	Q67040-S4421	D-Pack		R20	10kΩ	.0805
Q2	SPD03N60C3	Infineon	Q67040-S4422	D-Pack		R21	11,0kΩ (45,4kHz!)	.0805
Q3	SPD03N60C3	Infineon	Q67040-S4423	D-Pack		R22	27kΩ (64kHz!)	.0805
D1…D4	S1M	Fairchild	(1000V/1A/2µs)	DO-214AC		R23	12kΩ (1400ms!)	.0805
D5	MURS160T3	ON Semi	(600V/1A/75ns)	SMB		R24	1Ω	.1206
D6	BYG26J	Philips	(600V/1A/30ns)	SOD124		R25	1Ω	.1206
D7	BYG22D	Philips	(200V/1A/25ns)	DO214		R26	22Ω	.0805
D8	BYG22D	Philips	(200V/1A/25ns)	DO215		R27	22Ω	.0805
D9	BZX284C16	Philips		SOD110				
D10	BZX284C4V7	Philips		SOD110				
D11	S1M	Fairchild	(1000V/1A/2µs)	DO-214AC		R30	10Ω	.1206
L101	2x68mH/0,65A	Epcos	B82732F2651A001			R31	330kΩ	.1206
L1	2,2mH	Epcos	152turns/16turns	EFD25/13/9		R32	330kΩ	.1206
	total gap= 1,1mm	2 pcs	B66421-U160-K187			R33	390kΩ	.1206
L2	2,05mH	Epcos	182turns	EFD25/13/9		R34	470kΩ	.1206
	total gap= 2mm	2 pcs	B66421			R35	470kΩ	.1206
L21	not assembled					R36	56kΩ	.1206
L22	not assembled							
							LVS2 →GND	
C01	220nF/X2/305V	Epcos	B32922-C3224-M	RM15				
C02	220nF/X2/305V	Epcos	B32922-C3224-M	RM15			R31, R32, R33:	
C03	2,2nF/Y2	Epcos	B81122-C1222-M000	RM10		145Vpeak x 1,5/215µA= 1016kOhm		
C04	not assembled						330k+330k+390k= 1050k	
C05	not assembled							
C10	10µF/450V	Epcos	B43888-A5106-M000	single end				
C11	2,2nF/50V/X7R	AVX		.0805				
C12	3,3nF/50V/COG	AVX		.1206				
C13	1µF/63V/MKT	Epcos	B32529-C5105M000	RM5				
C14	100nF/50V/X7R	AVX		.0805				
C15	22nF/630V/MKT	Epcos	B32621-A6223K000	RM10				
C16	1nF/1kV/Ceramic			RM7,5				
C17	150nF/630V	Epcos	B32612A6154K008	RM15				
C18	82pF; /1kV			RM7,5				
C19	22nF	AVX	63V/X7R	.0805				
C23	6,8nF/1600V/MKP	Epcos	B32612-J1682J008	RM15				
C21	not assembled							
C22	not assembled							
C100	33pF	AVX	50V/COG	.0805				
Status:	09.08.2006							

Bill of Material for Single Lamp Ballast – voltage mode preheating in Fig. 54

	54W T5, single lamp, voltage mode preheat						ICB1FL02G	
	Input Voltage 180VAC...270V AC							
				Package				Package
F1	Fuse 1A slow	Wickmann	type 360					
K1	Filament1, side A					R10	390kΩ	.1206
K2	Filament1, side B	WAGO	B-Nr: 250-403			R11	330kΩ	.1206
K3	not connected					R12	330kΩ	.1206
K4	not connected					R13	33kΩ	.1206
K5	Filament2, side 1	WAGO	B-Nr: 250-403			R14	820kΩ	.1206
K6	Filament2, side 2					R15	820kΩ	.1206
K11	AC Input					R16	22Ω	.0805
K12	AC Input	WAGO	B-Nr: 250-403					
K13	PE					R18	2,2Ω	.1206
IC1	ICB1FL02G	Infineon	Q67045-A5088	SO-20		R19	2,2Ω	.1206
Q1	SPD03N60C3	Infineon	Q67040-S4421	D-Pack		R20	10kΩ	.0805
Q2	SPD03N60C3	Infineon	Q67040-S4422	D-Pack		R21	11,0kΩ (45,5kHz!)	.0805
Q3	SPD03N60C3	Infineon	Q67040-S4423	D-Pack		R22	8,2kΩ (106,4kHz!)	.0805
D1…D4	S1M	Fairchild	(1000V/1A/2µs)	DO-214AC		R23	8,2kΩ (1025ms!)	.0805
D5	MURS160T3	ON Semi	(600V/1A/75ns)	SMB		R24	0,82Ω	.1206
D6	BYG26J	Philips	(600V/1A/30ns)	SOD124		R25	0,82Ω	.1206
D7	BYG22D	Philips	(200V/1A/25ns)	DO214		R26	22Ω	.0805
D8	BYG22D	Philips	(200V/1A/25ns)	DO215		R27	22Ω	.0805
D9	BZX284C16	Philips		SOD110				
D10	BZX284C4V7	Philips		SOD110				
D11	S1M	Fairchild	(1000V/1A/2µs)	DO-214AC		R30	10Ω	.1206
L101	2x68mH/0,65A	EPCOS	B82732F2651A001			R31	330kΩ	.1206
L1	1,58mH	EPCOS	B78326P7373A005	T1904		R32	390kΩ	.1206
						R33	390kΩ	.1206
L2	1,46mH	EPCOS	B78326P7374A005	T1905		R34	2,2MΩ	.1206
						R35	2,2MΩ	.1206
L21	100µH	EPCOS	B82145A1104J			R36	56kΩ	.1206
L22	100µH	EPCOS	B82145A1104J					
							LVS2 →GND	
C01	220nF/X2/305V	EPCOS	B32922C3224M	RM15				
C02	220nF/X2/305V	EPCOS	B32922C3224M	RM15			R31, R32, R33:	
C03	2,2nF/Y2	EPCOS	B81122C1222M000	RM10		167Vpeak x 1,5/230µA= 1089kOhm		
C04	not assembled						330k+390k+390k= 1110k	
C05	not assembled							
C10	10µF/450V	EPCOS	B43888A5106M000	single end				
C11	2,2nF/50V/X7R	EPCOS	B37941K5222K60	.0805				
C12	3,3nF/50V/COG	EPCOS	B37871K5332J60	.1206				
C13	1µF/63V/MKT	EPCOS	B32529C0105M000	RM5				
C14	100nF/50V/X7R	EPCOS	B37941K5104K60	.0805				
C15	22nF/630V/MKT	EPCOS	B32621A6223K000	RM10				
C16	1nF/630V/MKT	EPCOS	B32529C8102K000	RM5				
C17	150nF/630V/MKP	EPCOS	B32612A6154K008	RM15				
C18	82pF/2kV/2D3	Roederstein		RM7,5				
C19	22nF/50V/X7R	EPCOS	B37941K5223K60	.0805				
C20	4,7nF/1600V/MKP	EPCOS	B32652J1472J008	RM15				
C21	22nF/400V/MKT	EPCOS	B32620A6223J000	RM7,5				
C22	22nF/400V/MKT	EPCOS	B32620A6223J000	RM7,5				
C100	33pF/50V/COG	EPCOS	B37940K5330J60	.0805				
Status:	13.10.2006							

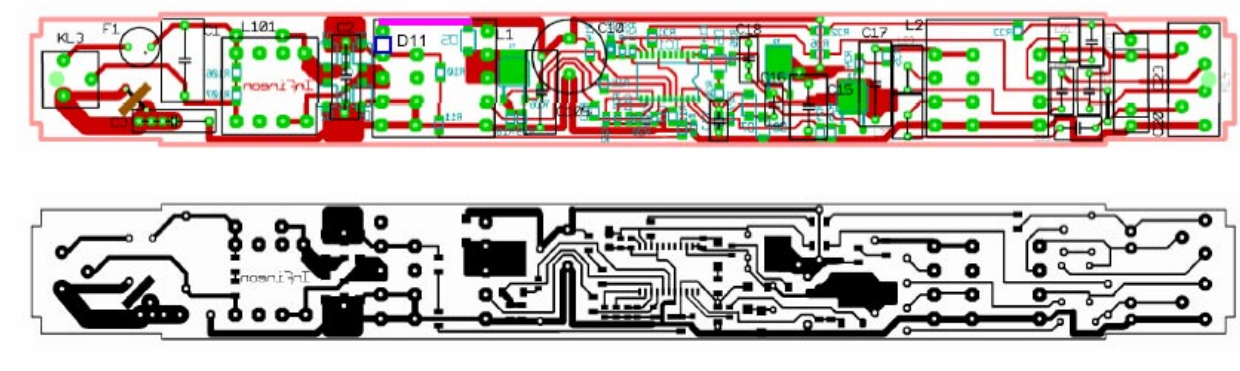


Fig. 55 Layout for Single FL Ballast Application with ICB1 for voltage mode preheating

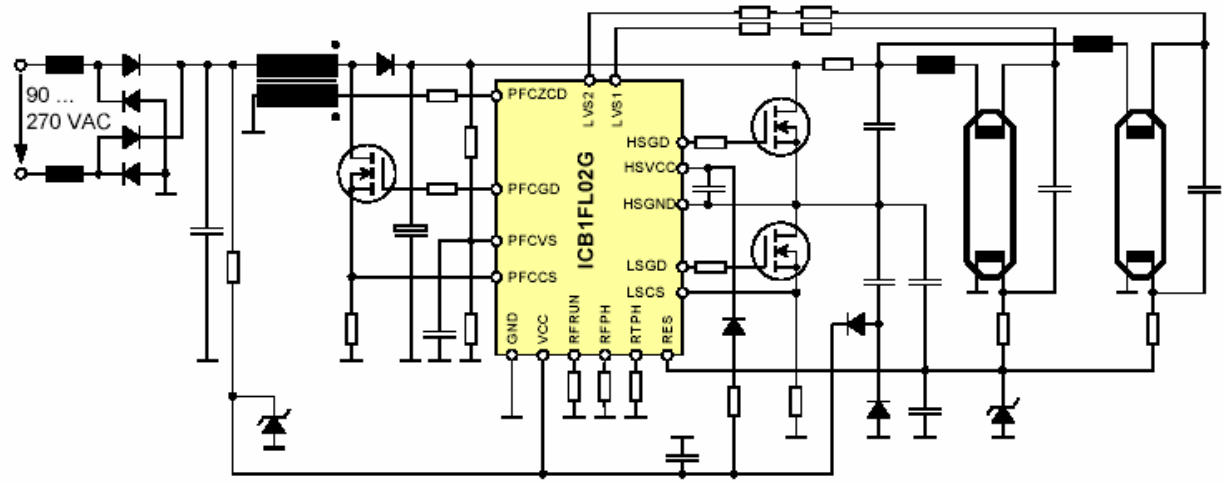


Fig. 56 Duo Parallel FL Ballast Application with ICB1 for current mode preheating

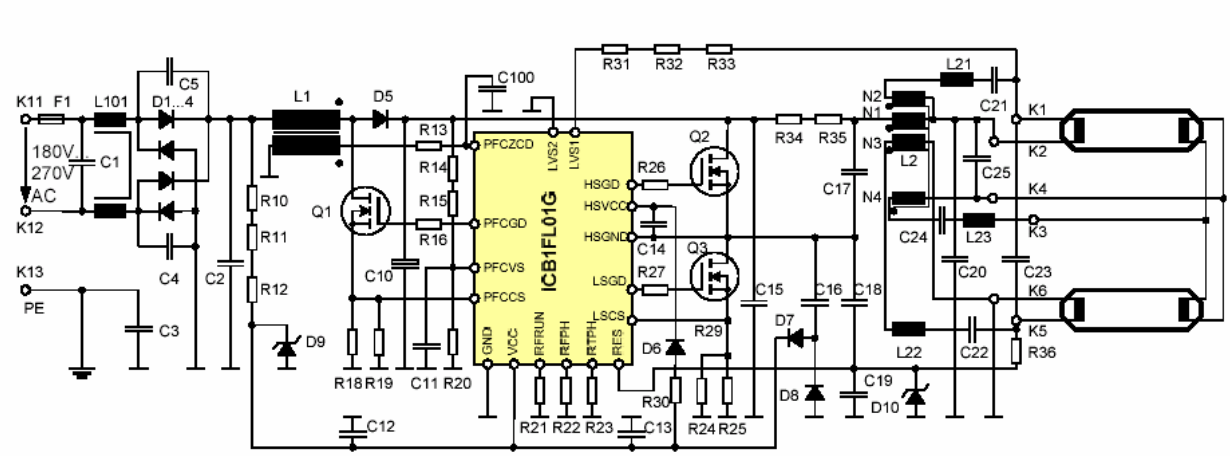


Fig. 57 Duo Serial FL Ballast Application with ICB1 for voltage mode preheating

6 Appendix

Design Equations - Example T5 54W-Ballast

Energy efficient Resonant Circuits can be dimensioned based on the outstanding ignition control functionality which allows an essential reduction of the lamp choke- volume by typically leading to decreased ferrite core losses. An additional effect on energy efficiency can be realized by using a resonant circuit dimensioning which minimizes the reactive currents during normal lamp operation. The following explicite equations deliver good initial values for the energy storing components:

$$L2 = \frac{0.635}{\sqrt{2}} \cdot \frac{U(C10)}{2 \cdot \pi \cdot f_{RUN} \cdot I_L}$$

$$L2 = \frac{0.635}{\sqrt{2}} \cdot \frac{411V}{2 \cdot \pi \cdot 45kHz \cdot 0.455A} = 1,43mH$$

$$C20_{min} = \frac{1}{\left(2 \cdot \pi \cdot f_{IGN}\right)^2 \cdot L2}$$

$$C20_{min} = \frac{1}{(2 \cdot \pi \cdot 70000kHz)^2 \cdot 1.43mH} = 3,6nF$$

$$C17_{min} = 10 \cdot C20_{min} = 36nF$$

I_L : effective lamp-current, U(C10) : bus voltage. The last equation satisfies the requirement of C20 << C17 for low reactive currents. The final values of C17 and C20 can be chosen with respect to costs / dimensions and preheat requirements respectively. Selected values: L2 = 1,46 mH , C20 = 4,7nF and C17 = 150 nF

Preheat Circuit

The dimensioning of the preheat circuit in constant current or constant voltage mode respectively is done according the standards IEC 60081 (double-capped fluorescent lamp performance specification) or IEC 60901 (single-capped fluorescent lamp performance specification) containing the valid preheat requirements.

PFC and Supply Section

Start-up resistors R11, R12:

$$R_{11} + R_{12} = \frac{V_{INMIN}}{I_{VCCqu2}} = \frac{200V}{150\mu A} = 1,33M\Omega$$

Selected value: R11= 470k; R12= 470k

Current limitation resistor R13 of PFC zero current detector (PFCZCD). The additional factor 2 is used in order to keep away from limit value.

$$R_{13} = \frac{V_{BUS} \cdot N_{SEC} \cdot 2}{I_{PFCZCD} \cdot N_{PRIM} \cdot 1} = \frac{410V \cdot 13 \cdot 2}{4mA \cdot 128 \cdot 1} = 20,8k\Omega$$

Selected value: R13= 33k.

PFC Voltage sense resistor R20:

$$R_{20} \le \frac{V_{REF}}{100 \cdot I_{PFCBIAS}} = \frac{2,50V}{100 \cdot 2.5\mu A} = 10k\Omega$$

Selected value: R20= 10kΩ.

PFC Voltage sense resistors R14, R15:

$$R_{14} + R_{15} = \frac{V_{BUS} - V_{REF}}{V_{REF}} \cdot R_{20}$$

$$R_{14} + R_{15} = \frac{410V - 2.5V}{2.5V} \cdot 10k = 1630k\Omega$$

Selected values: R14 = R15 = 820kΩ

Low pass capacitor C11:

$$C_{11} = \frac{1 \cdot \left(R_{20} + R_{14} + R_{15}\right)}{2 \cdot \pi \cdot f_{C1} \cdot R_{20} \cdot \left(R14 + R_{15}\right)}$$

$$C_{11} = \frac{1 \cdot (10k + 820k + 820k)}{2 \cdot \pi \cdot 10kHz \cdot 10k \cdot (820k + 820k)} = 1,60nF$$

Selected corner frequency f_{C1}= 10kHz.

Selected value C3= 2,2nF .

PFC Shunt resistors R18, R19:

$$\frac{R_{18} \cdot R_{19}}{R_{18} + R_{19}} = \frac{V_{PFCCSOFF} \cdot \eta \cdot V_{INACMIN} \cdot \sqrt{2}}{4 \cdot P_{OUTPFC}}$$

$$\frac{R_{18} \cdot R_{19}}{R_{18} + R_{19}} = \frac{1V \cdot 0.95 \cdot 180V \cdot \sqrt{2}}{4 \cdot 55W} = 1.1\Omega$$

Selected values: R18= 2,2 Ω; R19= 2,2 Ω

Set resistor R21 for run frequency, at a projected run frequency of 45kHz:

$$R_{21} = R_{FPH} = \frac{5 \cdot 10^8 \cdot \Omega Hz}{45kHz} = 11,1 \cdot k\Omega$$

Selected value: R21= 11,0k Ω

Set resistor R22 for preheating frequency, at a projected preheating frequency of 105kHz:

$$R_{22} = R_{FPH} = \frac{R_{FRUN}}{\frac{f_{PH} \cdot R_{FRUN}}{5 \cdot 10^8 \cdot \Omega Hz} - 1}$$

$$R_{22} = \frac{11k}{\frac{105kHz \cdot 11k}{5 \cdot 10^8 \cdot \Omega Hz} - 1} = 8.4k\Omega$$

Selected value: R22= 8,2kΩ

Set resistor R23 for preheating time, at a projected preheating time of 900ms:

$$R_{23} = R_{TPH} = \frac{T_{PH}(ms)}{\frac{112ms}{k\Omega}} = \frac{900ms}{\frac{112ms}{k\Omega}} = 8,93k\Omega$$

Selected value: R23 = 8,2kΩ .

Gate drive resistors R16, R26, R27 are recommended to be equal or higher than 10Ω.

Shunt resistors R24, R25:

The selected lamp type 54W-T5 requires an ignition voltage of V_{IGN}= 800V peak. In our application example the resonant inductor is evaluated to L2= 1,46mH and the resonant capacitor C20= 4,7nF. With this inputs we can calculate the ignition frequency f_{IGN} :

$$f_{IGN} = \sqrt{\frac{1 + \frac{V_{BUS} \cdot 2}{\pi \cdot V_{IGN}}}{4 \cdot \pi^2 \cdot L_2 \cdot C_{20}}}$$

$$f_{IGN} = \sqrt{\frac{1 + \frac{410V \cdot 2}{\pi \cdot 800V}}{4 \cdot \pi^2 \cdot 1.46mH \cdot 4.7nF}} = 70,0kHz$$

The second solution of this equation with a minus instead of a plus – sign leads to a result of 50163Hz is on the capacitive side of the resonant rise. This solution is not taken into account because the operating frequency approaches from the higher frequency level.

In the next step we can calculate the current through the resonant capacitor C20 when reaching a voltage level nof 800V peak.

$$I_{C20} = V_{IGN} \cdot 2 \cdot \pi \cdot f_{IGN} \cdot C_{20}$$

$$I_{C20} = 800V \cdot 2 \cdot \pi \cdot 69.759kHz \cdot 4.7nF = 1,65A$$

Finally the resistors R24, R25 can be calculated from IC20 and the current limitation threshold during ignition mode.

$$\frac{R_{24} \cdot R_{25}}{R_{24} + R_{25}} = \frac{V_{LSCSLIMIT}}{I_{C20}} = \frac{0,8V}{1,65A} = 0,485\Omega$$

Selected values are R24 = R25 = 0,82kΩ.

Lamp voltage sense resistors R31, R32, R33:

The selected lamp type 54W-T5 has a typical run voltage of 167V peak. We decide to set the EOL-thresholds at a level of 1,5 times the run voltage level (= 250,5V peak).

$$R_{31} + R_{32} + R_{33} = \frac{V_{LEOL}}{I_{LVSEOL}} = \frac{250,5V}{215\mu A} = 1165k\Omega$$

Selected values: R31= 390kΩ , R32= 390kΩ , R33= 390kΩ.

Current source resistors R34, R35 for detection of high-side filament:

$$R_{34} + R_{35} = \frac{V_{INMIN}}{ILVSSINKMAX} - \left(R_{31} + R_{32} + R_{33}\right)$$

$$R_{34} + R_{35} = \frac{200V}{26\mu A} - 1170k\Omega = 6522k\Omega$$

Selected values: R34= 2,2M; R35= 2,2M;

Current limitation resistor R30 for floating bootstrap capacitor C14:

A factor of 2 is provided in order to keep current level significant below LSCS turn-off threshold.

$$R_{30} \geq \frac{2 \cdot V_{CCON}}{V_{LSCSOVC}} \cdot \frac{R_{24} \cdot R_{25}}{R_{24} + R_{25}}$$

$$R_{30} \geq \frac{2 \cdot 14 \cdot V}{1,6 \cdot V} \cdot \frac{0,82 \cdot 0,82 \cdot \Omega}{0,82 + 0,82} = 7,18\Omega$$

Selected value: R30= 10Ω.

Low-side filament sense resistor R36:

For a single lamp ballast

$$R_{36} \leq \frac{V_{RESC1MIN}}{I_{RES3MIN}} = \frac{1,55V}{27,0\mu A} = 57,4k\Omega$$

Selected value: R36= 56kΩ

$$R_{36A} \geq \frac{V_{RESC1MAX}}{I_{RES3MAX}} = \frac{1,65V}{15,1\mu A} = 109,3k\Omega$$

Selected values in a topology with 2 lamps in parallel: R36A = 110kΩ , R36B = 110kΩ.

Low pass filter capacitor C19:

Capacitor C19 provides a low pass filter together with resistor R36 in order to suppress AC voltage drop at the low-side filament. When we estimate an AC voltage of 10V peak-to-peak at low-side filament during run mode at f_{RUN}= 40kHz, we need a suppression of at least a factor F_{LP} = 100 (-40dB).

$$C_{19} = \frac{\sqrt{\left(F_{LP}\right)^2 - 1}}{2 \cdot \pi \cdot f_{RUN} \cdot R_{36}}$$

$$C_{19} = \frac{\sqrt{100^2 - 1}}{2 \cdot \pi \cdot 40\text{kHz} \cdot 56\text{k}\Omega} = 7,1\text{nF}$$

Selected value for better ripple suppression:
C19 = 22nF.

Detection of capacitive mode operation via C18:

The DC level at pin RES is set by R36 and the source current I_{RES3}. The preferred AC level is in the range between ΔV_{ACRES}= 1,5V to 2,0V at a ΔV_{BUS}= 410V.

$$C_{18} = \frac{C_{19} \cdot \Delta V_{ACRES}}{\Delta V_{BUS}} = 22\text{nF} \cdot \frac{2\text{V}}{410\text{V}} = 107\text{pF}$$

Selected value: C18= 82pF.

Bandpass filters L21/C21 and L22/C22 can be used in order to conduct filament currents preferred at preheating frequency and to suppress these currents during run mode.

Inductor L1 of the boost converter:

The inductivity of the boost inductor typically is designed to operate within a specified voltage range above a minimum frequency in order to get an easier RFI suppression. It is well known, that in critical conduction mode (CritCM) there is a minimum operating frequency at low input voltages and another minimum at maximum input voltage. In state-of-the-art CritCM PFC controllers we use the lowest value out of these two criteria:

At minimum AC input voltage:

$$L_A = \frac{\left(V_{INACMIN} \cdot \sqrt{2}\right)^2 \cdot \left[V_{BUS} - \left(V_{INACMIN} \cdot \sqrt{2}\right)\right] \cdot \eta}{4 \cdot F_{MIN} \cdot P_{OUTPFC} \cdot V_{BUS}}$$

$$L_A = \frac{(180\text{V} \cdot \sqrt{2})^2 [410\text{V} - (180\text{V} \cdot \sqrt{2})] \cdot 0,95}{4 \cdot 25\text{kHz} \cdot 60\text{W} \cdot 410\text{V}} = 3,89\text{mH}$$

At maximum AC input voltage

$$L_B = \frac{\left(V_{INACMAX} \cdot \sqrt{2}\right)^2 \cdot \left[V_{BUS} - \left(V_{INACMAX} \cdot \sqrt{2}\right)\right] \cdot \eta}{4 \cdot F_{MIN} \cdot P_{OUTPFC} \cdot V_{BUS}}$$

$$L_B = \frac{(270\text{V} \cdot \sqrt{2})^2 [410\text{V} - (270\text{V} \cdot \sqrt{2})] \cdot 0,95}{4 \cdot 25\text{kHz} \cdot 60\text{W} \cdot 410\text{V}} = 1,58\text{mH}$$

With the new control principle for the PFC preconverter we have a third criteria that covers the maximum on-time $t_{PFCOM-MAX}$= 23,5µs:

$$L_C = \frac{\left(V_{INACMIN} \cdot \sqrt{2}\right)^2 \cdot T_{ONMAX} \cdot \eta}{4 \cdot P_{OUTPFC}}$$

$$L_C = \frac{(180\text{V} \cdot \sqrt{2})^2 \cdot (23,5\mu\text{s}) \cdot 0,95}{4 \cdot 60\text{W}} = 6,03\text{mH}$$

With the assumed conditions the lowest value out of L_A, L_B, L_C is 1,58mH.

Selected value: L1 = 1,58 mH .

Layout provisions

As some protection-functions require the detection and processing of small signals special care has to be taken regarding the influence of parasitic layout effects. In particular for the Lamp Voltage sensing Pins LVS1 / LVS2 the layout should possess conducting lines with minimum coupling capacitance to those having high slopes of temporal voltage variations.

Initial Operation with Fluorescent Lamp

1 Start with inverter

1.1 Supply a voltage (e.g.100V DC) from a current limited DC source direct to the bus capacitor. The operation will stop latest during Run Mode due to bus undervoltage. PFC Gate drive is active during this kind of test.

1.2 If a start-up cannot be achieved reduce value of start-up resistor (e.g. short one of a series connection of two or more). If supply voltage of IC (Vcc) has to be fed from an external voltage source avoid an overload of zener diode (15V...16V). Current source out of Pin 12 (RES) is active at Vcc > 10V. IC turns over into active mode only if Vcc > 14,5V , voltage at Pin 8 (PFCVS) > 15% of rated bus voltage, current into Pin 13 / 14 (LVS1 / 2) > 25µA and voltage at Pin 12 (RES) < 1,6V.

1.3 It is recommended to disable both LVS inputs by connecting to GND. This measure disables sense of High-Side filament and end-of-life (EOL) protection.

1.4 With the measures 1.1. – 1.3. the inverter should be able to achieve Run Mode and stop due to bus undervoltage. Otherwise a capacitive load operation , an over-current or a not sufficient Vcc supply current might stop operation earlier.

1.5 In order to avoid an overcurrent during ignition mode it can be helpful to increase the run frequency on a value higher than resonance frequency of LC.

1.6 Saving testing time during Ballast production the RTPH resistor can temporarily be paralled by an additional resistor in order to reduce preheating time.

2 Continue with PFC section

2.1 Use a load on bus voltage, e.g. the inverter itself or a resistor in parallel to bus capacitor. It is possible for start-up to feed an external DC supply via a diode to the bus capacitor. The diode will switch off the current from external supply when voltage via PFC boost converter becomes higher.

2.2 For test purposes the PFC voltage sense resistor value can be reduced (e.g. short one of a series connection of two or more) in order to achieve a lower output voltage.

2.3 PFC section starts with a delay of about 1ms in respect to inverter. It starts with a fixed frequent operation of 25kHz and changes over into DCM operation as soon as there is a sufficient voltage level available at Pin 7 (PFCZCD > 1,5V).

Operation with Lamp Substitution Resistor

For simplicity of operation and fast achievement of reproducible working conditions the usage of a lamp substitution resistor can be advantageous.

With initial insertion of both appropriate filament- and lamp- substitution resistors the reduced LVS-current is not sufficient for filament-detection. So it is necessary to start initially only with filament-substitution- resistor or -shortcut and provide an abrupt transition from open lamp circuit to specified lamp resistance during Preheat Mode. As alternative with a simplified handling it is possible to supply the ballast with main voltage and provide a sufficiently short interruption of the lamp substitution circuit which simulates a lamp removal.

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