F I N A L D E V I C E S P E C I F I C A T I O N

TYPE COMMERCIAL :UBA2010 (T)

EXPERIMENTAL :N5560

1. General description

The UBA2010 is a TL DIMMABLE HALF BRIDGE driver. The high voltage circuit is intended to drive and control fluorescent lamps (TL, PLL, and related types) with nominal mains voltages up to 277 VAC. It contains a driver circuit for an external half-bridge, an oscillator, and a control circuit for starting up, preheating, ignition, lamp burning and protection.

2. Features

- Dimming capability to about 1%
- Drives lamp types T12, T8 (2-4-5foot), PL-L(18-55W), PLC(18-26W) PLT(18-32W), and TLD(T8-6foot-70W)
- Lamp power dimming regulation
- High voltage level-shift for direct drive of 2 half-bridge power switches
- Adjustable preheat time
- Adjustable preheat current
- Prevents capacitive-mode operation of the half-bridge
- Stop function
- Flash reduction when starting at low dim levels
- Low power startup requirements
- Single ignition attempt

3. Block diagram

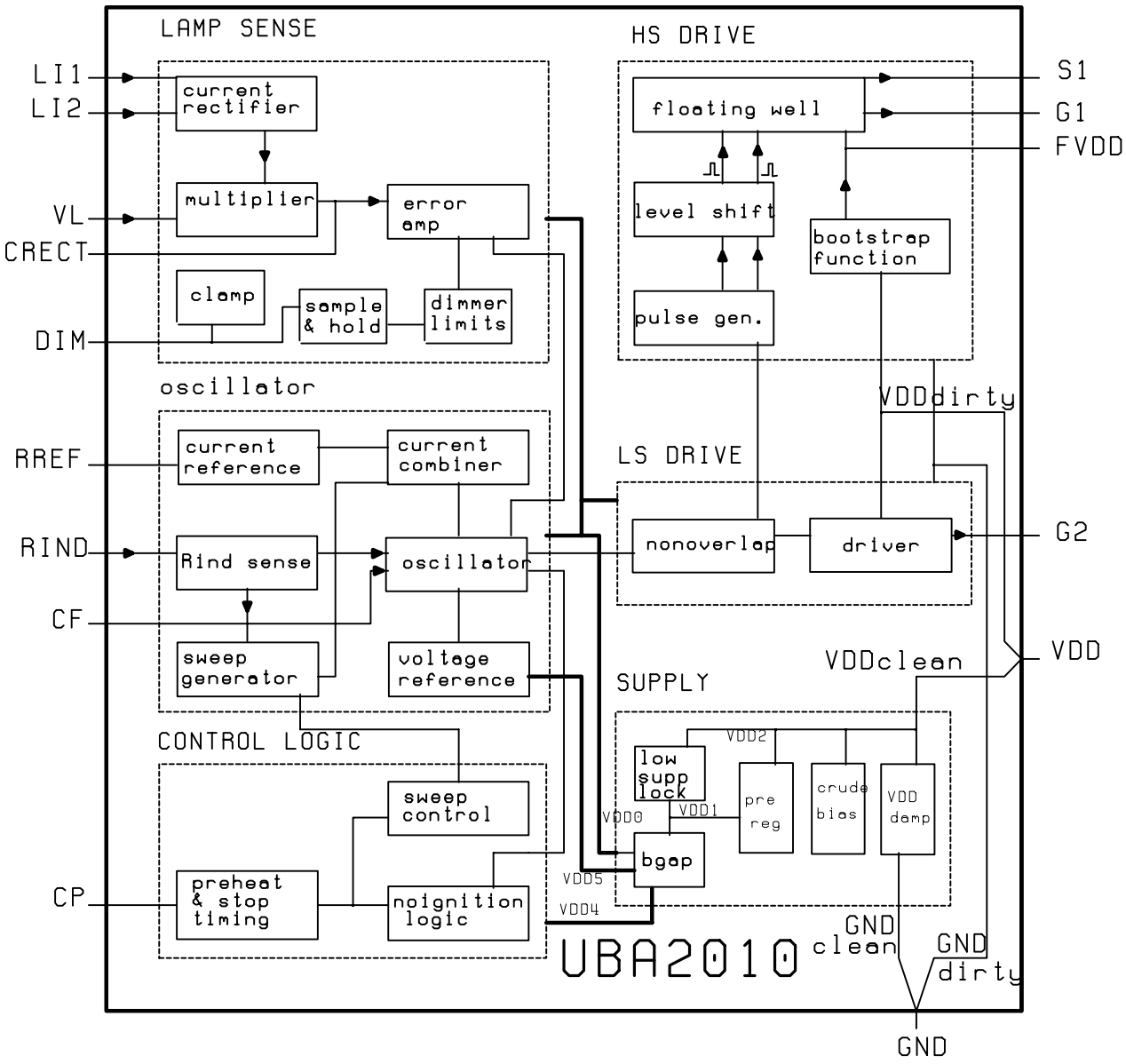

Figure 1

4. Package outline

SOT109 (SO 16 small) UBA2010 (T)
SOT38 (16p DIP) UBA2010

5. Pinning

1	CRECT	Lamp power filtering capacitor
2	VL	Sensing of averaged lamp voltage
3	CP	Preheat and stop timing capacitor
4	DIM	Dimming level control
5	nc	High-voltage spacer (only in case for SO encapsulation)
6	S1	Source of high-side switch
7	G1	Gate of high-side switch
8	FVDD	Floating supply; supply for high-side switch
9	GND	Ground
10	G2	Gate of low-side switch
11	VDD	Supply for ground level control and drive
12	RREF	Reference resistor
13	CF	Capacitor for setting VCO frequency
14	RIND	Inductor current monitoring input
15	LI1	Differential input for sensing lamp current
16	LI2	Differential input for sensing lamp current

6. Functional description

6.1 Introduction

A typical ballast system with the UBA2010 will consist of a separate preconditioner stage for power factor correction and inrush current limiting, and a half-bridge driven resonant stage that provides lamp drive and dimming control. The UBA2010 contains a half-bridge driver for two external power switches, and control circuits for preheat, ignition, on-state, dimming and protection. Dimming is achieved through closed loop control of a feedback sense current and voltage, down to 10% nominally, with 1% possible through external component changes, without "moding" or other instabilities. This is accomplished with a semi-triangular oscillator used to implement transistor forward conductance control, as described in this specification. In addition, the UBA2010 provides the means for reducing the visual aspects of a "flash" when starting at low dim levels, and with use of an external resistor, for minimizing or eliminating striations by employing an asymmetrical half-bridge drive waveform.
The UBA2010 can also be used effectively as a building block in a digital ballast system, together with a separate microprocessor for the digital communication interface. The UBA2010 provides a highly integrated solution to the need for half-bridge drive, lamp power feedback control, and other analog housekeeping functions. While the UBA2010 provides most of the half-bridge control functions, many of the control parameters (e.g. preheat time, stop time, lamp power, etc.) can be easily set by digital inputs from the microprocessor.

6.2 Initial startup

Initial charging of the supply capacitor tied to the VDD pin and the bootstrap capacitor tied to the FVDD pin is accomplished with a resistor connected directly to a high-voltage DC bus. Throughout the initial charging phase, which occurs for the voltage at the VDD pin in the range of 0 to VDon, the circuit is defined to be in the start-up phase. During the startup phase, the circuit is in a non- oscillating condition. In addition simultaneous conducting of T1 and T2 is prevented throughout this phase. For the voltage at the VDD pin exceeding the level of VDlow, switch T2 will be on and switch T1 will be off to ensure that the bootstrap capacitor is charged to a voltage level near VDD at the end of the initial charging phase. Also the capacitor at pin CF is charged to a level of Vreg during the start-up phase.
Note : For VDD < VDlow (during the start-up phase) transient voltages at the pins S1, G1, FVDD should be avoided.

6.3 Oscillation

Once the supply capacitor is charged to a value above VDon, the circuit is switched into the preheat state, and oscillation can commence. The oscillator alternately switches T1 and T2 into conduction with an identical forward conductance time. The duration of non-overlap between the conductance of T1 and T2 is fixed for the design value of Rref.
The oscillator normally operates in the forward conductance mode of control by implementing a semi-triangular

voltage waveform at the CF pin (see fig. 2). Given an inductive mode of operation of the halve-bridge, the flat portion of the waveform corresponds to the reverse conduction whereas the sloped portions coincide with the forward conduction. The duration of the sloped portions is referred to as the FWD time. Moreover, the rising slope coincides with the forward conductance of the top half-bridge switch and the falling slope with the forward conductance of the bottom half-switch. The end of the reverse conduction is detected by a zero crossing at the RIND pin. The resulting semi-square wave at pin S1 is then used to drive the power circuit and the lamp as shown in the application circuit.

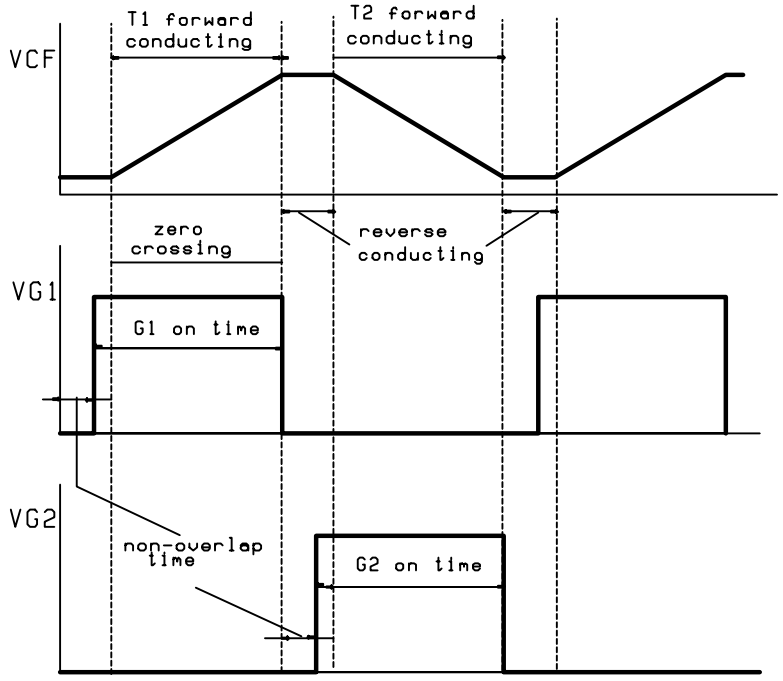

Figure 2

6.4 Starting oscillation

Once the supply capacitor is charged above VDon, the oscillation begins by discharging the CF capacitor. This capacitor has been charged to Vreg during the startup phase. When the voltage at pin CF reaches VCFl, switch T2 is turned off, and the non-overlap timing is started. Following the non-overlap duration, switch T1 is brought into the conducting state. During the first switching cycle the CF capacitor begins charging. After the first switching cycle of T1 and T2, the CF capacitor begins charging only after a zero crossing is detected at the RIND pin. Because, there is no guarantee that a zero crossing can be detected in the first switching cycle the non-overlap timer is temporarily used to start the first FWD charging period at the CF pin. Following this first cycle, the RIND

function works in the normal fashion.

Since there is no body diode current available during the first switching cycle to charge the half-bridge node, T1 is switched on the first time in the fully active mode rather than in the zero-voltage mode it normally operates. The gate drive voltage across T1 for this first switching cycle is about 2V lower compared to the normal running voltage.

6.5 Forward conductance time sweep and preheat control

The UBA2010 will start oscillation with its start FWD time (ICFst) and gradually increase this time at a controlled rate (see fig.3). This process continues until the inductor current results in a voltage at pin RIND below Vpre at the time T2 is switched off, and is then followed by a decrease in FWD time. This results in a regulated inductor current, and consequently a regulated lamp electrode current for the duration of the preheat cycle. The rate of increase in FWD time (SWPd) is 0,07% per cycle. The rate of decrease in FWD time (SWPup) is equal to 1.5 times SWPd, both at a typical frequency of 85kHz and Ccf=100pF. The ratio of increase and decrease in FWD time is internally fixed and is independent of the FWD time..

6.6 Preheat time

The preheat cycle begins at the instant oscillation starts and its duration, Tpre, is determined by the capacitor tied to the CP pin and reference current set by the resistor tied to pin RREF, For the design value of RREF, the preheat time is 0.94 second per 150nF connected to pin CP, and consists of 16 pulses at CP. While capacitive panic mode is detected the current charging CP is 10 times higher, rendering the CP pulses 10 times shorter for a continuous CM panic situation.

6.7 FWD sweep to ignition

After the preheat time is over, the FWD time increases further, now without regard to the Vpre level at pin RIND. The rate of increase in FWD time is equal to SWPdwn. During this upwards sweep in FWD time the circuit approaches the resonance frequency of the load. Consequently, a high voltage appears across the lamp which normally results in lamp ignition.
Also after the preheat time the stop timing circuit is activated. If after the stop time the current into the VL pin is higher then the IVLstop, the circuit goes into standby .

6.8 Failure to ignite

Failure to ignite will be detected by sensing the rectified open lamp voltage by means of pin VL. The averaged representation of the rectified lamp voltage must be fed as a current signal (determined by external components) into pin VL, which has a low impedance to ground (approximately 3kΩ). The STOP function is available at the instant ignition sweep starts and is present during normal operation. The stop timing circuit is activated at the end of the preheat period as well as if the current into the VL pin, sampled at the time T2 is switched off, exceeds the level IVLstop (corresponding to a lamp voltage of Vstop). The latter normally occurs during ignition sweep, lamp removal, or lamp failure. The stop timing duration, Tstop, is set by the capacitor tied to the CP pin and is equal to 8/16 of the preheat time. The activated stop timing circuit will count 8 pulses at the CP pin. At the end of the 8th pulse, if the lamp is below Vstop, the lamp is considered to have ignited, the stop timing counter is reset, and the multiplier acts normally, feeding a current proportional to the product of lamp voltage and current into the CRECT pin. However, if the lamp voltage exceeds Vstop, the lamp is considered to have not ignited. At the next conductance cycle for T2, the half-bridge will be put into the non-oscillating state or standby mode. The Vstop level should be chosen to be just above (+10%) the maximum lamp voltage under dimming conditions. The first time the lamp voltage exceeds Vstop after the occurrence of a preheat condition, the multiplier feeds no current into the CRECT pin as long as the lamp exceeds Vstop.

If the current into pin VL exceeds a second defined level, IVLmax (corresponding to an open circuit lamp voltage of Vmax), at the time T2 is switched off and before Tstop is exceeded, then the upward sweep in FWD time is stopped and is followed by a decrease in FWD time. When the open circuit lamp voltage drops below the Vmax the downward sweep stops and is followed by an increase in FWD time. The rate of increase and decrease in frequency (or 1/FWD) are equal to SWPup and SWPdwn respectively. This mode of dynamic lamp voltage regulation continues until the lamp ignites or the time Tstop is exceeded. Some wave forms during a failure are given in fig.4.

If the lamp voltage exceeds the Vpanic level (Vpanic=1.2 times Vmax) then the FWD time is decreased in a step change to its minimum value.

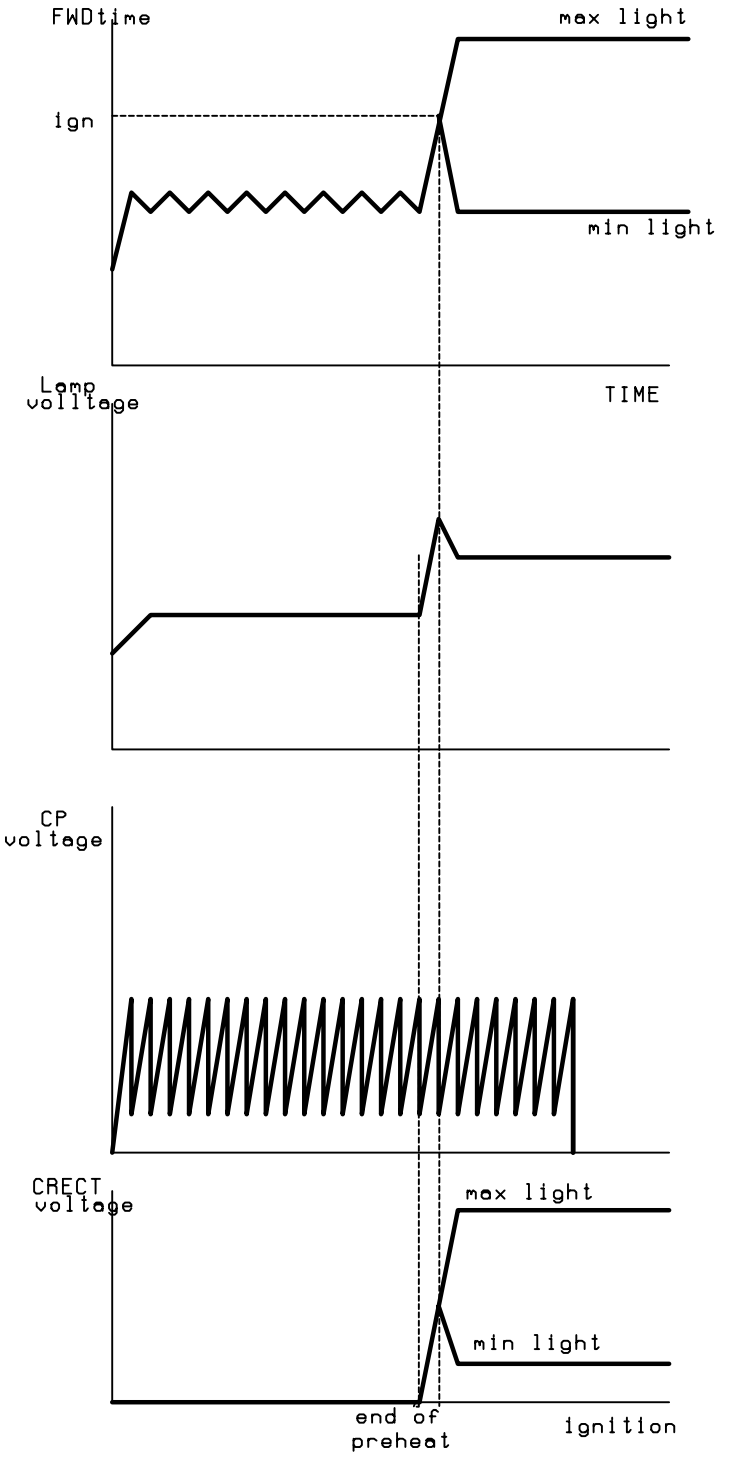

Figure 3 Preheat and ignition sequence

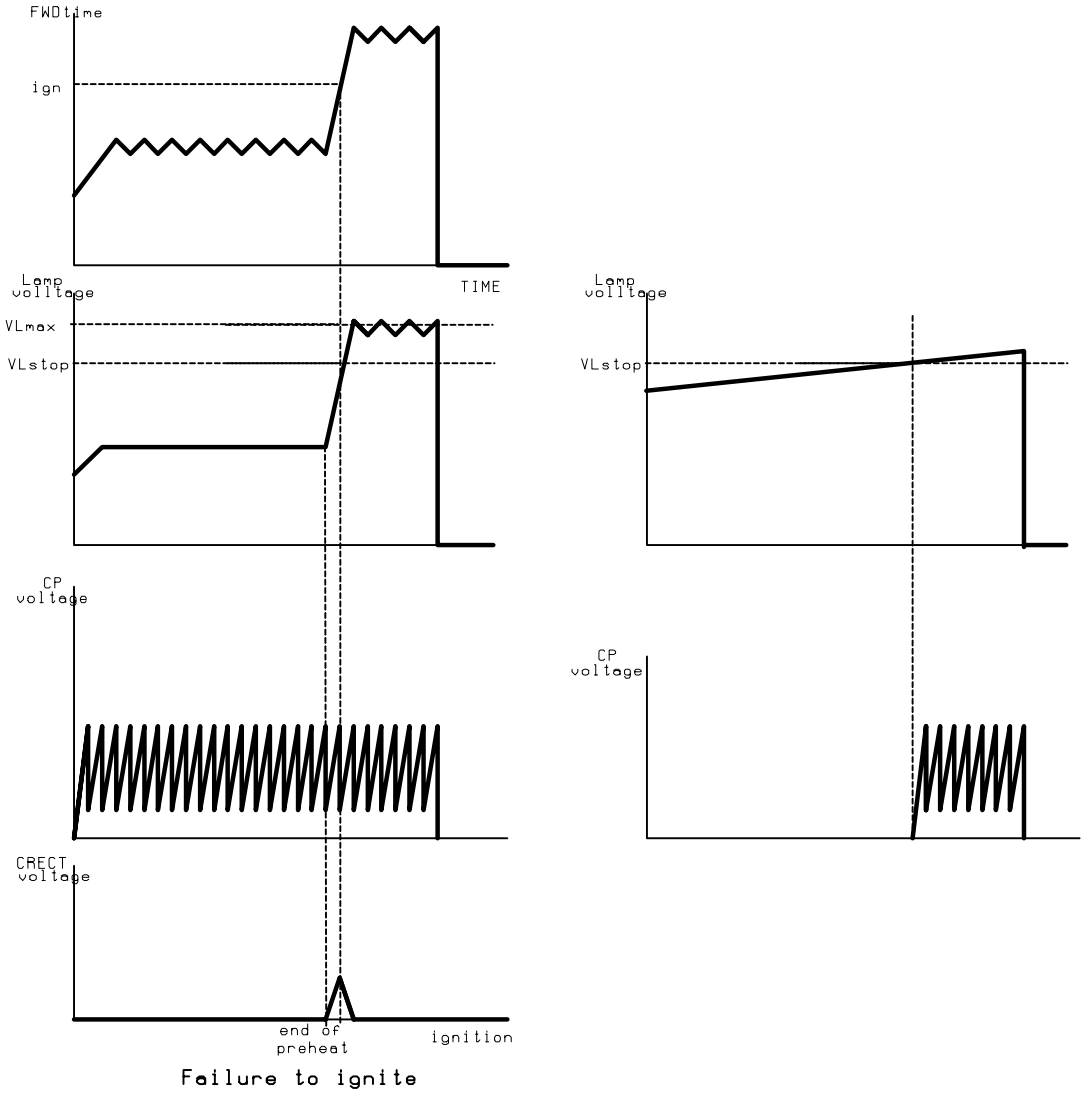

Figure 4

6.9 Standby state

The standby state is characterized by T1 being off and T2 being on. In this condition the voltage at pin VDD may rise to a maximum value of VDclmp, where it is limited by an on-chip zener function for current levels below 3mA. This state can only be exited by powering down the IC to below VDoff at the VDD pin, and powering back up to above VDon.

6.10 Normal operation

After a normal ignition, the FWD time continues to increase in a rate equal to SWPdwn. However since the lamp has ignited there is a large increase in the lamp power which is detected by the lamp current and voltage sensing pins (LI and VL), and converted into an output current at the CRECT pin which is proportional to the averaged lamp power. Consequently the capacitor tied to CRECT will start to charge. The initial value of Vcrect is zero volts.The voltage at the Crect pin is compared to an internal voltage Vcrect(ref). This voltage Vcrect(ref) is derived from the voltage at the DIM pin, as sampled during the last portion of the down going slope at the Cf pin. The voltage at Vcrect(ref) = {9/8(Vdim -1.62)+1.62} and is internally clamped to a minimum of 0.3V and a maximum of 3V. Once the control loop is closed (Vcrect virtually equals Vcrect(ref)) the error voltage between Vcrect and Vcrect(ref) affects the oscillator current.

The representation of the lamp voltage used to terminate the lamp power is internally clamped to a maximum of 85% of the stop level. For lamp voltages above 85% of the stop level, the circuit will therefore regulate the lamp current in stead of lamp power.

The delay from the moment of ignition to the time the lamp power reaches its regulated value is determined primarily by the charging time of the CRECT capacitor (refer to fig 5). With the dim level set at 100% light output, the FWD time continues to increase (at the rate SWPdwn) until the voltage at CRECT reaches its maximum value of 3V and the feedback loop closes. With the dim level set at its minimum level, the CRECT capacitor only has to charge to 0.3V before the feedback loop closes and drives the FWD time back down almost instantaneously to reduce the light level. As a result, the duration of the high light condition following ignition is very short for low dim settings, and the visual impact of the undesired "light flash" is minimized.

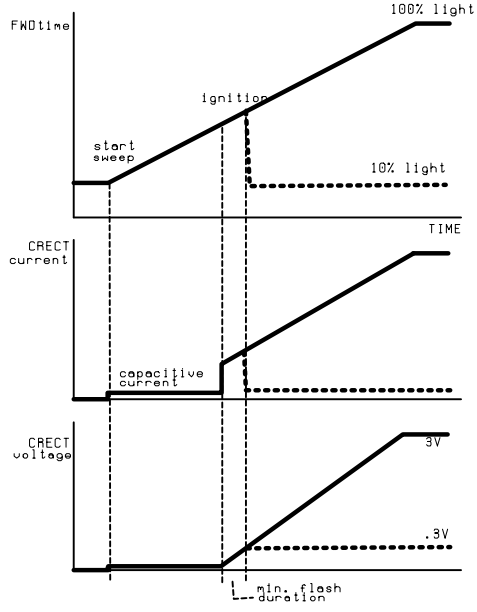

Figure 5 Ignition waveforms

6.11 Dimming

Dimming of the lamp is accomplished through the closed loop control of the average lamp power as long as the lamp voltage corresponds to IVL<IVLstopx.0.85, otherwise lamp current control. The voltage at the CRECT pin, representing the average lamp power, is compared to the reference voltage applied at the DIM pin. An internal high gain error amplifier drives the oscillator FWD time until the difference between these two inputs is reduced to near zero, resulting in a linear and proportional control of the lamp power with DIM voltage. The waveform at the DIM pin is internally sampled during the falling sloped portion of the VCO waveform, and held just prior to the falling edge of the T2 gate drive signal. The usefull input range at the DIM pin for dimming control is between a maximum level of 2.79V and a minimum level of 0.44. Outside these levels the DIM control voltage (which is internally limited) has the same effect as the maximum or minimum values. The lamp control loop is only closed following a successful lamp ignition as discussed in section 6.10. External changes in the DIM control voltage should be slower than the rate of change in voltage at the CRECT pin (set by Rrect and Crect) and must never be instantaneous.

6.12 Lamp current rectification

The lamp current rectifier function is used to provide a full wave rectified representation of the ac lamp current waveform for use in regulating the lamp power. It consists of a bipolar current amplifier, whose inputs are formed by pins LI1 and LI2, and an external resistor network including sense resistor, Rs1, and a pair of identical input resistors, Rli. The ac lamp current is converted by the resistor network into a differential current, ILdiff, at the amplifier inputs. The output of the amplifier feeds a current, which is equal to the absolute value of the differential input current, to one of the inputs of the multiplier circuit. Very low lamp current levels can be accurately rectified and controlled by employing such an active circuit for the rectifier function.

The rectifier function operates in the following way. A lamp current flowing through the sense resistor Rs1 results in a proportional voltage across its terminals. Each terminal of Rs1 is connected through an input resistor, Rli, to one of the two rectifier input pins. These pins acts as current sources that maintain a zero difference voltage between the pins, and a common mode voltage given by: Vli1=Vli2=max{V1,V2}+RlixILbias

where V1 and V2 are the voltages of the two terminals of Rs2. It is recommended that the peak common mode voltage at the pins is limited during operation to avoid saturation of the amplifier. Pins LI1 and LI2 normally operate with input bias currents levels between ILbias (72uA) and ILbias+ILdiff, where ILdiff must be less than ILDmax where ILDmax=800uA. The peak common mode voltage at the LI1, LI2 pins should not exceed VLImax=2V.

With zero lamp current there is no voltage across Rs1 and consequently no difference in voltage between the two Rli resistors.

Consequently, the Rli resistors will have identical voltage drops equal to RlixILbias. When a lamp current is present, the voltage induced across Rs1 is also dropped across one of the Rli resistors such that the current through it increases (by ILdiff) while the current through the other one remains at a constant value of ILbias.The output current from the rectifier is approximately equal to the absolute value of the differential input current which

the voltage at the RIND pin is positive at the moment that T2 is switched off, the circuit is assumed to be in capacitive mode. Consequently, the frequency (or 1/FWD) will immediately jump to its maximum value.

While capacitive panic mode is detected the current charging CP is 10 times higher, rendering the CP pulses 10 times shorter for a continuous CM panic situation. If at the end of the stop timing Ivl > Ivlstop and/or capacitive mode panic is detected the circuit enters the standby state.

The voltage waveforms on upper and lower gates, half-bridge node, and at pin RIND, showing detection of both capacitive and non-capacitive modes of operation are given in fig.6.

Capacitive mode : checked at the turn-on of T1,T2.

Capacitive mode panic : checked at the turn-off of T1,T2

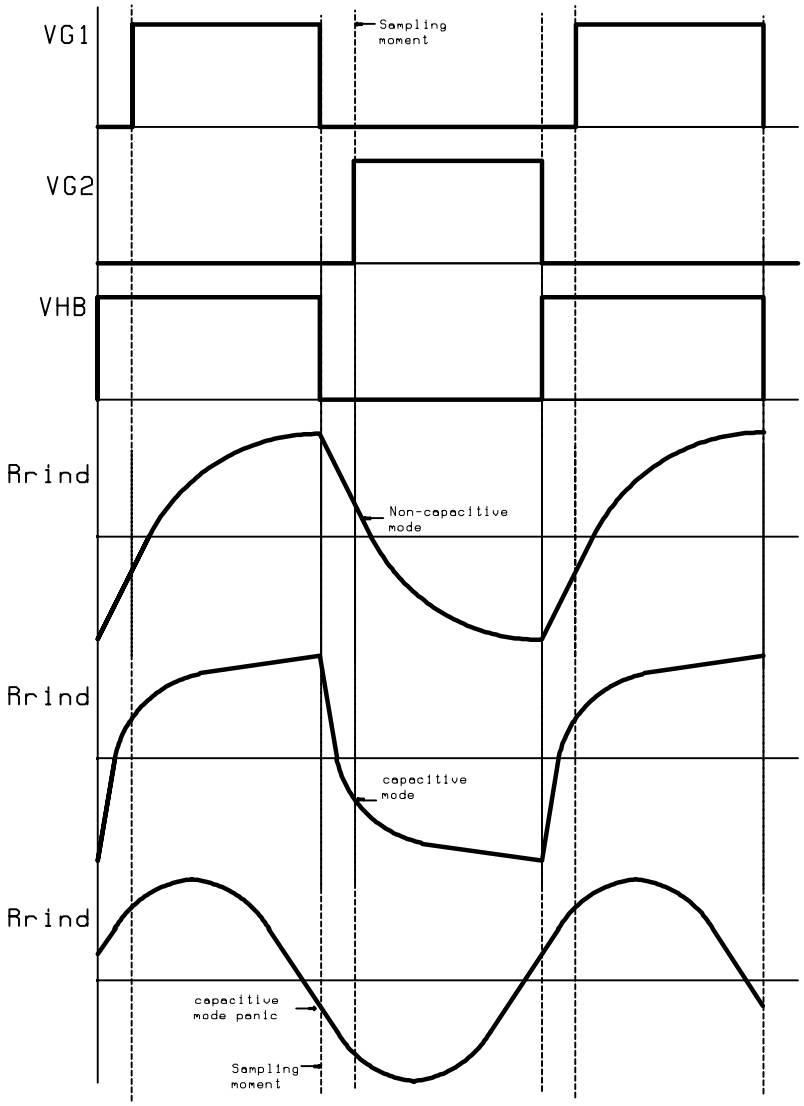

Figure 6 Capacitive and non-capacitive modes of operation

is given by: ILdiff=IlampxRsl/Rli

Several sources of error limit the minimum lamp current level that can be reliably sensed by the rectifier. These include a systematic error due to the input bias current which flows through the sense resistor Rs1, and random errors due to mismatch between the Rli resistors and bias current offset between pins LI1 and LI2. Generally, the resistor network should be designed such that the peak lamp current corresponds to the maximum allowed differential input current. This will ensure the minimum error at low current levels. Recommended values for Rli are in the range of 1kΩ and 4kΩ.

6.13 Lamp power regulation

An on-chip multiplier function is used to generate the product of lamp voltage and current during normal closed loop operation. The averaged representation of the rectified lamp voltage is fed as a current signal into pin VL where it is applied as one input to the multiplier circuit. A second input to the multiplier is obtained from the lamp current rectifier circuit. The product of the lamp voltage and lamp current is available as an output current at pin CRECT, where it is injected into the parallel network consisting of the Crect resistor and the Crect capacitor. The voltage at the CRECT pin provides a filtered representation of the average lamp power. Capacitor Crect is also used to stabilize the feedback control loop. In a typical application circuit, the 2.79 to .44V control range set by the DIM function results in a 3.0 to 0.3V variation in the CRECT voltage (for a linear resistor at CRECT), and consequently in a lamp power range of 10:1 with a minimum light level of 10%. However, this range can be extended to lower dim levels by injecting a fixed DC offset current at the CRECT pin and for applying a nonlinear impedance at CRECT. A maximum dynamic range of 100:1 for the average power level (dynamic range at CRECT remains the same) is possible with this circuit, corresponding to a minimum dim level of 1%.

6.14 Capacitive mode protection

The UBA2010 will protect the power circuit against getting too close to capacitive mode of operation. The voltage across the shunt resistor, Rind, is monitored by means of pin RIND. The state of the RIND pin is sampled at the start of conduction of either switch T1 or T2, and by checking the polarity of the signal a determination is made if the body diode is conducting. If the voltage at pin RIND is negative at the moment that T2 is switched into conduction, then the body diode in T2 has stopped conducting and the circuit is assumed to be close to or in capacitive mode. Similarly, if the voltage at pin RIND is positive at the moment that T1 is switched into conduction, the circuit is again assumed to be close to or in capacitive mode.

Consequently, if the lamp has not exceeded Vmax, the frequency (or 1/FWD) will increase at a rate of SWPup for as long as the capacitive mode is detected, and decrease at a rate of SWPdwn down to the regulated 1/FWD frequency if the capacitive mode is no longer detected. However, if the lamp voltage has exceeded Vmax, then a step increase of the frequency to its maximum value will take place.

The UBA2010 will also protect the power circuit against getting into capacitive mode. If the voltage at the RIND piin is negative at the moment that T1 is switching off, then the circuit is assumed to be in capacitive mode. Similarly, if

6.15 IC supply and regulation

All operating current for the UBA2010 is supplied via the VDD pin. During the startup phase the current is supplied by means of a resistor tied to the high voltage DC bus. When the voltage at VDD exceeds VDon, oscillation begins and a separate low voltage supply is used to provide the operating current required by the UBA2010. During normal operation, a minimum voltage of VDoff (equal to VDon-VDhys) is required at the VDD pin to ensure a minimum (static) gate to source voltage during the on-state of T1 or T2. If the circuit detects a drop in the VDD supply below VDoff, then the circuit is put into the non-oscillating state during conductance of T2. Once the VDD supply exceeds the VDon level again, the circuit starts oscillating at the minimum FWD time and begins a complete preheat and ignition cycle.

6.16 FWD time and changes in FWD time

At any point in time that the circuit is oscillating, the circuit will operate wit a FWD time between FWDmin and FWDmax. Any change in FWD time will be gradual with no stepwise changes allowed, except when capacitive mode is detected.

6.17 Stopping oscillation

Any action bringing the circuit from the oscillating state into the non-oscillating state will only be activated during the conductance of T2, ensuring a smooth transition from one state to the next by simply keeping T2 on.
The UBA2010 can enter the stop mode in the following conditions:

- VDD < VDoff exit VDD > VDon

After preheat also in the following conditions:

- At the end of stop timing..
  The stop timer is started after a detection of Ivl > Ivl,stop or capacitive mode panic
  If at the end of stop timing Ivl > Ivl,stop or capacitive mode panic is detected, the oscillation stops.

6.18 Voltage clamp of VDD pin

An internal zener clamp function is used to limit the startup voltage at pin VDD to VDclmp. The average current to be clamped into this pin has to be <3mA.

7. Pin descriptions.

7.1 DIM

This pin is used to set the lamp light level. The voltage at this pin, which is applied to a MOS-input sample and hold function, provides a reference level for the internal error amplifier used by the lamp power feedback loop. The input voltage is sampled internally at the end of the falling slope of the VCO waveform (switch T2 is conducting), when the voltage on the CF pin is between VCFsh and VCFsl.
The usable voltage control range for this pin is internally fixed between 2.79V and 0.44. Outside these levels the DIM control voltage (which is internally limited) has the same effect as the maximum or minimum values. ..

7.2 VL

The VL pin during the preheat time is pulled to VDD. This voltage can be used as a logic signal by the external power circuit to indicate the preheat state of the circuit. After preheat, VL is a low impedance current sensing input which serves the dual purpose of detecting an overvoltage condition during ignition, removal, or failure of the lamp, and sensing the lamp voltage for power regulation during the normal running phase. It forms the input to three current comparators and the multiplier function. VL is sampled by the comparators at the turn-off edge of T2. As soon as the input currents exceeds a current level of IVLstop (110uA for the design value of Rref), the stop timer is activated. If at the end of the Tstop period the IVLstop is exceeded, the circuit is switched into the standby state, with T1 off and T2 on. The circuit remains in the standby state when the VL input current drops below IVLstop, until the complete circuit is powered down below VDoff and back up to above VDon. If the input current exceeds a level of IVLmax (corresponding to Vmax), then the lamp voltage is dynamically regulated about the Vmax level by alternately sweeping the frequency up at the SWPup rate and down at the SWPdwn rate. If the current at VL is below the IVL stop at the end of Tstop, then the lamp is considered to be in a normal running state. The stop function remains active continuously following ignition. Only during the first time the stop timing circuit is activated, the multiplier feeds no current into the CRECT pin as long as the VL current exceeds IVLstop. If the current at the VL pin exceeds a level of IVLpanic (IVLpanic=1.2 x IVLmax) then the frequency is swept up to its maximum value at a step change.
After ignition the VL pin forms a current input to one side of the multiplier function. The current into VL should be a well filtered DC signal with a maximum value (corresponding to the maximum lamp voltage in the dimming state) of less than IVLstop. If the current into VL exceeds a level of IVLclamp then the input current at the multiplier is clamped to IVLclamp.

7.3 CRECT

The CRECT pin sources a current that represents the lamp power into an external capacitor and resistor network, Crect and Rrect. The capacitor is used for filtering of the high frequency ripple in the representation of the lamp power, derived from the product of the lamp current and the lamp voltage at the multiplier circuit. It also stabilizes the lamp control feedback loop. The resistor is used to set the gain of the multiplier circuit.
The first time the current into VL exceeds IVLstop after the occurance of a preheat condition the current source output at the CRECT pin is turned off, while the current into the VL pin exceeds IVLstop.

7.4 LI1, LI2

Pins LI1 and LI2 form the inputs to a bipolar differential current amplifier. The differential input current at the pins LI1 and LI2 is converted into a fully rectified output current which is fed to one input of the multiplier function. The magnitude of the output current is approximately equal to the absolute value of the differential input current. Pins LI1 and LI2 act as current sources such that at any time one of the inputs will be supplying a minimum current equal to ILbias and the other pin will be supplying a current equal to ILbias+ILdiff. The input pins must be connected through matched resistors, Rli, to the terminals of the voltage source which represents the lamp current. The external resistor network tied to pins LI1 and LI2 should be designed such that the rectifier normally operates with a peak differential input current near the maximum allowed level, IDLmax, but does not exceed it. This will minimize errors at low current levels and avoid amplifier saturation at high current levels. Recommended values for Rli are in the range between 1kΩ and 4kΩ. The value of ILDmax is 800uA.
The voltage at the VLI1, VLI2 pins should not exceeds the value of VLImax=2V and may not be below -0.3V.
The differential voltage between pins LI1 and LI2 is forced to be zero by the rectifier circuit, while the common mode voltage, Vli, can range between a minimum value equal to RlixILbias and a maximum value equal to Vlimax. For voltages greater than Vlimax the differential input current range is reduced due to saturation of the amplifier.

7.5 RREF

An external resistor Rref is connected to the RREF pin. This resistor converts the reference voltage at the RREF pin into a reference current. The reference voltage at this point is Vref. A value of Rref of 30kΩ will be referred to as the design value of Rref. in this text The nominal value of Rref will always be between 20kΩ and 40kΩ.

7.6 CF

An external capacitor is connected to the CF pin. The CF capacitor is precharged to Vreg during the start-up state (VDD,VDON). VCF will only reach the level of Vreg if the VDD exceeds 9Volt.

7.7 CP

An external capacitor Cp is connected to pin Cp, which serves two purposes. First, it is used to set the preheat timing. At the end of preheat the voltage at Cp is set to zero.
Second, the Cp pin is used to set the stop timing duration when the open circuit lamp voltage exceeds the Vstop level during the ignition phase. The stop timing duration is equal to 8/16 of the preheat time. This function only becomes active at the instant the ignition sweeps starts, however it remains active continuously after that. While capacitive mode panic is detected, the CP pulses become ten times shorter.

7.8 RIND

Pin RIND is a voltage input, used to monitor the current through the Rs1 and Rs2 resistor, Three comparators are provided at this pin to serve three functions. One of the comparators has a negative trip level of Vpre which is used to regulate the preheat current (through Rs1) during the preheat state. The other two comparators, which detects a zero crossing at RIND, are used for FWD control of the oscillator. Two comparators are used i.s.o. one in order to create a window around zero. In this way, a signal that actually is zero can properly be detected.
The zero crossing signal is also used for capacitive mode protection.

7.9 G1, G2

These pins are connected to the gates of T1 and T2 respectively. The output pin can absorb a limited value of Miller-current during high-side switching (depending of the application).

7.10 VDD

The supply current for the UBA2010 is supplied via this pin. Its provides a zener function, with a peak transient current capability to limit the voltage during standby to VDclmp. During any of the non-oscillating states, the average current requirement is less than IDstart. During oscillation the average current requirement, including the floating-well section and level-shifter, is <IDavg (without the gate drive) at large Tfwd.
The average current may increase proportional with the frequency. An under-voltage lockout function prevents

oscillation until the voltage at VDD exceeds VDon, and stops oscillation if the supply drops below VDoff.

7.11 FVDD

Supply voltage pin for the high-side logic and driver. An external bootstrap capacitor is connected between pins FVDD and S1 to serve as the floating voltage source for the high-side circuits. The minimum size of the capacitor is determined by the acceptable voltage ripple on the FVDD pin for a given external power switch. For an output charge of 20nC, a minimum capacitor value of 42nF is recommended to ensure that the gate voltage remains above 8V under worst case conditions. An on-chip high voltage bootstrap diode function is connected between pins VDD and FVDD, and serves to charge the bootstrap capacitor both during the startup phase and during each period that T2 is in the conducting state when oscillating.

7.12 S1

Floating source (ground) pin for the high-side logic and driver.

8. Ratings

(Absolute maximum ratings according to IEC 134)

Parameter	Conditions	Symbol	Min.	Max.	Unit
Low voltage supply		VDD		15	V
Low voltage supply clamp current		IDD		3	mA
DIM input voltage	at Idimmax	VDIM	0	4	V
DIM input current		IDIM	-100	100	uA
Common voltage at LI1, LI2		VLIcom	0	+5	V
Differential voltage at LI1, LI2		VLIdif	0	+2	V
VL input current		IVL	0	+1	mA
RIND input voltage		VRIND	-5	+5	V
Floating supply voltage	operating	FVDD		510	V
Floating supply voltage	during 5min	FVDD		550	V
Floating supply voltage	during 0.5sec.	FVDD		630	V
Slew rate on pin S1,FS w.r.t. GND	(repetitive)	SR		4	V/ns
Virtual junction temperature		Tvj		105	.°C
Ambient temperature range	Storage	Tamb	-55		.°C
	Operating	Tamb	-25	95	.°C

9. Thermal data

(according to IEC 747-1)

Parameter	Conditions	Symbol		Unit
SO16 encapsulation				
Thermal resistance to amb.	from junction to ambient	Rth vj-amb	100	K/W
Therm. res. to pr. circuit board	from junction to pcb	Rth vj-pcb	50	K/W
16p DIP encapsulation				
Thermal resistance to amb.	from junction to ambient	Rth vj-amb	60	K/W
Therm. res. to pr. circuit board	from junction to pcb	Rth vj-pcb	30	K/W

10. Characteristics

No	Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
	HIGH VOLTAGE FUNCTION						
1.0	Leakage current high side pins	FVDD,G1,S1 = 630V	Ileakage			30	uA
	(at T_{amb} = 25°C , FVDD = 13V and VDD = 13V, Rref=30kΩ unless otherwise specified) see fig. 9						
	START-UP STATE						
2.0	Supply voltage clamp	IDD=3mA	VDclmp	15	15.6	17	V
2.1	Supply for defined driver output	**note 1**	VDlow			6	V
2.2	Supply turn-on voltage		VDon	10.9	11.6	12.3	V
2.3	Low-supply lockout voltage		VDoff	9.1	9.7	10.3	V
2.4	Low-supply lockout hysteresis		VDhys	1.7	1.9	2.1	V
2.5	Startup current	VDD=10.5V	IDstart	230	310	450	uA
2.6	Standby current	VDD=10.5V	IDstart	255	345	475	uA
2.7	Operating supply current	without gate drive **note 2**	IDavg		3.4	5.5	mA
	REFERENCE SECTION						
3.0	Internal voltage reference	VDD=10.5V	Vreg	4.65	4.9	5.15	V
3.1	Voltage at RREF pin	Rref=30kΩ	Vrf	2.20	2.35	2.50	V
3.2	Load resistor		Rref	20	30	40	kΩ
	OSCILLATOR SECTION						
4.0a	Non-overlap time	T1off ->T2on	Tnonovlp	1.35	1.8	2.25	uS
4.0b	Non-overlap time	T2off ->T1on	Tnonovlp	1.25	1.70	2.15	uS
4.1	Rate of decrease in Icf per cycle		SWPup	45	75	95	nA/cy
4.2	Rate of increase in Icf per cycle		SWPdwn	55	110	165	nA/cy
4.3	High VCO threshold		VCFh	3.65	3.92	4.05	V
4.4	Low VCO threshold		VCFl	.95	.98	1.05	V
4.5a	Start VCO charge current	at the first cycles	ICFstc	120	130	140	uA
4.5b	Start VCO discharge current	at the first cycles	ICFstd	120	130	140	uA
4.6	Max VCO current	during active control	ICFmax	155	195	215	uA
4.7a	Min VCO charge current	during active control	ICFminc	28	31	34	uA
4.7b	Min VCO discharge current	during active control	ICFmind	28	31	34	uA
4.8a	Zero crossing offset	after G2 is off	VOFzc	10	25	40	mV
4.8b	Zero crossing offset	after G1 is off	VOFzc	-40	-25	-10	mV

No	Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
	PREHEAT AND STOP TIMING SECTION						
5.0	Preheat threshold voltage		Vpre	-.42	-.4	-.38	V
5.1	CP high threshold		VCPh	3.6	4	4.3	V
5.2	CP low threshold		VCPl	0.6	0.75	0.9	V
5.3	CP charging current	VCP=2.5V	ICPh	5.8	6.5	7.2	uA
5.4	CP charging current	at cap mode VCP=2.5V	ICPh	65	72	79	uA
5.5	CP discharge current	VCP=2.5V	ICPl	1	1.5	2	mA
5.6	Preheat time	CP=150nF	Tpre		1.2		sec
5.7	Stop delay time	CP=150nF	Tstop		0.6		sec
	STOP SECTION						
6.0	Clamp level **note 3**		IVLclamp	64	72	80	uA
6.1	Stop threshold level **note 3**		IVLstop	79	86	93	uA
6.2	Max level		IVLmax	160	175	190	uA
6.3	Ratio panic level/max.level		panic/max	1.1	1.2	1.3	
6.4	Impedance at VLin	normal operating	ZVL	2.5	3.7	4.2	kΩ
	DRIVER SECTION						
7.0	G1 source current	V(G1-S1)=5V	IG1so	40			mA
7.1	G1 sink current	V(G-S1)=5V	IG1si	100			mA
7.2	G2 source current	VG2=5V	IG2so	40			mA
7.3	G2 sink current	VG2=5V	IG2si	100			mA
7.4	G1 on voltage **note 4**	IG1so=1mA	VGS1h	10.8			V
7.5	G1 off voltage	IG1si=1mA	VGS1l			.5	V
7.6	G2 on voltage **note 4**	IG2so=1mA	VGS2h	12.5			V
7.7	G2 off voltage	IG2si=1mA	VGS2l			.5	V
7.8	Bootstrap diode fwd drop	G2 high after switching, I=6mA	VDboot			2	V
7.9	Bootstrap diode fwd drop	at VDD=9V, IFVVD=1mA	VDboot			2	V
7.A	Lockout voltage		FVDD	2.0		6.0	V
	DIMMING CONTROL SECTION						
8.0	CRECT voltage at max VDIM	VCF=1.4V,VDIM=4V Icf = 40uA	Vcrecth	2.75	2.90	3.05	V
8.1	CRECT voltage at min VDIM	VCF=1.4V,VDIM=0V Icf = 100uA	Vcrectl	0.25	0.29	0.33	V
8.2	CRECT output current at typ. 100% dimming **note 5**	V1=0V, V2=1.5V IVL=30u,Vcrect=3	Icrecth	255	280	305	uA

No	Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
8.3	CRECT output current at typ. 10% dimming **note 5**	VLI1=0V, VLI2=75mV IVL=60u,Vcrect=0.3	Icrectl	23	26	29	uA
8.4	CRECT output offset current	**note 6** IVL=50uA	Icrectoff	-3	0	3	uA
8.5	LI1 bias current	VLl=0, VL2=0, IVL=0u	IL1bias	76	80	84	uA
8.6	LI2 bias current	Vl=0, V2=0, IVL=0u	IL2bias	76	80	84	uA
8.7	Max VCF for sampling VDIM	G2=high	VCFsh	1.3	1.77	1.9	V
8.8	Min DIM voltage clamp	IDIM=-100uA	VDIMcl	-.2	0.0	.2	V
8.9	Max DIM voltage clamp	IDIM=+100uA	VDIMc	4.15	4.5	4.7	V
8.A	Transconductance error amplifier	VDIM=2V,Icf=100uA IVL=75, 175uA	TRerr	1.2	1.5	1.8	mA/V
8.B	Transconductance error amplifier	VDIM=2 V, Icf=40uA IVL=75, 175uA	TRerr	0.8	1.2	1.6	mA/V

11. Notes

1)The dV/dT of the Vdd should be **>** 0.2V/msec

2) Also without load at the VL pin and at the LI pins.

3) The clamp , stop, max levels are coupled to each other (IVLclamp = 0.85xIVLstop, IVLstop = 0.5 IVLmax)

4) These parameters are valid up to Tj=150^{O}C and at a maximum charge consumption of 1nC/V.
Below a frequency of 100kHz, the gate voltage is >8V.
Above a frequency of 100kHz, the gate voltage is >7V. Both values

5) ILIdif is (|V1| - |V2|) / 3.95kΩ

6) Icrectoff is defined as the difference between the Icrect at VLI2=+75mV and VLI2=-75mVK at VLI1=0V.

12. Design equations

1) Preheat current level : Ipre = Vpre/Rind

2) Preheat time : $T_{pre} = 1.2\ (s) \times \frac{R_{ref}}{30k\Omega} \times \frac{C_p(nF)}{150nF}$ seconds

If CM panic $T_{pre} = 0.115\ (s) \times \frac{R_{ref}}{30k\Omega} \times \frac{C_p(nF)}{150nF}$ seconds

3) Regulated lamp power : $P_{lamp(avg)} = \frac{R_{li}}{K_1 R_S} \times \frac{30k\Omega}{R_{ref}} \times I_{mul} \times \left(\frac{V_{crect}}{R_{rect}} - I_{offset}\right)$ (with a linear Rrect)

where K_1 = ratio of lamp voltage to DC current in the VL pin

Ioffset = externally defined current fed into Rrect

$I_{mul} = 1/K_2$ (see 4) at 100% dimming Imul = 40.6uA, at 10% Imul = 43.7uA.

Vcrect = 9/8 (Vdim-1.62) + 1.62

4) Current out of CRECT : $I_{crect} = K_2 \times IVL \times ILI_{diff} \times \frac{R_{ref}}{30k\Omega}$

with $K_2 = 24.64 \times 10^3$ at 100% dimlevel

with $K_2 = 22.88 \times 10^3$ at 10% dimlevel

5) FWD times : $FWD_{max} = 9.5\ (us) \times \frac{R_{ref}}{30k\Omega} \times \frac{C_f}{100pF}$

6) $T_{non\text{-}overlap} = 1.75\ (us) \times \frac{R_{ref}}{30k\Omega}$

7) Definition of Sweep Rates : $SW_{up} = \frac{d(1/FWD)}{dt} \times \frac{FWD}{f} \times 100$ (%/cycle)

13. Quality specification

Quality according to SNW/FQ-611 part E

14. Flow diagram

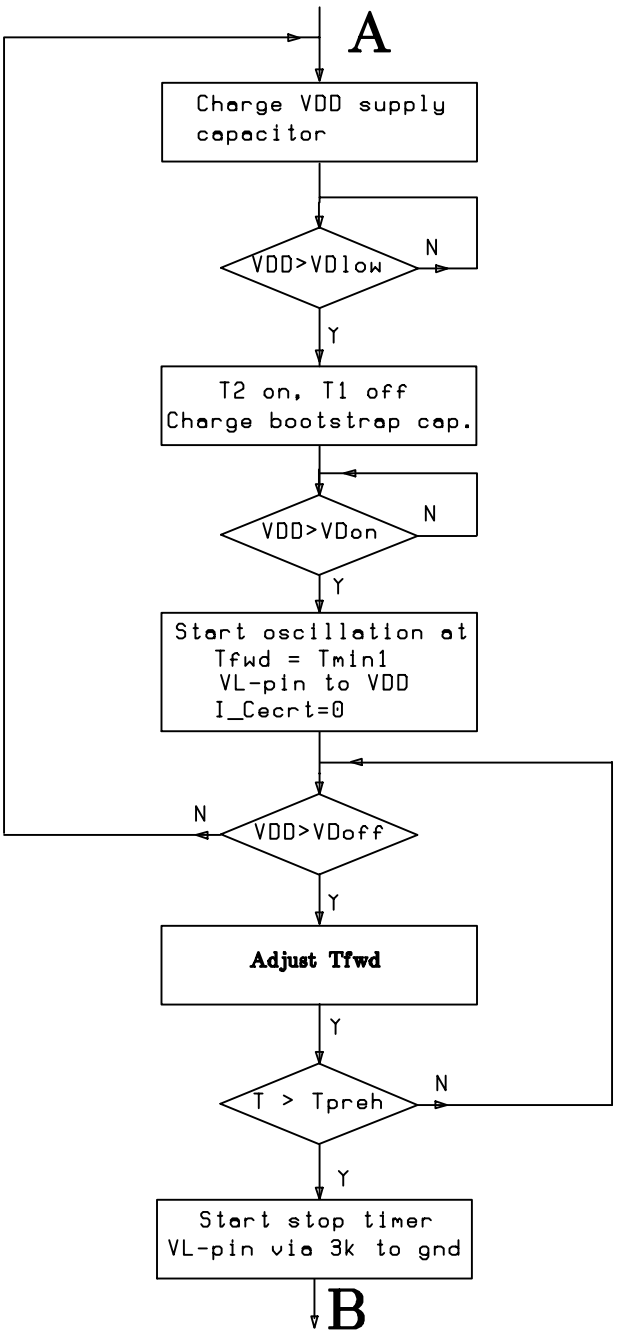

Figure 7 Start-up and Preheat

Not included: Increase in preheat- and stop-timing current by factor 10 during the time that a cap. mode condition exists

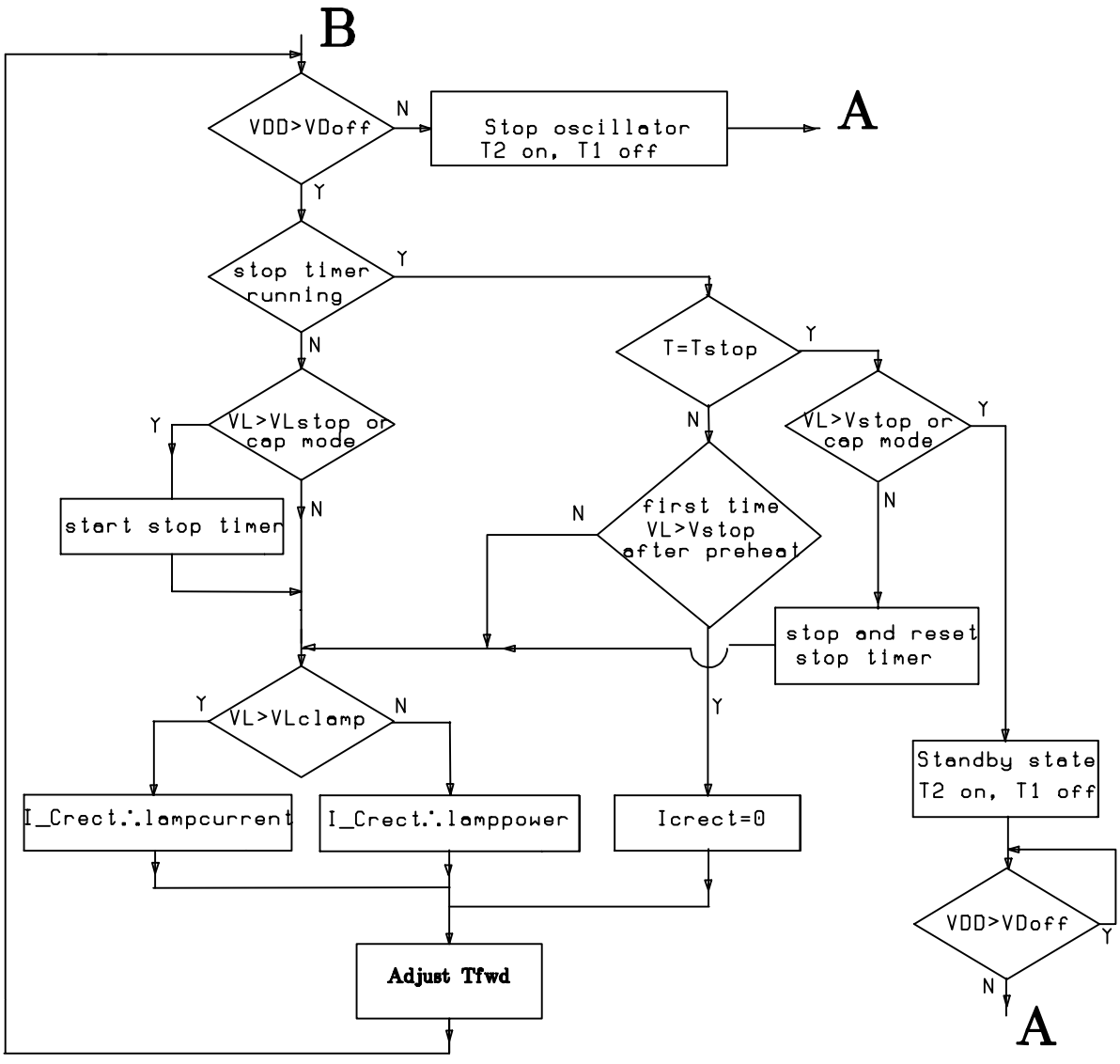

Figure 8 Ignition and normal operation

Not included: Increase in preheat- and stop-timing current by factor 10 during the time that a cap. mode condition exists

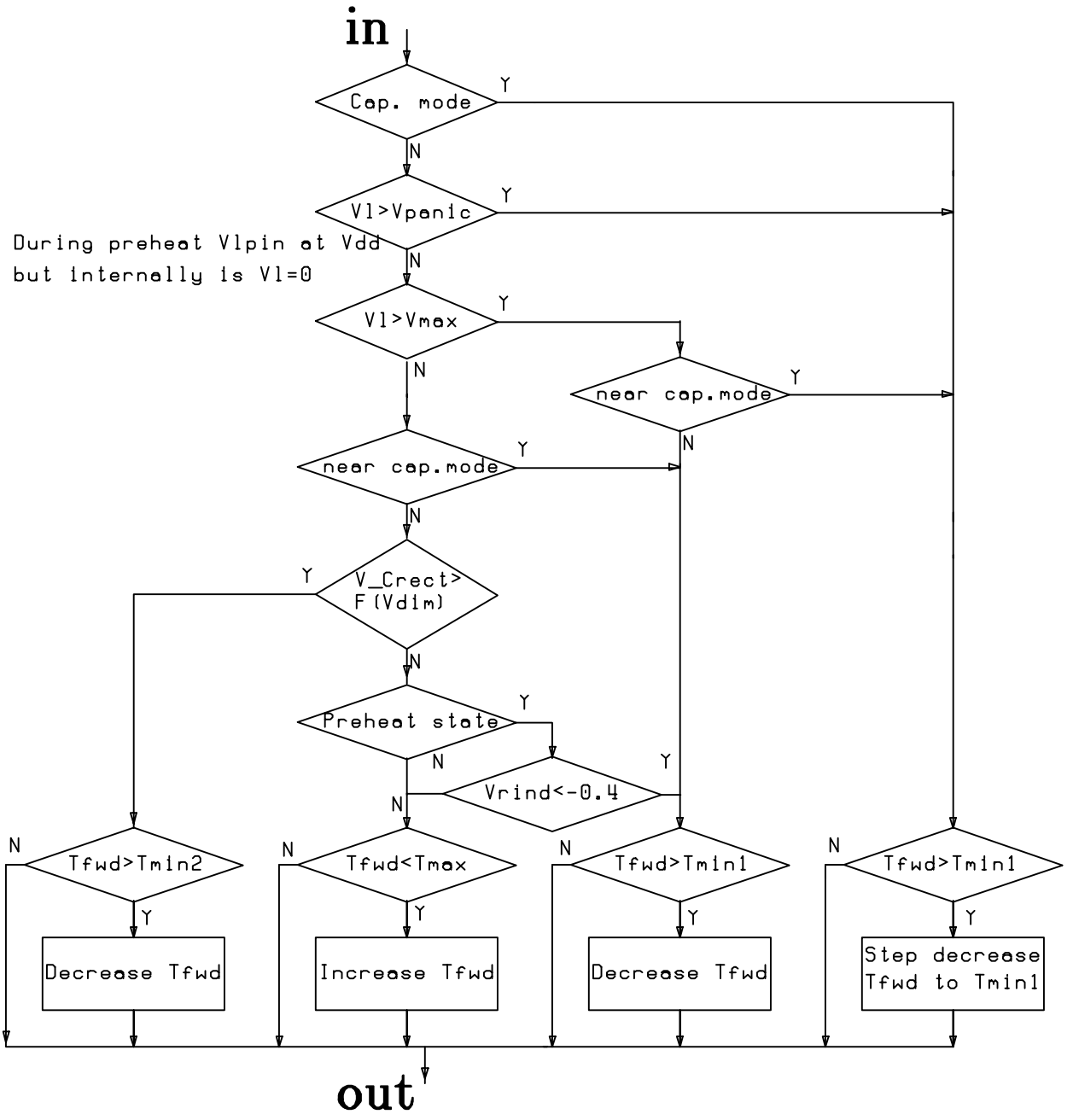

Figure 9 Adjust Tfwd

F(Vdim)=	0.3	for	Vdim $\leq$ 0.45	notes: Tmin1 acc. to10.4.5
F(Vdim)=	(9xVdim-1.62)/8	for	0.45<Vdim<2.85	Tmin2 acc. to10.4.6
F(Vdim)=	3.0	for	Vdi m $\geq$ 2.85	Tmax acc. to10.4.7

15. Application information

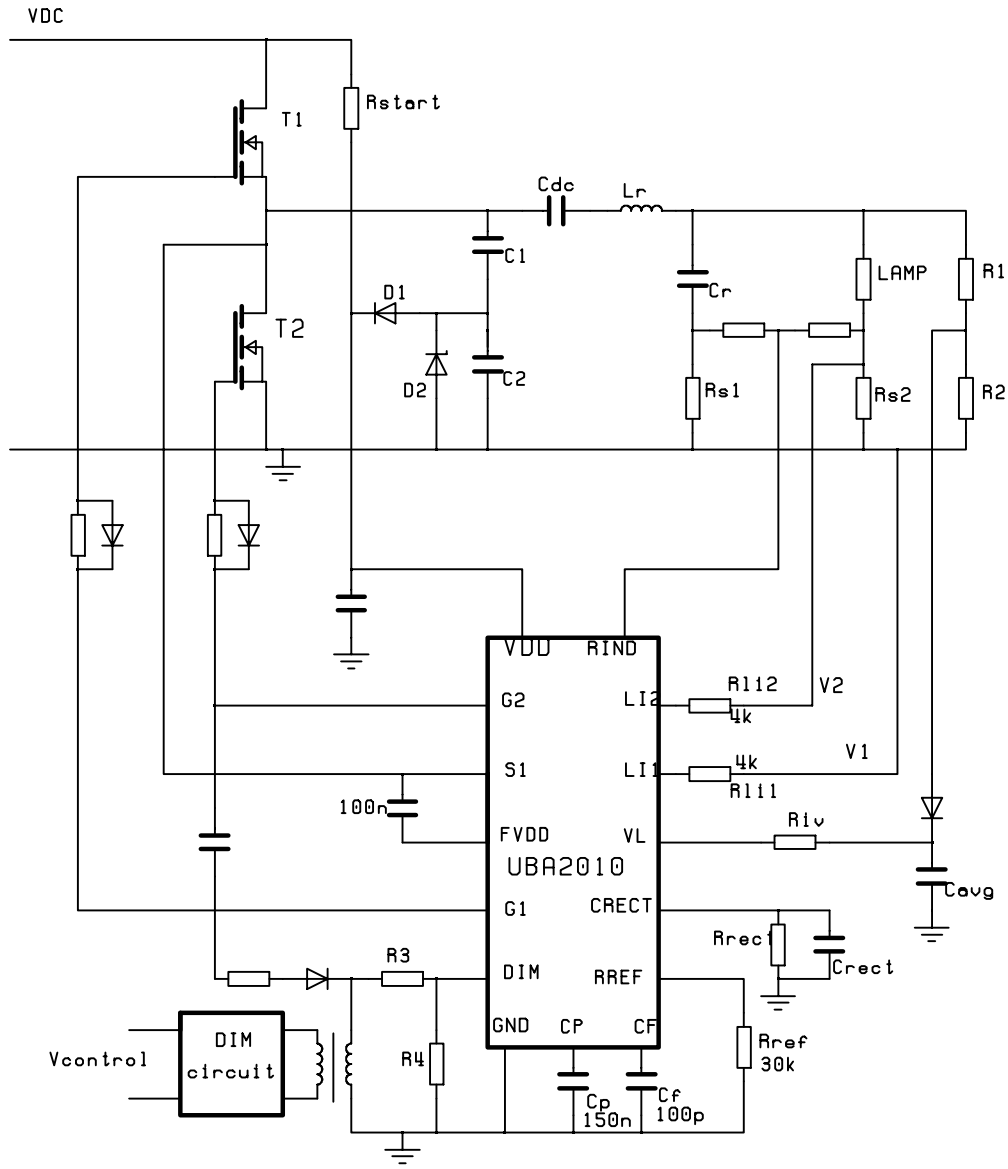

Figure 10

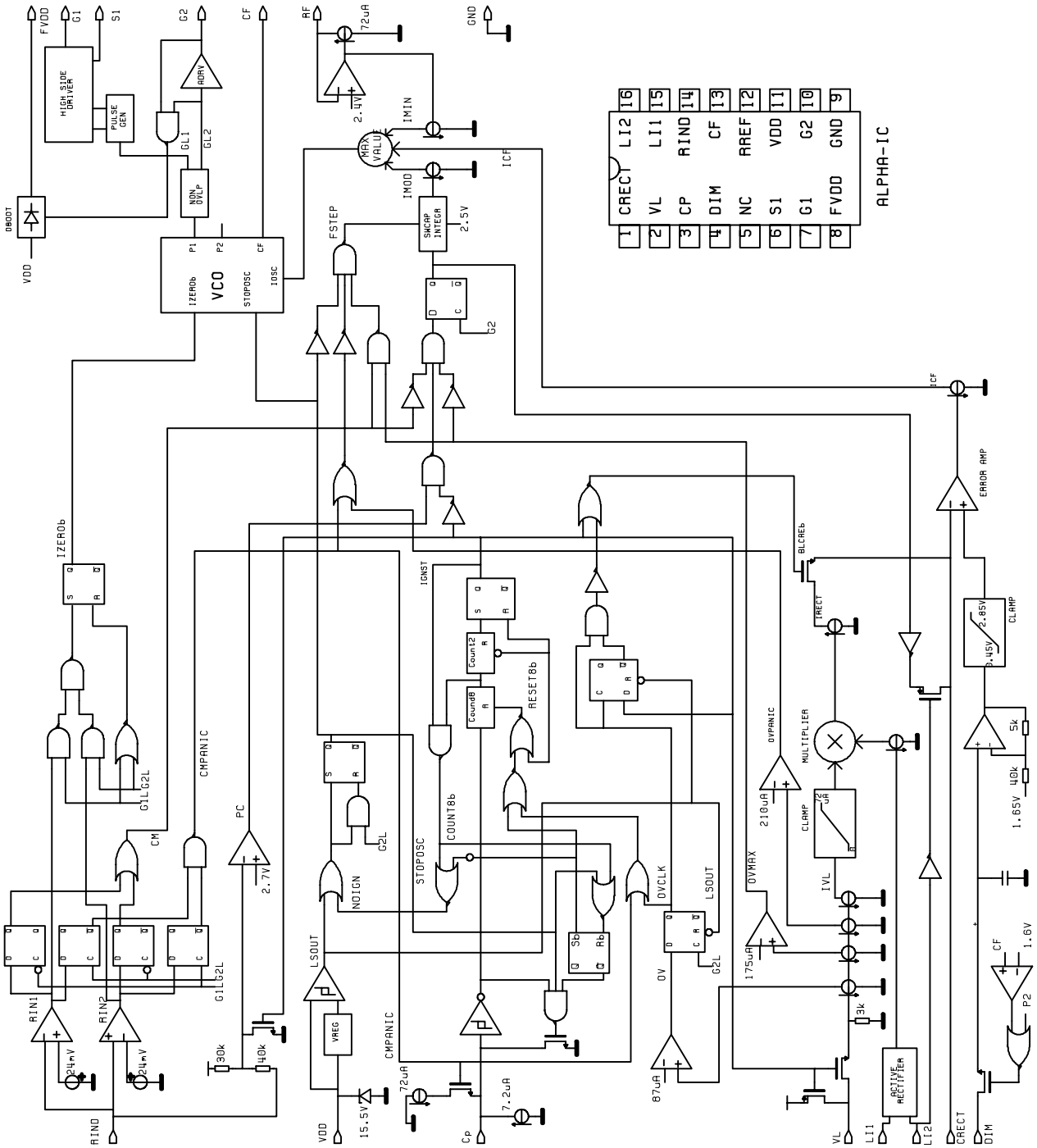

Figure 11 Logic Diagram

		UBA2010 N4 (T)			
NAME Emmerik/Verhoeven	**SUPERS**	**28**	**191 -**	- 28	010	A4
CHECK	DATE 03-june 97	(c) Nederlandse Philips bedrijven B.V.			

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1	2	3	4	5	6	7	8
SUPERSEDES:		Incoming Inspection					98-04-21
NAME G. Emmen			**UNIT** MM	PROJ. EUROP	01 **SH**	**SH** IQC-01	**A4**

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