

1.0 Features

- Primary-side feedback eliminates opto-isolators and simplifies design
- Multi-mode operation for highest overall efficiency
- $\pm 4\%$ output voltage regulation
- No external compensation components required
- Complies with CEC/EPA/IEC no load power consumption and average efficiency regulations
- Built-in secondary constant-current control with primary-side feedback
- Low start-up current (8 μA typical)
- Built-in soft start
- Built-in short circuit protection
- AC line under/overvoltage and output overvoltage protection
- Fixed 40 kHz switching frequency
- Available in a space-saving SOT-23 package

2.0 Description

The iW1689 is a high performance AC/DC power supply controller which uses digital control technology to build sensorless peak current mode PWM flyback power supplies. The device provides high efficiency along with a number of key built-in protection features while minimizing the external component count and bill of material cost. The iW1689 removes the need for secondary feedback circuitry while achieving excellent line and load regulation. It also eliminates the need for loop compensation components while maintaining stability over all operating conditions. Pulse-by-pulse waveform analysis allows for a loop response that is much faster than traditional solutions, resulting in improved dynamic load response. The built-in power limit function enables optimized transformer design in universal off-line applications and allows for a wide input voltage range.

The ultra-low start-up power and operating current at light load ensure that the iW1689 is ideal for applications targeting the newest regulatory standards for average efficiency and standby power.

3.0 Applications

- Low power AC/DC adapter/chargers for cell phones, PDAs, digital still cameras
- Standby supplies for televisions, DVDs, set-top boxes and other consumer electronics

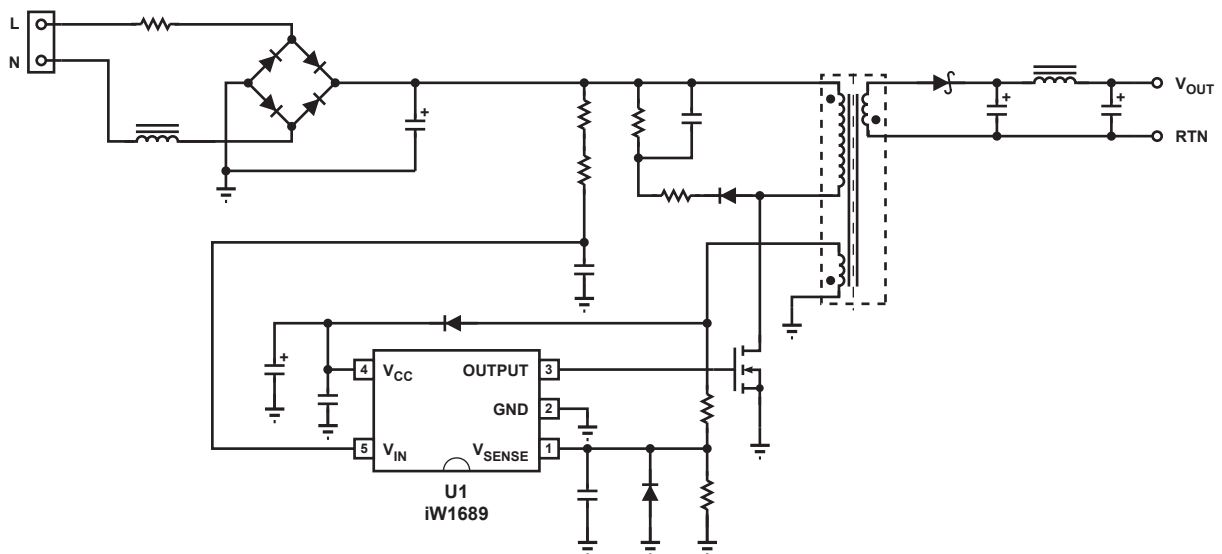
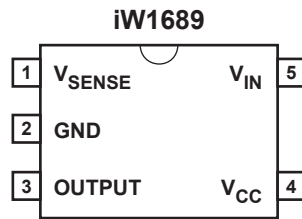


Figure 2.0.1 iW1689 Typical Application Circuit

4.0 Pinout Description



Pin #	Name	Type	Pin Description
1	V_{SENSE}	Input	Voltage sense input from the auxiliary winding.
2	GND	Ground	Ground connection.
3	OUTPUT	Output	Gate drive output for the external power MOSFET switch.
4	V_{CC}	Input	Supply voltage.
5	V_{IN}	Input	Average AC line voltage sense, rectified and attenuated. This pin also serves as the supply for the IC during start-up.

5.0 Absolute Maximum Ratings

Absolute maximum ratings are the parameteic values or ranges which can cause permanent damage if exceeded. For maximum safe operating conditions, refer to Electrical Characteristics in Section 6.0.

Parameter	Symbol	Value	Units
DC supply voltage range (pin 4, $I_{CC} = 20\text{mA max}$)	V_{CC}	-0.3 to 18	V
DC supply current at V_{CC} pin	I_{CC}	20	mA
Low voltage output (pin 3)		-0.3 to 18	V
V_{SENSE} input (pin 1)		-0.3 to 4.0	V
V_{IN} input (pin 5)		-0.3 to 18	V
Power dissipation at $T_A \leq 25^\circ\text{C}$	P_D	526	mW
Maximum junction temperature	$T_{J\text{MAX}}$	125	$^\circ\text{C}$
Storage temperature	T_{STG}	-65 to 150	$^\circ\text{C}$
Lead temperature during IR reflow for ≤ 15 seconds	T_{LEAD}	260	$^\circ\text{C}$
Thermal Resistance Junction-to-Ambient	θ_{JA}	190	$^\circ\text{C/W}$
ESD rating per JEDEC JESD22-A114 (HBM)		2,000	V
Latch-Up test per JEDEC 78		± 100	mA

6.0 Electrical Characteristics

$V_{CC} = 12\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, unless otherwise specified (Note 1)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{IN} SECTION (Pin 5)						
Start-up voltage threshold	V_{INST}	$T_A = 25^\circ\text{C}$, positive edge	366	407	448	mV
Start-up current	$I_{IN(ST)}$	$V_{CC} = 10\text{ V}$		8	12	μA
Shutdown low voltage threshold	V_{UVDC}	$T_A = 25^\circ\text{C}$, negative edge	216	240	264	mV
Shutdown high voltage threshold	V_{OVDC}	$T_A = 25^\circ\text{C}$, positive edge	1.737	1.930	2.123	V
Input impedance	Z_{IN}	After start-up		20		$\text{k}\Omega$
V_{SENSE} SECTION (Pin 1)						
Input leakage current	I_{BVS}	$V_{SENSE} = 2\text{ V}$			1	μA
Nominal voltage threshold	$V_{SENSE(NOM)}$	$T_A = 25^\circ\text{C}$, negative edge	1.507	1.538	1.569	V
Output OVP threshold	$V_{SENSE(MAX)}$	$T_A = 25^\circ\text{C}$, negative edge	1.667	1.700	1.734	V
OUTPUT SECTION (Pin 3)						
Output low level ON-resistance	$R_{DS(ON)LO}$	$I_{SINK} = 5\text{ mA}$		65	100	Ω
Output high level ON-resistance	$R_{DS(ON)HI}$	$I_{SOURCE} = 5\text{ mA}$		65	100	Ω
Rise time (Note 2)	t_R	$T_A = 25^\circ\text{C}$, $C_L = 330\text{ pF}$ 10% to 90%		40	75	ns
Fall time (Note 2)	t_F	$T_A = 25^\circ\text{C}$, $C_L = 330\text{ pF}$ 90% to 10%		40	75	ns
Output switching frequency (Note 3)	f_S	$I_{LOAD} > 15\%$ of maximum	36	40	44	kHz
V_{CC} SECTION (Pin 4)						
Maximum operating voltage	$V_{CC(MAX)}$				16	V
Start-up threshold	$V_{CC(ST)}$	V_{CC} rising	11.0	12.3	13.6	V
Undervoltage lockout threshold	$V_{CC(UVL)}$	V_{CC} falling	5.50	6.15	6.80	V
Operating current	I_{CCQ}	$C_L = 330\text{ pF}$, $V_{SENSE} = 1.5\text{ V}$		2.5	3.5	mA

Notes:

Note 1. Adjust V_{CC} above the start-up threshold before setting at 12 V.

Note 2. These parameters are not 100% tested, guaranteed by design and characterization.

Note 3. Frequency variation includes $\pm 1.2\%$ dithering for EMI suppression.

7.0 Typical Performance Characteristics

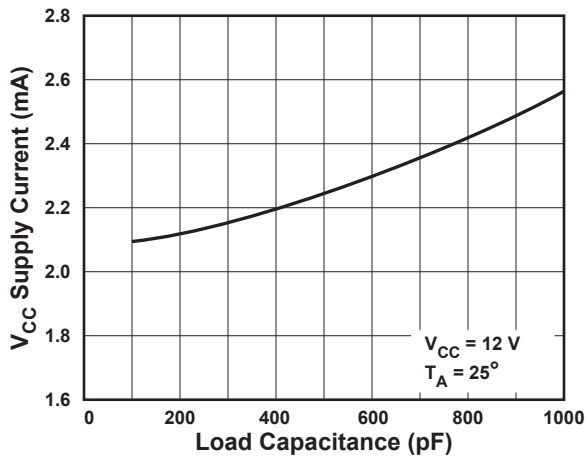


Figure 7.0.1 Supply Current vs. Load Capacitance

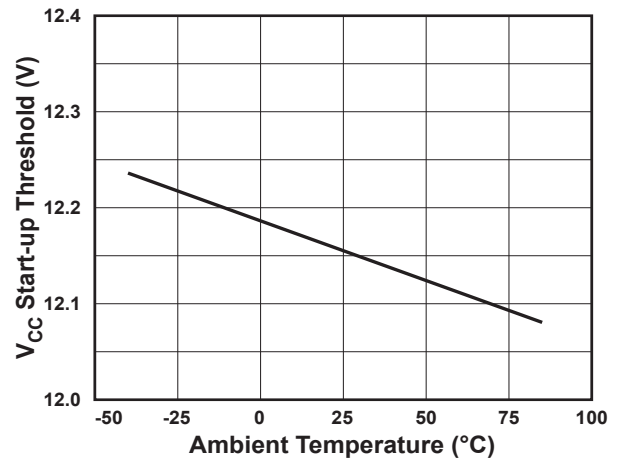


Figure 7.0.3 Start-Up Threshold vs. Temperature

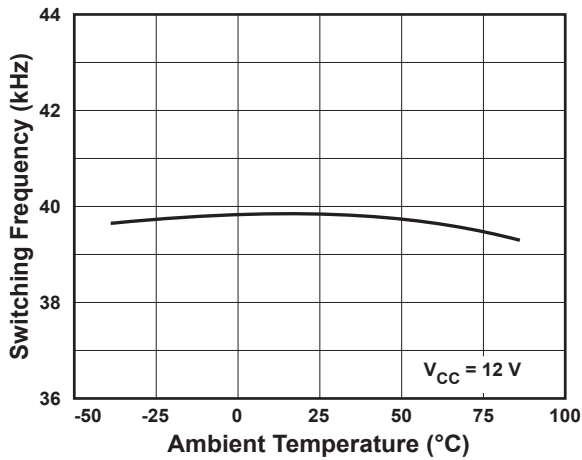


Figure 7.0.2 Switching Frequency vs. Temperature

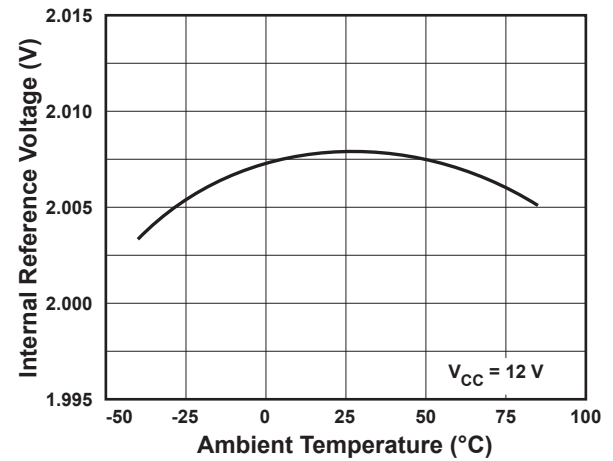


Figure 7.0.4 Internal Reference vs. Temperature

8.0 Functional Block Diagram

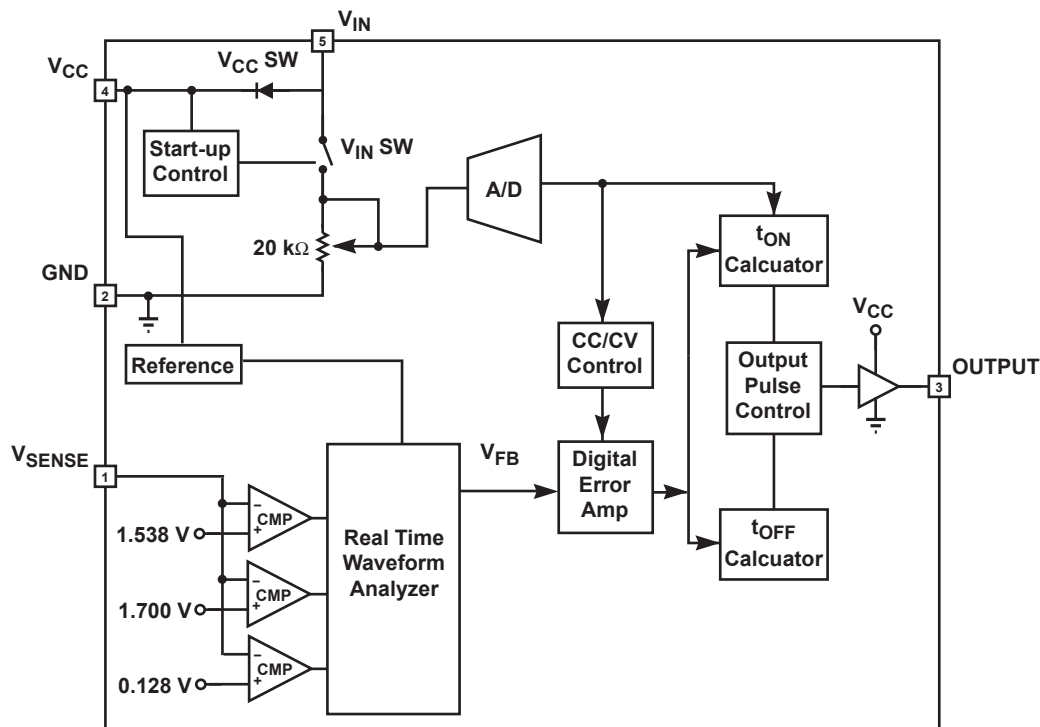


Figure 8.0.1 iW1689 Functional Block Diagram

9.0 Theory of Operation

The iW1689 is a digital controller which uses a new, proprietary primary-side control technology to eliminate the opto-isolated feedback and secondary regulation circuits required in traditional designs. This results in a low-cost solution for low power AC/DC adapters. The core PWM processor uses fixed-frequency Discontinuous Conduction Mode (DCM) operation at higher power levels and switches to variable frequency operation at light loads to maximize efficiency. Furthermore, iWatt's digital control technology enables fast dynamic response, tight output regulation, and full featured circuit protection with primary-side control.

Referring to the block diagram in Figure 8.0.1, the digital error amplifier and t_{ON}/t_{OFF} calculator blocks generate the switching on-time and off-time information based on the line voltage and the output voltage feedback signal. The system loop is automatically compensated internally by the digital error amplifier. Adequate system phase margin and gain margin are guaranteed by design and no external analog components are required for loop compensation. The iW1689 uses an advanced digital control algorithm to reduce system design time and improve reliability.

Furthermore, accurate secondary constant-current operation is achieved without the need for any secondary-side sense and control circuits.

The iW1689 uses PWM mode control at higher output power levels and switches to PFM mode at light load to minimize power dissipation to meet the Blue Angel specification. Additional built-in protection features include overvoltage protection (OVP), output short circuit protection (SCP) and soft-start.

iWatt's digital control scheme is specifically designed to address the challenges and trade-offs of power conversion design. This innovative technology is ideal for balancing new regulatory requirements for green mode operation with more practical design considerations such as lowest possible cost, smallest size and high performance output control.

9.1 Pin Detail

Pin 1 – V_{SENSE}

Sense signal input from auxiliary winding. This provides the secondary voltage feedback used for output regulation.

Pin 2 – GND

Analog signal and power ground.

Pin 3 – OUTPUT

Gate drive signal for the external power MOSFET switch.

Pin 4 – V_{CC}

Power supply for the controller during normal operation. The controller will start up when V_{CC} reaches 12 V (typical) and will shut-down when the V_{CC} voltage is 6 V (typical). A 100 nF decoupling capacitor should be connected between the V_{CC} pin and GND.

Pin 5 – V_{IN}

Sense signal input representing the instantaneous rectified line voltage at the top of the transformer primary. V_{IN} is used for line regulation. The input line voltage is scaled using a resistor network. The internal impedance is 20 k Ω and the scale factor is 0.0043. It also provides input undervoltage and overvoltage protection. This pin also provides the supply current to the IC during start-up.

9.2 Start-up

The iW1689 incorporates an internal soft-start function. The soft-start time is set at 3.5 ms. Once the V_{IN} pin voltage has reached its turn-on threshold, the iW1689 starts switching, but limits the on-time to a percentage of the maximum on-time. During the first 0.5 ms, the on-time is limited to 12.5%. During the next 1 ms, the on-time is limited to 25% and during the last 2 ms, the on-time is limited to 50%.

If the output voltage rises above the minimum threshold before soft-start is completed, the device assumes that the output load is very light and immediately changes to PFM operation.

The iW1689 will attempt to restart from any of these fault conditions after V_{CC} has discharged and then has recharged to the start-up threshold.

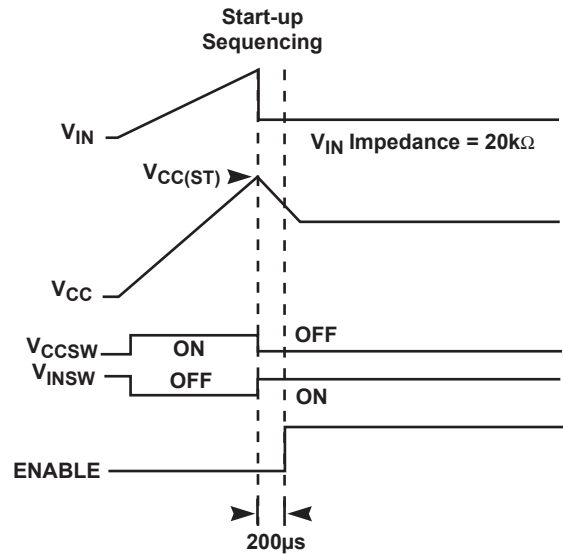


Figure 9.2.1 Start-up Sequencing Diagram

9.3 Understanding Primary Feedback

Figure 9.3.1 illustrates a simplified flyback converter. When the switch Q1 conducts during $t_{ON}(t)$, the current $i_g(t)$ is directly drawn from rectified sinusoid $v_g(t)$. The energy $E_g(t)$ is stored in the magnetizing inductance L_M . The rectifying diode D1 is reverse biased and the load current I_O is supplied by the secondary capacitor C_O . When Q1 turns off, D1 conducts and the stored energy $E_g(t)$ is delivered to the output.

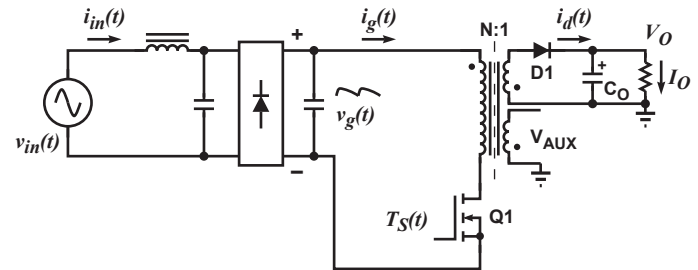


Figure 9.3.1 Simplified Flyback Converter

In order to regulate the output voltage within a tight specification, the information about the output voltage and load current needs to be accurately sensed. In the DCM flyback converter, this information can be read via the auxiliary winding or the primary magnetizing inductance (L_M). During the Q_1 on-time, the load current is supplied from the output filter capacitor C_O . The voltage across L_M is $v_g(t)$, assuming the voltage dropped across Q_1 is zero. The current in Q_1 ramps up linearly at a rate of:

$$\frac{di_g(t)}{dt} = \frac{v_g(t)}{L_M} \quad (9.1)$$

At the end of on-time, the current has ramped up to:

$$i_g(t) = \frac{v_g(t) \times t_{ON}(t)}{L_M} \quad (9.2)$$

This current represents a stored energy of:

$$E_g = \frac{L_M}{2} \times i_g(t)^2 \quad (9.3)$$

When Q_1 turns off at t_O , $i_g(t)$ in L_M forces a reversal of polarities on all windings. Ignoring the communication-time caused by the leakage inductance L_K at the instant of turn-off t_O , the primary current transfers to the secondary at an amplitude of:

$$i_d(t) = \frac{N_P}{N_S} \times i_g(t) \quad (9.4)$$

Assuming the secondary winding is master, the auxiliary winding is slave.

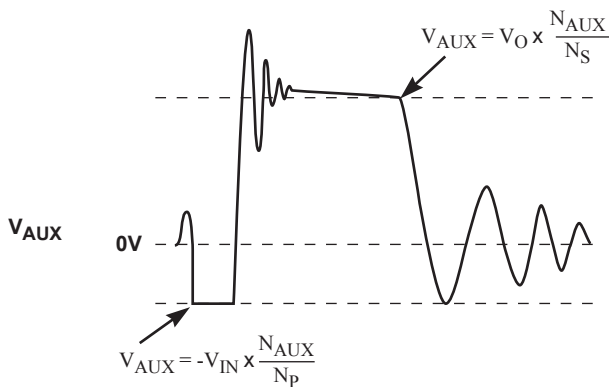


Figure 9.3.2 Auxiliary Voltage Waveforms

The auxiliary voltage is given by:

$$V_{AUX} = \frac{N_{AUX}}{N_S} (V_O + \Delta V) \quad (9.5)$$

and reflects the output voltage as shown in Figure 9.3.2.

The voltage at the load differs from the secondary voltage by a diode drop and IR losses. The diode drop is a function of current, as are IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage will be a fixed ΔV . Furthermore, if the voltage can be read when the secondary current is small, ΔV will also be small. With the iW1689, ΔV can be ignored.

The real-time waveform analyzer in the iW1689 reads this information cycle by cycle. The part then generates a

feedback voltage V_{FB} . The V_{FB} signal precisely represents the output voltage under most conditions and is used to regulate the output voltage.

9.4 Understanding CC and CV mode

The iW1689 has both a built-in output constant current (CC) mode with foldback, and a constant voltage (CV) mode. Both of these modes use iWatt's proprietary algorithm for primary feedback to control the secondary output. The CC mode is especially useful in battery charging applications. The load current is sensed indirectly by the primary sensing signal, cycle by cycle, to determine the appropriate controller mode for safe battery charging. The CC mode will override the CV mode so that the maximum safe operating area (SOA) of the power supply output is not exceeded.

9.5 Constant Voltage Operation

After soft-start has been completed, the digital control block measures output voltage. If this is in the normal range, the device will operate as a fixed frequency voltage-mode PWM circuit.

If no voltage is detected on V_{SENSE} after 20 pulses during normal operation, it is assumed that the auxiliary winding of the transformer is either open or shorted and the iW1689 shuts down.

In normal operation, when the load current is below the limit threshold, the device will operate as CV mode to regulate the output voltage through the primary feedback signal.

In CC operation mode, iW1689 will regulate the output current constant at the maximum level allowed regardless of the output voltage drop. When the output voltage reaches 20% of the typical output voltage the device will shut off (or output foldback), and will restart for the next startup cycle without AC recycling.

If the output overload is not reduced then system goes into hiccup mode with varied periods of time depending on the AC input. Figure 9.6.1 shows the ideal VI curve (voltage versus current output) of constant current limit.

9.6 Constant Current Operation

The iW1689 has been designed to work in constant-current mode for battery charging applications. If the output voltage drops, but does not go below 20% of the nominal designed value, the device operates in this mode. Note that during soft-start, the constant current operation mode is disabled.

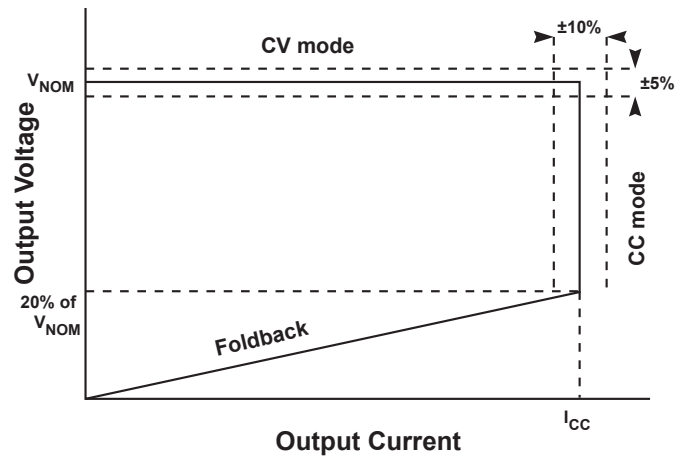


Figure 9.6.1 Power Envelope

9.7 CCM Protection

The iW1689 is designed to operate in discontinuous conduction (DCM) mode at a fixed frequency of 40 kHz in both CC and CV modes. To avoid operation in continuous conduction (CCM) mode, the iW1689 checks for the falling edge of the V_{SENSE} input on every cycle. If a falling edge of V_{SENSE} is not detected during the normal 25 μ s period, the switching period will be extended until the falling edge V_{SENSE} does occur. If the switching period reaches 75 μ s without V_{SENSE} being detected, the iW1689 will immediately shut off.

9.8 PFM Mode at Light Load

The iW1689 normally operates in a fixed frequency PWM mode when I_{OUT} is greater than approximately 5% of the specified maximum load current. As the output load I_{OUT} is reduced, the on-time t_{ON} is decreased. At the moment that the load current drops below 10% of nominal, the controller transitions to Pulse Frequency Modulation (PFM) mode. Thereafter, the on-time will be modulated by the line voltage and the off-time is modulated by the load current. The device automatically returns to PWM mode when the load current increases.

9.9 Internal Loop Compensation

The iW1689 incorporates an internal Digital Error Amplifier with no requirement for external loop compensation. The loop stability is guaranteed by design to provide at least 45 degrees of phase margin and -20dB of gain margin.

9.10 Voltage Protection Functions

The iW1689 includes functions that protect against input and output overvoltage.

The input voltage is monitored by the V_{IN} pin and the output voltage is monitored by the V_{SENSE} pin. If the voltage at these pins exceed their undervoltage or overvoltage thresholds for more than 4-8 cycles, the iW1689 will stop switching. However, the IC will remain biased which will discharge the V_{CC} supply. Once V_{CC} drops below the UVLO threshold, the controller will reset itself and then initiate a new soft-start cycle. The controller will continue to attempt to soft-start until the error condition is removed.

The output voltage can be high enough to damage the output capacitor when the feedback loop is broken. The iW1689 uses the primary feedback only with no secondary feedback loop. When the V_{SENSE} pin is shorted to GND (by shorting/open sense resistor). The controller will shut off with 6 consecutive pulses after start-up.

10.0 Design Example

10.1 5V/4W Adapter Reference Design

This design example gives the procedure for a flyback converter using iW1689. Refer to figure 11.01 for the application circuit. The design objectives for this adapter are given in table 10.1. It meets UL, IEC, and CEC requirements.

Parameter	Symbol	Range
Input Voltage	V_{IN}	90 - 264 V _{RMS}
Frequency	f_{IN}	47 - 64 Hz
No Load Input	P_{IN}	200 mW
Output Voltage	V_{OUT}	4.95 - 5.05 V
Output Current	I_{OUT}	800 mA
Output Ripple	V_{RIPPLE}	100 mV
Power Out	P_{OUT}	4 W
CEC Efficiency	η	61.5%

Table 10.1 iW1689 Measured Performance Table

10.2 Start-Up

The start-up is done by drawing a DC rail supply through V_{IN} (pin 5) via V_{INRES} . The start-up function of the iW1689 happens as soon as the V_{IN} reaches the typical start-up voltage of 12 V. Immediately after start-up the V_{IN} will drop to the operation level by a resistor network (V_{INRES} and a 20 K Ω internal resistor). At the same time the V_{CC} pin (4) will be supplied by the auxiliary winding through the bias rectifier diode and has to be maintained in operation voltage from 7 V to 16 V. V_{INRES} is also used to set a predetermined value to operate within the AC input range.

The auxiliary voltage is also the primary feedback signal. This is the information that the system will read cycle by cycle through the R_{SENSE} resistor and the clamp diode to regulate the output voltage by changing the frequency duty cycle.

10.3 Input Selection

For a universal AC input power supply the AC range will be from 90V_{RMS} to 264V_{RMS}:

$$V_{BULK} = \sqrt{2}V_{AC} - 1.5V$$

Due to the limited power range that this adapter is designed to handle, there is no special consideration needed to select the bridge diode. Any 1 A rated standard diode with a 600V reverse voltage is suitable.

10.4 Transformer Design

The following procedure is a step-by-step example of a transformer design that is controlled by the iW1689 digital controller core.

Core Selection:

The ideal transformer is one that offers a minimum core loss while requiring the least amount of space. Table 10.4 shows how to choose the core size that can handle the selected output power in the low power ranges.

Power	EE core (V _e mm ³)	EP core (V _e mm ³)	EPC core (V _e mm ³)
2 – 7 W	EE8 (134)	EP7 (162)	EPC10 (161)
	EE10 (315)	EP13 (472)	EPC13 (382)
	EE13 (385)		EPC17 (917)
	EE16 (754)	EPC19 (1097)	
8 – 14 W	EE19 (900)	EP17 (966)	EPC19 (1097)

Table 10.4 Core Selection per Output Power

From table 10.4 we selected the EE16 core. The core will be ferrite material (TDK # PC40 or equivalent) to handle 4 W output with low material and assembly costs.

The core specification EE16:

$$V_E = 754\text{mm}^3, A_E = 20.1\text{mm}^2, \text{Material} = \text{TDK}\#\text{PC40 or eq.}, B_{MAX} = 3000 \text{ Gauss.}$$

Calculate $C_{BULK(MIN)}$ and $V_{BULK(MIN)}$

In typical applications, the bulk capacitor is chosen so that the bulk capacitor voltage drops to 70% of the V_{INDC} peak before the next charging cycle. If a longer holdup time is needed then a larger bulk capacitor should be used.

$$V_{BULK(MIN)} = 0.7 \times 125V = 87.5V$$

$$V_{BULK(MAX)} = V_{INDC(MAX)} = 372V$$

$$C_{BULK} = \frac{P_{IN}}{\left[f_{IN} \times \left(V_{INDC(MIN)}^2 - V_{BULK(MIN)}^2 \right) \right]} \quad (10.1)$$

$$V_{BULK(MIN)} = \sqrt{V_{INDC(MIN)}^2 - \frac{P_{IN}}{f_{IN} \times C_{BULK}}} \quad (10.2)$$

With a 4 W output and 73% efficiency the input power (P_{IN}) will be:

$$P_{IN} = \frac{P_{OUT}}{\eta} \quad (10.3)$$

$$P_{IN} = \frac{4W}{73\%} = 5.48W$$

Substituting value of P_{IN} , $V_{BULK(MIN)}$ and $V_{BULK(MAX)}$ into equation (10.1) and solving for C_{BULK} :

$$C_{BULK} = \frac{5.48}{(125^2 - 87.5^2) \times 60} = 11.3\mu F$$

$$C_{BULK} = 10\mu F$$

Since we now know C_{BULK} then from equation (10.2):

$$V_{BULK(MIN)} = \sqrt{125^2 - \frac{5.48}{60 \times 10 \times 10^{-6}}}$$

$$V_{BULK(MIN)} = 82V$$

Calculating primary turns, inductance and peak current

The Volt-second product is limited in the iW1689 application to 1005V μ s. The primary turns will be:

$$N_{PR} = \frac{V_{IN} \times T_{ON}}{B_{MAX} \times AC} \times 10^8 \quad (10.4)$$

$$N_{PR} = \frac{1000 \times 10^{-6}}{.3 \times 20.1 \times 10^{-6}}$$

$$N_{PR} = 167$$

and

$$L_M = \frac{(V_{IN} \times T_{ON})^2}{2 \times P_{IN} \times T_P} \quad (10.5)$$

The maximum operating primary Volt-second product is set at 900V μ s. The magnetizing inductance should be calculated as:

$$L_M \approx \frac{900^2}{(2P_{IN} \times T_P)} \quad (10.6)$$

The primary peak current will be:

$$I_{PRPK} = \frac{V_{BULK(MIN)} \times T_{ON}}{L_M} \quad (10.7)$$

From equation (10.6):

$$L_M = \frac{(900)^2}{(2 \times 5.48 \times 25) 10^6} = 2.96mH$$

From equation (10.7)

$$I_{PRPK} = \frac{900}{3.65}$$

$$I_{PRPK} = 304mA$$

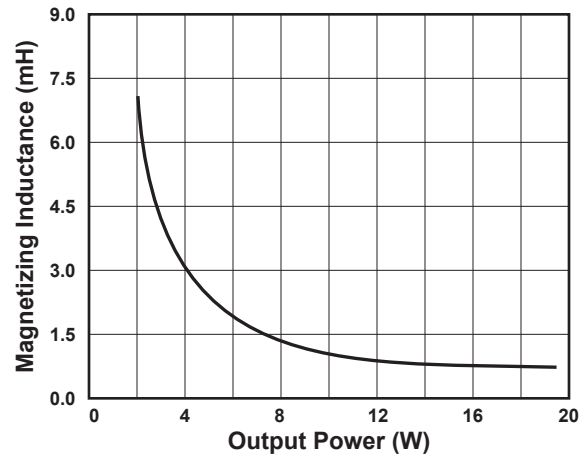


Figure 10.4.1 Magnetizing Inductance vs. Output Power

Calculating the turns ratio in Discontinuous Conduction Mode (DCM):

$$N = \frac{V_{IN} \times T_{ON}}{V_{OUT} \times T_{RESET}} \quad (10.8)$$

To ensure the circuit remains in DCM a dead time (T_{DEAD}) is established so that the maximum T_{ON} plus T_{RESET} is about 85% of full period (T_p or T_{DEAD} is 15% of T_p). If T_{DEAD} is more than 15% of T_p then lower efficiency can be expected. If T_{DEAD} is less than 15% then the iW1689 may go into variable frequency mode.

$$T_{RESET} = 85\%T_P - T_{ON} \quad (10.9)$$

$$V_{IN} \times T_{ON} = N V_{OUT} \times T_{RESET}$$

Or:

$$N = \frac{V_{IN} \times T_{ON}}{V_{OUT} \times T_{RESET}} \quad (10.10)$$

In the worst case of transformer working condition is 90 VAC input and full load output.

$$T_{ON} = \frac{900V\mu s}{V_{BULK(MIN)}}$$

$$T_{ON} = \frac{900V\mu s}{82V}$$

$$T_{ON} = 10.9\mu s$$

From 10.8:

$$T_{RESET} = 85\% \times 25\mu s - 10.9\mu s$$

$$T_{RESET} = 10.35\mu s$$

Allowing a maximum forward voltage drop at the Schottky diode of 0.7 V, substitute T_{ON} and T_{RESET} into equation (10.10):

$$N = \frac{900}{5.7 \times 10.35} = 15.2$$

Secondary and auxiliary turn:

$$N_{SEC} = \frac{N_{PR}}{N} \quad (10.11)$$

$$N_{AUX} = \frac{N_{PR} \times V_{AUX}}{V_{OUT}} \quad (10.12)$$

With $N_{PR} = 167$, and $N = 15$, from equation 10.10:

$$N_{SEC} = \frac{167}{15} = 11 \text{ turns}$$

From equation 10.11:

$$N_{AUX} = 11 \frac{13V}{5.7V}$$

$$N_{AUX} = 25 \text{ turns}$$

Primary RMS current: Primary current is a triangle of peak amplitude I_{PRPK} at maximum duration T_{ON} . It's RMS on a period T_p is:

$$I_{PRRMS} = \left(\frac{I_{PRPK}}{\sqrt{3}} \right) \sqrt{\frac{T_{ON}}{T_p}} \quad (10.13)$$

Substitute $I_{PRPK} = 304 \text{ mA}$ into equation (10.13)

$$I_{PRRMS} = \frac{304}{\sqrt{3}} \times \sqrt{\frac{10.9}{25}} = 115 \text{ mA}$$

Selecting a switching MOSFET:

For a flyback converter, the MOSFET will be selected so that V_{DS} is higher than the switching voltage plus the reflecting secondary and spike voltage.

$$V_{DS} > V_{BULK(MAX)} + NV_{OUT} + V_{SPIKE} \quad (10.14)$$

If $V_{SPIKE} = 100V$, then from equation (10.14):

$$V_{DS} > 372 + 15 \times 5.7 + 100 = 557V$$

And $I_{DS} > I_{PRPK} = 304 \text{ mA}$

Therefore, select a MOSFET = 600 V/0.4 A

The secondary current is a triangle of peak amplitude $I_{SECPK} = I_{PRPK} \times N$ at a maximum duration of T_{RESET} . It's RMS value during a period T_p is:

$$I_{SECRMS} = \left(I_{PRPK} \times \frac{N}{\sqrt{3}} \right) \times \sqrt{\frac{T_{RESET}}{T_p}} \quad (10.15)$$

Substituting $I_{PRPK} = 304 \text{ mA}$ into equation (10.15) yields:

$$I_{SECRMS} = \frac{0.304 \times 15}{\sqrt{3}} \times \sqrt{\frac{10.35}{25}} = 1.694$$

The working voltage of the rectifier diode includes the output voltage plus margin reverse voltage during the T_{ON} period. A 20% marginal voltage is suitable for safety:

$$V_{DIODE} = 120\% \left(\frac{V_{BULK(MAX)}}{N} \right) + V_{OUT}$$

$$V_{DIODE} = 1.2 \left(\frac{372}{15} \right) + 5 = 35V$$

Typically, we select the rated current of a Schottky diode rectifier that is twice the output current value. With a known value for I_{SECRMS} and V_{DIODE} the rectifier diode will be selected with ratings of 40 V and 3 A:

$$\text{Diode} = 3A / 40V$$

This maximum RMS current occurs at 130% of the rated output load. Therefore, the wire size will be based on $I_{SECRMS} / 1.3$.

10.5 Wire Selection

Transformer wire sizes are selected based on input/output rms current. Typically we select 500cir.mils for every 1A rms. If the length of wire is less than a meter, then 250cir.mils per amp rms is suitable. Therefore:

$$\text{Primary wire} = 500 \text{ cir.mils} \times 0.110 = 55 \text{ cir.mils}$$

$$\text{Primary wire} = 33\text{AWG} (50 \text{ cir.mils})$$

$$\text{Secondary wire} = 250 \text{ cir.mils} \times 1.9/1.3 = 367 \text{ cir.mils}$$

$$\text{Secondary wire} = 26\text{AWG} (320 \text{ cir.mils})$$

$$\text{Auxiliary wire} = 32\text{AWG} (63 \text{ cir.mils})$$

10.6 Output Selection

In a flyback converter design the output capacitors are under high stress. Absolute value, ESR, ESL, and ripple current ratings need to be considered when selecting the output capacitor.

$$C = \frac{(T_{OFF} \times I_{OUT(MAX)})}{V_P - P} \quad (10.16)$$

In the worst case:

$$T_{OFF(MAX)} = 25\mu s - 10.9\mu s = 14.1\mu s$$

ESR and ESL have a significant effect on the high frequency ripple voltage if a single stage output filter is used. For the best results low ESR capacitors should be used. However, the really low ESR capacitors are more expensive compared to an additional LC filter. The LC filter can have an adequate ripple rating as the ordinary-grade capacitor.

The Inductance reactance will be:

$$X_L = 2\pi \times f_{SW} \times L \quad (10.17)$$

The attenuation will be:

$$A_R = \frac{X_L}{ESR} \quad (10.18)$$

The ripple current (rms) rating is typically about 120% of the DC output current. The capacitor must be capable of conducting the output ripple without an excessive temperature rise.

For 100 mV ripple, from equation (10.16):

$$C = \frac{14.1 \times 10^{-6} \times 1.694}{0.1} = 239\mu F$$

For high ripple current in the flyback topology we will select the output capacitor with a high ripple current and a low ESR. $C = 470 \mu F/10 V$, ZL type (53 mΩ, and 1.03 A ripple)

With a small 7 μH inductance, from equation (10.17):

$$X_L = 2 \times 3.14 \times 40000 \times 7 \times 10^{-6} = 1.7\Omega$$

With a 100 μF/25 V XYG capacitor from Rubycon with an ESR of 22 mΩ at 100 kHz, then from equation (10.18):

$$A_R = \frac{1.7}{0.22} = 7.7$$

A ripple rejection of 18 dB is obtained with small, low cost LC components.

10.7 Signal Sensing Calculation

The V_{IN} signal input is a multi-function signal. It is used for setting AC input under/over voltage threshold (V_{UVDC}/V_{OVDC}), power supply source for the IC during startup, and fine tuning for the constant current limit. With a low startup current of 8 μA and the V_{IN} startup maximum at 488 mV set by the internal circuitry, the V_{IN} resistor will be approximately 4.63 MΩ.

Furthermore, the V_{IN} signal is used to correct on-time (T_{ON}) based on the line voltage. A bypass capacitor of 470-1000 pF is needed to filter high frequency noise. Higher values are not recommended.

If tight tolerance of the Constant Current (CC) limit is required then the V_{INRES} can be used as a CC limit setting. It can be trimmed with the maximum trimmed value of less than 10% of the V_{INRES} value.

The primary feedback signal from the auxiliary winding will reveal the secondary voltage at a different load. Short circuit and over voltage supply power to the system after starting up. From figure 9.6.1, the V_{AUX} corner (right before voltage starts falling) is the information that the system will read cycle by cycle to generate a feedback voltage (V_{FB}). V_{FB} precisely represents the output voltage and is used to regulate the output by changing T_{ON}/T_{OFF} . Pay close attention to this corner signal condition. To avoid any unwanted stray signals at that corner, the following things need to be done:

1. The bias rectifier diode must be a fast recovery diode (50ns or lower) to prevent reverse voltage from the bias voltage source.
2. The bias capacitor must be low ESR to minimize ripple & noise at V_{CC} . For example: YK type from Rubycon.

3. The distance from the transformer to V_{SENSE} should be as short as possible to minimize the parasitic effects.

4. The impedance between the transformer auxiliary winding and ground is 20 k Ω . Therefore $R_{SENSEIN} + R_{SENSE} = 20 \text{ k}\Omega$:

$$R_{SENSEIN} = 20k\Omega \frac{V_{AUX} - V_{REF}}{V_{AUX}} \quad (10.19)$$

If $V_{AUX} = V_{OUT_REG} \times N_{AUX}/N_{SEC} = 5.0 \times 25/11 = 11.384 \text{ V}$.

(See figure 9.3.2)

$$R_{SENSE} = 20k\Omega \frac{11.384 - 1.538}{11.384} = 17.29k\Omega$$

And $R_{SENSE} = 20 \text{ k}\Omega - 17.29 \text{ k}\Omega$. Standard values of 17.32 k Ω (10 k Ω + 7.32 k Ω) and 2.68 k Ω are used.

The V_{CC} pin is the input power supply for iW1689 after startup. An RC filter is used to filter any noise. The recommend values of the RC filter are 100 Ω and 470 nF ceramic capacitor (type X7R) in parallel with a 2.2 $\mu\text{F}/25\text{V}$ electrolytic capacitor.

10.8 Component Values

Component	Value
L_M	2.96 mH
N	15
N_{SEC}	11 turns
N_{PR}	167 turns
N_{AUX}	25 turns
Diode, D9	3 A/40 V
Secondary Wire	26 AWG
$R_{SENSEIN}$	17.32 k Ω
R_{SENSE}	2.68 k Ω
R1, R3	2.0 M Ω
R2	631 k Ω
C1	10 $\mu\text{F}/400 \text{ V}$

Table 10.3 Final Component Values for 5 V/4 W Adapter

10.9 PCB Layout

A switching power supply layout has multiple ground signals that must be appropriately managed. These include the power ground, the switching ground and the control logic ground signals. All ground traces must be kept as short as possible and terminate at the power ground. Using a thick trace for switching ground will reduce switching losses. Using a thick ground plane for the power ground will help reduce EMI and lower ripple noise. In addition, keeping the trace from the transformer to the V_{SENSE} pin as short as possible will improve the signal quality of the V_{SENSE} signal.

10.10 Critical Components

The primary feedback signal V_{SENSE} is the most important signal to control output performance (i.e. VI curve, ripple & noise, regulation) and the quality of the V_{SENSE} waveform is greatly influenced by the clamp diode, bias rectifier diode, and bias capacitor. These diodes have to be ultra fast recovery, and the filter cap needs to be low ESR to minimize noise and distortion of the V_{SENSE} signal. For this sample design we choose the following components:

- Clamp diode D5 is UF4006, and rectifier D7 is HER102
- C7 of Bias filter capacitor needs to be low ESR.

10.11 Performance

$V_{IN AC}$	$P_{OUT} = 0W$
90	130 mW
264	160 mW

Table 10.4 No load power input at 90/264VAC

Load (mA)	90V	115V	230V	264V
0	5.14V	5.14V	5.13V	5.13V
200	5.04V	5.04V	5.04V	5.34V
400	5.00V	5.00V	5.00V	5.00V
600	4.96V	4.96V	4.97V	4.97V
800	4.93V	4.93V	4.93V	4.93V

Table 10.6 Output Voltage vs. Line and Load

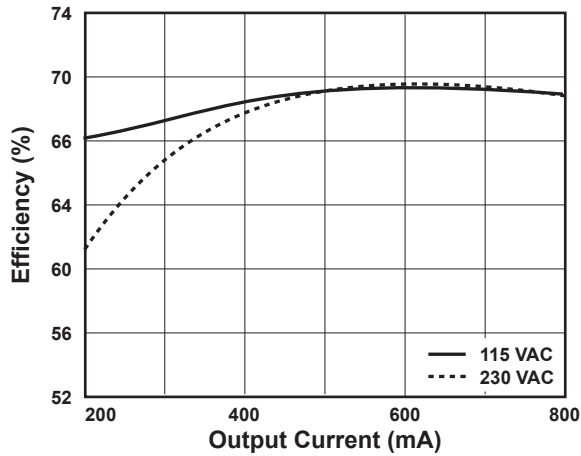


Figure 10.11.1 Efficiency vs. Output Load Measured at PCB output

$V_{IN AC}$	0A	200mA	400mA	600mA	800mA
90	13 mV	38 mV	46 mV	54 mV	60 mV
264	13 mV	41 mV	47 mV	54 mV	63 mV

Table 10.5 Ripple and Noise

11.0 Application Circuit

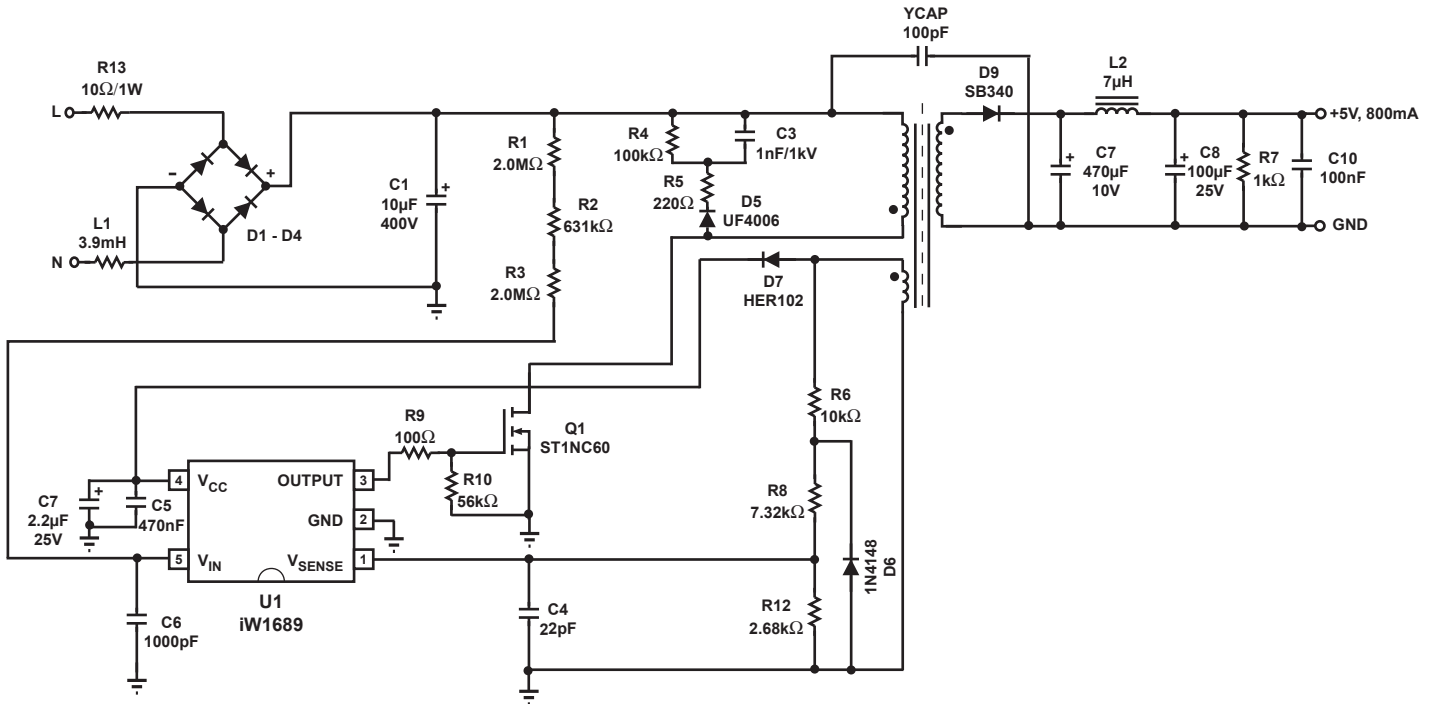
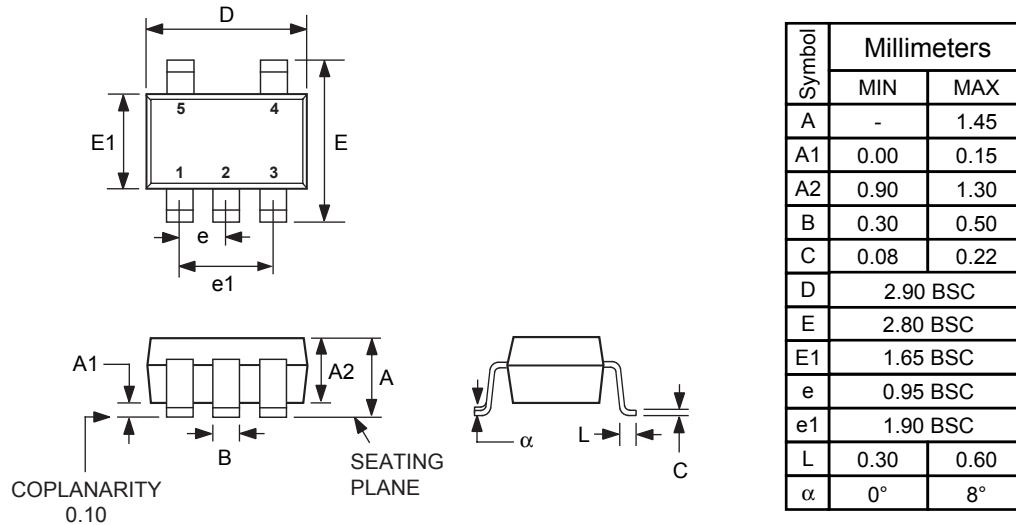


Figure 11.0.1. Typical Application Circuit

12.0 Physical Dimensions

5-Lead Small Outline Transistor Package



JEDEC Registered Outline: Drawing # MO-178, Variation AA
Controlling dimensions are in millimeters

Figure 12.0.1. Physical dimensions, 5-lead SOT-23 package

13.0 Ordering Information

Part Number	Package	Operating Temp. Range	Description
iW1689-00	SOT23-5L	$-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	iW1689 PWM Controller -Tape & Reel ¹

*Tape & Reel packing quantity is 3,000 units.

iW1689

Low-Power Off-line Digital PWM Controller



iW1689

Low-Power Off-line Digital PWM Controller



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Low-Power Off-line Digital PWM Controller



iW1689

Low-Power Off-line Digital PWM Controller



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