NCP1586

Low Voltage Synchronous Buck Controller

The NCP1586 is a low cost PWM controller designed to operate from a 5 V or 12 V supply. This device is capable of producing an output voltage as low as 0.8 V. This 8−pin device provides an optimal level of integration to reduce size and cost of the power supply. The NCP1586 provides a 1 A gate driver design and an internally set 275 kHz oscillator. In addition to the 1 A gate drive capability, other efficiency enhancing features of the gate driver include adaptive non−overlap circuitry. The NCP1586 also incorporates an externally compensated error amplifier and a capacitor programmable soft−start function. Protection features include programmable short circuit protection and under voltage lockout (UVLO). The NCP1586 comes in an 8−pin SOIC package.

Features

- Input Voltage Range from 4.5 to 13.2 V
- 275 kHz Internal Oscillator
- Boost Pin Operates to 26.5 V
- Voltage Mode PWM Control
- 0.8 V ±1.0 % Internal Reference Voltage
- Adjustable Output Voltage
- Capacitor Programmable Soft−start
- Internal 1 A Gate Drivers
- 80% Max Duty Cycle
- Input Under Voltage Lockout
- Programmable Current Limit
- This is a Pb−Free Device

Applications

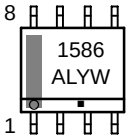
- Graphics Cards
- Desktop Computers
- Servers / Networking
- DSP & FPGA Power Supply
- DC−DC Regulator Modules

ON Semiconductor®

http://onsemi.com

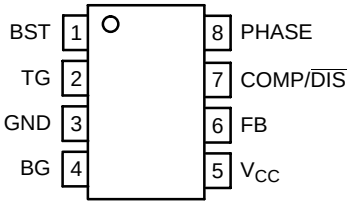
MARKING DIAGRAM

SOIC−8
D SUFFIX
CASE 751



1586 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Device

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1586DR2G	SOIC−8 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

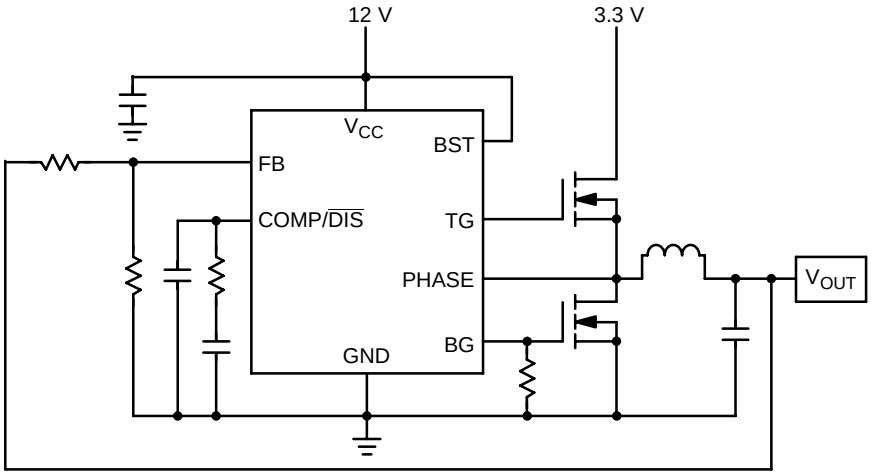


Figure 1. Typical Application Diagram

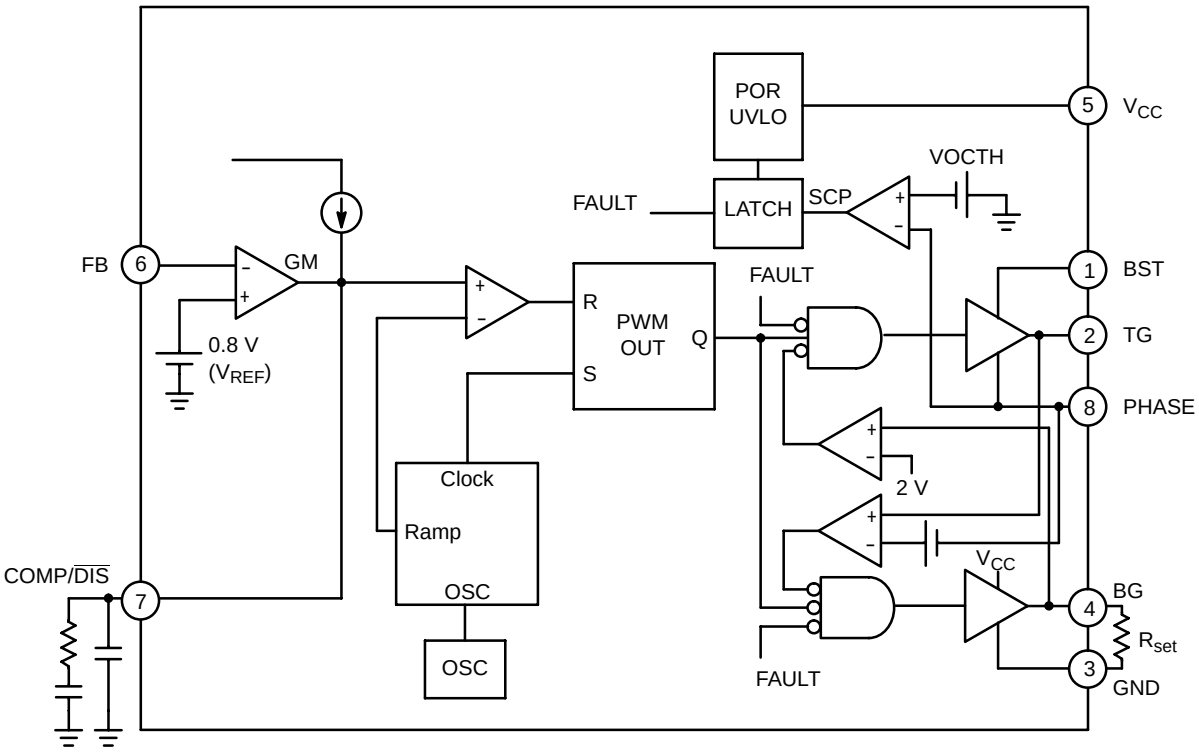


Figure 2. Detailed Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Description
1	BST	Supply rail for the floating top gate driver. To form a boost circuit, use an external diode to bring the desired input voltage to this pin (cathode connected to BST pin). Connect a capacitor (C_{BST}) between this pin and the PHASE pin. Typical values for C_{BST} range from 0.1 μF to 1 μF. Ensure that C_{BST} is placed near the IC.
2	TG	Top gate MOSFET driver pin. Connect this pin to the gate of the top N−Channel MOSFET.
3	GND	IC ground reference. All control circuits are referenced to this pin.
4	BG	Bottom gate MOSFET driver pin. Connect this pin to the gate of the bottom N−Channel MOSFET.
5	V_{CC}	Supply rail for the internal circuitry. Operating supply range is 4.5 V to 13.2 V. Decouple with a 1 μF capacitor to GND. Ensure that this decoupling capacitor is placed near the IC.
6	FB	This pin is the inverting input to the error amplifier. Use this pin in conjunction with the COMP pin to compensate the voltage−control feedback loop. Connect this pin to the output resistor divider (if used) or directly to V_{out}.
7	COMP/$\overline{DIS}$	Compensation Pin. This is the output of the error amplifier (EA) and the non−inverting input of the PWM comparator. Use this pin in conjunction with the FB pin to compensate the voltage−control feedback loop. The compensation capacitor also acts as a soft−start capacitor. Pull this pin low for disable.
8	PHASE	Switch node pin. This is the reference for the floating top gate driver. Connect this pin to the source of the top MOSFET.

ABSOLUTE MAXIMUM RATINGS

Pin Name	Symbol	V_{MAX}	V_{MIN}
Main Supply Voltage Input	V_{CC}	15 V	−0.3 V
Bootstrap Supply Voltage Input	BST	30 V wrt/GND 15 V wrt/PHASE	−0.3 V
Switching Node (Bootstrap Supply Return)	PHASE	25 V	−0.7 V −5.0 V for < 50 ns
High−Side Driver Output (Top Gate)	TG	30 V wrt/GND 15 V wrt/PHASE	−0.3 V wrt/PHASE
Low−Side Driver Output (Bottom Gate)	BG	15 V	−0.3 V −2.0 V for < 200 ns
Feedback	FB	5.5 V	−0.3 V
COMP/$\overline{DISABLE}$	COMP/$\overline{DIS}$	5.5 V	−0.3 V

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	165	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	45	°C/W
NCP1586 Operating Junction Temperature Range	T_J	0 to 125	°C
NCP1586 Operating Ambient Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Temperature Soldering (10 sec): Reflow (SMD styles only) Pb−Free		260	°C
Moisture Sensitivity Level	MSL	1	−

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS ($0°C < T_A < 70°C$; $4.5\ V < V_{CC} < 13.2\ V$, $4.5\ V < BST < 26.5\ V$, $C_{TG} = C_{BG} = 1.0\ nF$ (REF:NTD30N02), for min/max values unless otherwise noted.)

Characteristic	Conditions	Min	Typ	Max	Unit
Input Voltage Range	−	4.5	−	13.2	V
Boost Voltage Range	−	4.5	−	26.5	V
Supply Current					
Quiescent Supply Current	V_{FB} = 1.0 V, No Switching V_{CC} = 13.2 V	0.1	−	0.9	mA
Boost Quiescent Current	V_{FB} = 1.0 V, No Switching, V_{CC} = 13.2 V	2.0	3.0	4.0	mA
Under Voltage Lockout					
UVLO Threshold	V_{CC} Rising Edge	3.9	4.0	4.1	V
UVLO Hysteresis	−	365	415	465	mV
Switching Regulator					
VFB Feedback Voltage, Control Loop in Regulation	T_A = 0 to 70°C	0.792	0.8	0.808	V
Oscillator Frequency	T_A = 0 to 70°C	250	275	300	kHz
Ramp−Amplitude Voltage		0.8	1.1	1.4	V
Minimum Duty Cycle		0	−	−	%
Maximum Duty Cycle		70	75	80	%
BG Minimum On Time		−	500	−	ns
Error Amplifier (GM)					
Transconductance		3.0	−	4.4	mmho
Open Loop DC Gain		55	70	−	DB
Output Source Current Output Sink Current	V_{FB} < 0.8 V V_{FB} > 0.8 V	80 80	120 120	− −	μA
Input Offset Voltage		−2.0	0	2.0	mV
Input Bias Current		−	0.1	1.0	μA
Soft−Start					
SS Source Current	V_{FB} < 0.8 V	8.0	−	14	μA
Switch Over Threshold	V_{FB} = 0.8 V	−	100	−	% of Vref
Gate Drivers					
Upper Gate Source	V_{CC} = 12 V, VTG = VBG = 2.0 V	−	1.0	−	A
Upper Gate Sink		−	1.0	−	A
Lower Gate Source		−	1.0	−	A
Lower Gate Sink		−	1.0	−	A
TG Falling to BG Rising Delay	V_{CC} = 12 V, TG < 2.0 V, BG > 2.0 V	−	40	90	ns
BG Falling to TG Rising Delay	V_{CC} = 12 V, BG < 2.0 V, TG > 2.0 V	−	40	60	ns
Enable Threshold		0.3	0.4	0.5	V
Over−Current Protection					
OCSET Current Source	Sourced from BG pin, before SS	−	10	−	μA
OC Switch−Over Threshold		−	700	−	mV
Fixed OC Threshold		−	−375	−	mV

TYPICAL CHARACTERIZATION CURVES

(T_A = 25°C unless otherwise noted)

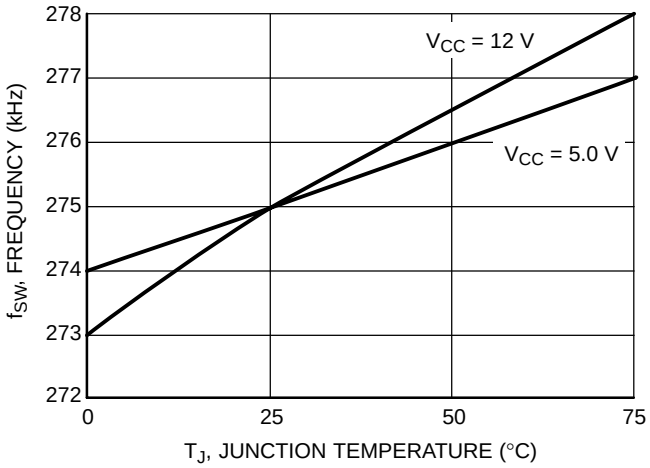


Figure 3. Oscillator Frequency (f_{SW}) vs. Temperature

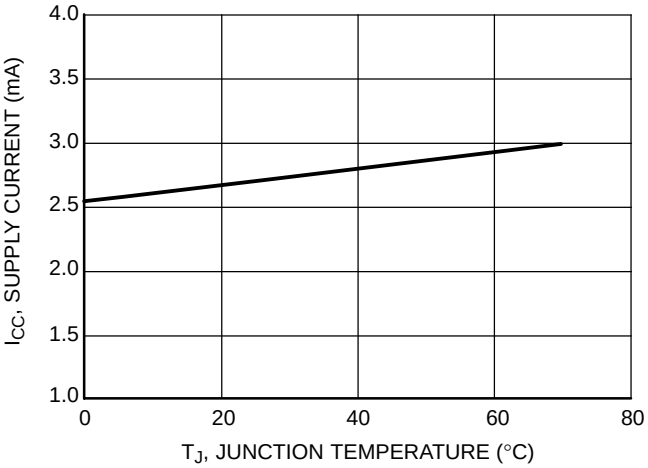


Figure 4. Quiescent Current (I_{CC}) vs. Temperature

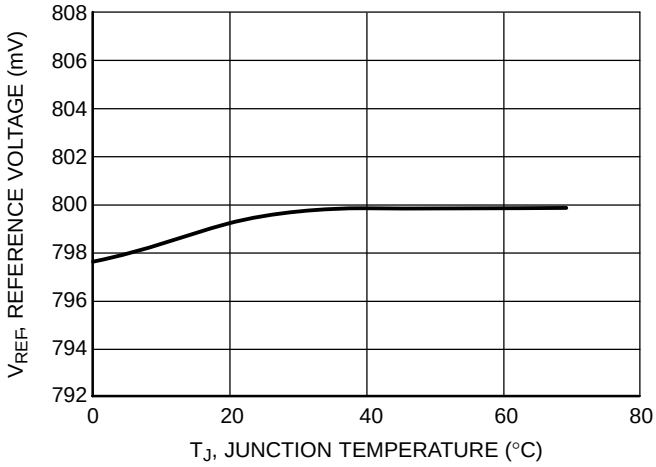


Figure 5. Reference Voltage (V_{REF}) vs. Temperature

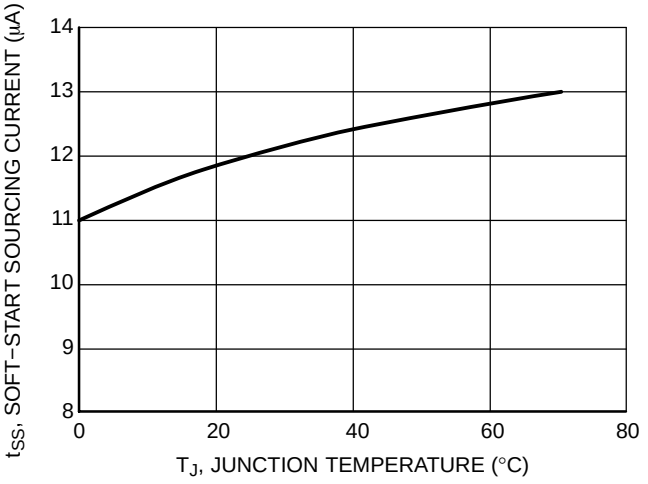


Figure 6. Soft−Start Sourcing Current (t_{SS}) vs. Temperature

DETAILED OPERATING DESCRIPTION

General

The NCP1586 is an 8−pin PWM controller intended for DC−DC conversion from 5.0 V & 12 V buses. The NCP1586 has a 1 A internal gate driver circuit designed to drive N−channel MOSFETs in a synchronous−rectifier buck topology. The output voltage of the converter can be precisely regulated down to 800 mV ±1.0% when the V_{FB} pin is tied to V_{OUT}. The switching frequency, is internally set to 275 kHz. A high gain operational transconductance error amplifier (OTA) is used.

Duty Cycle and Maximum Pulse Width Limits

In steady state DC operation, the duty cycle will stabilize at an operating point defined by the ratio of the input to the output voltage. The NCP1586 can achieve an 80% duty cycle. There is a built in off−time which ensures that the bootstrap supply is charged every cycle. The NCP1586 can allow a 12 V to 0.8 V conversion at 275 kHz.

Input Voltage Range (V_{CC} and BST)

The input voltage range for both V_{CC} and BST is 4.5 V to 13.2 V with respect to GND and PHASE, respectively. Although BST is rated at 13.2 V with respect to PHASE, it can also tolerate 26.4 V with respect to GND.

External Enable/Disable

When the Comp pin voltage falls or is pulled externally below the 400 mV threshold, it disables the PWM Logic and the gate drive outputs. In this disabled mode, the operational transconductance amplifier (EOTA) output source current is reduced and limited to the Soft−Start mode of 10 μA.

Normal Shutdown Behavior

Normal shutdown occurs when the IC stops switching because the input supply reaches UVLO threshold. In this case, switching stops, the internal SS is discharged, and all GATE pins go low. The switch node enters a high impedance state and the output capacitors discharge through the load with no ringing on the output voltage.

External Soft−Start

The NCP1586 features an external soft−start function, which reduces inrush current and overshoot of the output voltage. Soft−start is achieved by using the internal current source of 10 μA (typ), which charges the external integrator capacitor of the transconductance amplifier. Figure 7 is a typical soft−start sequence. This sequence begins once V_{CC} surpasses its UVLO threshold and OCP programming is complete. During soft−start, as the Comp Pin rises through 400 mV, the PWM Logic and gate drives are enabled. When the feedback voltage crosses 800 mV, the EOTA will be given control to switch to its higher regulation mode output current of 120 μA.

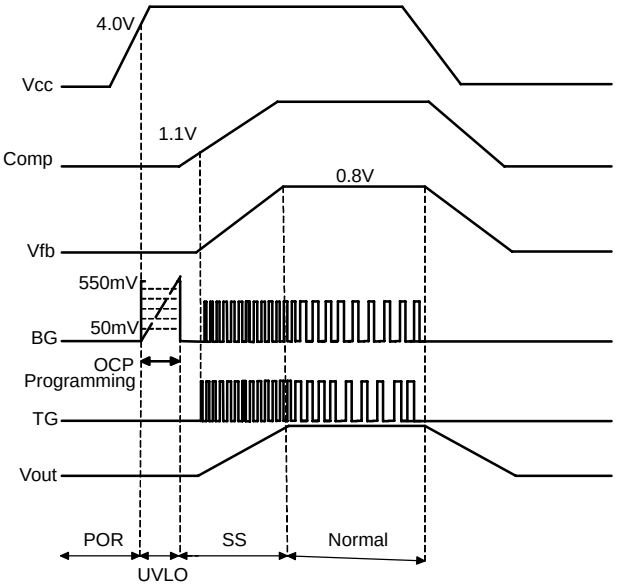


Figure 7. Soft−Start Implementation

UVLO

Undervoltage Lockout (UVLO) is provided to ensure that unexpected behavior does not occur when V_{CC} is too low to support the internal rails and power the converter. For the NCP1586, the UVLO is set to ensure that the IC will start up when V_{CC} reaches 4.0 V and shutdown when V_{CC} drops below 3.7 V. This permits operation when converting from a 5.0 input voltage.

Overcurrent Threshold Setting

NCP1586 allows to easily program an Overcurrent Threshold ranging from 50 mV to 550 mV, simply by adding a resistor (RSET) between BG and GND. During a short period of time following V_{CC} rising over UVLO threshold, an internal 10 μA current (I_{OCSET}) is sourced from BG pin, determining a voltage drop across R_{OCSET}. This voltage drop will be sampled and internally held by the device as Overcurrent Threshold. The OC setting procedure overall time length is about 6 ms. Connecting a R_{OCSET} resistor between BG and GND, the programmed threshold will be:

$$I_{OCth} = \frac{I_{OCSET} \cdot R_{OCSET}}{R_{DS(on)}} \qquad \text{(eq. 1)}$$

RSET values range from 5 kΩ to 55 kΩ. In case R_{OCSET} is not connected, the device switches the OCP threshold to a fixed 375 mV value: an internal safety clamp on BG is triggered as soon as BG voltage reaches 700 mV, enabling the 375 mV fixed threshold and ending OC setting phase. The current trip threshold tolerance is ±25 mV. The accuracy of the set point is best at the highest set point (550 mV). The accuracy will decrease as the set point decreases.

Current Limit Protection

In case of a short circuit or overload, the low−side (LS) FET will conduct large currents. The controller will shut down the regulator in this situation for protection against overcurrent. The low−side $R_{DS(on)}$ sense is implemented at the end of each of the LS−FET turn−on duration to sense the over current trip point. While the LS driver is on, the Phase voltage is compared to the internally generated OCP trip voltage. If the phase voltage is lower than OCP trip voltage, an overcurrent condition occurs and a counter is initiated. When the counter completes, the PWM logic and both HS−FET and LS−FET are turned off. The controller will retry to see if the short circuit or overload condition is removed through the soft start cycle. The minimum turn−on time of the LS−FET is set to be 500 nS.

Drivers

The NCP1586 includes 1 A gate drivers to switch external N−channel MOSFETs. This allows the NCP1586 to address high−power as well as low−power conversion requirements. The gate drivers also include adaptive non−overlap circuitry. The non−overlap circuitry increase efficiency, which minimizes power dissipation, by minimizing the body diode conduction time.

A detailed block diagram of the non−overlap and gate drive circuitry used in the chip is shown in Figure 8.

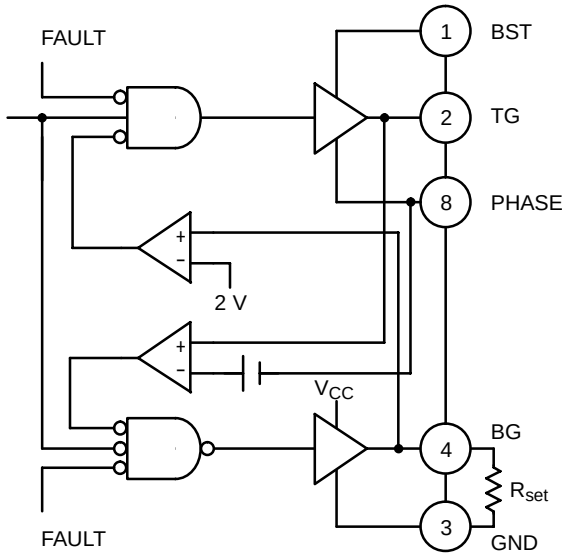
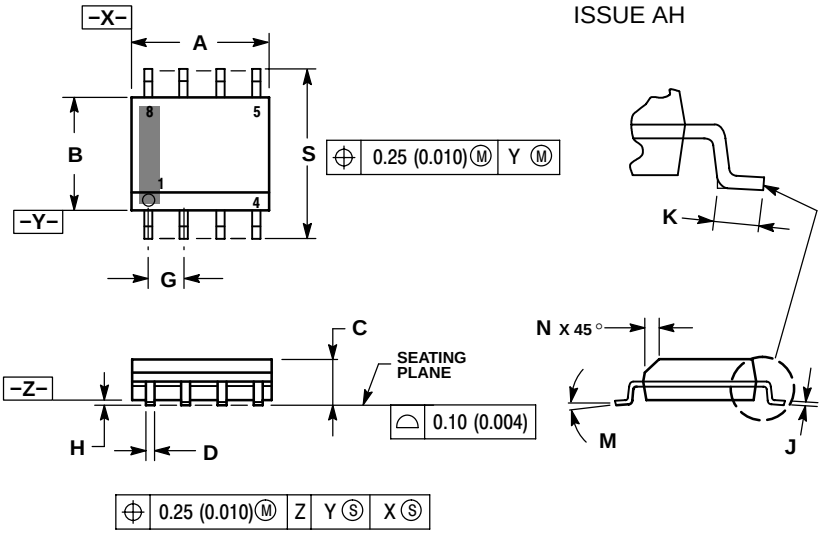


Figure 8. Block Diagram

Careful selection and layout of external components is required, to realize the full benefit of the onboard drivers. The capacitors between V_{CC} and GND and between BST and SWN must be placed as close as possible to the IC. The current paths for the TG and BG connections must be optimized. A ground plane should be placed on the closest layer for return currents to GND in order to reduce loop area and inductance in the gate drive circuit.

PACKAGE DIMENSIONS

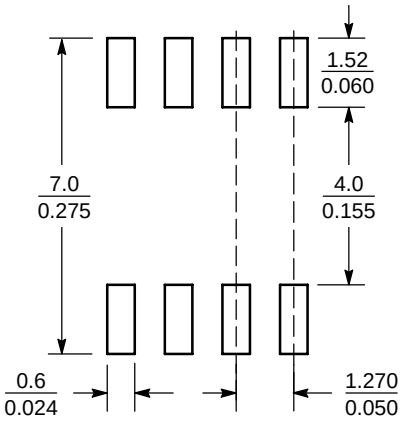
SOIC−8
D SUFFIX
CASE 751−07
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative