NCP3121

Product Preview

Dual 3.0 A, Step−Down DC/DC Switching Regulator

The NCP3121 is a dual buck converter designed for low voltage applications requiring high efficiency. This device is capable of producing an output voltage as low as 0.8 V. The NCP3121 provides dual 3.0 A switching regulators with an adjustable 200 kHz − 750 kHz switching frequency. Switching frequency is set by an external resistor. The NCP3121 also incorporates an auto−tracking and sequencing feature. Protection features include cycle−by−cycle current limit and undervoltage lockout (UVLO). The NCP3121 comes in a 32−pin QFN package.

Features

- Input Voltage Range from 4.5 V to 13.2 V
- 12 V_{in} to 3.3 V_{out} = 80% Min @ 3.0 A
- 3.0 A Integrated Switch
- 200−750 kHz Operation
- 0.8 ±1.5% FB Reference Voltage
- External Soft−Start
- 180°, Out of Phase Operation of OUT1 & OUT2
- Auto−Tracking and Sequencing
- Enable/Disable Capability
- QFN32 5x5 mm
- This is a Pb−Free Device

Typical Applications

- Set−Top Boxes
- DSP/μP/FPGA Core and I/O Voltages
- Networking and Telecommunications

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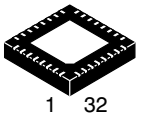
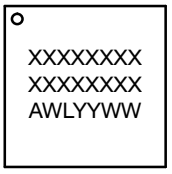


QFN32, 5x5
CASE 488AM

MARKING DIAGRAM



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G or ▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
NCP3121	QFN32	TBD

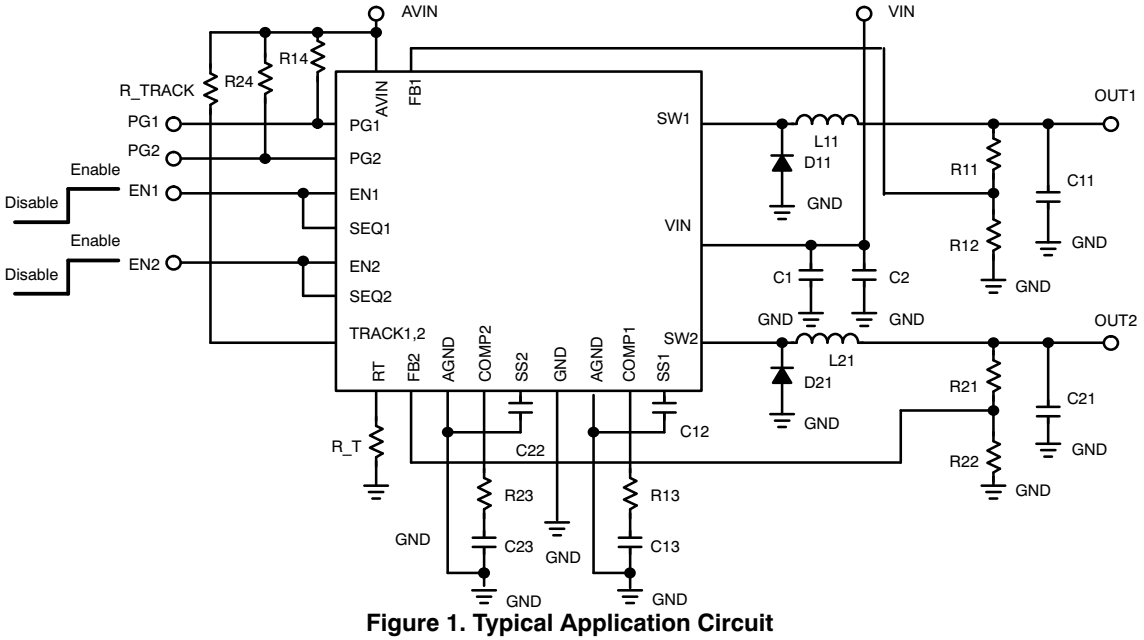


Figure 1. Typical Application Circuit

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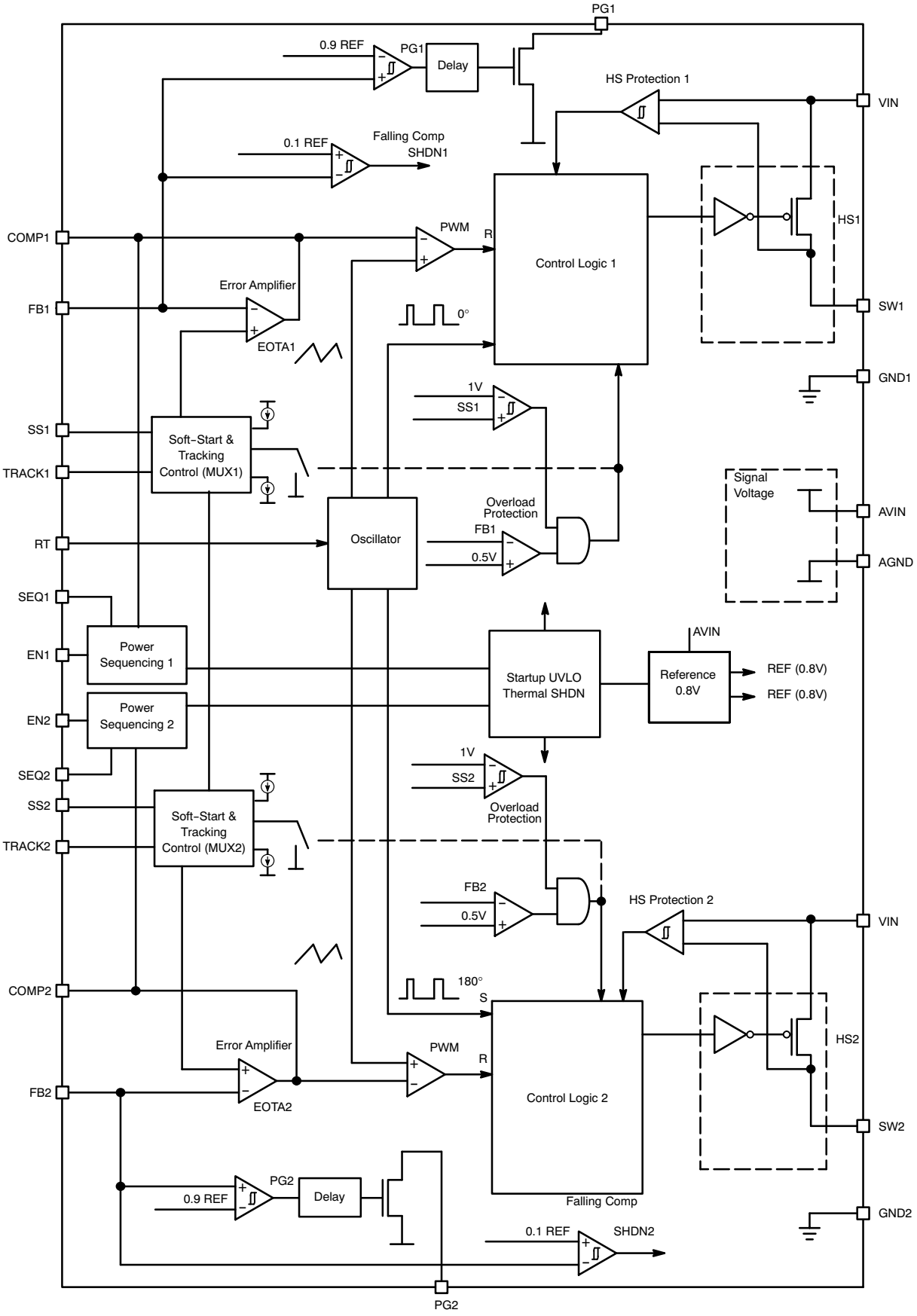


Figure 2. Block Diagram

PIN DESCRIPTION

Pin	Symbol	Description
1, 31, 32	SW1	Inductor connection to the first internal power switch. Connect an inductor between SW1 and the regulator output.
2 – 7	V_{IN}	Input power supply voltage pins. These pins should be connected together to the input signal supply voltage pin.
8 – 10	SW2	Inductor connection to the first internal power switch. Connect an inductor between SW2 and the regulator output.
11	GND2	Power ground for 2nd output
12	SS2	Soft−start control input to the regulator 2. An internal current source charges an external capacitor connected to this pin to set the soft−start time.
13	COMP2	Compensation pin of the second inside regulator. This is the output of the error amplifier and inverting input of the PWM comparator.
14	AGND	Analog ground; connect to GND1 and GND2.
15	FB2	Buck second output voltage feedback input. Inverting switch to the error amplifier 2.
16	RT	Frequency setting resistor input. Connect a resistor from RT pin to AGND to set the frequency of the master oscillator. The set frequency is twice that of the individual switching regulator.
17	TRACK 2	Tracking input 1. This pin allows the user to control the rise time of the second output.
18	TRACK 1	Tracking input 2. This pin allows the user to control the rise time of the first output.
19	SEQ2	Output turn−on sequencing pin of the second regulator. Connect to the EN pin of the next regulator if the power sequencing is needed. Connect SEQ to EN for normal operation of a standalone device.
20	EN2	Enable input of the second regulator.
21	SEQ1	Output turn−on sequencing pin of the first regulator. Connect to the EN pin of the next regulator if the power sequencing is needed. Connect SEQ to EN for normal operation of a standalone device.
22	EN1	Enable input of the first regulator.
23	PG2	Power good open−drain output of the second inside regulator Output logic is pulled to ground when the output is less than desired output voltage. Tie to external pull−up resistor.
24	PG1	Power good open−drain output of the first inside regulator. Output logic is pulled to ground when the output is less than desired output voltage. Tie to external pull−up resistor.
25	A_{VIN}	Input signal supply voltage pin.
26	FB1	Buck first output voltage feedback input. Inverting switch to the error amplifier 1.
27	AGND	Analog ground; connect to GND1 and GND2.
28	COMP1	Compensation pin of the first inside regulator. This is the output of the error amplifier and inverting input of the PWM comparator.
29	SS1	Soft−start control input to the regulator 1. An internal current source charges an external capacitor connected to this pin to set the soft−start time.
30	GND1	Power ground for first output.
	Exposed Pad (GND)	The exposed pad at the bottom of the package is the electrical ground connection of the NCP3121. This node must be tied to ground!!!

MAXIMUM RATINGS

Characteristics	Symbol	Min	Max	Unit
Power Supply Voltage Input	V_{VIN}	−0.3	15	V
Signal Supply Voltage Input	V_{AVIN}	−0.3	15	V
SW Pin Voltage	V_{SW}	−0.7 −5V for < 50 nsec	V_{VIN}	V
SW Pin Source Current (V_{VIN} to SW)	I_{SW}		Internally Limited	A
EN Pin Voltage Input (Note 1)	V_{EN}	−0.3	8.0	V
SEQ Pin Voltage Output (Note 1)	V_{SEQ}		8.0	
PGOOD Pin Voltage	V_{PG}	−0.3	5.5	V
PGOOD Pin Current	I_{PG}		10	mA
All Other Pins	−	−0.3	5.5	°V
Thermal Resistance, Junction−to−Ambient (Notes 2, 3)	Rthja	50		°C/W
Thermal Resistance, Junction−to−Case (Notes 2, 3)	Rthjc	TBD		°C/W
Operating Ambient Temperature Range	T_A	−40 to +85		°C
Storage Temperature Range	T_{STG}	−55 to +150		°C
Junction Operating Temperature	T_J	−40 to +150		°C
ESD Withstand Voltage (Note 4) Human Body Model Machine Model	Vesd	 2.0 200		 kV V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The bias current above this voltage will increase current value to about 1 mA.Therefore, it is strongly recommended to retain the max ratings values.
2. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = 25°C.
3. According JEDEC standard JESD22−A108B.
4. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) +/−2.0 kV per JEDEC standard: JESD22−A114.
   Machine Model (MM) +/−200V per JEDEC standard: JESD22−A115.
5. Latchup current maximum rating: +/−100 mA per JEDEC standard: JESD78.
6. The maximum package power dissipation limit must not be exceeded

$$P_D = \frac{T_{J\ (max)} - T_A}{R_{\theta JA}}$$

ELECTRICAL CHARACTERISTICS (−40°C < T_J < 125°C (Note 7), T_J = 25°C for typical values, V_{AVIN} =12 V, V_{VIN} =12 V, unless otherwise noted.) R_T = open kΩ

Characteristic	Conditions	Min	Typ	Max	Unit
RECOMMENDED OPERATING CONDITIONS					
Input Voltage Range		4.5		13.2	V
SUPPLY CURRENT					
Quiescent Supply Current	V_{EN} = H, V_{FB} = 1.0 V No Switching	−	5.0	7.0	mA
Shutdown Supply Current	V_{EN} = 0 V			100	μA
UNDERVOLTAGE LOCKOUT					
UVLO Threshold	V_{IN} Rising Edge V_{IN} Falling Edge	 3.9	4.3 4.1	4.5	V
UVLO Hysteresis		0.15	0.20	0.25	V
SWITCHING REGULATOR					
Minimum Switch On−Time	Comp = TBD			20	ns
Minimum Duty Cycle	Comp = 0.6 V	−	−	0	%
Maximum Duty Cycle	Comp = 2.6 V	90			%
High Side MOSFET $R_{DS(on)}$	V_{IN} = 5 V, A_{VIN} = 5 V, I_{SW} = 0.5 A, T_J = 25°C	TBD	250	TBD	mΩ
High Side Leakage Current	V_{EN} = 0V, V_{SW} = 0V			10	μA
High Side Switch Current Limit Set Point		3.6	4.2	4.8	A
Current Loop Transient Response	(Note 7)		100		nsec
FB					
V_{FB} Feedback Voltage	T_J = 25°C T_J = −40 to 125°C 4.5 V < V_{IN} < 13.2V	 0.788 0.784	0.8 −	 0.812 0.816	V
OSC					
Oscillator Frequency	T_J = 25°C, T_J = −40 to 125°C T_J = 25°C, T_J = −40 to 125°C	180 TBD −15%	200 TBD 750	220 TBD +15%	kHz kHz kHz
Oscillator Typical Frequency Range	T_J = 25°C	200		750	kHz
ERROR AMPLIFIER (GM)					
Transconductance	(Note 7)	0.9	1.0	1.1	ms
DC Gain	(Note 7)	50	55	60	dB
Unity Gain Bandwidth	(Note 7)		4.0	−	MHz
Output Sink Current	V_{FB} = 1.0 V, Vcomp = 1.5 V	80	120		μA
Output Source Current	V_{FB} = 0.6V, Vcomp = 1.5V	80	120		μA
Input Bias Current	V_{FB} = 0.8 V	−	0.1	1.0	μA
Comp Pin Operating Voltage Range	(Note 7)	0.6		2.6	V
SOFT−START					
Soft−Start Period	V_{FB} < 0.8 V, C_S = 0.1 μF		10		ms
Soft−Start Voltage Range		0		V_{FB}	V
Soft−Start Current Source	Charging, V_{SS} = 1 V Discharging, V_{SS} = 1 V	8.5 8.5	10 10	11.5 11.5	μA μA

7. Guaranteed by design.
8. Power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (−40°C < T_J < 125°C (Note 7), T_J = 25°C for typical values, V_{AVIN} =12 V, V_{VIN} =12 V, unless otherwise noted.) R_T = open kΩ

Characteristic	Conditions	Min	Typ	Max	Unit
TRACK					
Tracking Voltage Range		0		V_{FB}	V
Tracking Voltage Offset	V_{TRACk} = 0.4 V			15	mV
Track Bias Current	V_{TRACk} = 0.4 V		500	1000	nA
POWER GOOD					
PG Threshold	Feedback Voltage Rising, EN Tied to SEQ, V_{PG} = 3.3 V	90% V_O			V
PG Shutdown Mode	Feedback Voltage Falling, EN Tied to SEQ, $V_{EN,SEQ}$ = 0V, V_{PG} = 3.3V	10% V_O	15% V_O	20% V_O	V
PG Delay	Rising Edge of V_{out} Falling Edge of V_{out}		35 10		μs μs
PG Low Level Voltage	$I_{(PG)}$ = 1 mA			0.3	V
PG Hysteresis			30		mV
PG Leakage Current	V_{PG} = 5.5 V			5.0	μA
ENABLE/POWER SEQUENCING					
Enable Internal Pullup Current			4.0		μA
Sequence Internal Pulldown Current			16		μA
Enable Threshold High	EN Tied to SEQ	2.0			V
Sequence Threshold Low	EN Tied to SEQ			0.8	V
THERMAL SHUTDOWN					
Overtemperature Trip Point	(Note 7)	–	160	–	°C
Hysteresis			15		°C

7. Guaranteed by design.
8. Power dissipation limits must be observed.

Ratio−Metric Sequencing

Both ICs use a single soft−start capacitor to accomplish startup. Since each converter uses the same capacitor voltage ramp to govern the move to regulation, both converters start in unison and will achieve regulation in the same time period. It should be noted that the startup ramp will occur in one half of the specified timing since the soft−start capacitor is fed from two current sources.

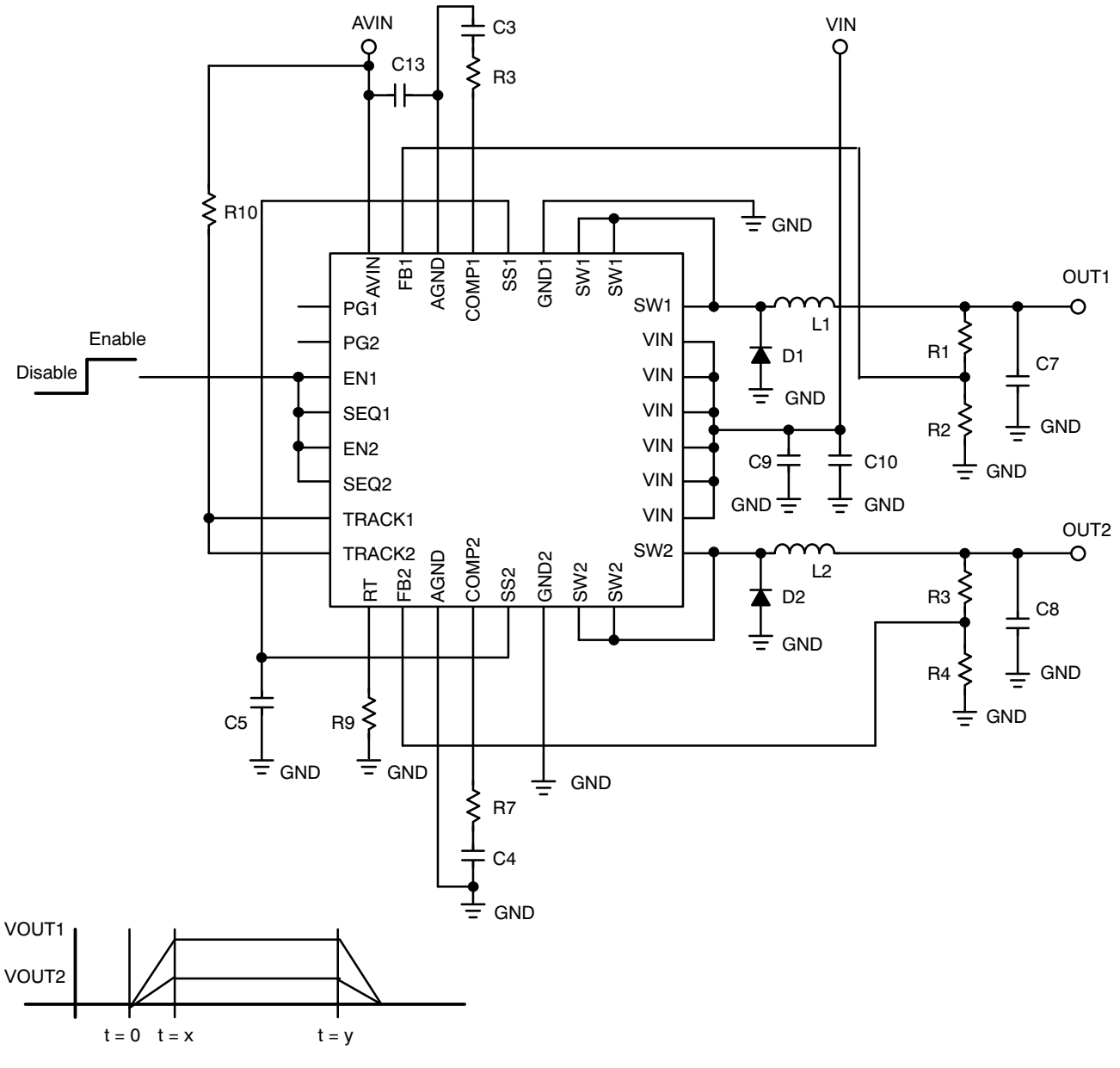


Figure 3. Ratiometric Sequencing
(Independent Slew Rate for Both Outputs So that the Regulation Voltage is Achieved at the Same Time)

Sequential Sequencing

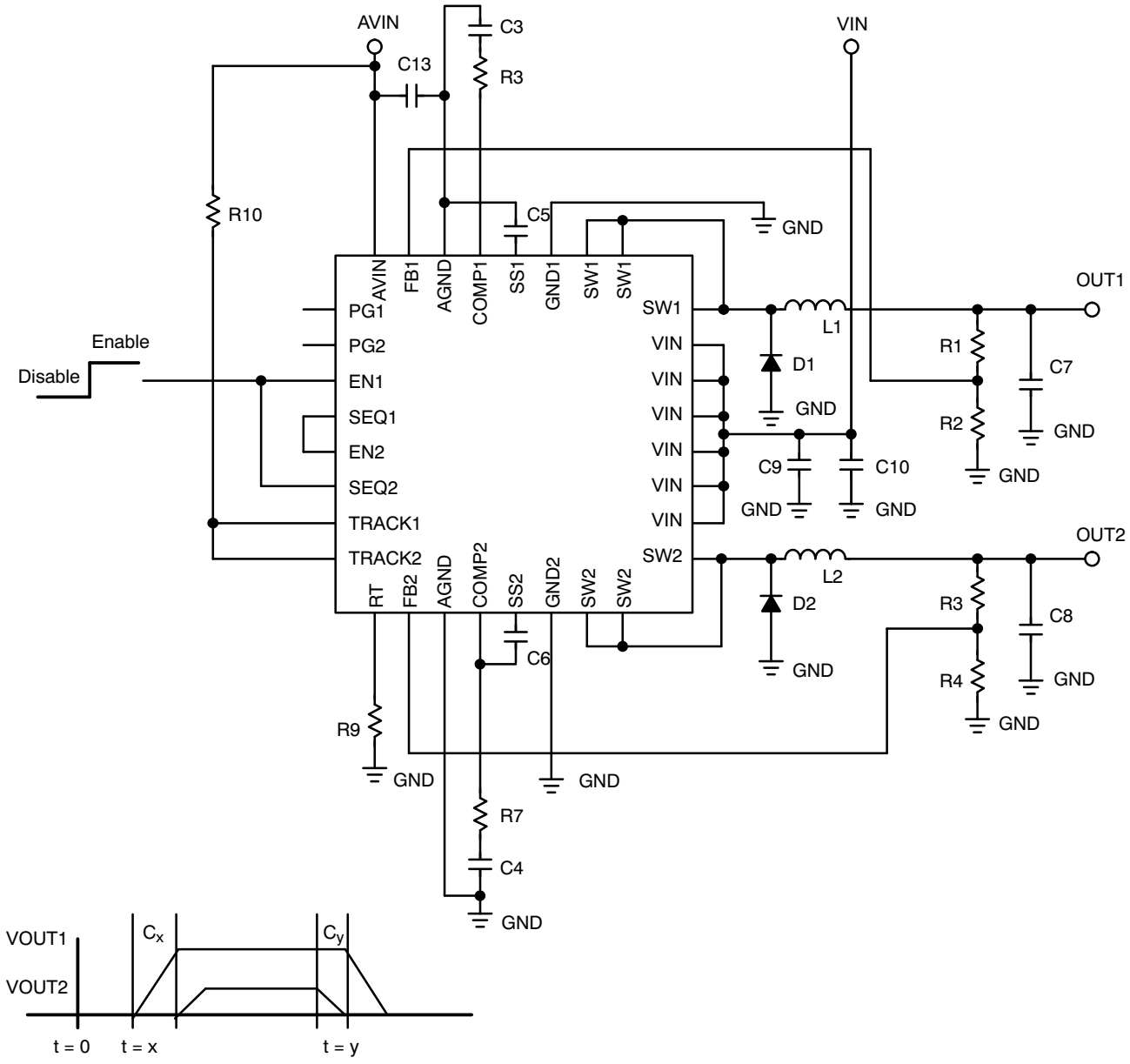


Figure 4. Sequential Sequencing
(Independent Start Time for Both Outputs So that the Second Output Starts after the First Output Reaches) Regulation

Sequential

In this startup sequence, the EN and SEQ is used to daisy chain the startup sequence as shown below:

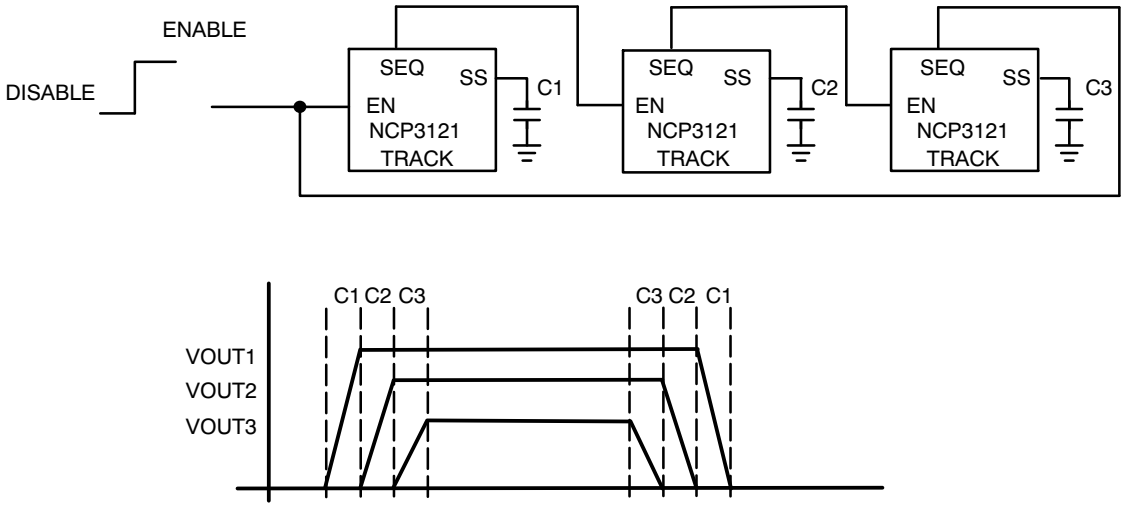


Figure 5. Simplified Drawing of Daisy−Chained NCP3121's

Although the NCP3121 has only two outputs, multiple devices can be daisy chained to control additional outputs.

The last up first down power output has it's SEQ pin tied to the EN of the first up last down power output. Each output in the chain has its powerup delay set by the soft−start ramp up of the supply that feeds its EN and its power down delay set by the soft−start ramp down of the supply that feeds its SEQ pin.

Tracking

The output voltage during tracking can be calculated with the following equation:

$$V_{OUT} = V_{TRACK} = \left(1 + \frac{R5}{R6}\right) \qquad V_{TRACK} < 0.8\ V$$

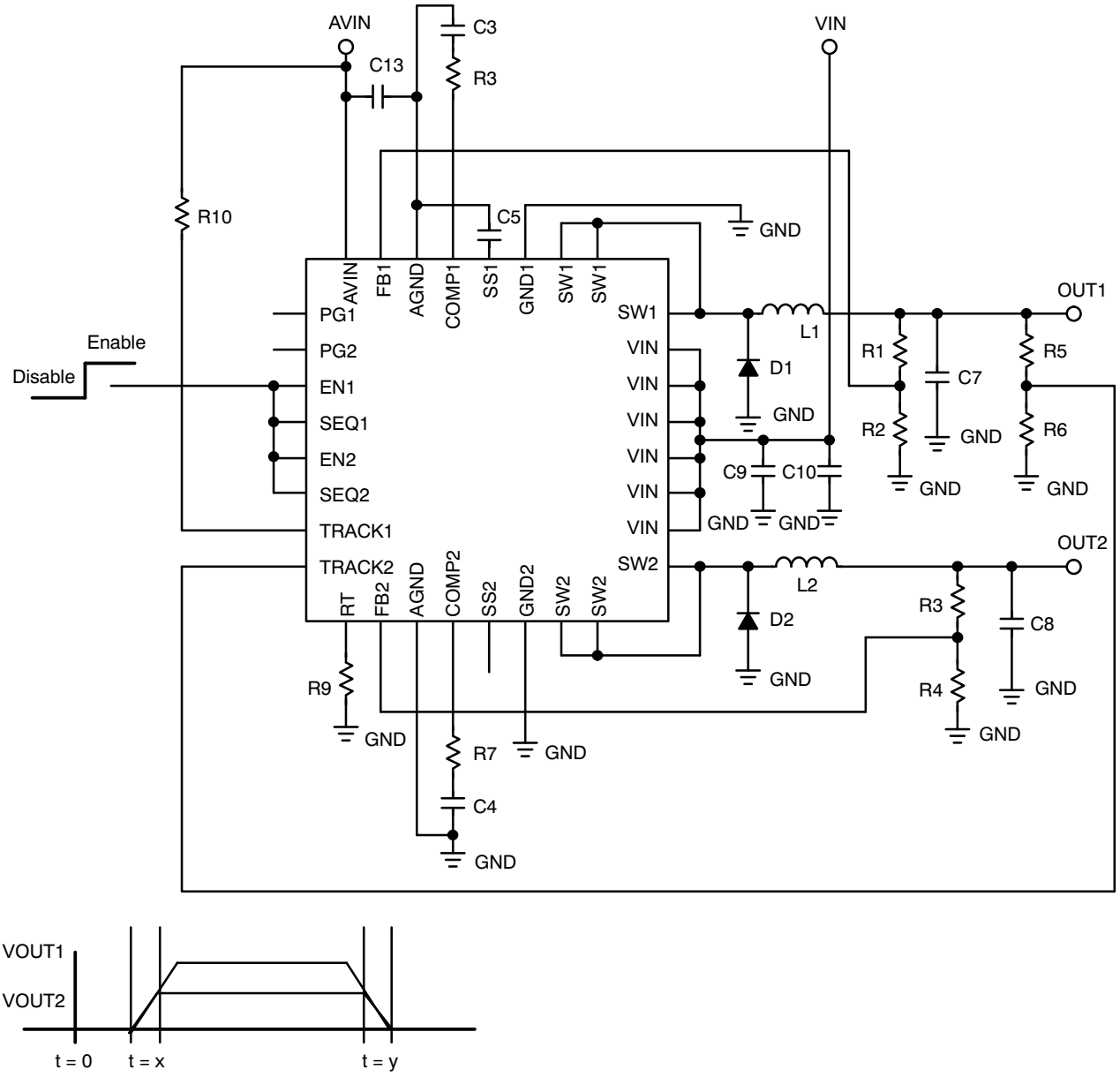
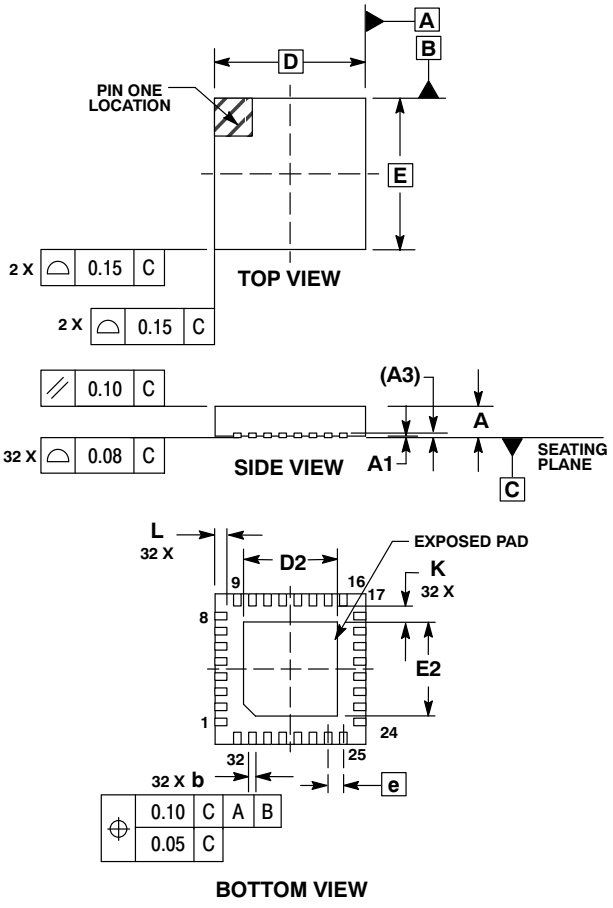


Figure 6. Tracking (Matched Slew Rate for Both Outputs so that Outputs Rise and Fall at the Same Rate)

PACKAGE DIMENSIONS

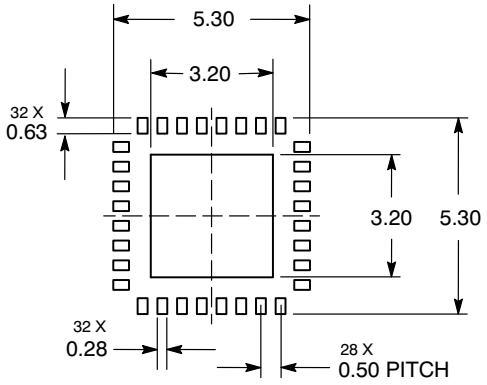
QFN32 5x5, 0.5 P
CASE 488AM−01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.800	0.900	1.000
A1	0.000	0.025	0.050
A3		0.200 REF	
b	0.180	0.250	0.300
D		5.00 BSC	
D2	2.950	3.100	3.250
E		5.00 BSC	
E2	2.950	3.100	3.250
e		0.500 BSC	
K	0.200	---	---
L	0.300	0.400	0.500

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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