# AN2450
# Application note

## LLC resonant half-bridge converter design guideline

## Introduction

The growing popularity of the LLC resonant converter in its half-bridge implementation (see *Figure 1*) is due to its high efficiency, low level of EMI emissions, and its ability to achieve high power density. Such features perfectly fit the power supply demand of many modern applications such as LCD and PDP TV or 80+ initiative compliant ATX silver box. One of the major difficulties that engineers are facing with this topology is the lack of information concerning the way the converter operates and, therefore, the way to design it in order to optimize its features.

The purpose of this application note is to provide a detailed quantitative analysis of the steady-state operation of the topology that can be easily translated into a design procedure.

Exact analysis of LLC resonant converters (see [*1.*] ) leads to a complex model that cannot be easily used to derive a handy design procedure. R. Steigerwald (see [*2*]) has described a simplified method, applicable to any resonant topology, based on the assumption that input-to-output power transfer is essentially due to the fundamental Fourier series components of currents and voltages.

This is what is commonly known as the "first harmonic approximation" (FHA) technique, which enables the analysis of resonant converters by means of classical complex ac-circuit analysis. This is the approach that has been used in this paper.

The same methodology has been used by Duerbaum (see [*3*] ) who has highlighted the peculiarities of this topology stemming from its multi-resonant nature. Although it provides an analysis useful to set up a design procedure, the quantitative aspect is not fully complete since some practical design constraints, especially those related to soft-switching, are not addressed. In (see [*4*] ) a design procedure that optimizes transformer's size is given but, again, many other significant aspects of the design are not considered.

The application note starts with a brief summary of the first harmonic approximation approach, giving its limitations and highlighting the aspects it cannot predict. Then, the LLC resonant converter is characterized as a two-port element, considering the input impedance, and the forward transfer characteristic. The analysis of the input impedance is useful to determine a necessary condition for Power MOSFETs' ZVS to occur and allows the designer to predict how conversion efficiency behaves when the load changes from the maximum to the minimum value. The forward transfer characteristic (see *Figure 3*) is of great importance to determine the input-to-output voltage conversion ratio and provides considerable insight into the converter's operation over the entire range of input voltage and output load. In particular, it provides a simple graphical means to find the condition for the converter to regulate the output voltage down to zero load, which is one of the main benefits of the topology as compared to the traditional series resonant converter.

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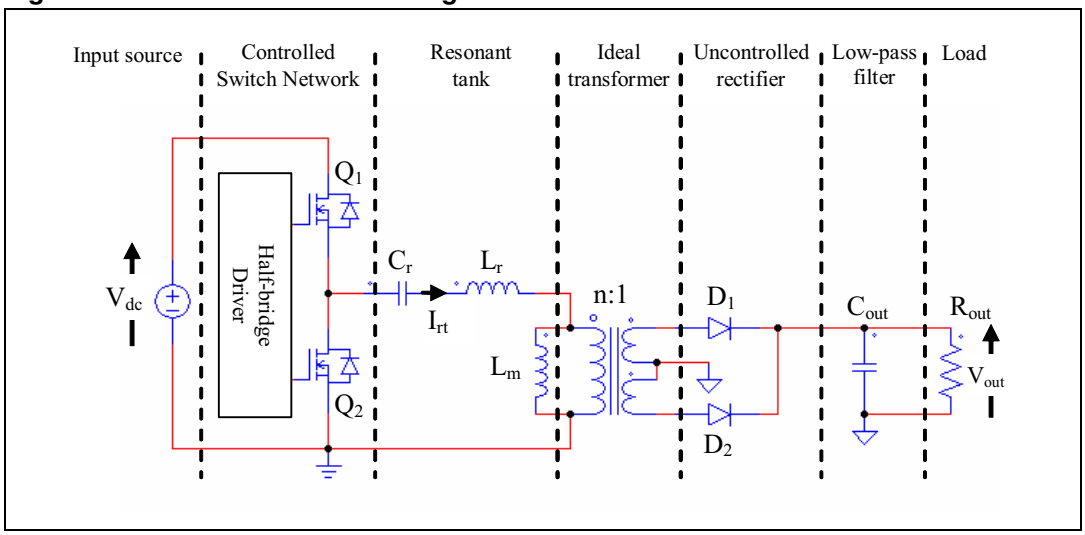
# 1 FHA circuit model

The FHA approach is based on the assumption that the power transfer from the source to the load through the resonant tank is almost completely associated to the fundamental harmonic of the Fourier expansion of the currents and voltages involved. This is consistent with the selective nature of resonant tank circuits.

**Figure 1. LLC resonant half-bridge converter**




The harmonics of the switching frequency are then neglected and the tank waveforms are assumed to be purely sinusoidal at the fundamental frequency: this approach gives quite accurate results for operating points at and above the resonance frequency of the resonant tank (in the continuous conduction mode), while it is less accurate, but still valid, at frequencies below the resonance (in the discontinuous conduction mode).

It is worth pointing out also that many details of circuit operation on a cycle-to-cycle time base will be lost. In particular, FHA provides only a necessary condition for MOSFETs' zero-voltage switching (ZVS) and does not address secondary rectifiers' natural ability to work always in zero-current switching (ZCS). A sufficient condition for Power MOSFETs' ZVS will be determined in *Section 3: ZVS constraints* still in the frame of FHA approach.

Let us consider the simple case of ideal components, both active and passive.

The two Power MOSFETs of the half-bridge in *Figure 1* are driven on and off symmetrically with 50% duty cycle and no overlapping. Therefore the input voltage to the resonant tank $v_{sq}(t)$ is a square waveform of amplitude $V_{dc}$, with an average value of $V_{dc}/2$. In this case the capacitor $C_r$ acts as both resonant and dc blocking capacitor. As a result, the alternate voltage across $C_r$ is superimposed to a dc level equal to $V_{dc}/2$.

The input voltage waveform $v_{sq}(t)$ of the resonant tank in *Figure 1* can be expressed in Fourier series:

**Equation 1**

$$v_{sq}(t) = \frac{V_{dc}}{2} + \frac{2}{\pi}V_{dc} \sum_{n = 1,\ 3,\ 5...} \frac{1}{n}\sin(n2\pi f_{sw}t)$$

whose fundamental component $v_{i.FHA}(t)$ (in phase with the original square waveform) is:

**Equation 2**

$$v_{iFHA}(t) = \frac{2}{\pi} V_{dc} \sin(2\pi f_{sw} t)$$

where fsw is the switching frequency. The rms value $V_{i.FHA}$ of the input voltage fundamental component is:

**Equation 3**

$$v_{i.FHA} = \frac{\sqrt{2}}{\pi} V_{dc}$$

As a consequence of the above mentioned assumptions, the resonant tank current $i_{rt}(t)$ will be also sinusoidal, with a certain rms value $I_{rt}$ and a phase shift $\Phi$ with respect to the fundamental component of the input voltage:

**Equation 4**

$$i_{rt}(t) = \sqrt{2} I_{rt} \sin(2\pi f_{sw} t - \Phi) = \sqrt{2} I_{rt} \cos\Phi \bullet \sin(2\pi f_{sw} t) - \sqrt{2} I_{rt} \sin\Phi \bullet \cos(2\pi f_{sw} t)$$

This current lags or leads the voltage, depending on whether inductive reactance or capacitive reactance dominates in the behavior of the resonant tank in the frequency region of interest. Irrespective of that, $i_{rt}(t)$ can be obtained as the sum of two contributes, the first in phase with the voltage, the second with 90° phase-shift with respect to it.

The dc input current $I_{i.dc}$ from the dc source can also be found as the average value, along a complete switching period, of the sinusoidal tank current flowing during the high side MOSFET conduction time, when the dc input voltage is applied to the resonant tank:

**Equation 5**

$$I_{idc} = \frac{1}{T_{sw}} \int_0^{\frac{T_{sw}}{2}} i_{rt}(t) dt = \frac{\sqrt{2}}{\pi} I_{rt} \cos\Phi$$

where $T_{sw}$ is the time period at switching frequency.

The real power $P_{in}$, drawn from the dc input source (equal to the output power $P_{out}$ in this ideal case) can now be calculated as both the product of the input dc voltage $V_{dc}$ times the average input current $I_{i.dc}$ and the product of the rms values of the voltage and current's first harmonic, times $\cos\Phi$:

**Equation 6**

$$P_{in} = V_{dc} I_{idc} = V_{iFHA} I_{rt} \cos\Phi$$

the two expressions are obviously equivalent.

The expression of the apparent power $P_{app}$ and the reactive power $P_r$ are respectively:

**Equation 7**

$$P_{app} = V_{iFHA} I_{rt} \qquad P_r = V_{iFHA} I_{rt} \sin\Phi$$

Let us consider now the output rectifiers and filter part. In the real circuit, the rectifiers are driven by a quasi-sinusoidal current and the voltage reverses when this current becomes zero; therefore the voltage at the input of the rectifier block is an alternate square wave in phase with the rectifier current of amplitude $V_{out}$.

The expressions of the square wave output voltage $v_{o.sq}(t)$ is:

**Equation 8**

$$V_{osq}(t) = \frac{4}{\pi}V_{out}\sum_{n=1,\ 3,\ 5...}\frac{1}{n}\sin(n2\pi f_{sw}t - \Psi)$$

which has a fundamental component $v_{o.FHA}(t)$:

**Equation 9**

$$V_{o.FHT}(t) = \frac{4}{\pi}V_{out}\sin(2\pi f_{sw}t - \Psi)$$

whose rms amplitude is:

**Equation 10**

$$V_{o.FHA} = \frac{2\sqrt{2}}{\pi}V_{out}$$

where $\Psi$ is the phase shift with respect to the input voltage. The fundamental component of the rectifier current $_{irect}(t)$ will be:

**Equation 11**

$$i_{rect}(t) = \sqrt{2}I_{rect}\sin(2\pi f_{sw}t - \Psi)$$

where $I_{rect}$ is its rms value.

Also in this case we can relate the average output current to the load $I_{out}$ and also derive the ac current $I_{c.ac}$ flowing into the filtering output capacitor:

**Equation 12**

$$I_{out} = \frac{2}{T_{sw}}\int_{0}^{\frac{T_{sw}}{2}}|i_{rect}(t)|dt = \frac{2\sqrt{2}}{\pi}I_{rect} = \frac{P_{out}}{V_{out}} = \frac{V_{out}}{R_{out}}$$

**Equation 13**

$$I_{cac} = \sqrt{I_{rect}^{2} - I_{out}^{2}}$$

where $P_{out}$ is the output power associated to the output load resistance $R_{out}$.

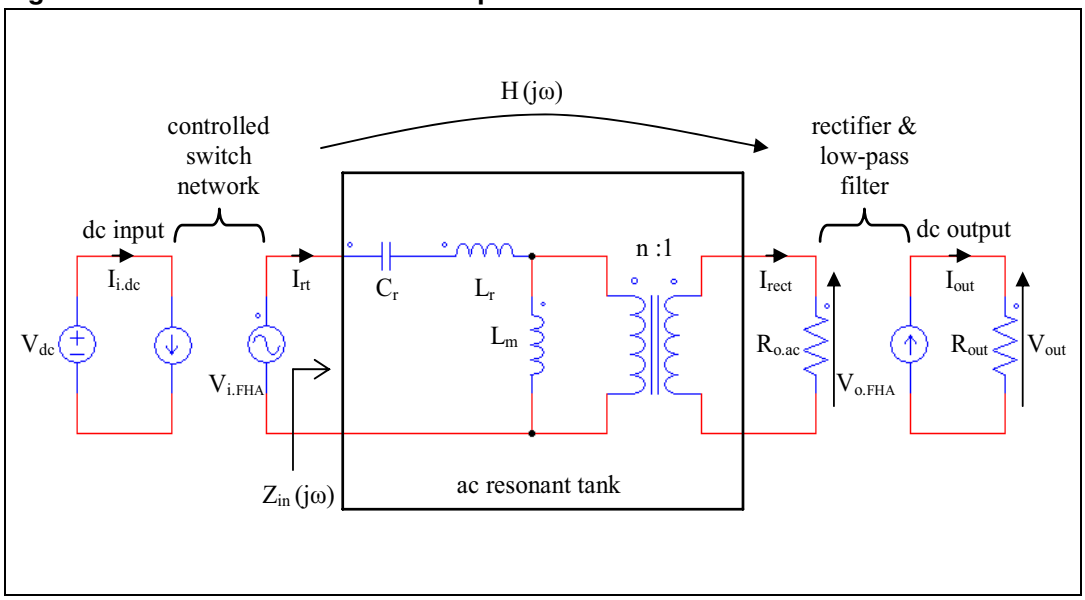
Since $v_{o.FHA}(t)$ and $i_{rect}(t)$ are in phase, the rectifier block presents an effective resistive load to the resonant tank circuit, $R_{o.ac}$, equal to the ratio of the instantaneous voltage and current:

**Equation 14**

$$R_{oac} = \frac{v_{o.FHA}(t)}{i_{rect}(t)} = \frac{V_{o.FHA}}{I_{rect}} = \frac{8}{\pi^2}\frac{V^2_{out}}{P_{out}} = \frac{8}{\pi^2}R_{out}$$

Thus, in the end, we have transformed the non linear circuit of *Figure 1* into the linear circuit of *Figure 2*, where the ac resonant tank is excited by an effective sinusoidal input source and drives an effective resistive load. This transformation allows the use of complex ac-analysis methods to study the circuit and, furthermore, to pass from ac to dc parameters (voltages and currents), since the relationships between them are well-defined and fixed (see equations *Equation 3*, *Equation 5*, *Equation 6*, *Equation 10* and *Equation 12* above).

**Figure 2. FHA resonant circuit two port model**




The ac resonant tank in the two-port model of *Figure 2* can be defined by its forward transfer function H(s) and input impedance $Z_{in}(s)$:

**Equation 15**

$$H(s) = \frac{V_{o.FHA}(s)}{V_{i.FHA}(s)} = \frac{1}{n}\frac{n^2 R_{oac} \,||\, sL_m}{Z_{in}(s)}$$

**Equation 16**

$$Z_{in}(s) = \frac{V_{i.FHA}(s)}{I_{rt}(s)} = \frac{1}{sC_r} + sL_r + n^2 R_{oac} \,||\, sL_m$$

For the discussion that follows it is convenient to define the effective resistive load reflected to the primary side of the transformer $R_{ac}$:

**Equation 17**

$$R_{ac} = n^2 R_{oac}$$

and the so-called "normalized voltage conversion ratio" or "voltage gain" $M(f_{sw})$:

**Equation 18**

$$M(f_{sw}) = n\left\|H(j2\pi f_{sw})\right\| = n\frac{V_{o.FHA}}{V_{i.FHA}}$$

It can be demonstrated (by applying the relationships *Equation 3*, *Equation 10* and *Equation 18* to the circuit in *Figure 2*) that the input-to-output dc-dc voltage conversion ratio is equal to:

**Equation 19**

$$\frac{V_{out}}{V_{dc}} = \frac{1}{2n}M(f_{sw})$$

In other words, the voltage conversion ratio is equal to one half the module of resonant tank's forward transfer function evaluated at the switching frequency.

# 2 Voltage gain and input impedance

Starting from *Equation 18* we can obtain the expression of the voltage gain:

**Equation 20**

$$M(f_n,\ \lambda,\ Q) = \frac{1}{\sqrt{\left(1+\lambda-\frac{\lambda}{f_n^2}\right)^2 + Q^2\left(f_n-\frac{1}{f_n}\right)^2}}$$

with the following parameter definitions:

resonance frequency: $f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$

characteristic impedance: $Z_o = \sqrt{\frac{L_r}{C_r}} = 2\pi f_r L_r = \frac{1}{2\pi f_r C_r}$

quality factor: $Q = \frac{Z_o}{R_{ac}} = \frac{Z_o}{n^2 R_{oac}} = \frac{\pi^2}{8}\frac{Z_0}{n^2}\frac{P_{out}}{V^2_{out}}$

inductance ratio: $\lambda = \frac{L_r}{L_m}$

normalized frequency: $f_n = \frac{f_{sw}}{f_r}$

Under no-load conditions, (i.e. Q = 0) the voltage gain assumes the following form:

**Equation 21**

$$M_{OL}(f_n,\ \lambda) = \frac{1}{\left|1+\lambda-\frac{\lambda}{f_n^2}\right|}$$

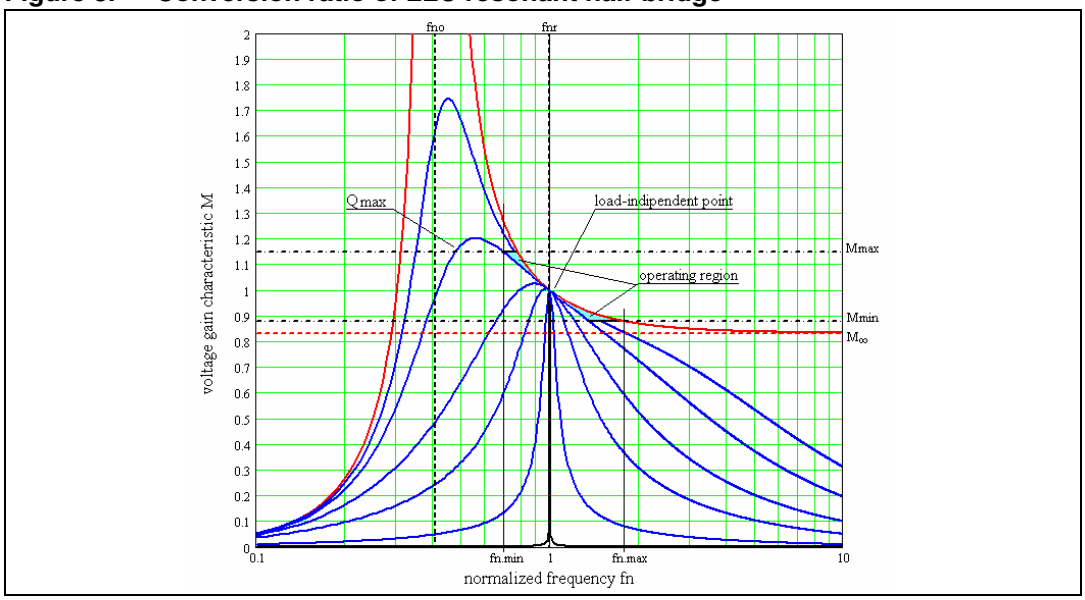
*Figure 3* shows a family of plots of the voltage gain versus normalized frequency. For different values of Q, with $\lambda = 0.2$, it is clearly visible that the LLC resonant converter presents a load-independent operating point at the resonance frequency $f_r$ ($f_n = 1$), with unity gain, where all the curves are tangent (and the tangent line has a slope $-2\lambda$). Fortunately, this load-independent point occurs in the inductive region of the voltage gain characteristic, where the resonant tank current lags the input voltage square waveform (which is a necessary condition for ZVS behavior).

The regulation of the converter output voltage is achieved by changing the switching frequency of the square waveform at the input of the resonant tank: since the working region is in the inductive part of the voltage gain characteristic, the frequency control circuit that keeps the output voltage regulated acts by increasing the frequency in response to a decrease of the output power demand or to an increase of the input dc voltage. Considering this, the output voltage can be regulated against wide loads variations with a relatively narrow switching frequency change, if the converter is operated close to the load-independent point. Looking at the curves in *Figure 3*, it is obvious that the wider the input dc

voltage range is, the wider the operating frequency range will be, in which case it is difficult to optimize the circuit. This is one of the main drawbacks common to all resonant topologies.

This is not the case, however, when there is a PFC pre-regulator in front of the LLC converter, even with a universal input mains voltage (85 $V_{ac}$ - 264 $V_{ac}$). In this case, in fact, the input voltage of the resonant converter is a regulated high voltage bus of ~400 $V_{dc}$ nominal, with narrow variations in normal operation, while the minimum and maximum operating voltages will depend, respectively, on the PFC pre-regulator hold-up capability during mains dips and on the threshold level of its over voltage protection circuit (about 10-15% over the nominal value). Therefore, the resonant converter can be optimized to operate at the load-independent point when the input voltage is at nominal value, leaving to the step-up capability of the resonant tank (i.e. operation below resonance) the handling of the minimum input voltage during mains dips.

**Figure 3. Conversion ratio of LLC resonant half-bridge**




The red curve in *Figure 3* represents the no-load voltage gain curve $M_{OL}$; for normalized frequency going to infinity, it tends to an asymptotic value $M_\infty$:

**Equation 22**

$$M_\infty = M_{OL}(f_n \to \infty;\ \lambda) = \frac{1}{1+\lambda}$$

Moreover, a second resonance frequency $f_o$ can be found, which refers to the no-load condition or when the secondary side diodes are not conducting (i.e. the condition where the total primary inductance $L_r + L_m$ resonates with the capacitor $C_r$); $f_o$is defined as:

**Equation 23**

$$f_o = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}} = f_r\sqrt{\frac{\lambda}{1+\lambda}}$$

or in normalized form:

**Equation 24**

$$f_{no} = \frac{f_o}{f_r} = \sqrt{\frac{\lambda}{1+\lambda}}$$

At this frequency the no-load gain curve $M_{OL}$ tends to infinity.

By imposing that the minimum required gain $M_{min}$ (at max. input dc voltage) is greater than the asymptotic value $M_{\infty}$ it is possible to ensure that the converter can work down to no-load at a finite operating frequency (which will be the maximum operating frequency of the converter):

**Equation 25**

$$M_{min} = 2n\frac{V_{out}}{V_{dc.max}} > \frac{1}{1+\lambda}$$

The maximum required gain $M_{max}$ (at min. input dc voltage) at max. output load (max. $P_{out}$), that is at max. Q, will define the min. operating frequency of the converter:

**Equation 26**

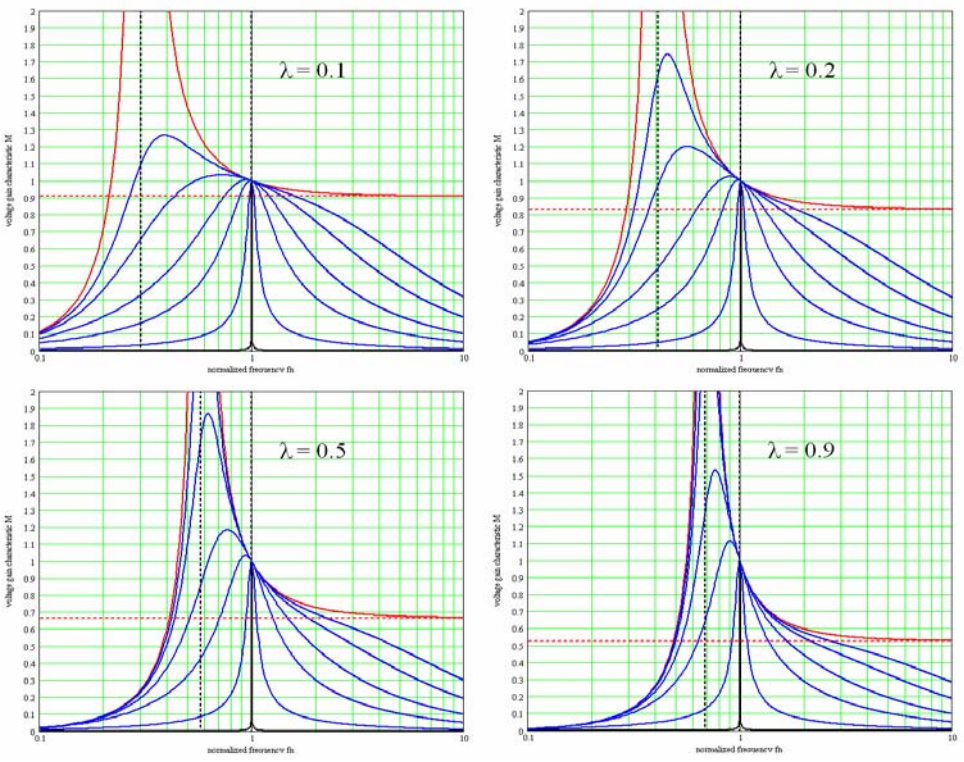
$$M_{max} = 2n\frac{V_{out}}{V_{dc.min}}$$

Given the input voltage range ($V_{dc.min}$ - $V_{dc.max}$), three types of operations are possible:

- always below resonance frequency (step-up operations)
- always above resonance frequency (step-down operations)
- across the resonance frequency (shown in *Figure 3*).

Looking at *Figure 4*, we can see that an increase of the inductance ratio value $\lambda$ has the effect of shrinking the gain curves in the M - $f_n$ plane toward the resonance frequency $f_{nr}$ (which means the no-load resonance frequency $f_{no}$ increases) and contemporaneously reduces the asymptotic level $M_{\infty}$ of the no-load gain characteristic. At the same time the peak gain of each curve increases.

**Figure 4. Shrinking effect of λ value increase**




Starting from *Equation 16* we can obtain the expression of the normalized input impedance $Z_n$ of the resonant tank:

**Equation 27**

$$Z_n(f_n,\ \lambda,\ Q) = \frac{Z_{in}(f_n,\ \lambda,\ Q)}{Z_o} = \frac{jf_n}{\lambda + jf_nQ} + \frac{1 - f_n^2}{jf_n}$$

whose magnitude is plotted in *Figure 5*, at different Q values, with λ = 0.2.

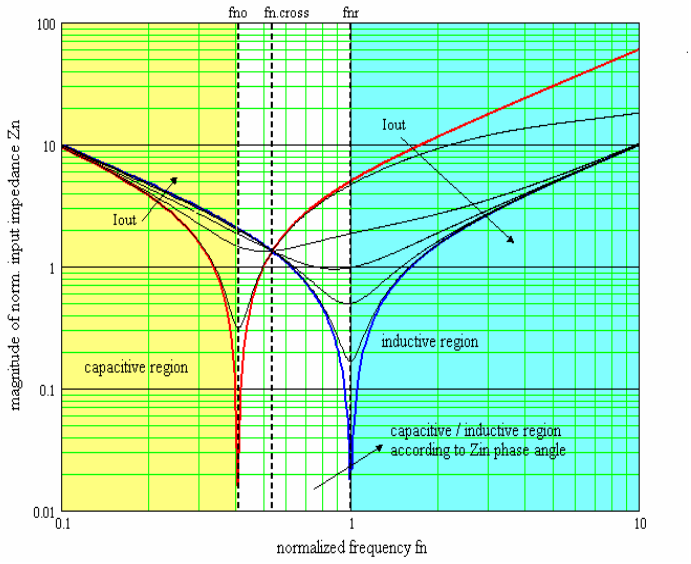
The red and blue curves in the above mentioned figure represent the no-load and short circuit cases respectively, and are characterized by asymptotes at the two normalized resonance frequencies $f_{no}$ and $f_{nr}$ (= 1). All the curves at different values of Q intercept at normalized frequency $f_{n.cross}$:

**Equation 28**

$$f_{n.cross} = \sqrt{\frac{2\lambda}{1 + 2\lambda}}$$

At frequencies higher than the crossing frequency $f_{n.cross}$, the input impedance behaves such that at increasing output current Iout (that is at increasing $P_{out}$ and Q) it decreases (coherently to the load resistance); the opposite happens at frequencies lower than $f_{n.cross}$, where the input impedance increases, while the output load resistance decreases.

**Figure 5. Normalized input impedance magnitude**




The ac analysis can also help to estimate converter's efficiency η and predict how this changes with the load. Considering the generic model similar to the one in *Figure 2*, where the resonant tank includes also the dissipative elements (i.e. series resistors for magnetic components winding losses and capacitor's ESR, and parallel resistors for magnetic losses of inductors and transformer), we can compute the transfer function $H_{LOSS}(j\omega)$ and the input impedance $Z_{in.LOSS}(j\omega)$. By calculating input and output power in terms of $H_{LOSS}$ and $Z_{in.LOSS}$, we get:

**Equation 29**

$$\eta = \frac{P_{out}}{P_{in}} = \frac{\|H_{LOSS}(j\omega)\|^2}{R_{o.ac}\,Re[Y_{in.LOSS}(j\omega)]}$$

where $Y_{in.LOSS}$ is the admittance (reciprocal of $Z_{in.LOSS}$) and the input and output power are expressed as:

**Equation 30**

$$P_{in} = V_{i.FHA} I_{rt} \cos\Phi = V_{i.FHA}^2 Re\left[\frac{1}{Z_{in.LOSS}(j\omega)}\right]$$

**Equation 31**

$$P_{out} = V_{o.FHA} I_{rect} = \frac{V_{o.FHA}^2}{R_{o.ac}} = \frac{V_{i.FHA}^2}{R_{o.ac}} \|H_{LOSS}(j\omega)\|$$

The region on the left-hand side of the diagram in *Figure 5*, i.e. for a normalized frequency lower than $f_{no}$, is the capacitive region, where the tank current leads the half-bridge square voltage; at normalized frequency higher than the resonance frequency $f_{nr}$ (= 1), on the right-hand side region, the input impedance is inductive, and the resonant tank current lags the input voltage. In the region between the two resonance frequencies the impedance can be either capacitive or inductive, depending on the value of the impedance phase angle.

By imposing that the imaginary part of $Z_n(f_n, \lambda, Q)$ is zero (which means imposing that $Z_{in}$ has zero phase angle, as $Z_o$ is real and does not affect the phase), we can find the

boundary condition between capacitive and inductive mode operation of the LLC resonant converter.

The analytical results are the following:

**Equation 32**

$$f_{nZ}(\lambda,\ Q) = \sqrt{\frac{Q^2 - \lambda(1+\lambda) + \sqrt{[Q^2 - \lambda(1+\lambda)]^2 + 4Q^2\lambda^2}}{2Q^2}}$$

**Equation 33**

$$Q_Z(f_n,\ \lambda) = \sqrt{\frac{\lambda}{1 - f_n^{\ 2}} - \left(\frac{\lambda}{f_n}\right)^2}$$

where $f_{nZ}$ represents the normalized frequency where, for a fixed couple ($\lambda$- Q), the input resonant tank impedance is real (and only real power is absorbed from the source); while $Q_Z$ is the maximum value of the quality factor, below which, at a fixed normalized frequency and inductance ratio ($f_n$ - $\lambda$) the tank impedance is inductive; hence, the maximum voltage gain available in that condition is also found:

**Equation 34**

$$M_{MAX}(\lambda,\ Q) = M(f_{nZ}(\lambda,\ Q),\ \lambda,\ Q)$$

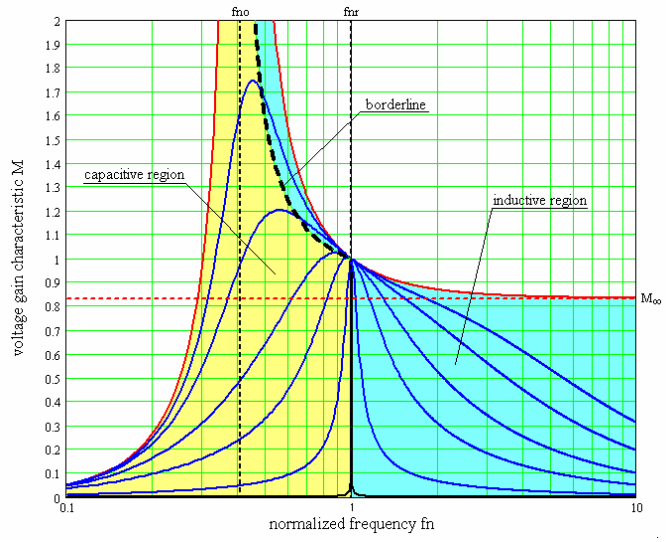
By plotting the locus of operating points [$M_{MAX}(\lambda, Q)$, $f_{nZ}(\lambda,Q)$], whose equation on M - $f_n$ plane is the following:

**Equation 35**

$$M_Z(f_n,\ \lambda) = \frac{f_n}{\sqrt{f_n^{\ 2}(1+\lambda) - \lambda}}$$

we can draw the borderline between capacitive and inductive mode in the region between the two resonance frequencies, shown in *Figure 6* It is also evident that the peak value of the gain characteristics for a given quality factor Q value, already lies in the capacitive region.

**Figure 6. Capacitive and inductive regions in M - $f_n$ plane**



Moreover, by equating the second term of (*Equation 35*) to the maximum required gain $M_{max}$ (at minimum input voltage), and solving for $f_n$, we get the minimum operating frequency $f_{n.min}$ which allows the required maximum voltage gain at the boundary between capacitive and inductive mode:

**Equation 36**

$$f_{n.min} = \sqrt{\frac{1}{1+\frac{1}{\lambda}\left(1-\frac{1}{M_{max}^{2}}\right)}}$$

Furthermore, by substituting the minimum frequency (*Equation 36*) into the *Equation 33*, we get the maximum quality factor $Q_{max}$ which allows the required maximum voltage gain at the boundary between capacitive and inductive mode:

**Equation 37**

$$Q_{max} = \frac{\lambda}{M_{max}}\sqrt{\frac{1}{\lambda}+\frac{M_{max}^{2}}{M_{max}^{2}-1}}$$

Finally, by equating the second term of the no-load transfer function (*Equation 21*) to the minimum required voltage gain $M_{min}$, it is possible to find the expression of the maximum normalized frequency $f_{n.max}$:

**Equation 38**

$$f_{n.max} = \sqrt{\frac{1}{1+\frac{1}{\lambda}\left(1-\frac{1}{M_{min}}\right)}}$$

# 3 ZVS constraints

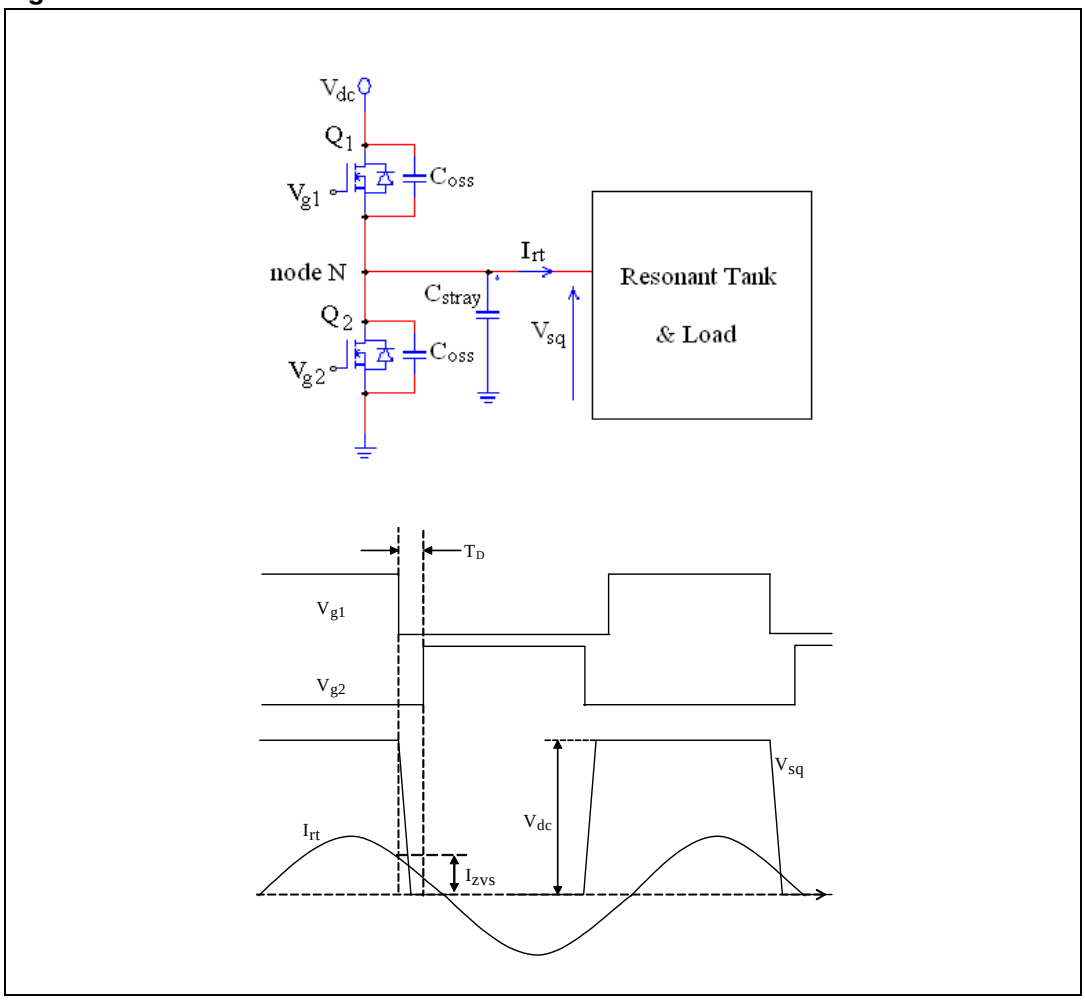
The assumption that the working region lies inside the inductive region of operation is only a necessary condition for the ZVS of the half bridge MOSFETs, but not sufficient; this is because the parasitic capacitance of the half bridge midpoint, neglected in the FHA analysis, needs energy to be charged and depleted during transitions. In order to understand ZVS behavior, refer to the half bridge circuit in *Figure 7*, where the capacitors $C_{oss}$ and $C_{stray}$ are, respectively, the effective drain-source capacitance of the Power MOSFETs and the total stray capacitance present across the resonant tank impedance, so that the total capacitance $C_{zvs}$ at node N is:

**Equation 39**

$$C_{zvs} = 2C_{OSS} + C_{stray}$$

which, during transitions, swings by $\Delta V = V_{dc}$. To allow ZVS, the MOSFET driving circuit is such that a dead time $T_D$ is inserted between the end of the ON-time of either MOSFET and the beginning of the ON-time of the other one, so that both are not conducting during $T_D$.

**Figure 7. Circuit behavior at ZVS transition**




Due to the phase lag of the input current with respect to the input voltage, at the end of the first half cycle the inductor current $I_{rt}$ is still flowing into the circuit and, therefore it can deplete $C_{ZVS}$ so that its voltage swings from $\Delta V$ to zero (it will be vice versa during the second half cycle).

In order to guarantee ZVS, the tank current at the end of the first half cycle (considering the dead time negligible as compared to the switching period, so that the current change is negligible as well) must exceed the minimum value necessary to deplete $C_{ZVS}$ within the dead time interval $T_D$, which means:

**Equation 40**

$$I_{zvs} = i_{rt}\left(\frac{T_{sw}}{2}\right) = C_{zvs}\frac{\Delta V}{T_D} = (2C_{OSS} + C_{stray})\frac{V_{dc}}{T_D}$$

This current equals, of course, the peak value of the reactive current flowing through the resonant tank (it is 90° out-of-phase); the one that determines the reactive power level into the circuit:

**Equation 41**

$$I_{zvs} = \sqrt{2} I_{rt} \sin\Phi$$

Moreover, as the rms component of the tank current associated to the active power is:

**Equation 42**

$$I_{act} = I_{rt}\cos\Phi = \frac{P_{in}}{V_{iFHA}}$$

we can derive also the rms value of the resonant tank current and the phase lag $\Phi$ between input voltage and current (that is the input impedance phase angle at that operating point):

**Equation 43**

$$I_{rt} = \sqrt{I_{rt}^2\cos(\Phi)^2 + I_{rt}^2\sin(\Phi)^2} = \sqrt{\left(\frac{P_{in}}{V_{iFHA}}\right)^2 + \frac{I_{zvs}^2}{2}}$$

**Equation 44**

$$\Phi = a\cos\left(\frac{P_{in}}{V_{iFHA}I_{rt}}\right)$$

Thus we can write the following analytic expression:

**Equation 45**

$$\tan(\Phi) = \frac{\mathrm{Im}[Z_n(f_n, \lambda, Q)]}{\mathrm{Re}[Z_n(f_n, \lambda, Q)]} \geq \frac{C_{zvs}V_{dc}^2}{\pi T_D P_{in}}$$

which is the sufficient condition for ZVS of the half-bridge Power MOSFETs, to be applied to the whole operating range. The solution of *Equation 45* for the quality factor $Q_{zvs}$ that ensures ZVS behavior at full load and minimum input voltage is not convenient. Therefore, we can calculate the $Q_{max}$ value (at max. output power and min. input voltage), where the input impedance has zero phase, and take some margin (5% - 10%) by choosing:

**Equation 46**

$$Q_{zvs.1} = 90\% \div 95\% \bullet Q_{max}$$

and check that the condition (*Equation 45*) is satisfied at the end of the process, once the resonant tank has been completely defined. The process will be iterated if necessary.

Of course the sufficient condition for ZVS needs to be satisfied also at no-load and maximum input voltage; in this operating condition it is still possible to find an additional constraint on the maximum quality factor at full load to guarantee ZVS. In fact the input impedance at no-load $Z_{in.OL}$ has the following expression:

**Equation 47**

$$Z_{inOL}(f_n) = jZ_o\left[f_n\left(1 + \frac{1}{\lambda}\right) - \frac{1}{f_n}\right]$$

Taking into account that:

**Equation 48**

$$Z_o = R_{ac}Q$$

and writing the sufficient condition for ZVS in this operating condition, that is:

**Equation 49**

$$\frac{V_{iFHAmax}}{\left\|Z_{inOL}(f_{nmax})\right\|} \geq \frac{I_{zvs(Vdcmax)}}{\sqrt{2}}$$

we get the constraint on the quality factor for the ZVS at no-load and maximum input voltage:

**Equation 50**

$$Q_{zvs2} \leq \frac{2}{\pi} \frac{\lambda f_{n.max}}{(\lambda + 1) f_{n.max}^{2} - \lambda} \frac{T_D}{R_{ac} C_{zvs}}$$

Therefore, in order to guarantee ZVS over the whole operating range of the resonant converter, we have to choose a maximum quality factor value lower than the smaller of $Q_{zvs.1}$ and $Q_{zvs.2}$.

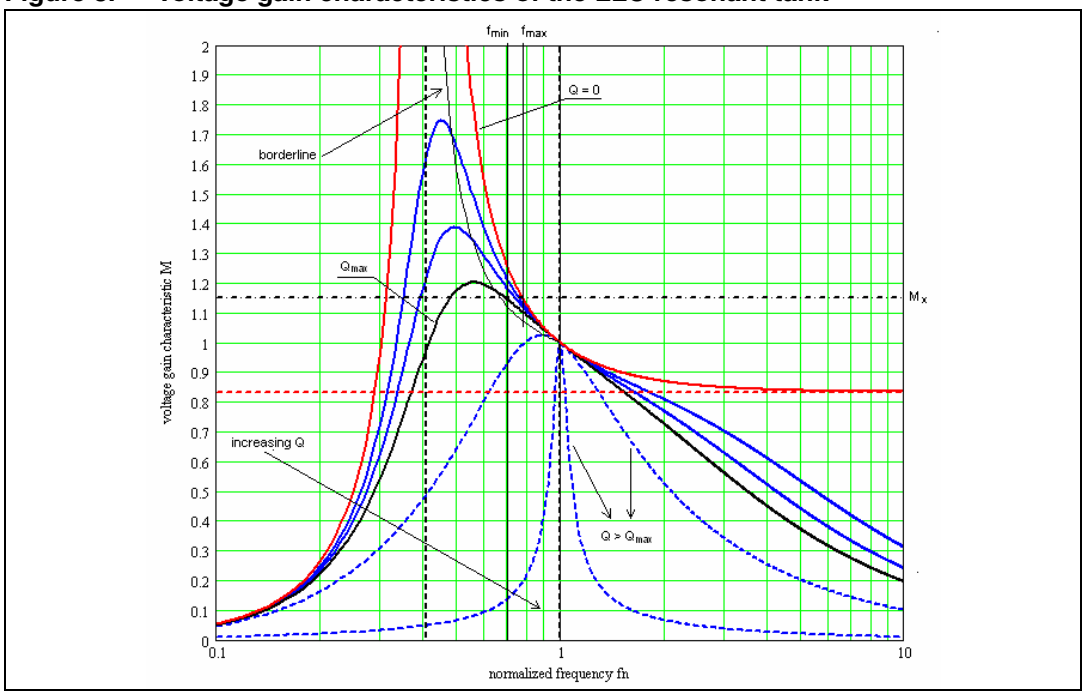
# 4 Operation under overload and short-circuit condition

An important aspect to analyze is the converter's behavior during output over-load and/or short-circuit.

Referring to the voltage gain characteristics in *Figure 8*, let us suppose that the resonant tank has been designed to operate in the inductive region for a maximum output power $P_{out.max}$ (corresponding to the curve $Q = Q_{max}$) at a given output-to-input voltage ratio (corresponding to the horizontal line $M = M_x$) greater than 1,

When the output power is increased from zero to the maximum value, the gain characteristic relative to each power level changes progressively from the red curve (Q = 0) to the black one ($Q_{max}$). The control loop keeps the value of M equal to $M_x$, then the quiescent point moves along the horizontal line $M = M_x$ and the operating frequency at each load condition is given by the abscissa of the crossover between the horizontal line $M = M_x$ and the voltage gain characteristic relevant to the associated value of Q.

**Figure 8. Voltage gain characteristics of the LLC resonant tank**



If the load is increased over the maximum specified (associated to the curve Q = $Q_{max}$) eventually the converter's operating point will invariably enter the capacitive region, where hard switching of power MOSFETs may cause device failures, if no corrective action is taken.

In fact, for values of Q sufficiently greater than $Q_{max}$ the intersection with the M = $M_x$ line will take place on the left-hand side of the borderline curve and, then, in the capacitive region; moreover, if Q exceeds the value corresponding to the characteristic curve tangent to M = $M_x$ there will no longer be a possible operating point with M=$M_x$. This means that the converter will no longer be able to keep the output voltage regulated and the output voltage will fall despite the reduction of the operating frequency (feedback reversal).

Limiting the minimum operating frequency (e.g. at the frequency value corresponding to the intersection of M=$M_x$ with Q=$Q_{max}$) is not enough to prevent the converter from entering the capacitive region of operation. In fact, as the minimum frequency is reached, from that point onwards a further load increase will make the operating point move along the vertical line f=$f_{min}$ and eventually cross the borderline.

Limiting the minimum operating frequency is effective in preventing capacitive mode operation only if the minimum (normalized) frequency value is greater than 1. This suggests that, in response to an overload / short circuit condition at the output, the converter operating frequency must be pushed above the resonance frequency (it is better if well above it) in order to decrease power throughput.

It is worth noticing that, if the converter is specified to deliver a peak output power (where output voltage regulation is to be maintained) greater than the maximum continuous output power for a limited time, the resonant tank must be designed for peak output power to make sure that it will not run in capacitive mode. Of course, its thermal design will consider only the maximum continuous power.

In any case, whatever the converter specified, short circuit conditions or, in general, overload conditions exceeding the maximum specified for the tank circuit, need to be handled with additional means, such as a current limitation circuit.

# 5 Magnetic integration

The LLC resonant half-bridge is well suited for magnetic integration, i.e. to combine the inductors as well as the transformer into a single magnetic device. This can be easily recognized looking at the transformer's physical model in *Figure 9*, where the topological analogy with the inductive part of the LLC tank circuit is apparent. However, the real transformer has leakage inductance on the secondary side as well, which is completely absent in the model considered so far. To include the effect of secondary leakage in the FHA analysis, we need a particular transformer model and a simplifying assumption.

It is well known that there are an infinite number of electrically equivalent models of a given transformer, depending on the choice of the turn ratio of the ideal transformer included in the model. With an appropriate choice of this "equivalent" turn ratio n (obviously different from the "physical" turn ratio $n_t$ = N1/N2) all the elements related to leakage flux can be located on the primary side.

This is the APR (All-Primary-Referred) model shown in *Figure 10*, which fits the circuit considered in the FHA analysis. It is possible to show that the APR model is obtained with the following choice of n:

**Equation 51**

$$n = k\sqrt{\frac{L_1}{L_2}}$$

with k transformer's coupling coefficient, $L_1$ inductance of the primary winding and $L_2$ inductance of each secondary winding. Note that $L_r$ still has physical meaning: it is the primary inductance measured with the secondary windings shorted. Note also that the primary inductance $L_1$ must be unchanged. It is only differently split in the 2 models of *Figure 9* and *Figure 10*, hence, $L_m$ will be the difference between $L_1$ and $L_r$.

In the end, the analysis done so far is directly applicable to real-world transformers provided they are represented by their equivalent APR model. Vice versa, a design flow based on the FHA analysis will provide the parameters of the APR model; hence, an additional step is needed to determine those of the physical model. In particular this applies to the turn number $n_t$, since $L_r$ and $L_m$ still have a connection with the physical world ($L_r+L_m = L_{L1}+L_\mu=L_1$).

**Figure 9. Transformer's physical model**

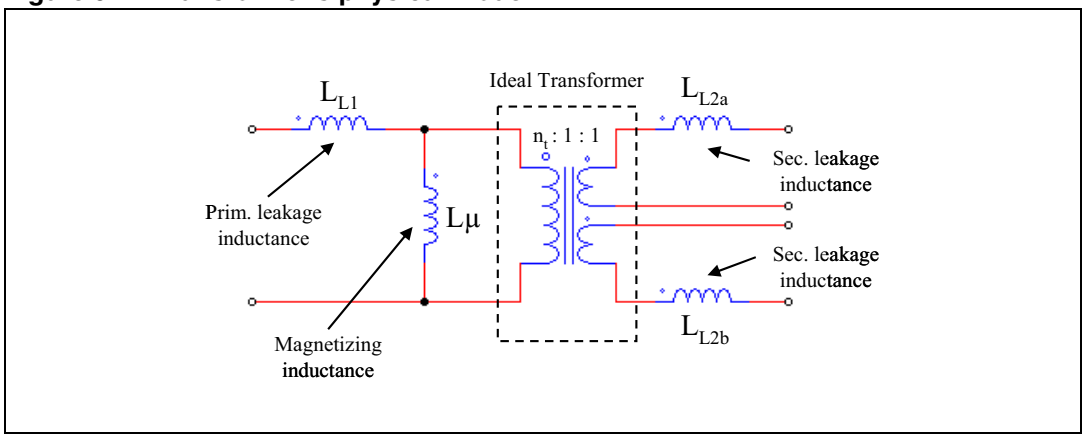
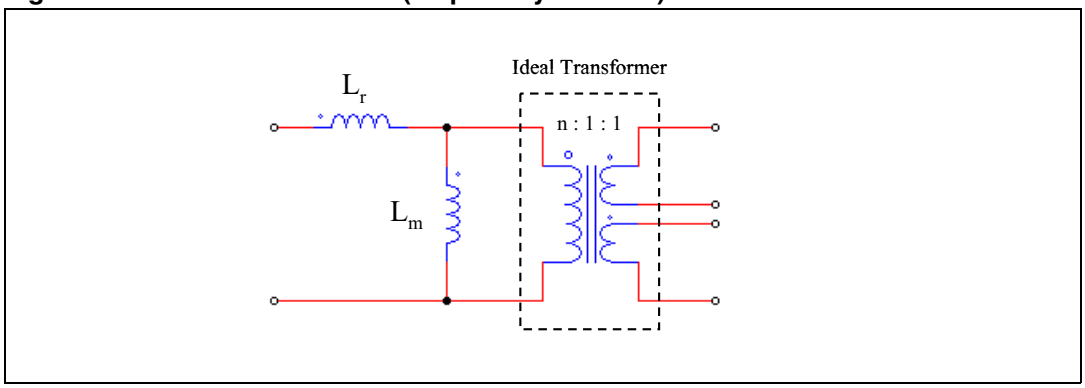



**Figure 10. Transformer's APR (all-primary-referred) model**




The problem is mathematically undetermined: there are 5 unknowns ($L_{L1}$, $L_\mu$, $n_t$, and $L_{L2a}$, $L_{L2b}$) in the physical model and only three parameters in the APR model. The simplifying assumption that overcomes this issue is that of magnetic circuit symmetry: flux linkage is

assumed to be exactly the same for both primary and secondary windings. This provides the two missing conditions:

**Equation 52**

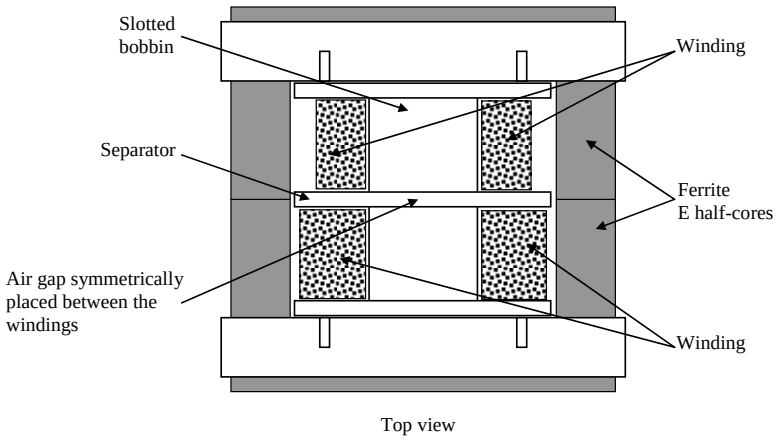
$$L_{L2a} = L_{L2b} = \frac{L_{L1}}{n_t^2}$$

With this assumption it is now possible to find the relationship between n and $n_t$:

**Equation 53**

$$n_t = n\sqrt{\frac{L_m + L_r}{L_m}} = n\sqrt{1+\lambda}$$

**Figure 11. Transformer construction: E-cores and slotted bobbin**




It is not difficult to find real-world structures where the condition of magnetic symmetry is quite close to reality. Consider for example the ferrite E-core plus slotted bobbin assembly, using side-by-side winding arrangement, shown in *Figure 11*.

# 6 Design procedure

Based on the analysis presented so far, a step-by-step design procedure of an LLC resonant converter is now proposed, which fulfills the following design specification and requires the additional information listed below:

- Design specification:
  - Input voltage range: $V_{dc.min}$ - $V_{dc.max}$
  - Nominal input voltage: $V_{dc.nom}$
  - Regulated output voltage: $V_{out}$
  - Maximum output power: $P_{out}$
  - Resonant frequency: $f_r$
  - Maximum operating frequency: $f_{max}$
- Additional info:
  - Parasitic capacitance at node N: $C_{zvs}$
  - Dead time of driving circuit: $T_D$
- General criteria for the design:
  - The converter will be designed to work at resonance at nominal input voltage.
  - The converter must be able to regulate down to zero load at maximum input voltage.
  - The converter will always work in ZVS in the whole operating range.
- 10 step procedure:
  - Step 1 - to fulfill the first criterion, impose that the required gain at nominal input voltage equals unity and calculate the transformer turn ratio:

**Equation 54**

$$M_{nom} = 2n\frac{V_{out}}{V_{dc.nom}} = 1 \quad \Rightarrow \quad n = \frac{1}{2}\frac{V_{dc.nom}}{V_{out}}$$

  - Step 2 - calculate the max. and min. required gain at the extreme values of the input voltage range:

**Equation 55**

$$M_{max} = 2n\frac{V_{out}}{V_{dc.min}}$$

**Equation 56**

$$M_{min} = 2n\frac{V_{out}}{V_{dc.max}}$$

  - Step 3 - calculate the maximum normalized operating frequency (according to the definition):

**Equation 57**

$$f_{n.max} = \frac{f_{max}}{f_r}$$

– Step 4 - calculate the effective load resistance reflected at transformer primary side, from *Equation 14* and *Equation 17*:

**Equation 58**

$$R_{ac} = \frac{8}{\pi^2} n^2 \frac{V_{out}^2}{P_{out}}$$

– Step 5 - impose that the converter operates at maximum frequency at zero load and maximum input voltage, calculating the inductance ratio from *Equation 38*:

**Equation 59**

$$\lambda = \frac{1 - M_{min}}{M_{min}} \frac{f_{nmax}^2}{f_{nmax}^2 - 1}$$

– Step 6 - calculate the max Q value to work in the ZVS operating region at minimum input voltage and full load condition, from *Equation 37* and *Equation 46*:

**Equation 60**

$$Q_{zvs1} = 95\% \bullet Q_{max} = 95\% \bullet \frac{\lambda}{M_{max}} \sqrt{\frac{1}{\lambda} + \frac{M_{max}^2}{M_{max}^2 - 1}}$$

– Step 7 - calculate the max Q value to work in the ZVS operating region at no-load condition and maximum input voltage, applying *Equation 50*:

**Equation 61**

$$Q_{zvs2} = \frac{2}{\pi} \frac{\lambda f_{nmax}}{(\lambda + 1) f_{nmax}^2 - \lambda} \frac{T_D}{R_{ac} C_{zvs}}$$

– Step 8 - choose the max quality factor for ZVS in the whole operating range, such that:

**Equation 62**

$$Q_{zvs} \leq \min\{Q_{zvs1}, Q_{zvs2}\}$$

– Step 9 - calculate the minimum operating frequency at full load and minimum input voltage, according to the following approximate formula:

**Equation 63**

$$f_{min} = f_r \sqrt{\frac{1}{1 + \frac{1}{\lambda}\left(1 - \frac{1}{1 + \left(\frac{Q_{zvs}}{Q_{max}}\right)^4}\right)}}$$

– Step 10 - calculate the characteristic impedance of the resonant tank and all component values (from definition):

**Equation 64**

$$Z_o = Q_{zvs} R_{ac} \quad C_r = \frac{1}{2\pi f_r Z_o} \quad L_r = \frac{Z_o}{2\pi f_r} \quad L_m = \frac{L_r}{\lambda}$$

# 7 Design example

Here below, a design example follows for a 400 W resonant converter intended to be operated with a front-end PFC with a typical regulated bus voltage of about 400 V.

The STMicroelectronics resonant controller L6599 is particularly suitable for this application. In fact it incorporates the necessary functions to properly drive the two half-bridge MOSFETs by a 50 percent fixed duty cycle with a fixed dead-time $T_D$, (between high side and low side MOSFET driving signals), changing the frequency according to the feedback signal in order to regulate the output voltages against load and input voltage variations. The main features of the L6599 are a non linear soft-start, a new current protection mode allowing to program the hiccup mode timing, a dedicated pin for sequencing or brown-out (pin LINE) and a stand-by pin (pin STBY) allowing for the burst mode operation at light load.

The converter specification data are the following:

- Nominal input DC voltage: 390 V
- Input DC voltage range: from 320 to 420 V
- Output voltages: 200 V@ 1.6 A continuous current - 75 V@ 1.0 A continuous current
- Resonance frequency: 120 kHz
- Max operating frequency: 150 kHz
- Delay time (L6599 data-sheet): 270 ns
- Foreseen half-bridge total stray capacitance (at node N): 350 pF

The calculations have been done assuming that all power is delivered to the 200 V output voltage. Afterward, once the turn ratio has been defined, the transformer is designed to deliver the two output voltages, using the correct number of turns and the proper wire section.

The results of the 10 step procedure are summarized in *Table 1*:

**Table 1. Desing results**

| Step | Parameter |
|---|---|
| 1 | $n = 0.975$ |
| 2 | $M_{max} = 1.22$<br>$M_{min} = 0.93$ |
| 3 | $f_{n.max} = 1.25$ |
| 4 | $R_{ac} = 77.05\ \Omega$ |
| 5 | $\lambda = 0.21$ |
| 6 | $Q_{zvs.1} = 0.41$ |
| 7 | $Q_{zvs.2} = 1.01$ |
| 8 | $Q_{zvs} = 0.41$ |
| 9 | $f_{min} = 80.6$ kHz |
| 10 | $Z_o = 31.95\ \Omega$ $C_r = 41.51$ nF<br>$L_r = 42\ \mu H$ $L_m = 197\ \mu H$ |

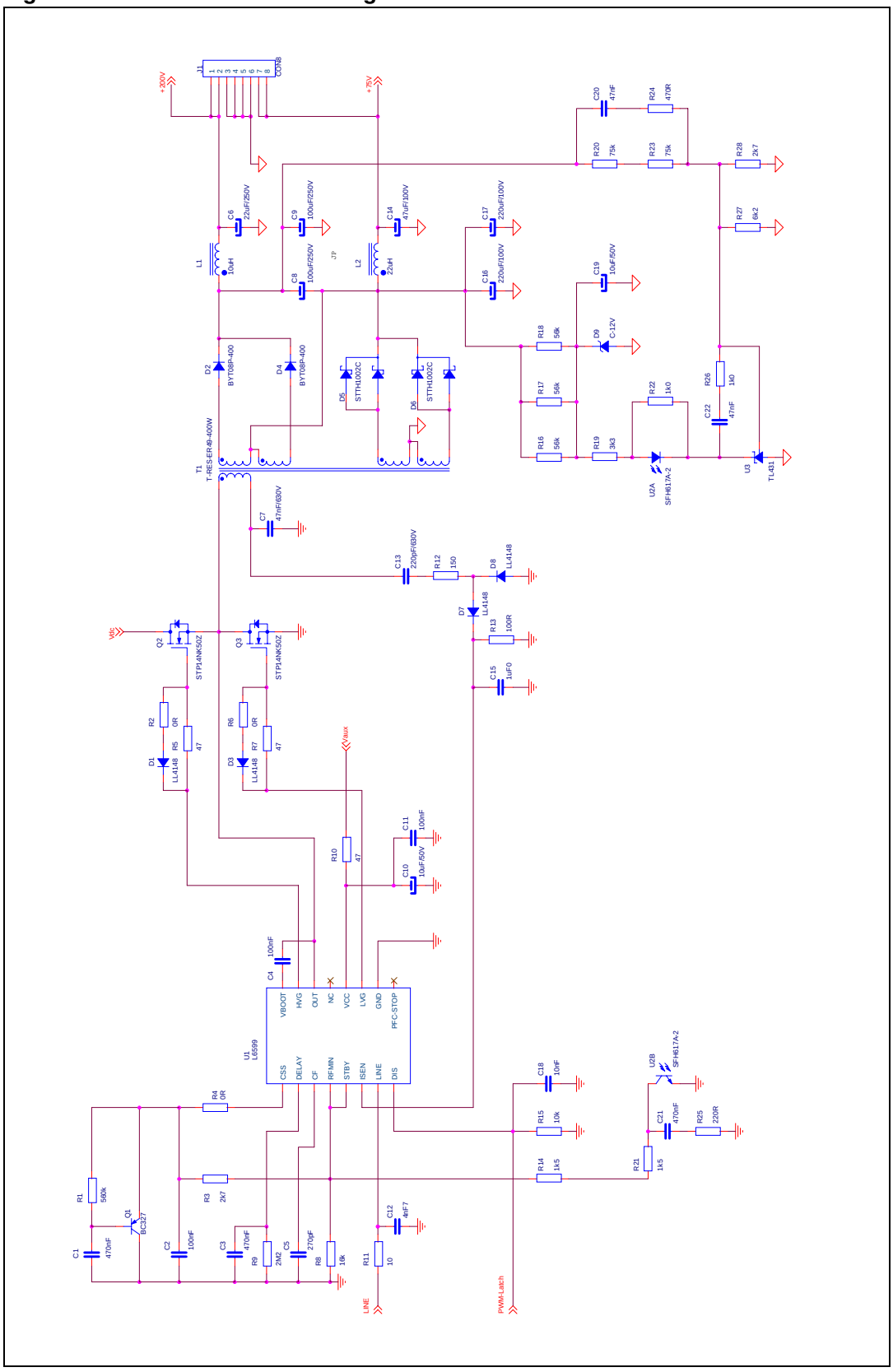
The chosen standard value of the resonant capacitor is 4 7nF. The transformer has been designed using a two slot coil-former and integrating both the series inductance $L_r$ and the shunt inductance $L_m$, in order to obtain a magnetic component with the following parameters:

- $L_{p(SO)} = L_r + L_m = 240\ \mu H$ primary inductance (with secondary windings open)
- $L_{p(SS)} = L_r = 40\ \mu H$ primary inductance with secondary windings shorted
- $n_t = n \bullet \sqrt{1+\lambda} = 1.08$ transformer turn ratio

The number of primary turns has been found experimentally, by measuring the "specific leakage inductance" (i.e. the leakage inductance per square turns) of a few suitable ferrite cores, using a two slot winding configuration. The procedure consists of winding a few layers of turns on both slots of the coil-former (same copper area for primary and secondary) and then measuring the inductance of one winding with the other one short circuited. Dividing this measured value by the squared number of turns gives the specific leakage inductance of the core - coil-former construction. The chosen ferrite core is a ER-49-27-17 type, material grade PC44, and the necessary number of primary turns to obtain the required leakage inductance is 19. Therefore, the total number of secondary turns for 200 V output is 18 (from the required turn ratio $n_t$).

The secondary side of the transformer consists of two center-tap windings, one for each output, and the two output voltages (+75 V and +200 V) are obtained by series connecting the two secondary windings on the DC side (refer to the electrical schematic in *Figure 12* for better understanding of circuit configuration). The bottom winding (for +75 V output) has 7 turns, while the top winding consists of 11 (18-7) turns.

**Figure 12. LLC resonant half-bridge converter electrical schematic**



# 8 Electrical test results

## 8.1 Efficiency measurements

*Table 2*, *Table 3* and *Table 4* below show the output voltage and current measurements at the various dc input voltage (nominal 390 Vdc, min 360 Vdc and max 420 Vdc) and several load conditions. For all measurements, both at full load and at light load operation, the input power has been measured by a digital power meter (Yokogawa WT-210). Particular attention has to be paid when measuring input power at full load in order to avoid measurement errors due to the voltage drop on cables and connections (connecting the WT-210 voltmeter termination to the board input connector). For the same reason, the measurements of the output voltages have been taken directly at the output connector, by using the remote sense option of the active load (Chroma 63108 and 63103) connected to the outputs.

**Table 2. Efficiency measurements @ $V_{in}$ = 390 $V_{dc}$**

| +200 V | @load(A) | +75 (V) | @load (A) | Pout (W) | Pin (W) | Efficiency % |
|---|---|---|---|---|---|---|
| 198.76 | 1.603 | 76.74 | 1.010 | 396.12 | 408.80 | 96.90% |
| 198.75 | 1.300 | 76.80 | 0.811 | 320.66 | 330.81 | 96.93% |
| 198.76 | 1.001 | 76.87 | 0.613 | 246.08 | 253.90 | 96.92% |
| 198.79 | 0.751 | 76.95 | 0.414 | 181.15 | 187.54 | 96.59% |
| 198.84 | 0.500 | 77.03 | 0.200 | 114.83 | 120.24 | 95.50% |
| 198.87 | 0.151 | 77.06 | 0.107 | 38.27 | 42.70 | 89.64% |

**Table 3. Efficiency measurements @ $V_{in}$ = 360 $V_{dc}$**

| +200 V | @load(A) | +75 (V) | @load (A) | Pout (W) | Pin (W) | Efficiency % |
|---|---|---|---|---|---|---|
| 198.68 | 1.603 | 76.68 | 1.010 | 395.93 | 409.47 | 96.69% |
| 198.64 | 1.301 | 76.74 | 0.811 | 320.67 | 331.26 | 96.80% |
| 198.62 | 1.000 | 76.81 | 0.613 | 245.70 | 254.17 | 96.67% |
| 198.60 | 0.751 | 76.88 | 0.414 | 180.98 | 187.23 | 96.66% |
| 198.57 | 0.500 | 76.94 | 0.198 | 114.52 | 120.43 | 95.09% |
| 198.57 | 0.151 | 76.94 | 0.107 | 38.22 | 43.20 | 88.46% |

**Table 4. Efficiency measurements @ $V_{in}$ = 420$V_{dc}$**

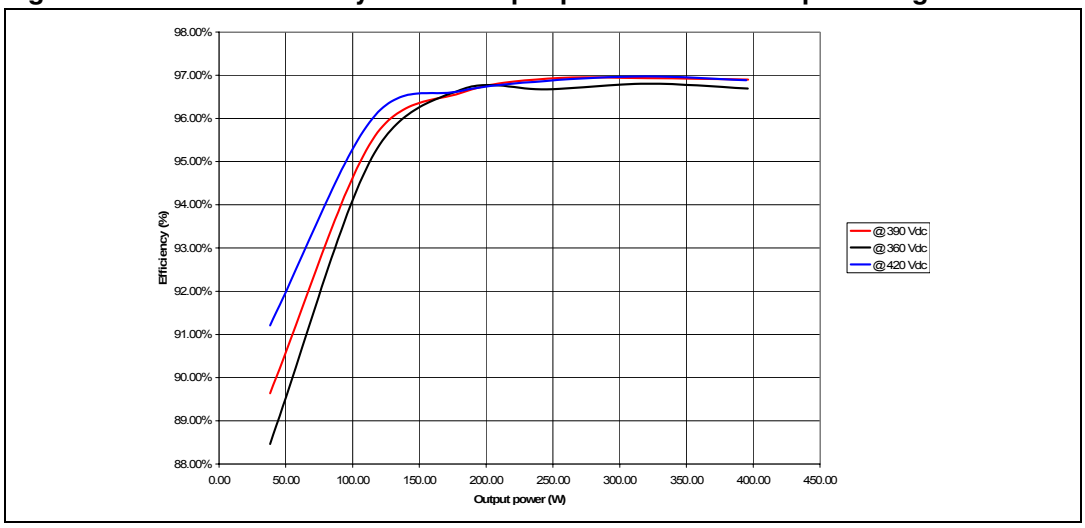
| +200 V | @load(A) | +75 (V) | @load (A) | Pout (W) | Pin (W) | Efficiency % |
|---|---|---|---|---|---|---|
| 198.35 | 1.601 | 76.57 | 1.008 | 394.74 | 407.45 | 96.88% |
| 198.20 | 1.301 | 76.55 | 0.808 | 319.71 | 329.70 | 96.97% |
| 197.87 | 1.001 | 76.47 | 0.609 | 244.64 | 252.55 | 96.87% |
| 196.85 | 0.750 | 76.20 | 0.410 | 178.88 | 185.13 | 96.62% |

**Table 4. Efficiency measurements @ $V_{in}$ = 420$V_{dc}$ (continued)**

| +200 V | @load(A) | +75 (V) | @load (A) | Pout (W) | Pin (W) | Efficiency % |
|---|---|---|---|---|---|---|
| 198.01 | 0.504 | 76.74 | 0.198 | 114.99 | 119.78 | 96.00% |
| 198.67 | 0.151 | 76.98 | 0.107 | 38.24 | 41.92 | 91.21% |

The measurements have been done after 30 minutes of warm-up at maximum load. The circuit efficiency has been calculated at each load condition and input dc voltage and is plotted in *Figure 13*, showing very high values at maximum load level, higher than 96.5%. Also at light load, at an output power of about 10% of the maximum level, the converter efficiency is very good, reaching a value better than 88% in the whole DC input voltage range.

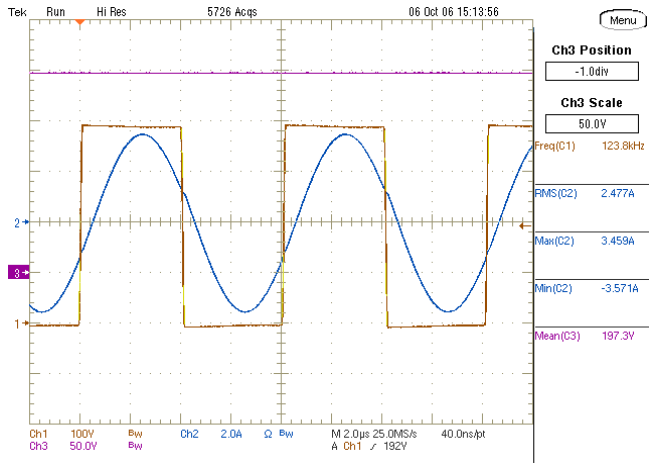
**Figure 13. Circuit efficiency versus output power at various input voltages**




## 8.2 Resonant stage operating waveforms

*Figure 14* shows some waveforms during steady state operation of the resonant circuit at nominal dc input voltage and full load. The Ch1 waveform is the half-bridge square voltage on pin 14 of L6599, driving the resonant circuit. The trace Ch2 represents the transformer primary current flowing into the resonant tank. As shown, it is almost sinusoidal, because the operating frequency (about 123 kHz) is close to the resonance of the leakage inductance of the transformer and the resonant capacitor (C6). In this condition the circuit has a good margin for ZVS operation, providing good efficiency, while the almost sinusoidal current waveform just allows for an extremely low EMI generation.

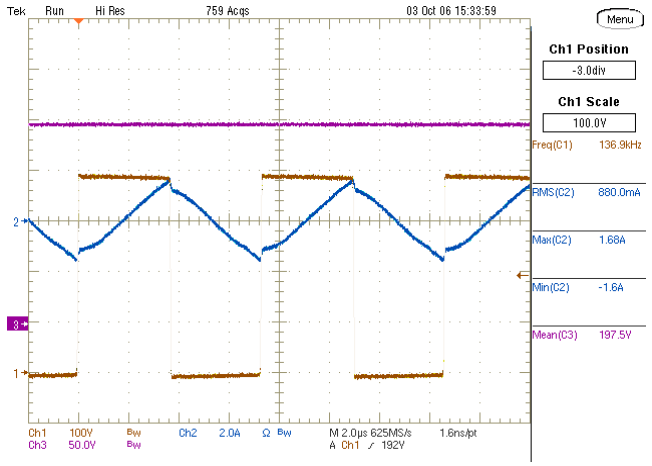
**Figure 14. Resonant circuit primary side waveforms at nominal dc input voltage and full load**




Ch1: half-bridge square voltage
Ch2: resonant tank current
Ch3: +200 V output voltage

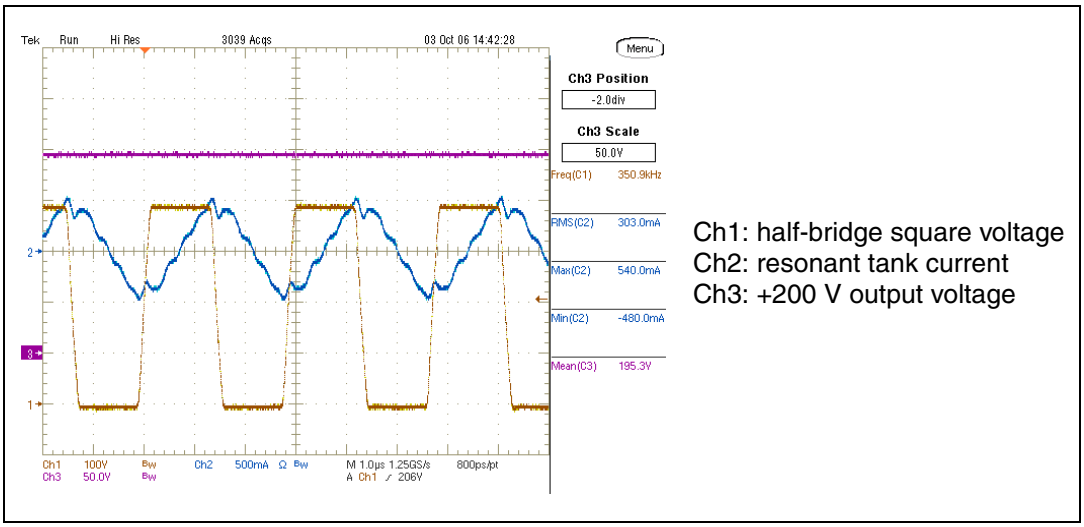
*Figure 15* and *Figure 16* show the same waveforms as *Figure 14* with both outputs lightly loaded (50 mA each) and not loaded, respectively. These graphs demonstrate the ability of the converter to operate down to zero load, with the output voltages still within regulation limits (as can be seen looking at Ch3 waveform, representing the +200 V output voltage). The resonant tank current, in this load condition, assumes, obviously, an almost triangular shape and represents the magnetizing current flowing into the transformer primary side.

**Figure 15. Resonant circuit primary side waveforms at nominal dc input voltage and light load**




Ch1: half-bridge square voltage
Ch2: resonant tank current
Ch3: +200 V output voltage

**Figure 16. Resonant circuit primary side waveforms at nominal dc input voltage and no-load**




In *Figure 17*, the Ch1 waveform shows a detail of the half-bridge square voltage (directly taken across pin14 and pin10 of L6599 controller) to highlight the softness of voltage edge, without abrupt negative voltage spikes that would be generated in presence of large stray inductance of wiring. The layout is very critical in this respect and needs to be optimized in order to minimize this effect, which could damage the controller itself.

In *Figure 18* and *Figure 19*, waveforms relevant to the secondary side are represented. The rectifiers reverse voltage is measured by CH1 (for both +200 V and +75 V outputs) and the peak-to-peak value is indicated on the right of the graph. Waveform CH2 shows the current flowing into one of the two output diodes for each output voltage (respectively D6 and D8). Also this current shape is almost a sine wave, whose average value is one half the output current.

**Figure 17. Resonant circuit primary side waveforms at nominal dc input voltage and light load**

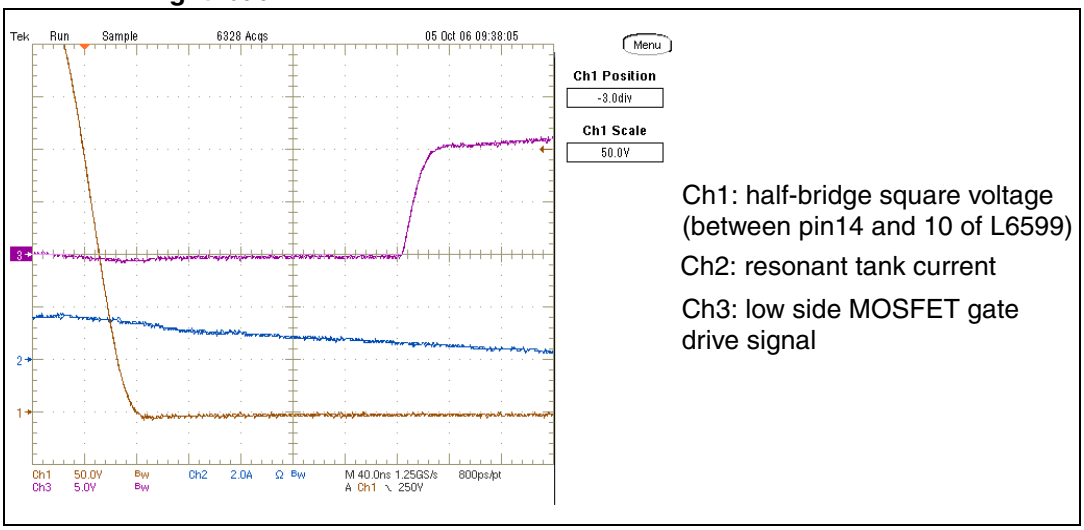


**Figure 18. +200 V output diode voltage and current waveforms**

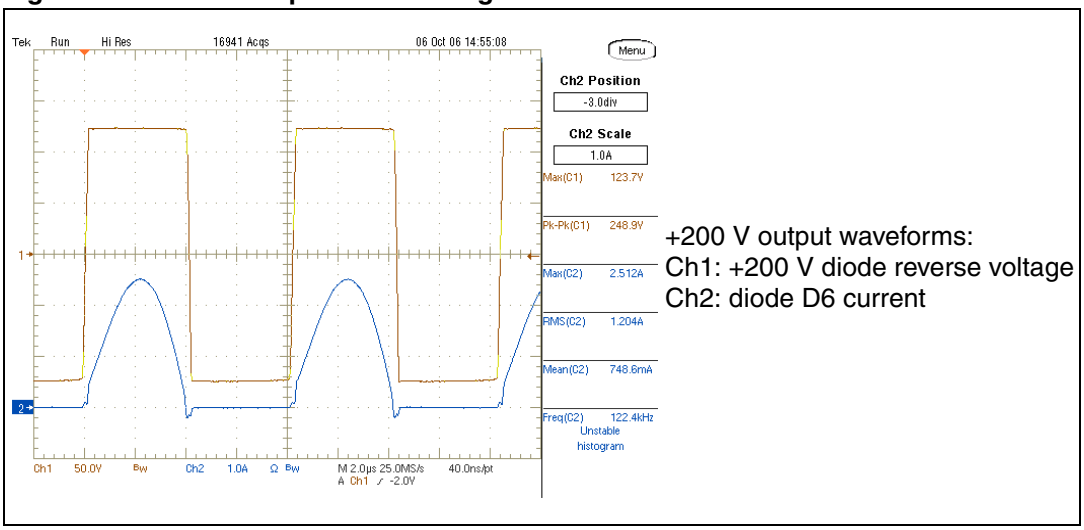
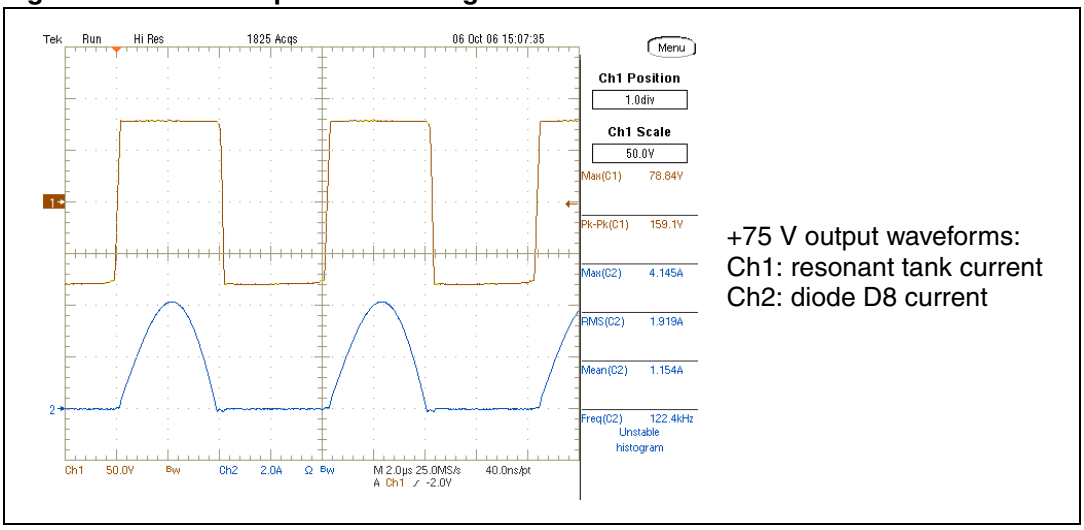



**Figure 19. +75 V output diode voltage and current waveforms**



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# 10 Revision history

**Table 5. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 11-Jan-2007 | 1 | First issue |
| 06-Mar-2007 | 2 | Minor text change |
| 26-Mar-2007 | 3 | *Equation 53* modified |
| 24-Jul-2007 | 4 | Quality factor (Q) modified |
| 25-Oct-2007 | 5 | Modified: *Equation 14* and *Equation 33* |