AOZ1212

EZBuck™ 3A Simple Buck Regulator

Preliminary

General Description

The AOZ1212 is a high efficiency, simple to use, 3A buck regulator flexible enough to be optimized for a variety of applications. The AOZ1212 works from a 4.5V to 28V input voltage range, and provides up to 3A of continuous output current on each buck regulator output. The output voltage is adjustable down to 0.8V.

Features

- 4.5V to 28V operating input voltage range
- 70 mΩ internal NFET, efficiency: up to 95%
- Internal soft start
- Output voltage adjustable down to 0.8V
- 3A continuous output current
- Fixed 370kHz PWM operation
- Cycle-by-cycle current limit
- Short-circuit protection
- Thermal shutdown
- Small size SO-8 packages

Applications

- Point of load DC/DC conversion
- Set top boxes
- DVD drives and HDD
- LCD Monitors & TVs
- Cable modems
- Telecom/Networking/Datacom equipment

Typical Application

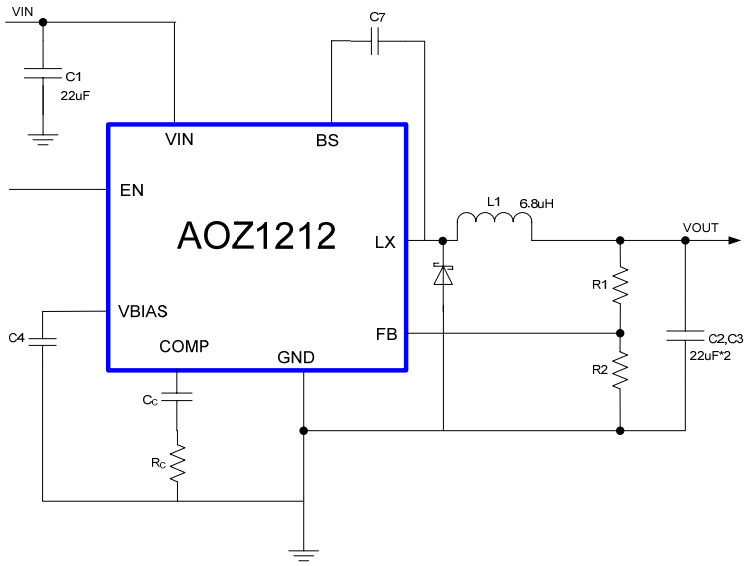
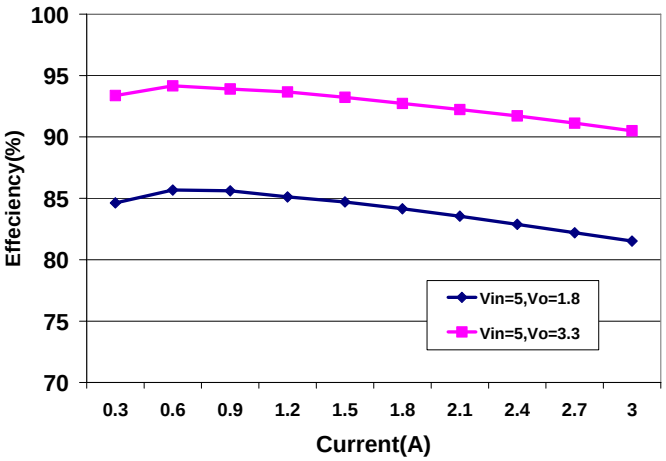


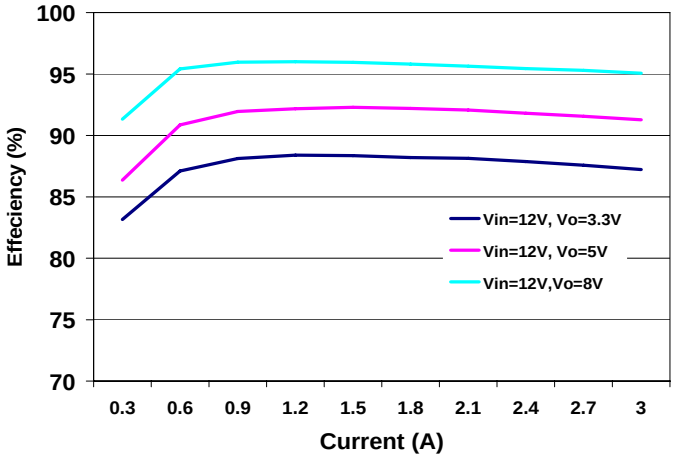
Figure 1. 3.3V/3A Buck Regulator

Efficiency curve

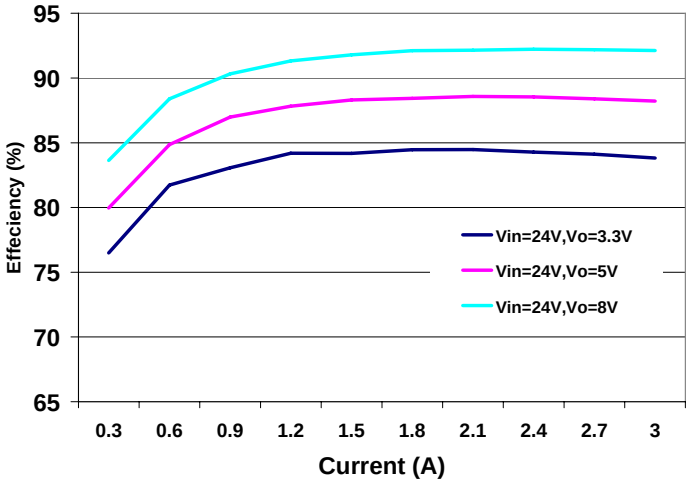
Efficiency Vin=5V



Efficiency Vin=12V



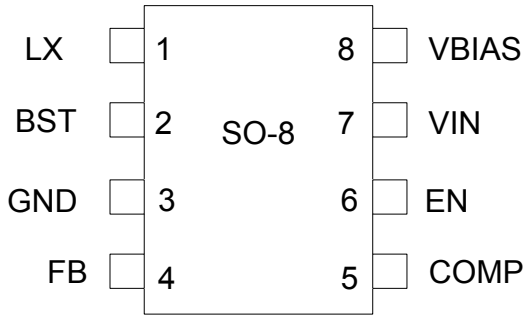
Efficiency Vin=24V



Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ1212AI	-40°C to +85°C	SO-8	RoHS

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Function
1	LX	PWM output connection to inductor. LX pin needs to be connected externally. Thermal connection for output stage.
2	BST	Bootstrap voltage input. High side driver supply. Connected to 0.1uF capacitor between BST and LX.
3	GND	Ground.
4	FB	Feedback input. It is regulated to 0.8V. The FB pin is used to determine the PWM output voltage via a resistor divider between the output and GND.
5	COMP	External loop compensation. Output of internal error amplifier. Connect a series RC network to GND for control loop compensation.
6	EN	Enable pin. The enable pin is active high. Connect EN pin to VIN if not used. Do not leave the EN pin floating.
7	VIN	Supply voltage input. Range from 4.5V to 28V. When VIN rises above the UVLO threshold the device starts up. All VIN pins need to be connected externally.
8	VBIAS	Compensation pin of internal linear regulator. Place put a 1uF capacitor between this pin and ground.

Absolute Maximum Ratings[1]

Supply Voltage (VIN)..... 30V
LX to GND .....-0.7V to V_{IN}+0.3V
EN to GND.....-0.3V to V_{IN}+0.3V
FB to GND .....-0.3V to 6V
COMP to GND.....-0.3V to 6V
BS to GND..... VLX + 6V
PGOOD to GND ..... -0.3V to 30V
Junction Temperature (T_J).....+150°C
Storage Temperature (T_S) ..... -65°C to +150°C
ESD Rating[3] 2kV

Recommend Operating Ratings[2]

Supply Voltage (V_{IN})..... 4.5V to 28V
Output Voltage Range ..... 0.8V to V_{IN}
Ambient Temperature (T_A).....-40°C to +85°C
Package Thermal Resistance
SO-8 (Θ_{JA}).....105°C/W

Electrical Characteristics

T_A = 25°C, V_{IN} = V_{EN} = 12V, unless otherwise specified[4].

Parameter	Symbol	Conditions	MIN	TYP	MAX	UNITS
Supply Voltage	VIN		**4.5**		**28**	V
Input Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising V_{IN} falling		**4.3** **4.1**		V V
Supply Current (Quiescent)	I_{IN}	I_{OUT} = 0, VFB = 1.2V, V_{EN} >2V		**2**	**3**	mA
Shutdown Supply Current	I_{OFF}	V_{EN} = 0V		**3**	**20**	μA
Feedback Voltage	V_{FB}		0.782	0.8	0.818	V
Load Regulation				0.5		**%**
Line Regulation				0.08		**%/V**
Feedback Voltage Input Current	I_{FB}				200	nA
Enable						
EN Input Threshold	V_{EN}	Off threshold On threshold	 **2.5**		**0.6**	V V
EN input Hysteresis	V_{HYS}			**200**		mV
Enable Sink/Source current	I_{EN}				50	nA
Modulator						
Frequency	f_O		330	370	410	kHz
Maximum Duty Cycle	D_{MAX}		85			%
Minimum Duty Cycle	D_{MIN}				6	%
Error Amplifier Voltage Gain	G_{VEA}			500		V/V
Error Amplifier Transconductance	G_{EA}			200		μA/V
Protection						
Current Limit	I_{LIM}		3.5		5.0	A
Over-Temperature Shutdown Limit		T_J rising T_J falling		145 100		°C °C
Short Circuit Hiccup Frequency	f_{sc}	V_{FB}=0V		24		kHz
Soft Start Interval	t_{SS}			6		ms

Electrical Characteristics (cont)

T_A = 25°C, V_{IN} = V_{EN} = 12V, unless otherwise specified[4].

PWM Output Stage						
High-Side Switch On-Resistance	$R_{DS(ON)}$			70	100	mohm
High-Side Switch Leakage		V_{EN}=0V, V_{LX}=0V			10	uA

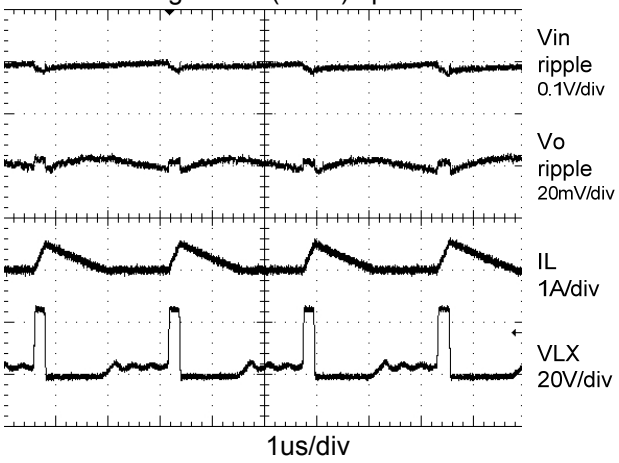
Notes:

1. Exceeding the Absolute Maximum ratings may damage the device.
2. The device is not guaranteed to operate beyond the Maximum Operating ratings.
3. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5KΩ in series with 100pF.
4. Specification in BOLD indicate an ambient temperature range of -40°C to +85°C. These specifications are guaranteed by design.

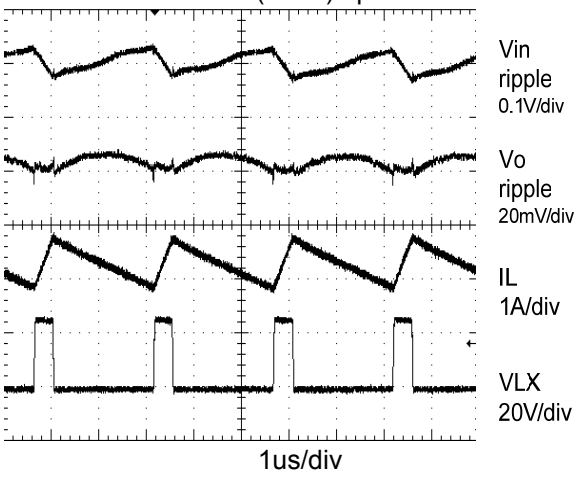
Typical Performance Characteristics

Circuit of figure 1. T_A = 25°C, V_{IN} = V_{EN} = 24V, V_{OUT} = 3.3V unless otherwise specified.

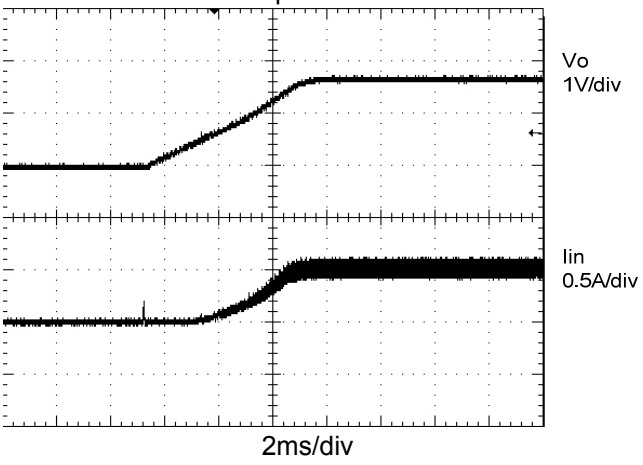
Light load (DCM) operation



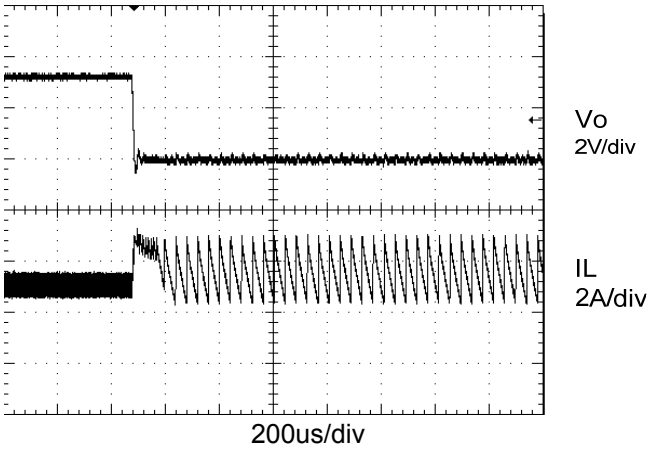
Full load (CCM) operation



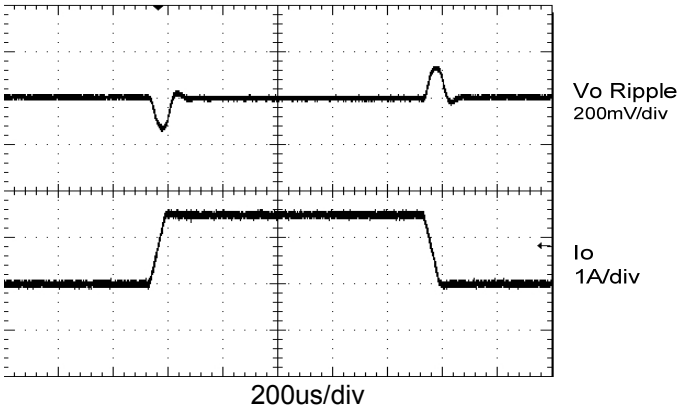
Start up to full load



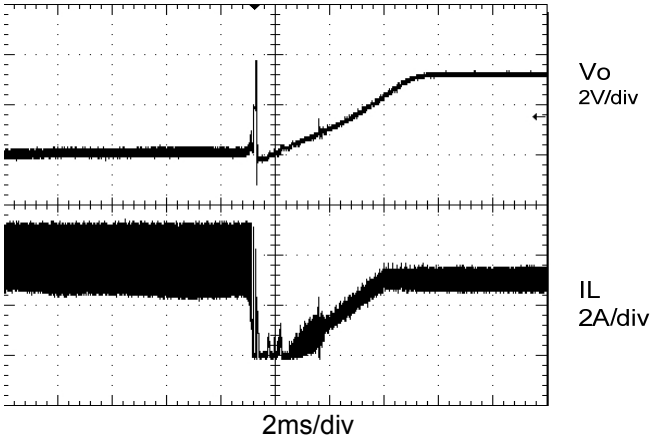
Short circuit protection



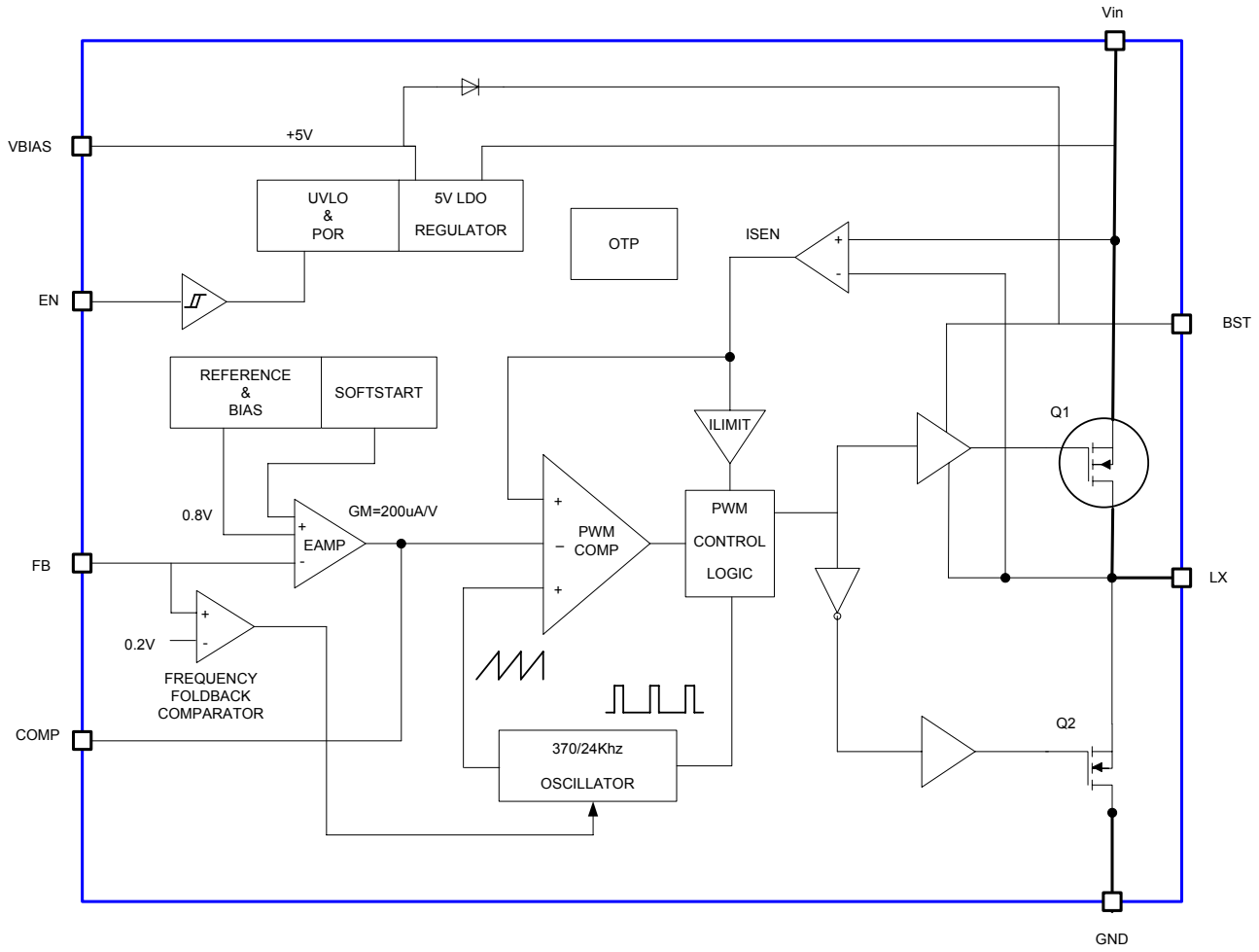
50% to 100% load transient



Short circuit recovery



Functional Block Diagram



Detailed Description

The AOZ1212 is a current-mode step down regulator with integrated high side NMOS switch. It operates from a 4.5V to 28V input voltage range and supplies up to 3A of load current. The duty cycle can be adjusted from 6% to 85% allowing a wide range of output voltage. Features include enable control, Power-On Reset, input under voltage lockout, fixed internal soft-start and thermal shut down.

The AOZ1212 is available in SO-8 package.

Enable and Soft Start

The AOZ1212 has internal soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulation voltage. A soft start process begins when the input voltage rises to 4.1V and voltage on EN pin is HIGH. In soft start process, the output voltage is ramped to regulation voltage in typically 6.8ms. The 6.8ms soft start time is set internally.

Connect the EN pin to VIN if enable function is not used. Pull it to ground will disable the AOZ1212. Do not leave it open. The voltage on EN pin must be above 2.5 V to enable the AOZ1212. When voltage on EN pin falls below 0.6V, the AOZ1212 is disabled. If an application circuit requires the AOZ1212 to be disabled, an open drain or open collector circuit should be used to interface to EN pin.

Steady-State Operation

Under steady-state conditions, the converter operates in fixed frequency and Continuous-Conduction Mode (CCM).

The AOZ1212 integrates an internal N-MOSFET as the high-side switch. Inductor current is sensed by amplifying the voltage drop across the drain to source of the high side power MOSFET. Since the N-MOSFET requires a gate voltage higher than the input voltage, a boost capacitor connected between LX pin and BST pin drives the gate. The boost capacitor is charged while LX is low. An internal 10 ohm switch from LX to GND is used to insure that LX is pulled to GND even in the light load. Output voltage is divided down by the external voltage divider at the FB pin. The difference of the FB pin voltage and reference is amplified by the internal transconductance error amplifier. The error voltage, which shows on the COMP pin, is compared against the current signal, which is sum of inductor current signal and ramp compensation signal, at PWM comparator input. If the current signal is less than the error voltage, the internal high-side switch is on. The inductor current flows from the input through the inductor to the output. When the current signal exceeds the error voltage, the high-side switch is off. The inductor current is freewheeling through the Schottky diode to output.

Switching Frequency

The AOZ1212 switching frequency is fixed and set by an internal oscillator. The switching frequency is set 370 Khz.

Output Voltage Programming

Output voltage can be set by feeding back the output to the FB pin with a resistor divider network. In the application circuit shown in Figure 1. The resistor divider network includes R_2 and R_3. Usually, a design is started by picking a fixed R_3 value and calculating the required R_2 with equation below.

$$V_O = 0.8 \times (1 + \frac{R_1}{R_2})$$

Some standard value of R_1, R_2 for most commonly used output voltage values are listed in Table 1.

Table 1.

Vo (V)	R1 (kΩ)	R2 (kΩ)
0.8	1.0	Open
1.2	4.99	10
1.5	10	11.5
1.8	12.7	10.2
2.5	21.5	10
3.3	31.6	10
5.0	52.3	10

Combination of R1 and R2 should be large enough to avoid drawing excessive current from the output, which will cause power loss.

Protection Features

The AOZ1212 has multiple protection features to prevent system circuit damage under abnormal conditions.

Over Current Protection (OCP)

The sensed inductor current signal is also used for over current protection. Since the AOZ1212 employs peak current mode control, the COMP pin voltage is proportional to the peak inductor current. The COMP pin voltage is limited to be between 0.4V and 2.5V internally. The peak inductor current is automatically limited cycle by cycle.

The cycle by cycle current limit threshold is internally set. When the load current reaches the current limit threshold, the cycle by cycle current limit circuit turns off the high side switch immediately to terminate the current duty cycle. The inductor current stop rising. The cycle by cycle current limit protection directly limits inductor peak current. The average inductor current is also limited due to the limitation on peak inductor current. When cycle by cycle current limit circuit is triggered, the output voltage drops as the duty cycle decreasing.

The AOZ1212 has internal short circuit protection to protect itself from catastrophic failure under output short circuit conditions. The FB pin voltage is proportional to the output voltage. Whenever FB pin voltage is below 0.2V, the short circuit protection circuit is triggered. To prevent current limit running away, when comp pin voltage is higher than 2.1 V, the short circuit protection is also triggered. As a result, the converter is shut down and hiccups at a frequency equals to 1/16 of normal switching frequency. The converter will start up via a soft start once the short circuit condition disappears. In short circuit protection mode, the inductor average current is greatly reduced because of the low hiccup frequency.

Power-On Reset (POR)

A power-on reset circuit monitors the input voltage. When the input voltage exceeds 4.3V, the converter starts operation. When input voltage falls below 4.1V, the converter will stop switching.

Thermal Protection

An internal temperature sensor monitors the junction temperature. It shuts down the internal control circuit and high side NMOS if the junction temperature exceeds 145ºC. The regulator will restart automatically under the control of soft-start circuit when the junction temperature decreases to 100ºC.

Application Information

The basic AOZ1212 application circuit is shown in Figure 1. Component selection is explained below.

Input capacitor

The input capacitor (C_1 in Figure 1) must be connected to the V_{IN} pin and GND pin of the AOZ1212 to maintain steady input voltage and filter out the pulsing input current. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_O}{f \times C_{IN}} \times (1 - \frac{V_O}{V_{IN}}) \times \frac{V_O}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}}(1 - \frac{V_O}{V_{IN}})}$$

if let *m* equal the conversion ratio:

$$\frac{V_O}{V_{IN}} = m$$

The relation between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Fig. 2 below. It can be seen that when V_O is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is $0.5 \cdot I_O$.

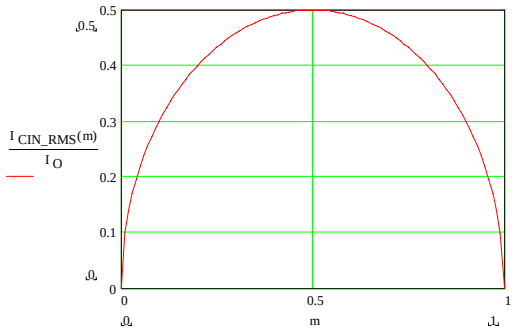


Figure 2. I_{CIN} vs. voltage conversion ratio

For reliable operation and best performance, the input capacitors must have current rating higher than $I_{CIN-RMS}$ at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high ripple current rating. Depending on the application circuits, other low ESR tantalum capacitor or aluminum electrolytic capacitor may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors are preferred for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures is based on certain amount of life time. Further de-rating may be necessary for practical design requirement.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is,

$$\Delta I_L = \frac{V_O}{f \times L} \times (1 - \frac{V_O}{V_{IN}})$$

The peak inductor current is:

$$I_{Lpeak} = I_O + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor needs to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_O = \Delta I_L \times (ESR_{CO} + \frac{1}{8 \times f \times C_O})$$

where C_O is output capacitor value and ESR_{CO} is the Equivalent Series Resistor of output capacitor.

When low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_O = \Delta I_L \times \frac{1}{8 \times f \times C_O}$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_O = \Delta I_L \times ESR_{CO}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum capacitor or aluminum electrolytic capacitor may also be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected

to be very small and inductor ripple current is high, output capacitor could be overstressed.

Schottky Diode Selection

The external freewheeling diode supplies the current to the inductor when the high side NMOS switch is off. To reduce the losses due to the forward voltage drop and recovery of diode, Schottky diode is recommended to use. The maximum reverse voltage rating of the chosen Schottky diode should be greater than the maximum input voltage, and the current rating should be greater than the maximum load current.

Loop Compensation

The AOZ1212 employs peak current mode control for easy use and fast transient response. Peak current mode control eliminates the double pole effect of the output L&C filter. It greatly simplifies the compensation loop design.

With peak current mode control, the buck power stage can be simplified to be a one-pole and one-zero system in frequency domain. The pole is dominant pole and can be calculated by:

$$f_{P1} = \frac{1}{2\pi \times C_O \times R_L}$$

The zero is a ESR zero due to output capacitor and its ESR. It is can be calculated by:

$$f_{Z1} = \frac{1}{2\pi \times C_O \times ESR_{CO}}$$

Where C_O is the output filter capacitor;
R_L is load resistor value;
ESR_{CO} is the equivalent series resistance of output capacitor;

The compensation design is actually to shape the converter close loop transfer function to get desired gain and phase. Several different types of compensation network can be used for AOZ1212. For most cases, a series capacitor and resistor network connected to the COMP pin sets the pole-zero and is adequate for a stable high-bandwidth control loop.

In the AOZ1212, FB pin and COMP pin are the inverting input and the output of internal transconductance error amplifier. A series R and C compensation network connected to COMP provides one pole and one zero. The pole is:

$$f_{P2} = \frac{G_{EA}}{2\pi \times C_C \times G_{VEA}}$$

Where G_{EA} is the error amplifier transconductance, which is $200 \cdot 10^{-6}$ A/V;
G_{VEA} is the error amplifier voltage gain, which is 500 V/V;
C_C is compensation capacitor;

The zero given by the external compensation network, capacitor C_C (C_5 in Figure 1) and resistor R_C (R_1 in Figure 1), is located at:

$$f_{Z2} = \frac{1}{2\pi \times C_C \times R_C}$$

To design the compensation circuit, a target crossover frequency f_C for close loop must be selected. The system crossover frequency is where control loop has unity gain. The crossover frequency is also called the converter bandwidth. Generally a higher bandwidth means faster response to load transient. However, the bandwidth should not be too high due to system stability concern. When designing the compensation loop, converter stability under all line and load condition must be considered.

Usually, it is recommended to set the bandwidth to be less than 1/10 of switching frequency. It is recommended to choose a crossover frequency less than 30kHz.

$$f_C = 30kHz$$

The strategy for choosing R_C and C_C is to set the cross over frequency with R_C and set the compensator zero with C_C. Using selected crossover frequency, f_C, to calculate R_C:

$$R_C = f_C \times \frac{V_O}{V_{FB}} \times \frac{2\pi \times C_O}{G_{EA} \times G_{CS}}$$

where f_C is desired crossover frequency;
V_{FB} is 0.8V;
G_{EA} is the error amplifier transconductance, which is $200 \cdot 10^{-6}$ A/V;
G_{CS} is the current sense circuit transconductance, which is 5.64 A/V;

The compensation capacitor C_C and resistor R_C together make a zero. This zero is put somewhere close to the dominate pole f_{p1} but lower than 1/5 of selected crossover frequency. C_C can is selected by:

$$C_C = \frac{1.5}{2\pi \times R_C \times f_{P1}}$$

Equation above can also be simplified to:

$$C_C = \frac{C_O \times R_L}{R_C}$$

An easy-to-use application software which helps to design and simulate the compensation loop can be found at www.aosmd.com.

Thermal management and layout consideration

In the AOZ1212 buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the VIN pin, to the LX pins, to the filter inductor, to the output capacitor and load, and then return to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from inductor, to the output capacitors and load, to the GND pin of the AOZ1212, to the LX pins of the AZO1212. Current flows in the second loop when the low side diode is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is recommended to connect input capacitor, output capacitor, and GND pin of the AOZ1212.

In the AOZ1212 buck regulator circuit, the three major power dissipating components are the AOZ1212, external diode and output inductor. The total power dissipation of converter circuit can be measured by input power minus output power.

$$P_{total\_loss} = V_{IN} \cdot I_{IN} - V_O \cdot I_O$$

The power dissipation of inductor can be approximately calculated by output current and DCR of inductor.

$$P_{indcutor\_loss} = I_O{}^2 \cdot R_{inductor} \cdot 1.1$$

The power dissipation of diode is

$$P_{diode\_loss} = I_O \cdot V_F \cdot (1 - \frac{Vo}{Vin})$$

The actual AOZ1212 junction temperature can be calculated with power dissipation in the AOZ1212 and thermal impedance from junction to ambient.

$$T_{junction} = (P_{total\_loss} - P_{inductor\_loss} - P_{diode\_loss}) \cdot \Theta_{JA} + T_{ambient}$$

The maximum junction temperature of AOZ1212 is 145ºC, which limits the maximum load current capability. Please see the thermal de-rating curves for the maximum load current of the AOZ1212 under different ambient temperature.

The thermal performance of the AOZ1212 is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.

Several layout tips are listed below for the best electric and thermal performance.

1. Do not use thermal relief connection to the VIN and the GND pin. Pour a maximized copper area to the GND pin and the VIN pin to help thermal dissipation.
2. Input capacitor should be connected to the VIN pin and the GND pin as close as possible.
3. Make the current trace from LX pins to L to Co to the GND as short as possible.
4. Pour copper plane on all unused board area and connect it to stable DC nodes, like VIN, GND or VOUT.
5. Keep sensitive signal trace such as trace connected with FB pin and COMP pin far away form the LX pins.