The POWER Behind Your Designs

Active Clamp Forward Converters

Design Using UCC2897

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Presentation Content

- Review of Active Clamp and Reset Technique in Single-Ended Forward Converters

- Design Material/Tools
- Design procedure and concern

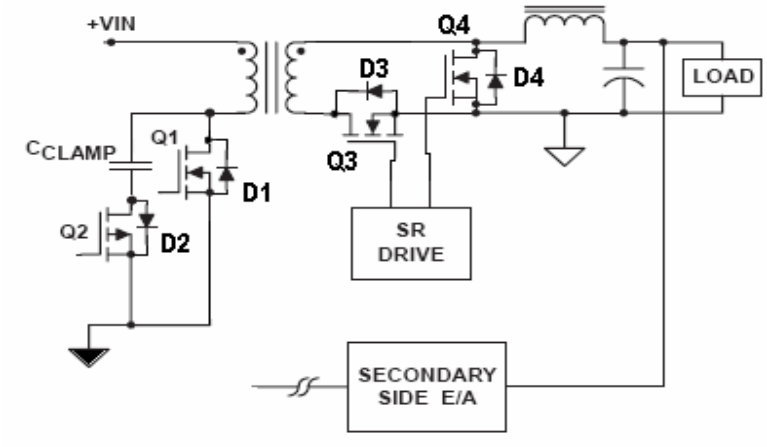
- Common Problems in Self-driven Sync Rectifier
- Control-driven and TPS28225

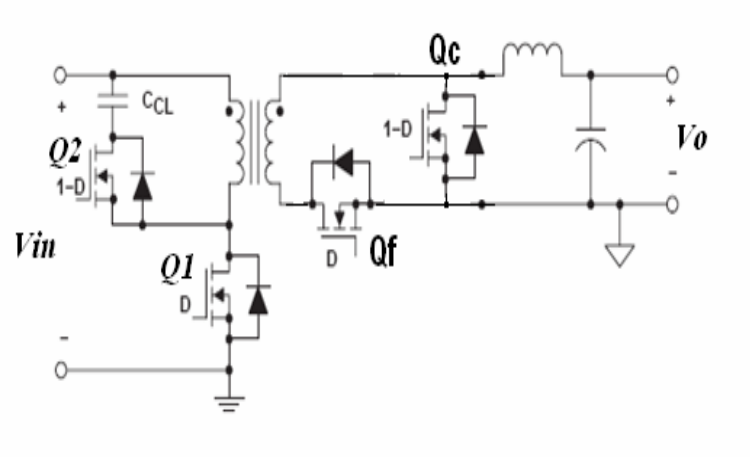
- Main switch ZVS / VVS
- Comparison ACFC and HB in telecom applications

- Gate Drive Signals

- Solution to the problem of power-off oscillation

Review of Active Clamp Reset Technique





Typical configurations (a) Low side clamp (b) high side clamp

- Detailed comparison can be found in TI Application Note (SLUA322)
  Active Clamp Transformer Reset: High Side or Low Side?

- Main differences:
  (a) Gate driving scheme
  (b) Clamp and Reset voltage ratings
  (c) MOSFET type for clamping

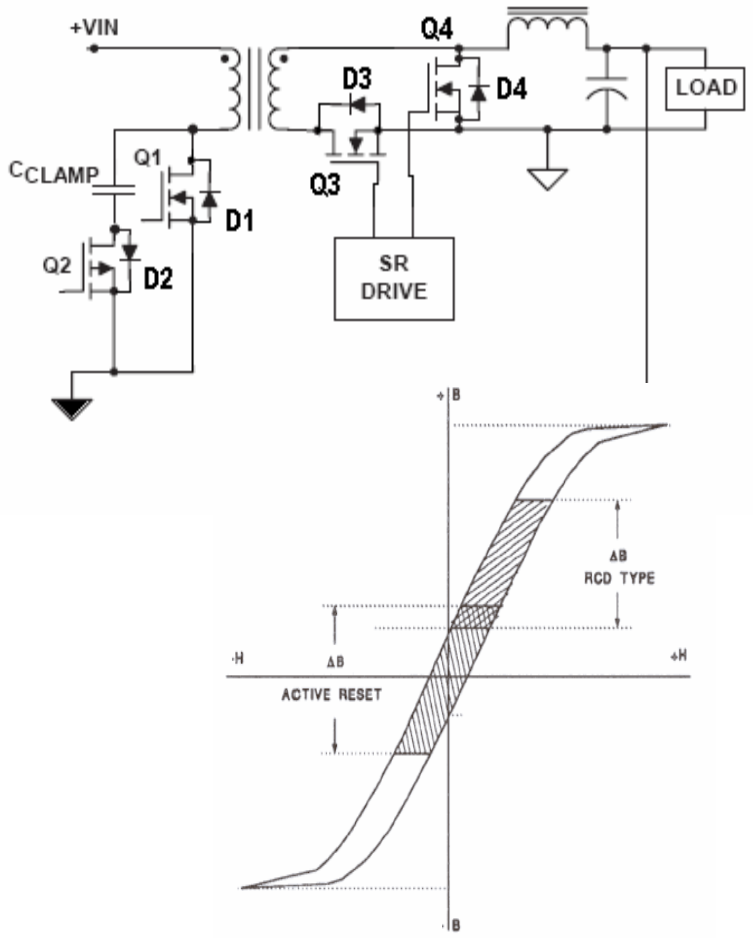
The POWER Behind Your Designs

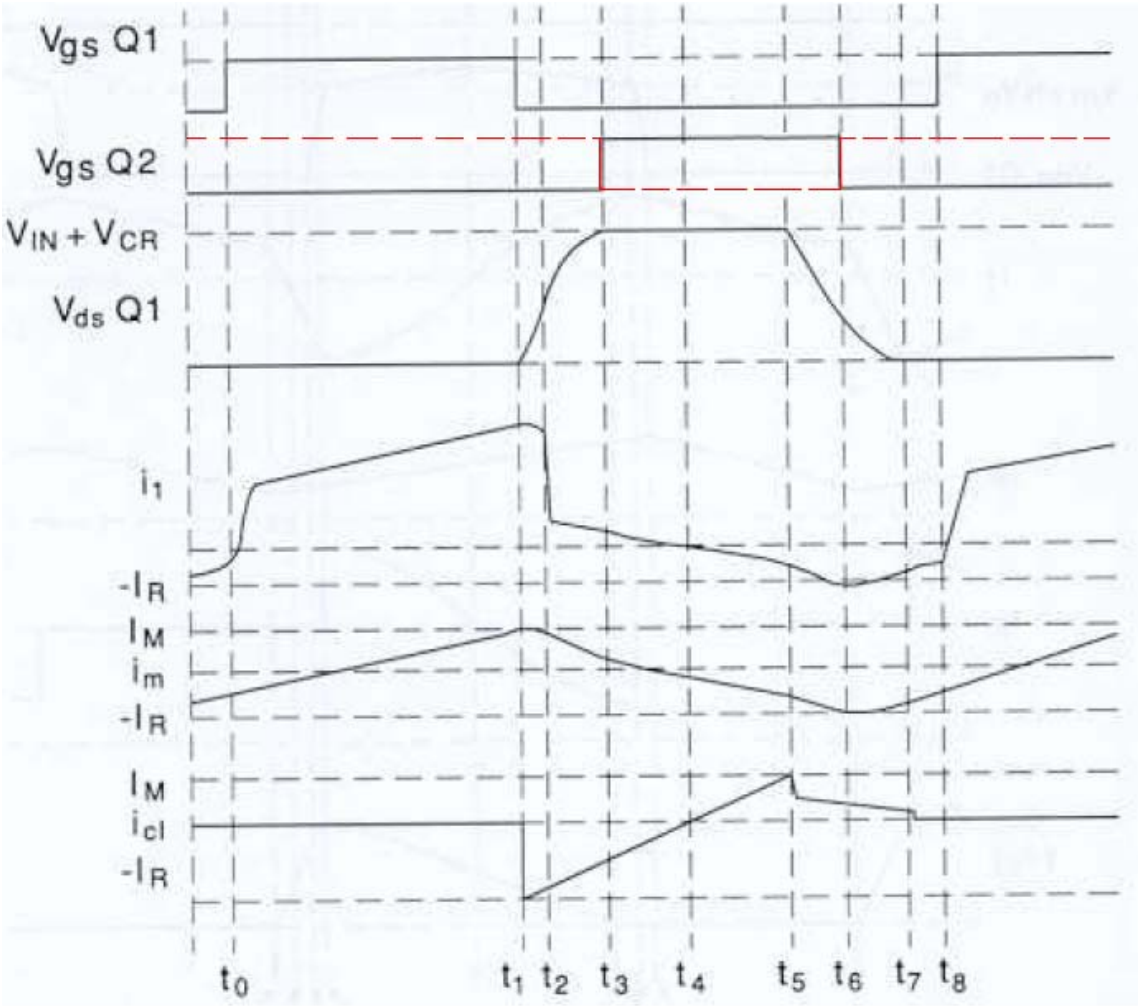
Review of Active Clamp Reset Technique

PARAMETER	HIGH-SIDE CLAMP	LOW-SIDE CLAMP
V_{DS}	$\left(\frac{1}{1-D}\right) \times V_{IN}$	$\left(\frac{1}{1-D}\right) \times V_{IN}$
V_{RESET}	$\left(\frac{D}{1-D}\right) \times V_{IN}$	$\left(\frac{D}{1-D}\right) \times V_{IN}$
V_C	$\left(\frac{D}{1-D}\right) \times V_{IN}$	$\left(\frac{1}{1-D}\right) \times V_{IN}$
C_{cl} (applied voltage)	Lower voltage by V_{IN} Volts Highest V_{cl} occurs at D_{MAX} Careful attention for wide V_{IN} applications	Higher voltage by V_{IN} Volts Transformer turns ratio critical at for limiting V_{cl} Careful attention for off-line, high voltage applications
C_{cl} (component value)	Same value as low side for given ripple voltage	Same value as high side for given ripple voltage
AUX MOSFET	N-Channel Must be used for 400-V (off−line) input applications	P-Channel Can't be used for 400V applications due to limited VDS rating of available devices
Gate drive	Gate drive transformer required AUX MOSFET V_{GS} out of phase with main MOSFET V_{GS} – UCC2893 PWM Controller	Simple RCD clamp gate drive AUX MOSFET V_{GS} in phase with main MOSFET V_{GS} – UCC2891 PWM Controller

Comparison of High- and Low-Side Clamp

Review of Active Clamp Reset Technique





- Voltage Clamp
- Transformer reset

Design Material/Tools

- Step-by-Step Design Procedure

  - Designing for High Efficiency with the Active Clamp UCC2891 PWM Controller (SLUA303)

  - Advances / Differences of UCC2897 from UCC2891

    (a) 20 –pin, QFN

    (b) LineOV

    (c) PGND

    (d) Hiccup OCP

    (e) Bi-directional f-sync

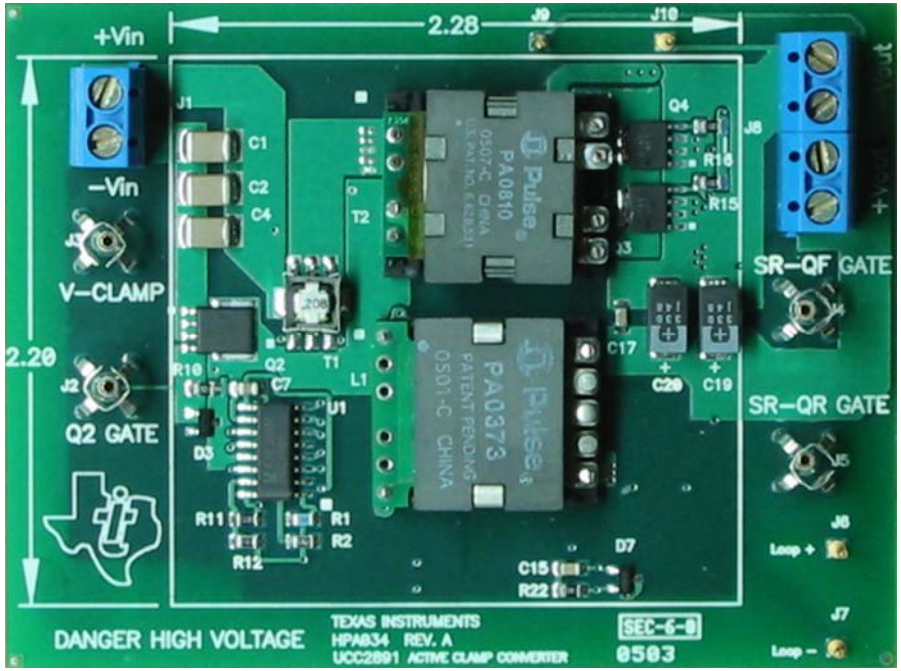
    (d) FB and SS 2.5V instead of 1.25V

- MathCad Design Files (Power stage and Loop design)

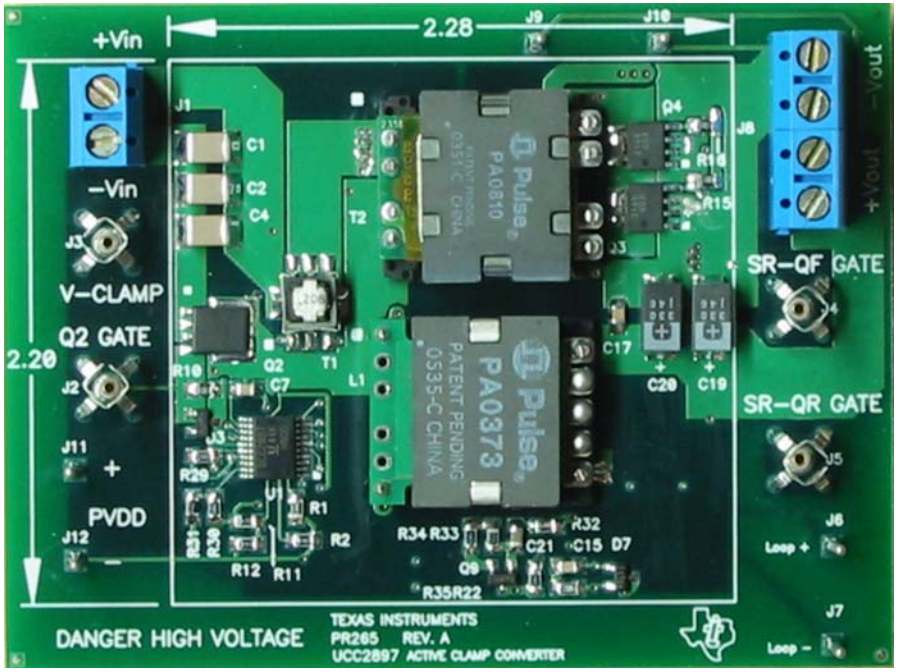
- EVMs (UCC2891, UCC2897, UCC2894)

Active Clamp single-ended forward converter in telecom applications

- EVM Specs: Vin = 36V to 75V, Vo = 3.3V, Io = 30A, Po = 100W



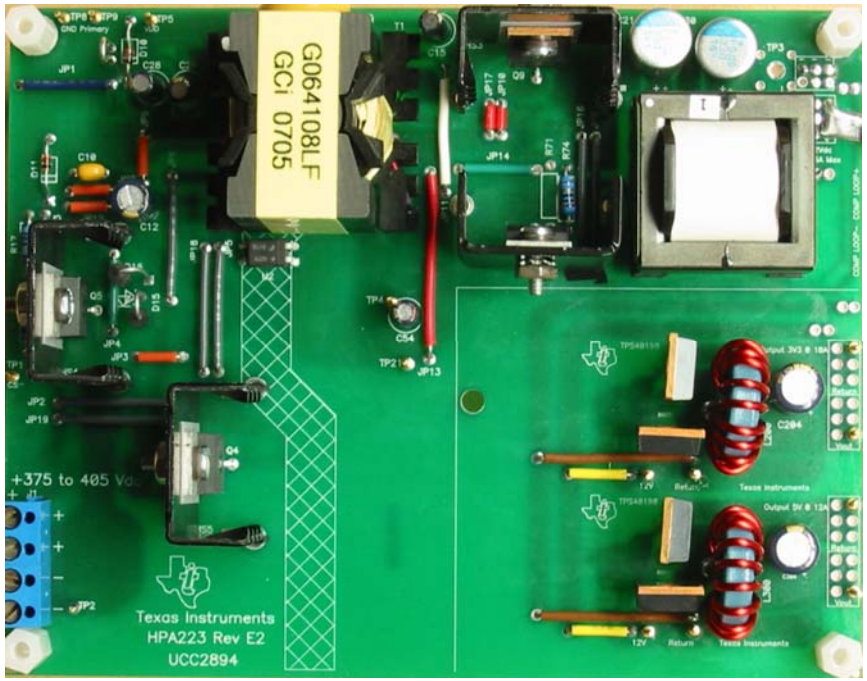
UCC2891 EVM

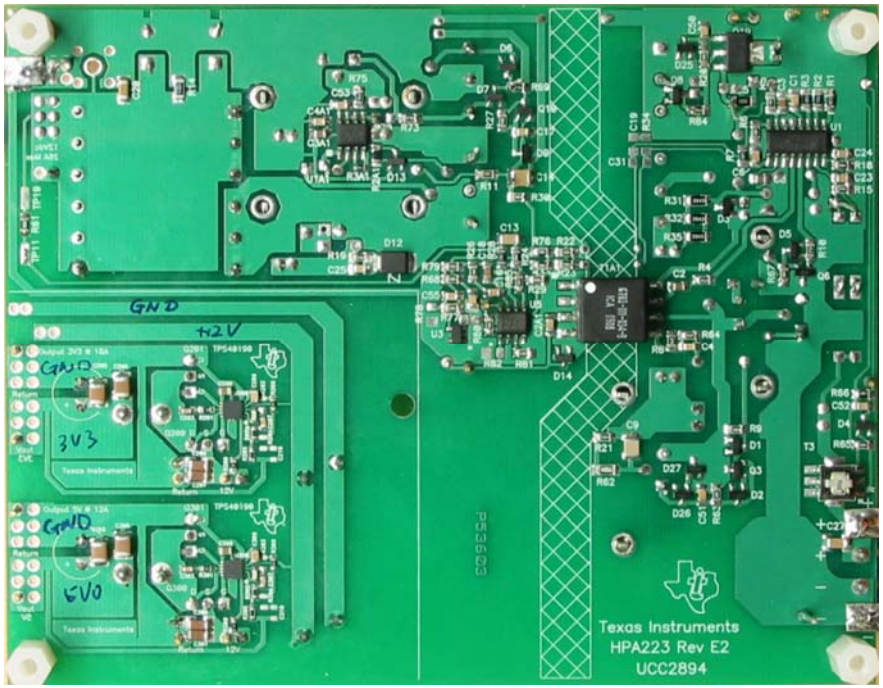


UCC2897 EVM

UCC2984 EVM

Input voltage: 390Vdc
Rated Power: 320W
Output voltage: 12Vdc
Output current: 26A





Design Procedures and Concerns

- Power stage design
- Program IC
- Switching frequency, magnetizing inductance, two resonant frequencies, and dead-time
- Switching losses and ZVS/VVS
- Capacitance at Vref and VDD should be minimum ratio 1:10 (e.g. if Vref cap is .1uF then VDD cap minimum 1.0uF)
- Observing Vref maximum load capability, less than 5mA. If tie a resistor between FB and Vref, that resistor typical value is about 2k ohm.

- Duty cycle (D) and turns ratio (N) to balance MOSFET voltage ratings

  - N ↑ → D ↑ → **more stress on main FET (primary)**

  - N ↓ → D ↓ → **more stress on catch FET (secondary)**

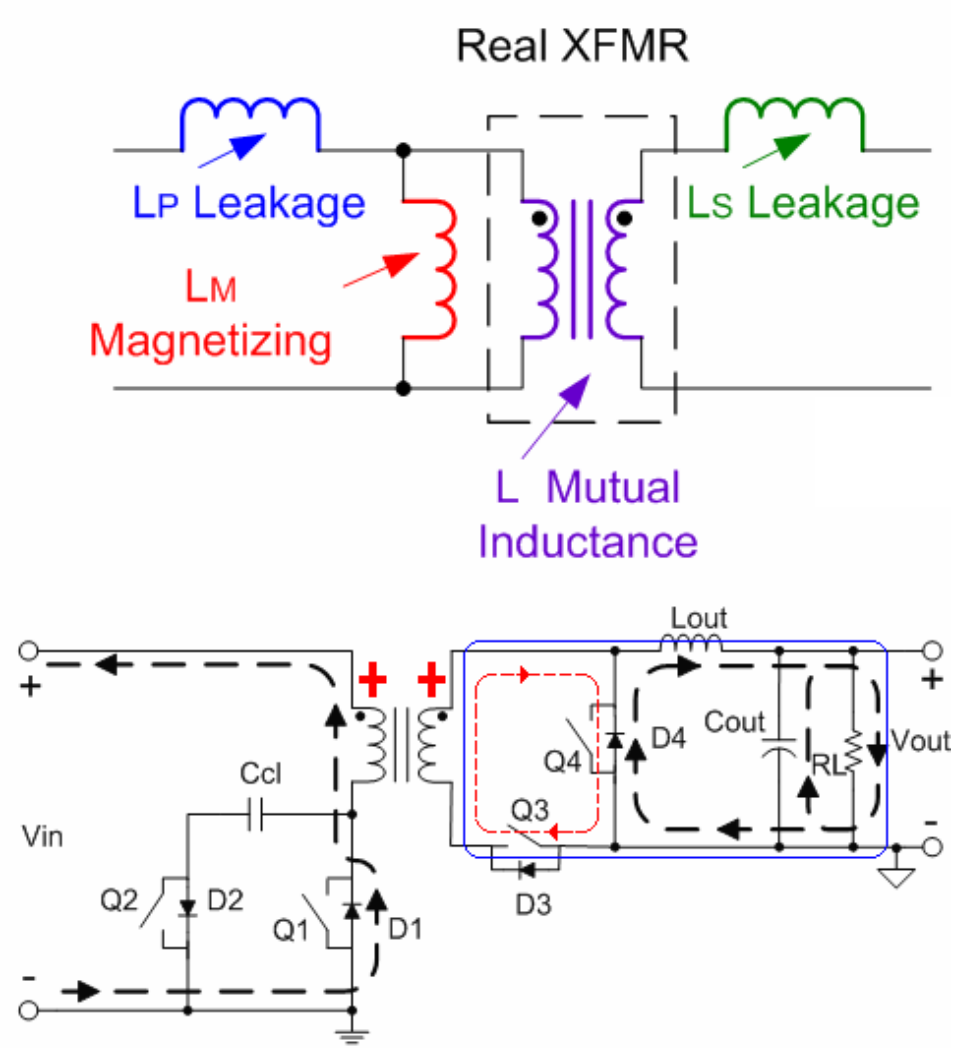
  (a) forward FET Vds = (Vin/N) x D/(1-D) + Vo;

  (b) catch FET Vds = Vin/N;

  (c) primary main FET Vds = Vin x 1/(1-D);

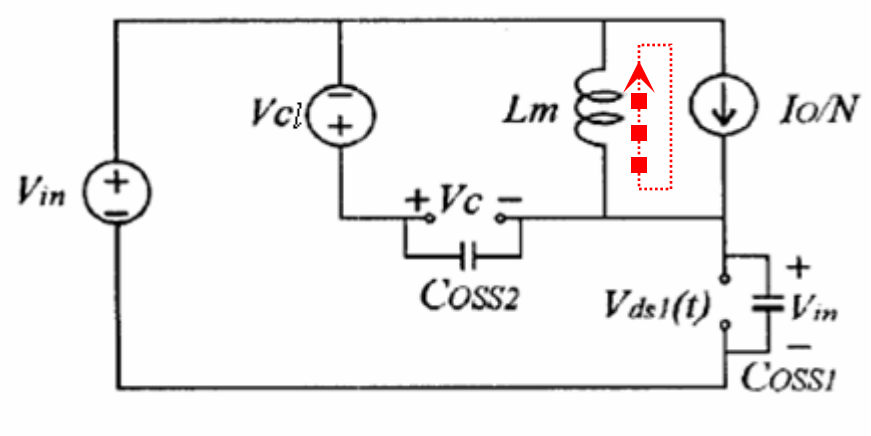
  (d) clamp FET Vds = Vin x 1/(1-D) - Vin = Vin x D/(1-D)

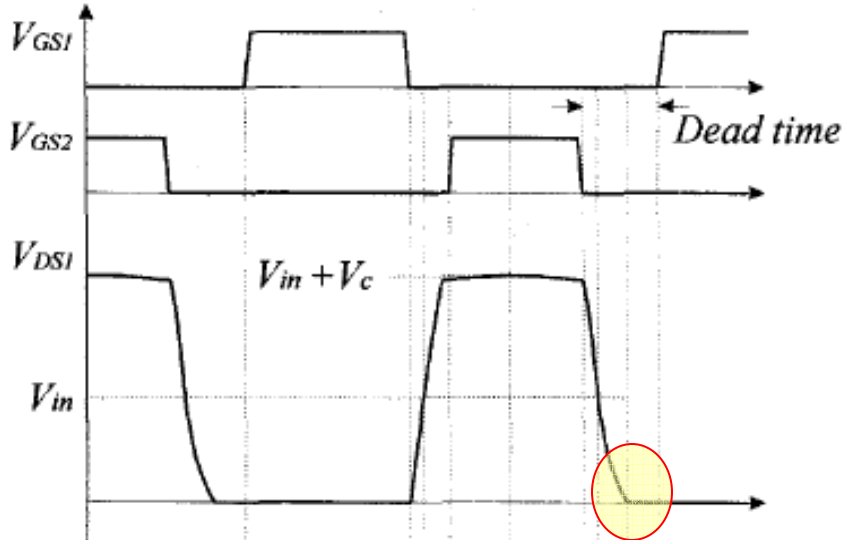
How to achieve primary main switch ZVS / VVS



- If the secondary side leakage is small the magnetizing energy necessary to turn D1 on will be diverted through D3 (Q3) during the reverse recovery of D4 (or Q4 reverse conduction)
- After the reverse recovery of D4, the magnetizing energy will continue discharging through the loop shown in blue
- Since there is no energy to turn D1 ON, ZVS of Q1 does not take place.

Principle of ZVS/VVS turning on

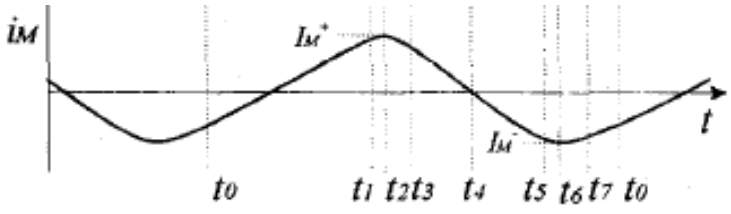




Vds reversed and clamped by the body diode.

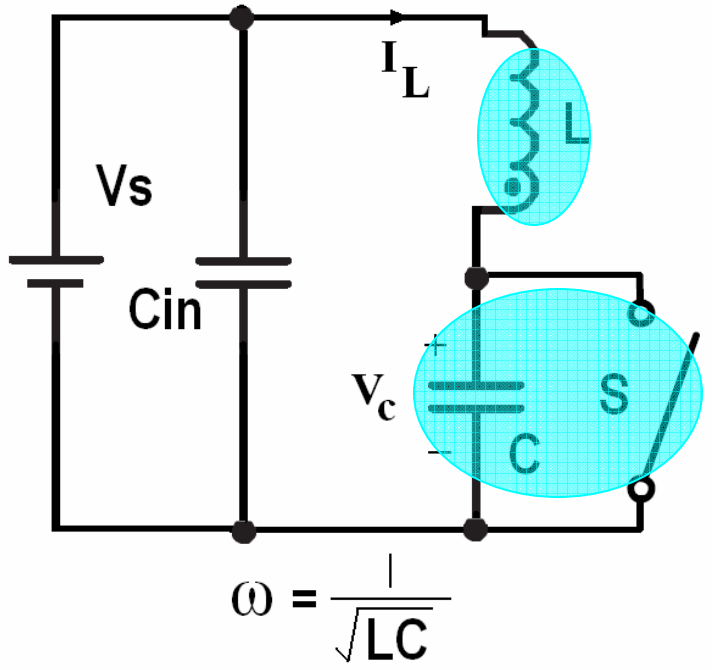
$$I_M^+ = \frac{NV_O}{2L_m f_S}$$

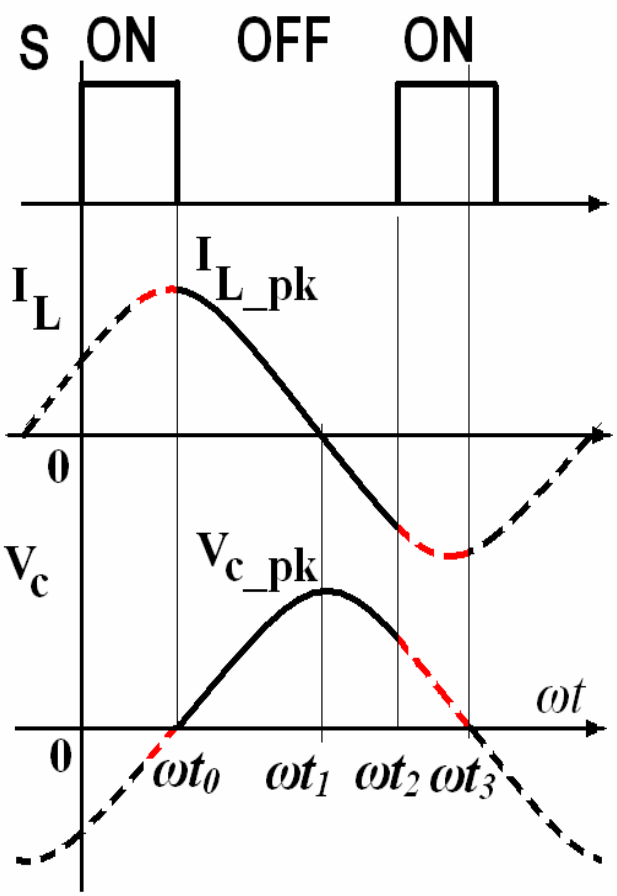
$$\sqrt{\frac{L_m}{C_S}}\left(\frac{NV_O}{2L_m f_S}\left|\cos\frac{1}{\sqrt{L_m C_{cl}}}t_{off}\right| - \frac{I_O}{N}\right) \geq V_{in} + V_{cl}$$



(b) Theoretical waveforms

Fundamentals of LC Resonance





- LC resonance as its nature can recycle the energy back to the source.
- MOSFET turn-on at reduced voltages will make less power losses.
- Efficiency is then improved.

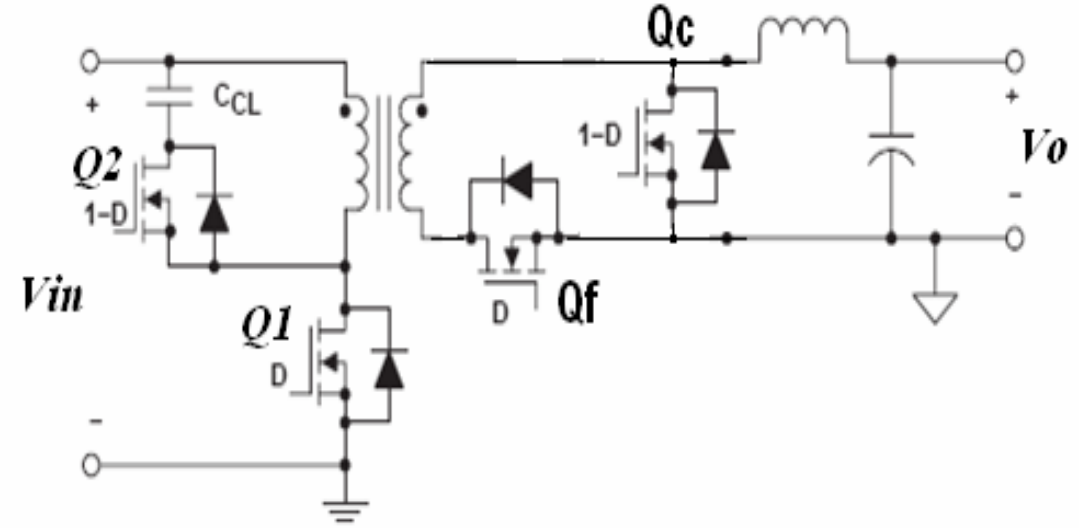
UCC2891/2/3/4/7 achieves ZVS / VVS

Two resonance present:

- Magnetizing inductance and clamp capacitor
- Magnetizing inductance and equivalent Cds

$$\omega_{CL} = \frac{1}{\sqrt{L_M \times C_{CL}}}$$

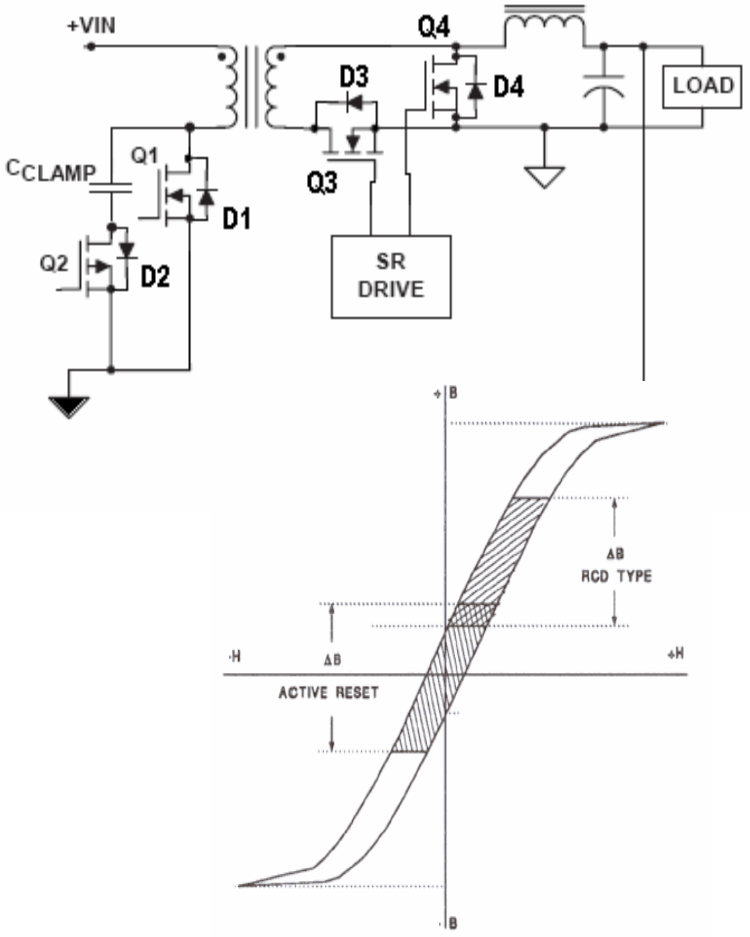
$$\omega_R = \frac{1}{\sqrt{L_M \times C_{DS}}}$$

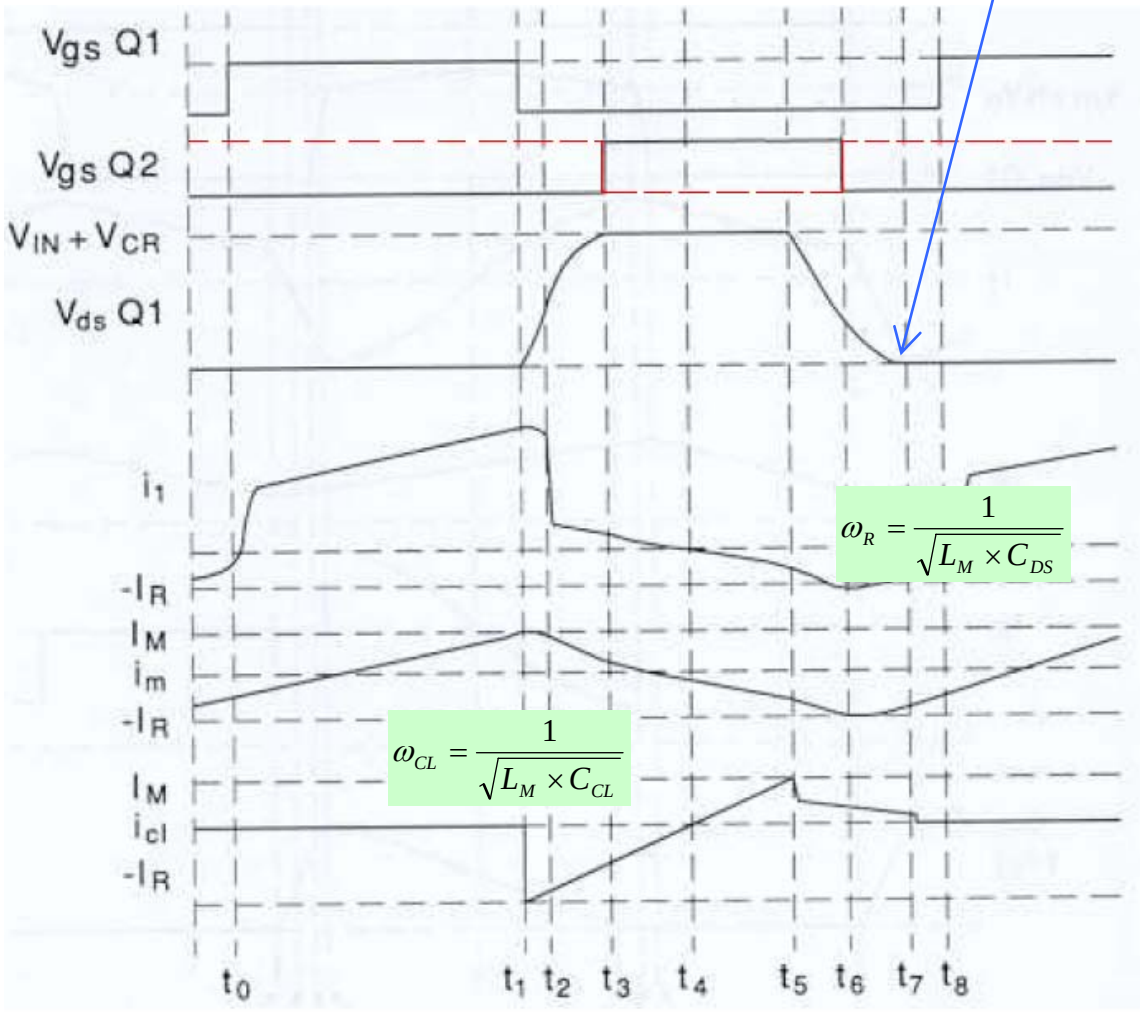


$$\sqrt{\frac{L_M}{C_{DS}}}\left(\frac{N \times (V_O + V_{O,misc})}{2 \times L_M \times f_{sw}}\left|\cos\left(\frac{1}{\sqrt{L_M \times C_{CL}}} \times t_{off}\right)\right| - \frac{I_O}{N}\right) \geq V_{in} + V_{CL}$$

Review of Active Clamp Reset Technique

Vds reversed, body diode clamped





- Voltage Clamp
- Transformer reset

How to get ZVS?

- **Magnetizing current direction reversed before clamp FET turns off**

- **Magnetic field energy (current) sufficient:**
  - lower the magnetizing inductance

- **Primary side:**
  - a higher primary leakage or an external saturable inductor (MagAmp)

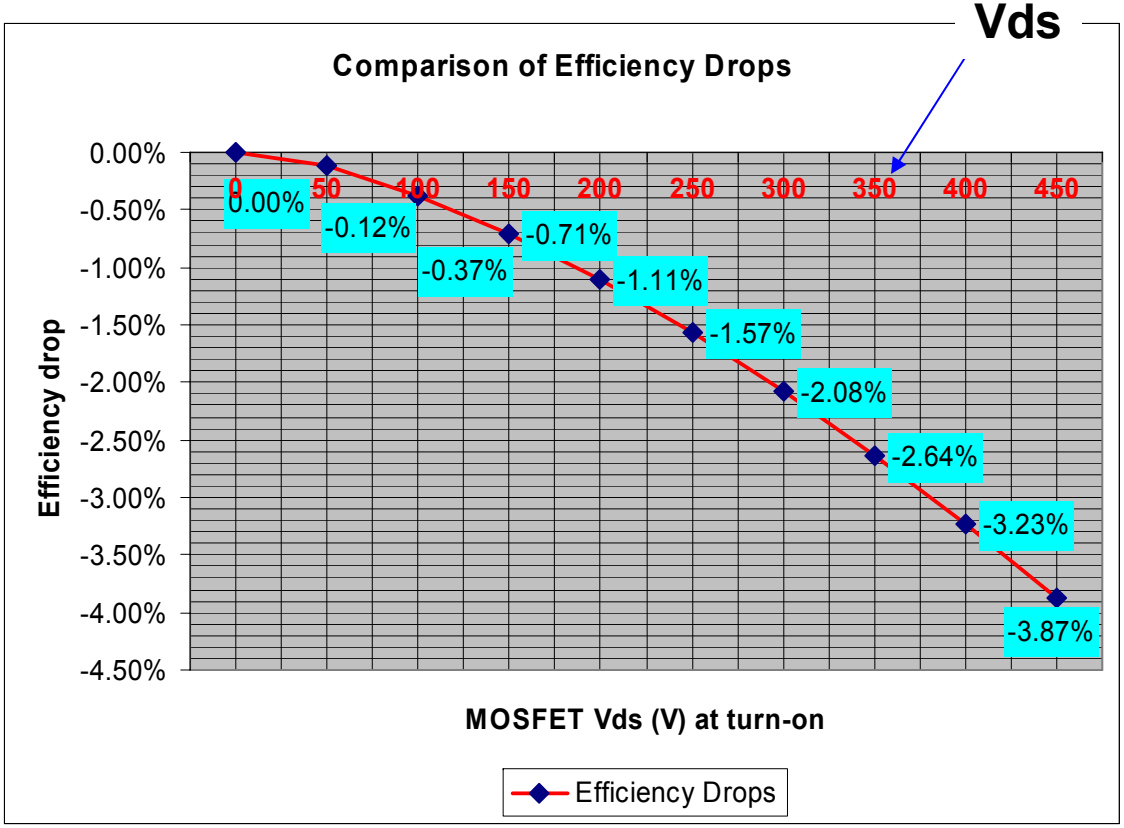
- **Secondary side:**
  - an external saturable inductor (MagAmp) to block magnetizing current discharging from the secondary loop for a short time.

Switching Power Loss due to Cds Energy Discharged at Turn-on with respect to the Vds

The efficiency drops when turn on at different Vds from a 300W converter at 20% load level:

- Turn on at Vds = 350V, -2.64%
- Turn on at Vds = 150V, -0.71%

In lower voltage applications, efficiency improvement may not be significant.



- Efficiency drop vs Vds variation.

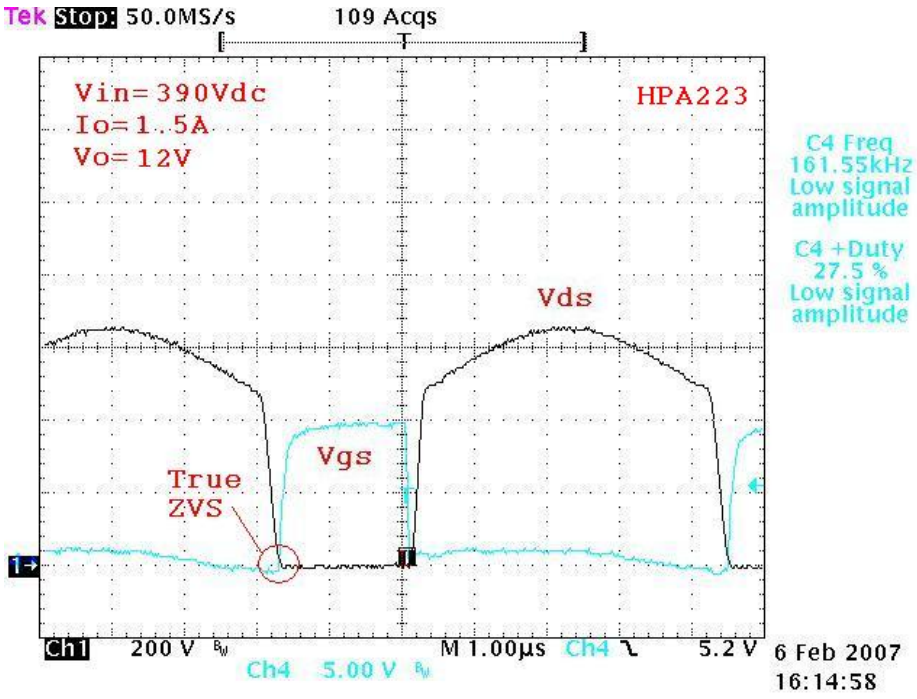
fsw = 200kHz and Cds = 500pF @ Vds = 25V.

ZVS / VVS Observation Using UCC2984

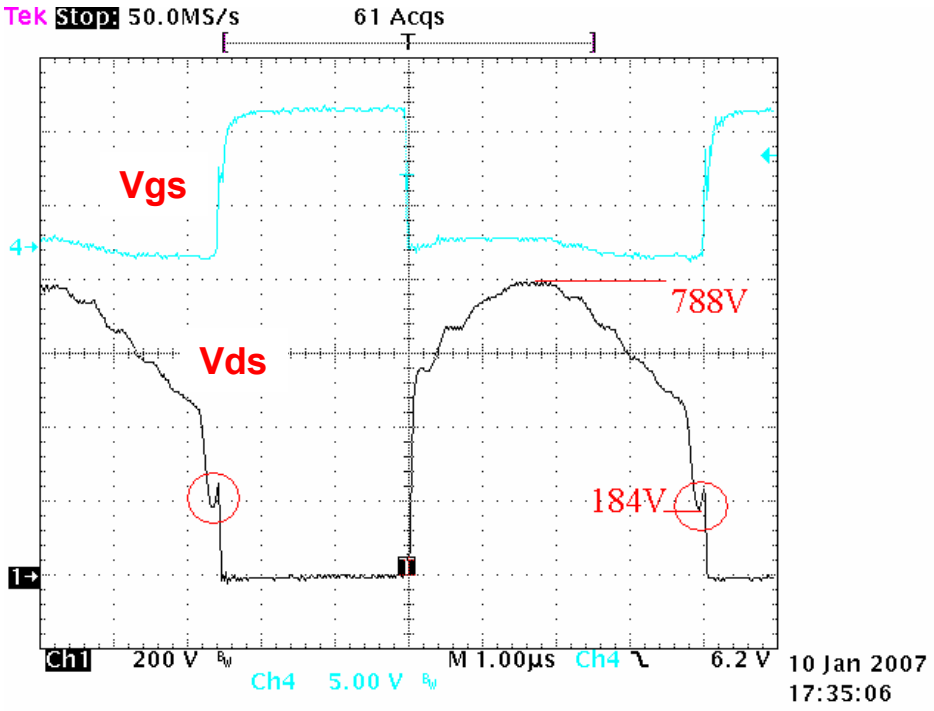
ZVS/VVS can be achieved by properly and adequately lowering the magnetizing inductance Lm to improve the efficiency in off-line applications.

Vin = 390V, Vo = 12V, Lm = 0.65 mH

ZVS achieved at Io = 1.5A



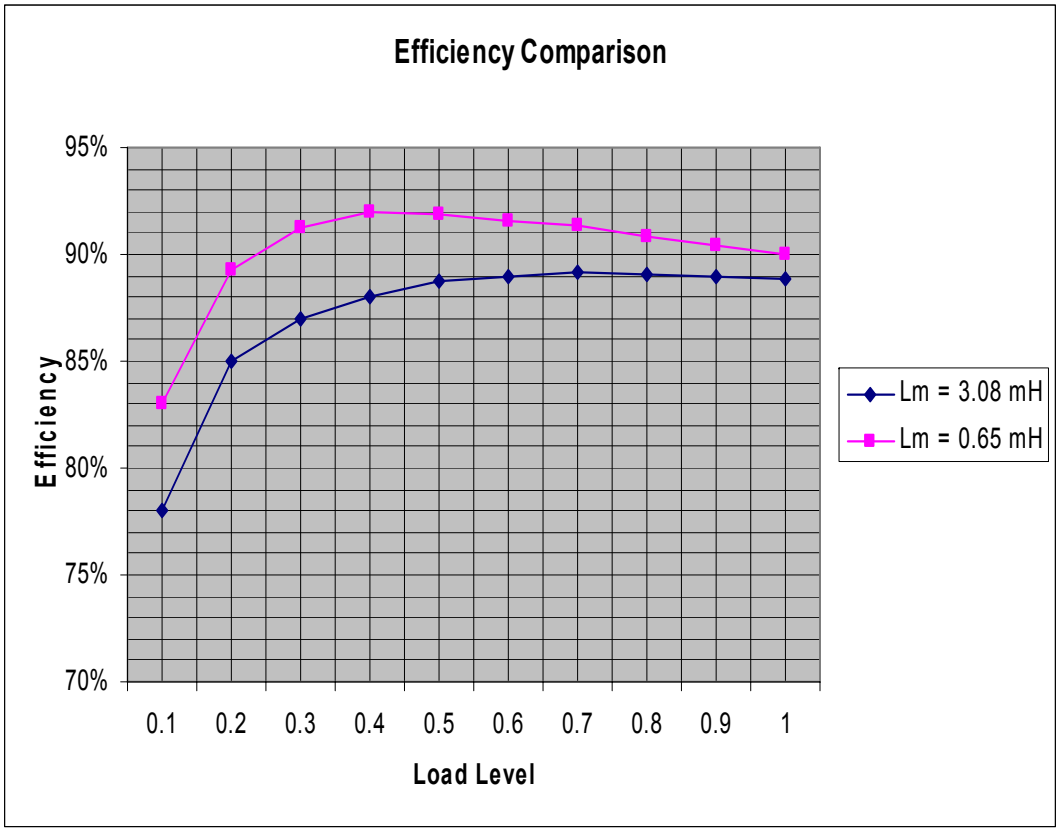
VVS achieved at Io = 26A



UCC2984 EVM Efficiency Test Results and Comparison

Efficiency results from different design of magnetizing inductance:

- Lm = 3.08mH, valley voltage about 350V
- Lm = 0.65mH, valley voltage about 180V
- test conditions:
  - fsw = 160kHz
  - Vin = 390V
  - Vo = 12V
  - Full load = 320W

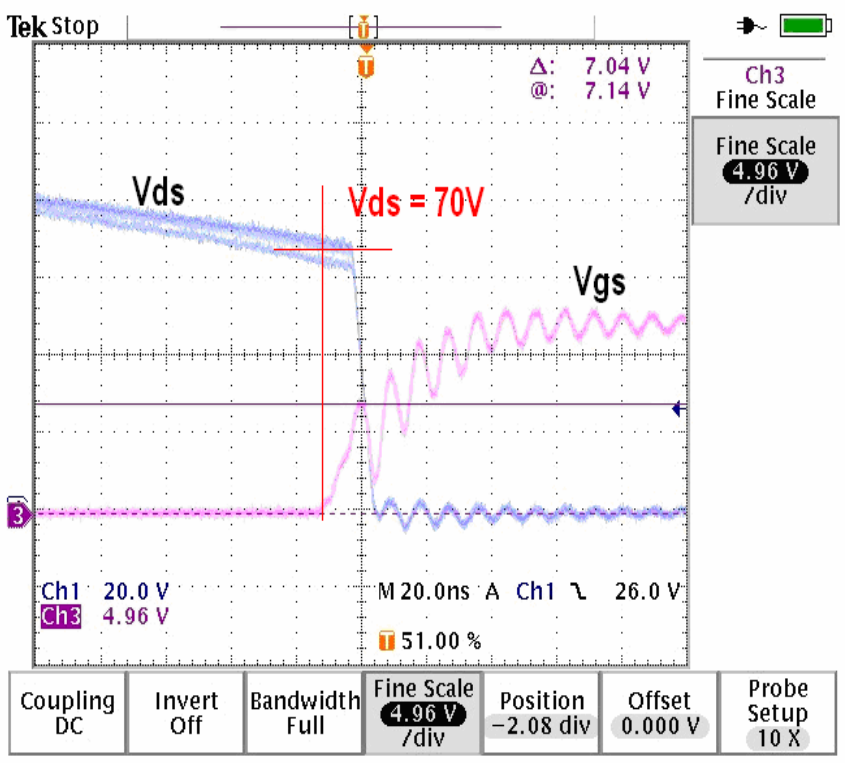


Load Level = 1 representing full load 320W

ZVS observations on ACFC (UCC2891/7 EVM)

Lm = 95 µH

Vin = 42V, Vo = 3.3V, Io = 0A



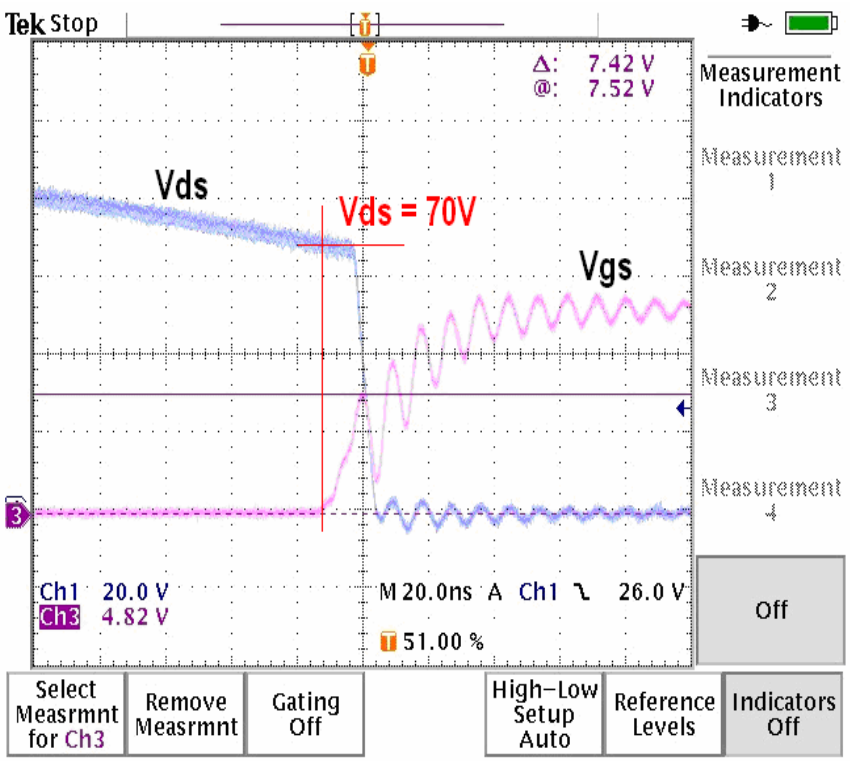
Lm = 25 µH

Vin = 40V, Vo = 3.3V, Io = 0A

ZVS observations on Active Clamp Forward Converter

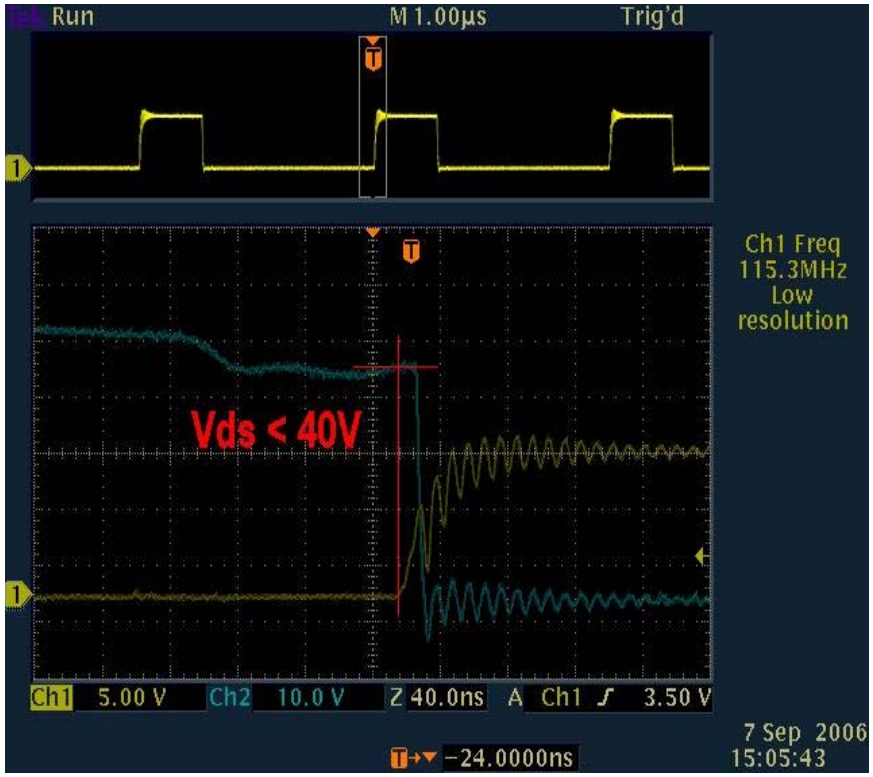
Lm = 95 µH

Vin = 42V, Vo = 3.3V, Io = 15A



Lm = 25 µH

Vin = 40V, Vo = 3.3V, Io = 10A



Issues from self-driven SR in ACFC

- **Power shutdown oscillation**

  * cause: self-driven SR feedback the capacitor stored energy to the primary

  * solutions:

  - soft stop to control secondary capacitor discharge – most effective way

  - using control-driven SR

  - rating the avalanche energy high enough ($\frac{1}{2}C_O V_O^2$), or the voltage rating high enough

- **Oscillation from fast load step down change**

  * cause:

  - control lost after duty cycle reached zero from the load step down change

  - self-driven SR feedback the capacitor stored energy to the primary

  * solutions:

  - slower loop response design;

  - higher Dmax design

- **Reversing current at light load and no load**

  * cause: self-driven SR catch FET conducting

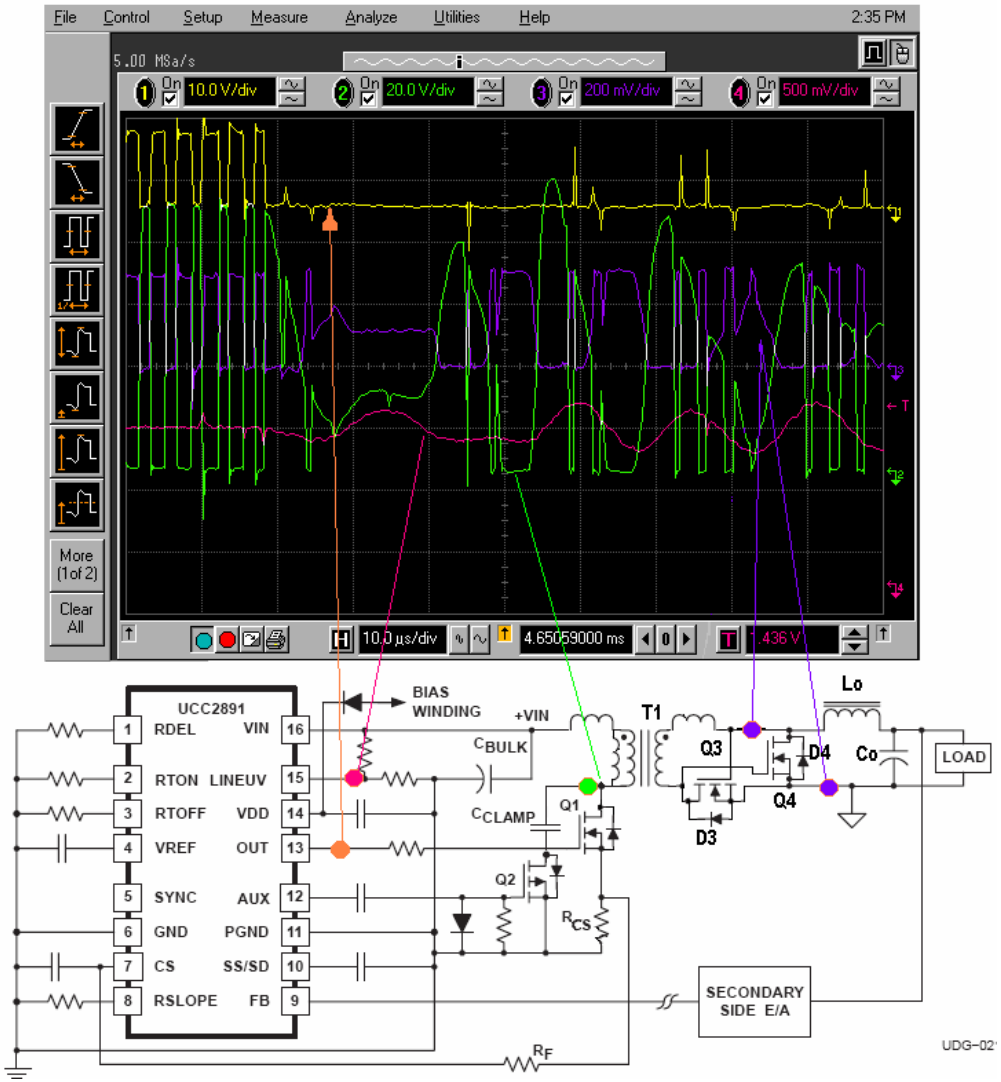
  * Solutions:

  - Using control-driven SR

  - Turning off SR

Power Shutdown (LineUV) Oscillation

- Observations



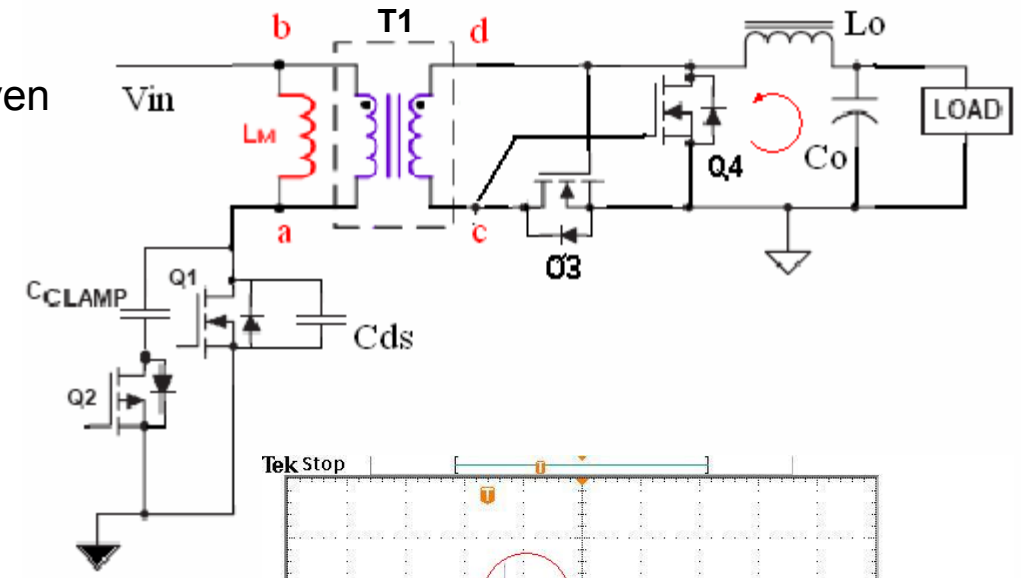
Mechanism of the Oscillation during Power Shutdown

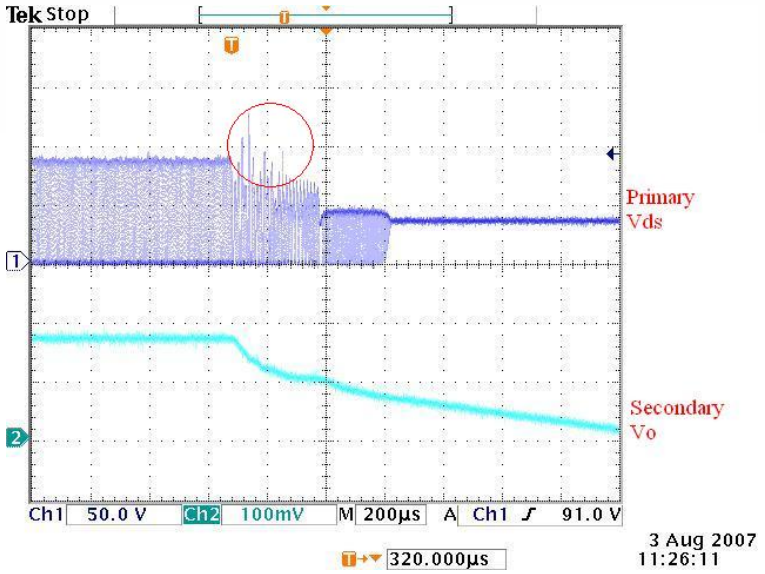
- Oscillation from secondary energy feedback to the primary from self-driven SR during power shutdown

LineUV (power shutdown) →

T1 a(+) and c(+) →
Q4 on and reverse Lo current →
T1 b(+) and d(+) →
Q3 on (energy transfer to primary) →
Magnetizing current reduction →

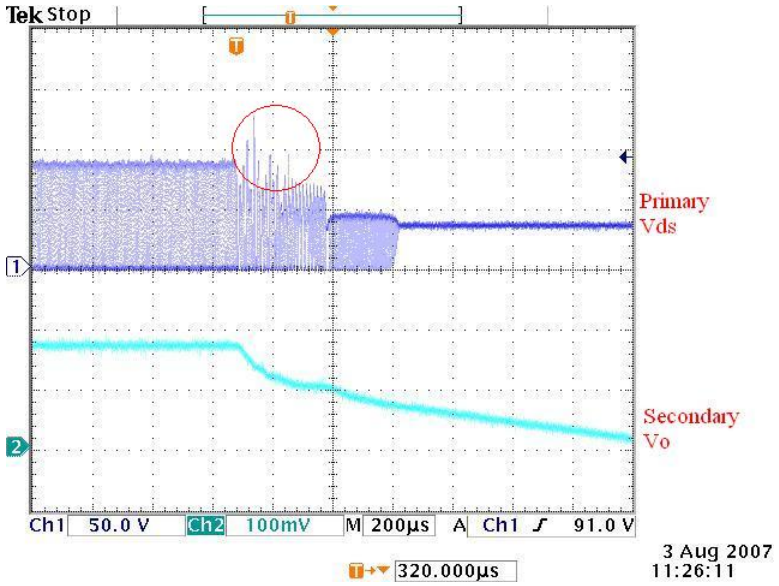
T1 a(+) and c(+) → Loop…

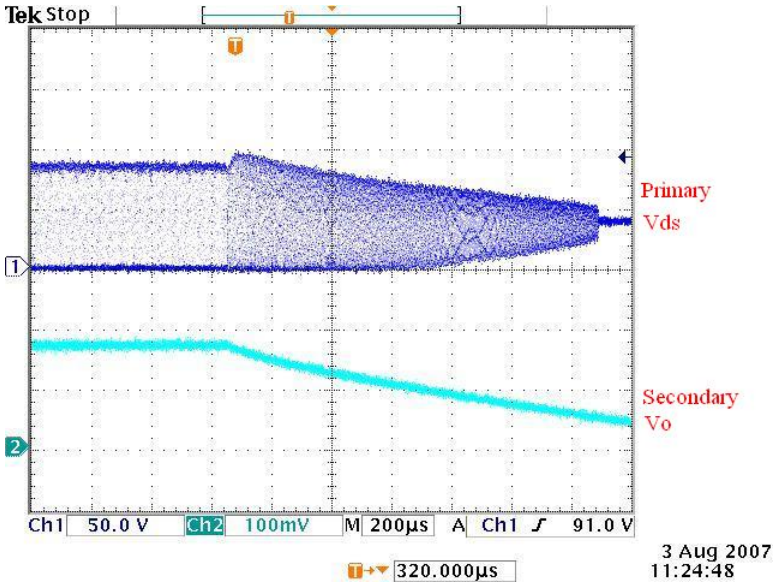




With soft stop, both Q1 and Q2 are controlled during power down. The secondary stored energy will be discharged in control manner. The oscillation then will be eliminated, refer to the 2nd slide.

Power Shutdown (LineUV) Oscillation





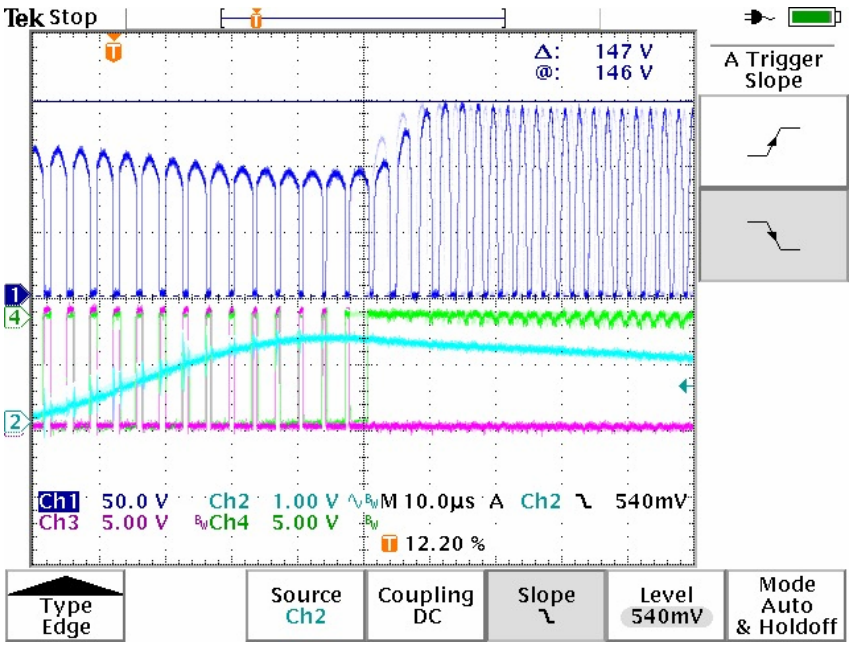
- Oscillation appears during power shutdown without soft stop

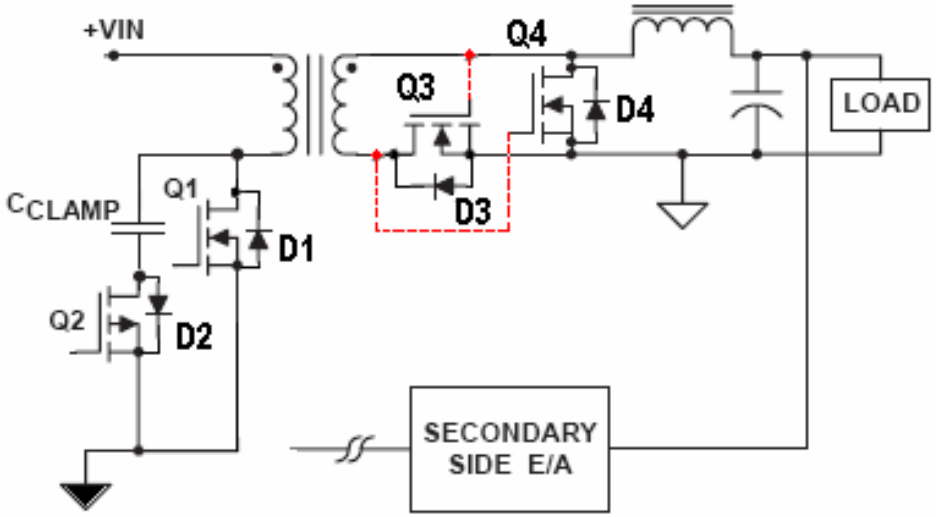
- Oscillation does not appear during power shutdown with soft stop
  - using SS/SD pin and a comparator
  - feature to be added

Load Transient Ringing

- Load step down change (30A to 3A) at 72Vin, 3.3Vo:

  High voltage swing across Q1 drain and source

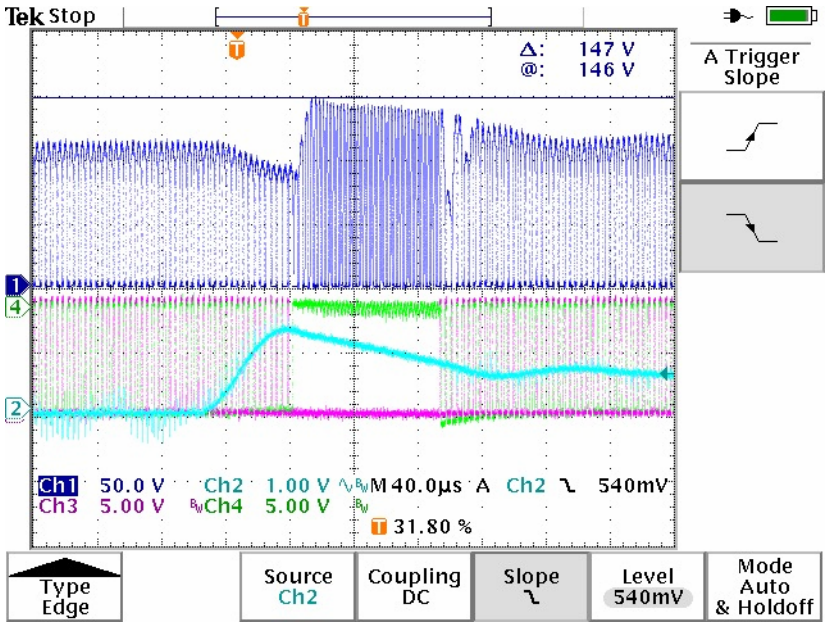


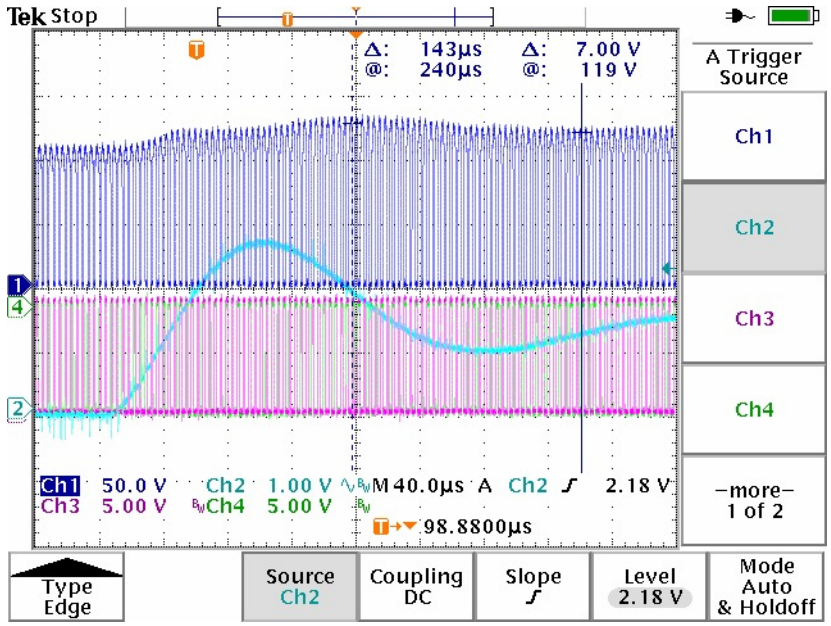


Load Transient Ringing

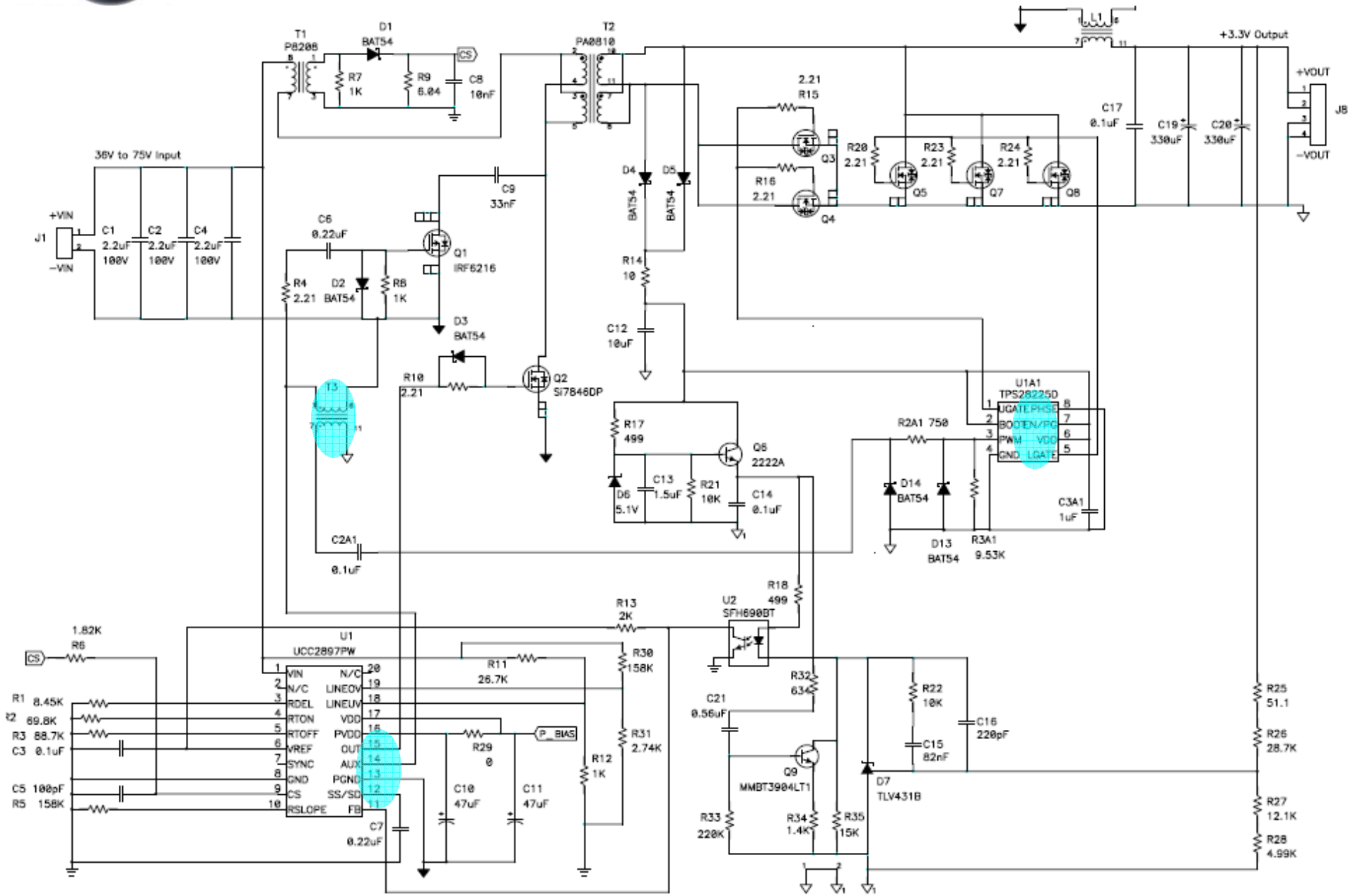
- Mechanism
  - control lost after duty cycle reached zero from load step down change
  - secondary self-driven SR oscillation
- Fast loop compensation, or
- High maximum duty cycle setup

- With slower loop compensation or reduced maximum duty cycle
- Vds swing peak reduced
- Vo load transient response becomes slower



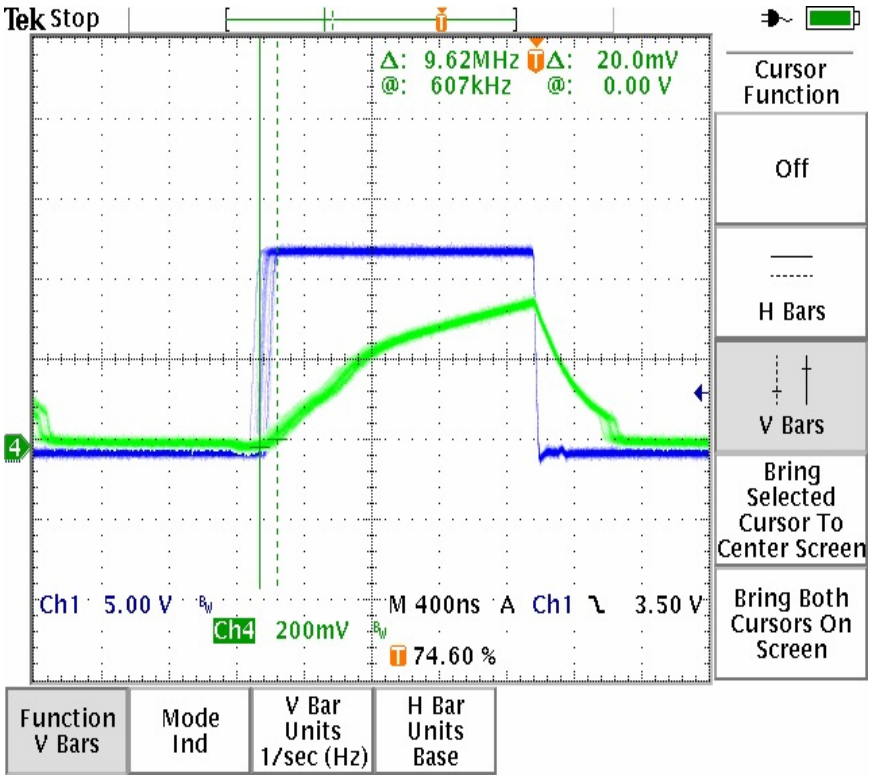


TPS28225 used for the control drive

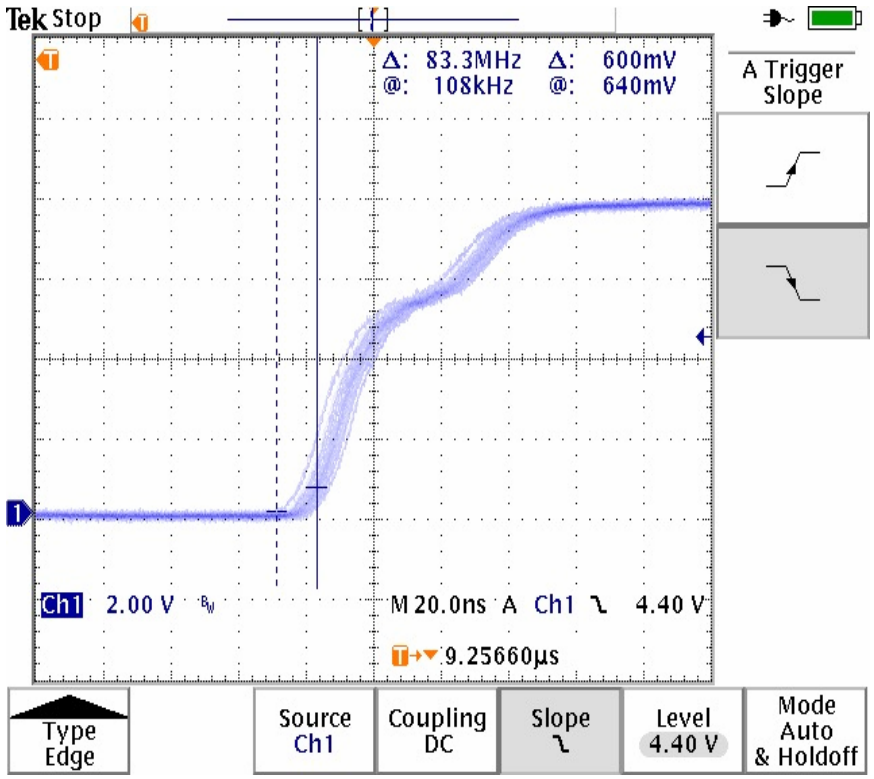


Gate Drive Signal Jitter - solutions

- Jitter: 120 ns (VDD ≥ 9.2V)



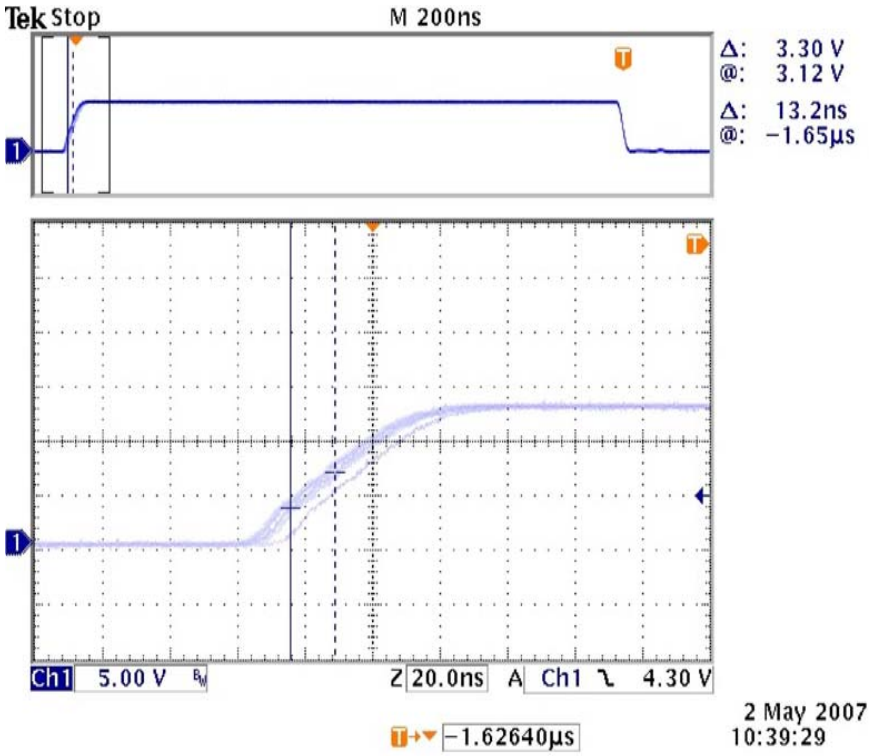
- Jitter 12 ns (VDD < 9.2V)



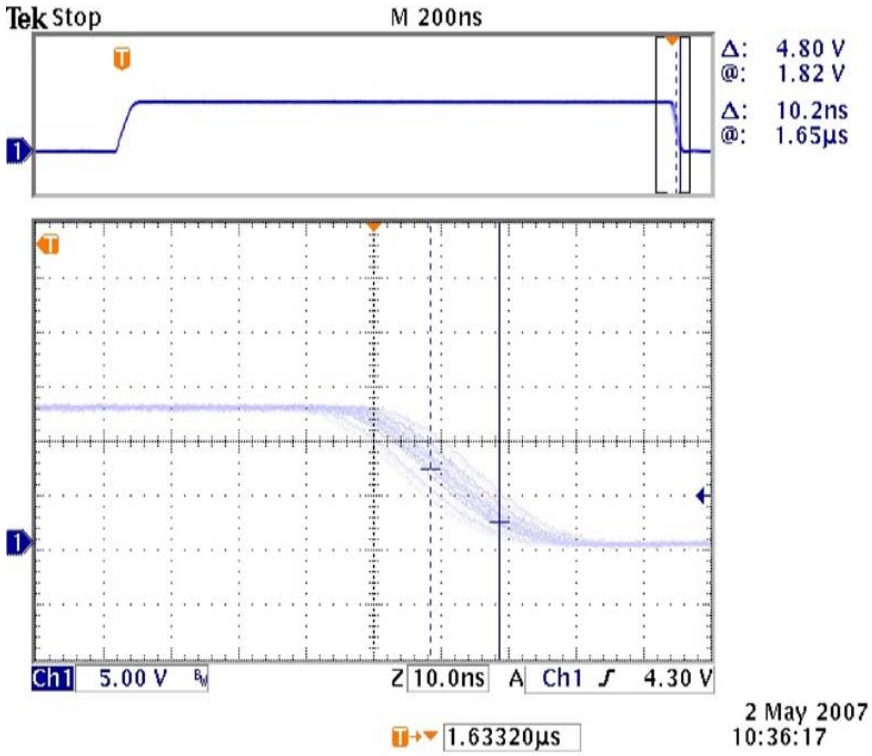
External Solution: set up VDD between 8.5V and 9.2V

Gate Signal Jitter (root cause) – fixed and tested

Persistence = 13.2ns (rising edge)



Persistence = 10.2ns (falling edge)



New Silicon (UCC2897)

- Fix gate signal jitter
- Keep LineUV as before (latch off)
- Add soft stop feature

Volt x second clamp: external solution

Off-time and On-time

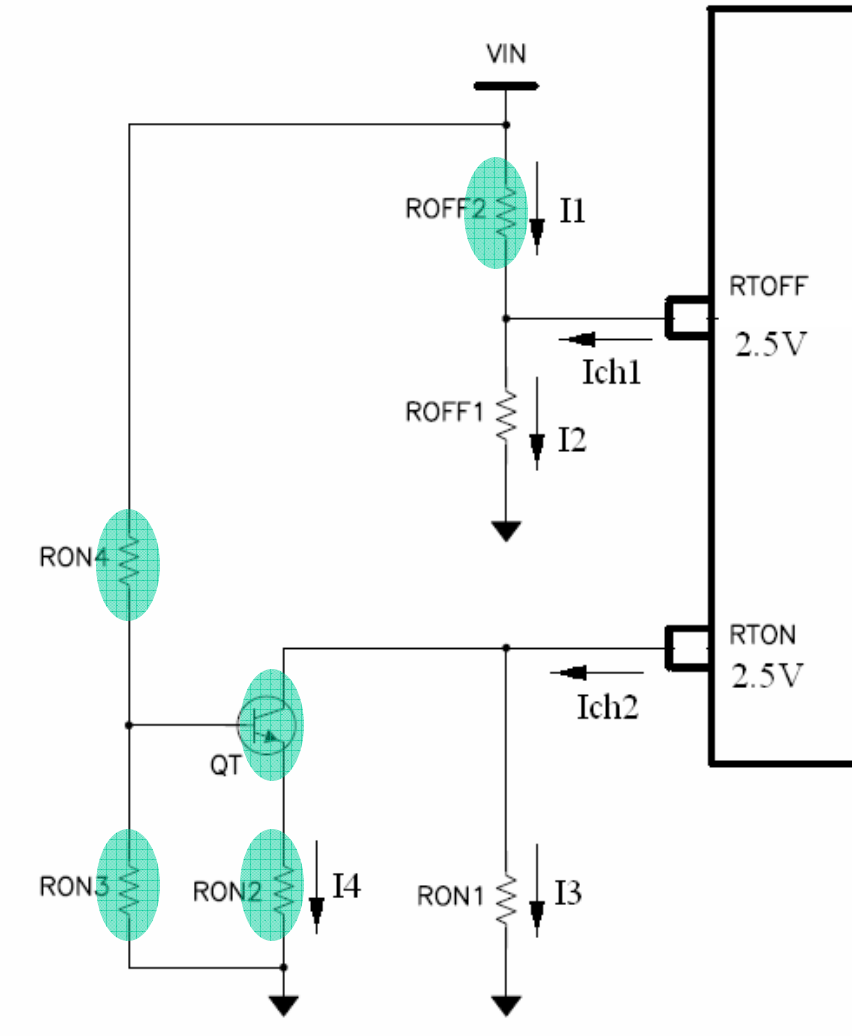
- inversely proportional to *Ich1* and *Ich2*, respectively

$$Ich1 = I2 - I1$$
$$= \frac{2.5V}{R_{OFF1}} - \frac{Vin - 2.5V}{R_{OFF2}}$$

Vin ↑ → *I*ch1 ↓ → toff ↑

$$Ich2 = I3 + I4$$
$$= \frac{2.5V}{R_{ON1}} + \left(\frac{R_{ON3} \times V_{IN}}{R_{ON3} + R_{ON4}} - V_{BE}\right) \times \frac{1}{R_{ON2}}$$

Vin ↑ → *I*ch2 ↑ → ton ↓



Volt x second clamp: external solution

Off-time and On-time

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$$Ich1 = I2 - I1$$
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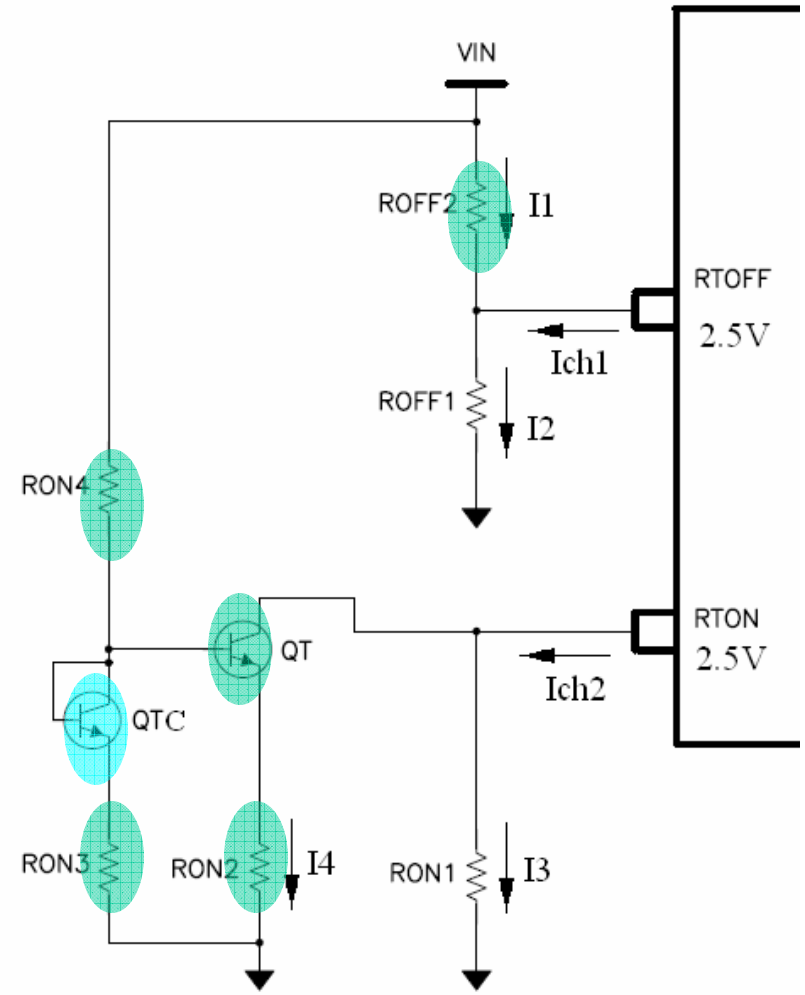
Vin ↑ → *I*ch1 ↓ → toff ↑

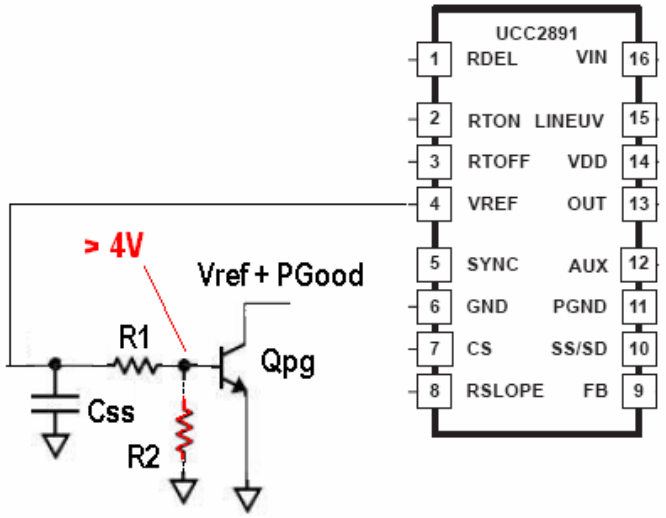
$$Ich2 = I3 + I4$$
$$= \frac{2.5V}{R_{ON1}} + \left(\frac{R_{ON3} \times V_{IN}}{R_{ON3} + R_{ON4}}\right) \times \frac{1}{R_{ON2}}$$

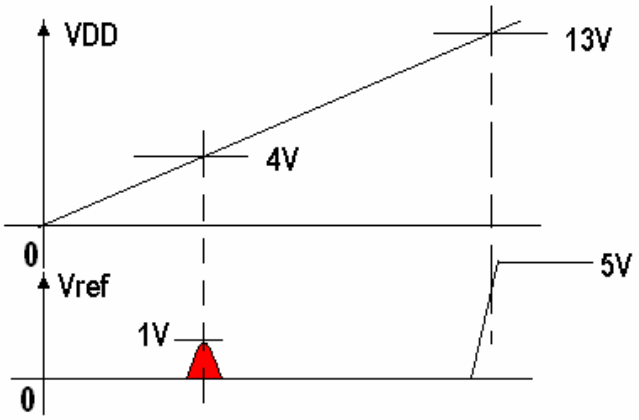
Vin ↑ → *I*ch2 ↑ → ton ↓



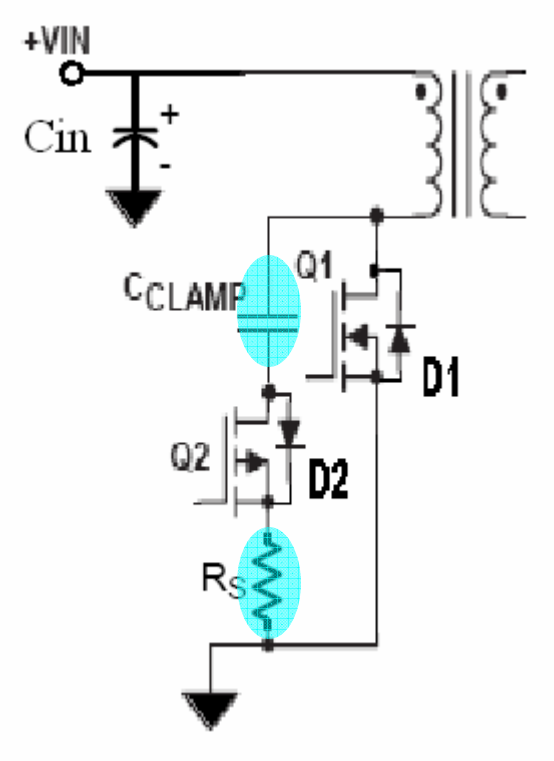
Vref-pin Glitch 1V During Power Up

- Vref has a 1-Volt spike when VDD arises about 4V during start
- When using Vref+PGood for power good signal, this may cause false Power-Good signal without R2.
- By adding R2, the 1-V spike influence on the transistor can be eliminated.

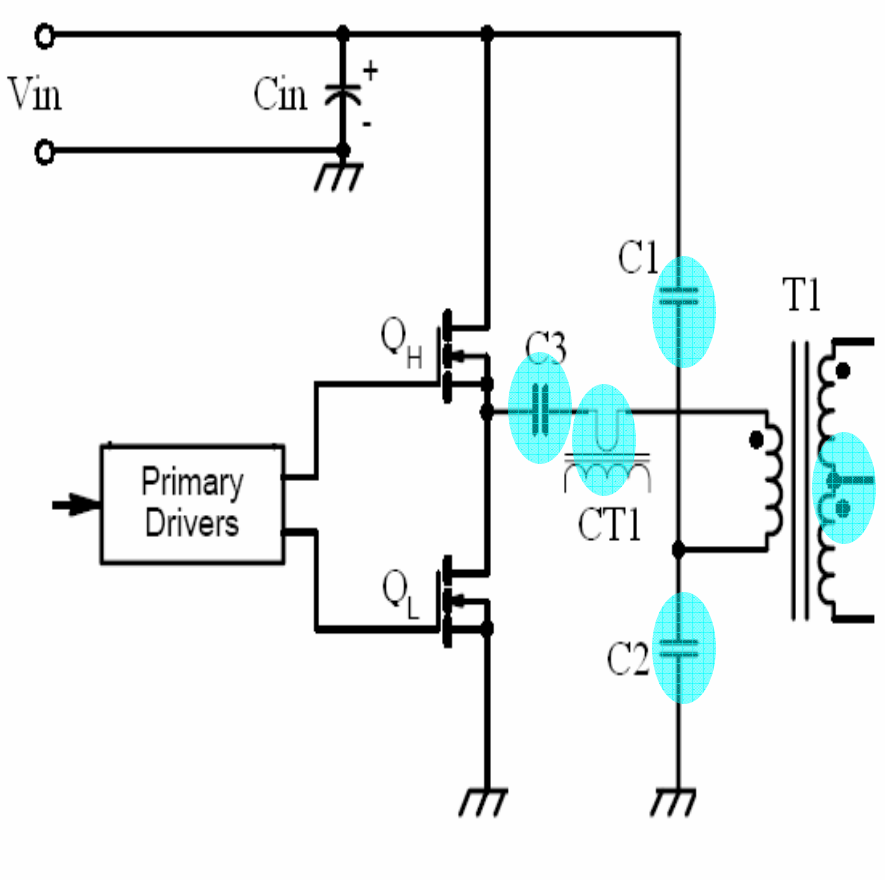




Comparison between Active Clamp Forward and HB in telecom applications



Low-side Active Clamp Forward Converter



Symmetrical HB Converter

Comparison between Active Clamp Forward and HB in telecom applications

- **Efficiency**
  - Symmetrical HB may not provide ZVS
  - ACFC ZVS/VVS
  - Critical with higher switching frequency and power density in 1/4 or 1/8 bricks

- **Switching frequency:**
  - HB doubled FET's frequency seen at input and output – may help to reduce the caps but the switching losses proportional to 0.5 x Vin hard switching
  - ACFC: MOSFET freq seen at input/output. VV Switching losses – partially soft

- **Components and board space**
  - HB: (a) High side gate driver, (b) flux imbalance caps, (c) caps for center tap point, (d) same size of high- and low side MOSFETs
  - ACFC: (a) - (b) no, (c) clamp cap, (d) clamp FET smaller one, (e) x2 voltage rating

- **Cost**
  - HB: cost for (a) – (c)
  - ACFC: cost for (c) - (e)

- **Secondary Sync Rectifier (control-driven SR)**

Comparison between Active Clamp Forward and HB in telecom applications

- **Current sensing:**
  - HB: current sensing transformer or floating sensing resistor (OpAmp may need)
  - ACFC: CT or resistor – flexibility, cost and board space

- **Transformer:**
  - HB: two windings at secondary – PCB design complication, center-tap, more space
  - ACFC: single winding at secondary
  - Critical with higher switching frequency and power density in 1/4 or 1/8 bricks

- **Transient response:**
  - HB may be faster than ACFC (clamp cap)

- **Secondary Sync Rectifier**
  - HB: not able to make self-driven (extra winding may need)
  - ACFC: self-driven ok (control-driven available with TPS28225 or similar)

- **Summary:**
  (a) Similar total cost with ACFC slightly lower
  (b) ACFC slightly less component count
  (c) ACFC higher efficiency and less board space – higher power density possible for the same cost and board space

The POWER Behind Your Designs

THANK YOU!

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