Application Report
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Designing for High Efficiency with the Active Clamp UCC2891 PWM Controller

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ABSTRACT

The UCC2891 Current Mode Active Clamp PWM Controller offers a highly integrated feature set resulting in precision control required for an active clamp forward or flyback converter. The UCC2891 data sheet contains all the design details necessary for accurately programming the IC. However, there are significant design considerations and trade-offs unique to the active clamp power stage that must be defined prior to setting up the control IC. Using the active clamp forward topology as an example, the clamp, power stage and control loop compensation is detailed in the following application note, which is intended to complement the information presented in the UCC2891/2/3/4 data sheet.

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1 INTRODUCTION

The single ended forward converter is a popular choice for single and multiple output power supplies within the range of 50 W to 500 W. While there are several widely used techniques for achieving transformer reset, the active clamp approach is by far the best in terms of simplicity and optimal performance. ZVS (zero voltage switching), lower switch voltage stress, extended duty cycle range and reduced EMI (electro-magnetic interference) combined with significant efficiency improvements are just a few of the reasons to consider the active clamp reset technique.

One of the disadvantages associated with the active clamp is the need for a precise duty clamp. If not clamped to some maximum value, increased duty cycle can result in transformer saturation or additional voltage stress on the main switch which can be catastrophic. Another disadvantage has been the need for an advanced control technique to synchronize delay timing between the active clamp and main switch gate drive. One of the many features of the UCC2891 is the programmable maximum duty cycle clamp accurate to within ±3 percent. The UCC2891/2/3/4 offers the capability to drive either a P-channel or N-channel clamp switch in either a high-side or low-side configuration. With a programmable delay time between the main switch and clamp switch, the disadvantages historically associated with using the active clamp technique are non-existent when the UCC2891 is used as the control IC.

For any power supply design, the success of meeting a set of given design specifications starts with a carefully designed power stage, control loop and finally setting up the PWM controller. For the active clamp forward topology there are some additional considerations that shall be discussed within the context of the following design example. While the example presented herein highlights the use of the UCC2891 PWM control IC, the design procedure for the power stage, active clamp, control loop and PWM set-up as well as the theoretical development pertaining to ZVS are applicable UCC2891/2/3/4 and UCC2897.

2 ACTIVE CLAMP SWITCHING FUNDAMENTALS

Before the power stage can be designed, it is important to first understand the basic timing that is fundamentally unique to the active clamp reset. References [6] and [7] present eight distinct switching intervals, delving deeply into the active clamp current commutation. Using a low-side active clamp configuration as an example, a complete switching cycle, t0→t4, can be simplified and explained by four distinct switching intervals as detailed in Figure 1 through Figure 4.

2.1 t0 → t1: Power Transfer

During this state power is transferred to secondary as the main switch, Q_{MAIN}, is conducting and, under the right conditions, has just turned on under ZVS since its body-diode was previously conducting (see Figure 4). The primary current is flowing through the channel resistance of Q_{MAIN} and is made up of the transformer magnetizing current plus the reflected secondary current. On the secondary side, the forward synchronous rectifier, Q_F, is on and carrying the full load current. In the previous state, the load current was freewheeling through the body-diode of the reverse synchronous rectifier, Q_R, so Q_F is subjected to some turn-on loss as it is hard switched.

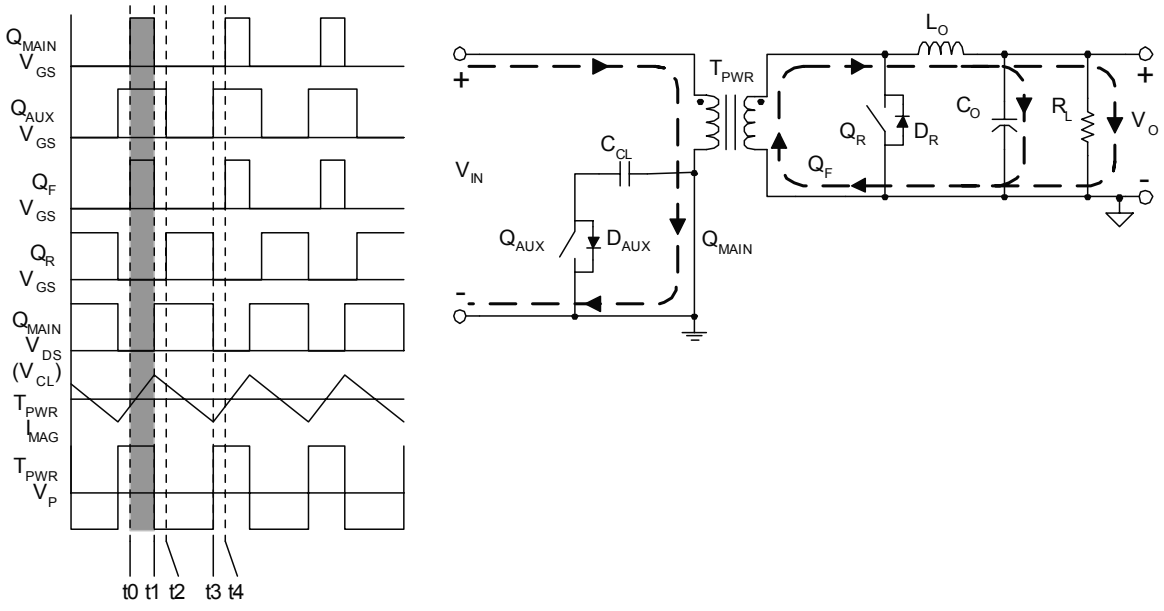


Figure 1. t0 → t1: Power Transfer Interval

2.2 t1 → t2: Resonant

This is the first of two resonant states occurring within one full switching cycle. During this state Q_{MAIN} has turned off under ZVS and the primary current remains continuous as it is diverted through the body diode, D_{AUX}, of the clamp switch, Q_{AUX}. Because of the direction of the primary current flowing through D_{AUX}, Q_{AUX} must be a P-channel MOSFET (body-diode pointing down) for low-side active clamp applications. Since the secondary load current is freewheeling, there is no reflected primary current, so the only current flowing through D_{AUX} is the transformer magnetizing current. Therefore the body-diode conduction loss of Q_{AUX} is minimal and the conditions are set for Q_{AUX} to turn on under ZVS. The delay time between Q_{MAIN} turn-off and Q_{AUX} turn-on, also known as the resonant period, distinguishes the active clamp from other single ended transformer reset methodologies. On the secondary side Q_F has turned off under hard switching, and the full output load current is now freewheeling through D_R. For high current applications the body-diode conduction loss of D_R, can be a major contributor to total power loss, and is often one of the key factors limiting higher frequency operation. However, the conduction of D_R is also necessary for Q_R to turn on under ZVS. Although not possible with self-driven synchronous rectification, we would prefer to minimize the conduction time of D_R ideally to zero, but still allow Q_R to turn-on under ZVS.

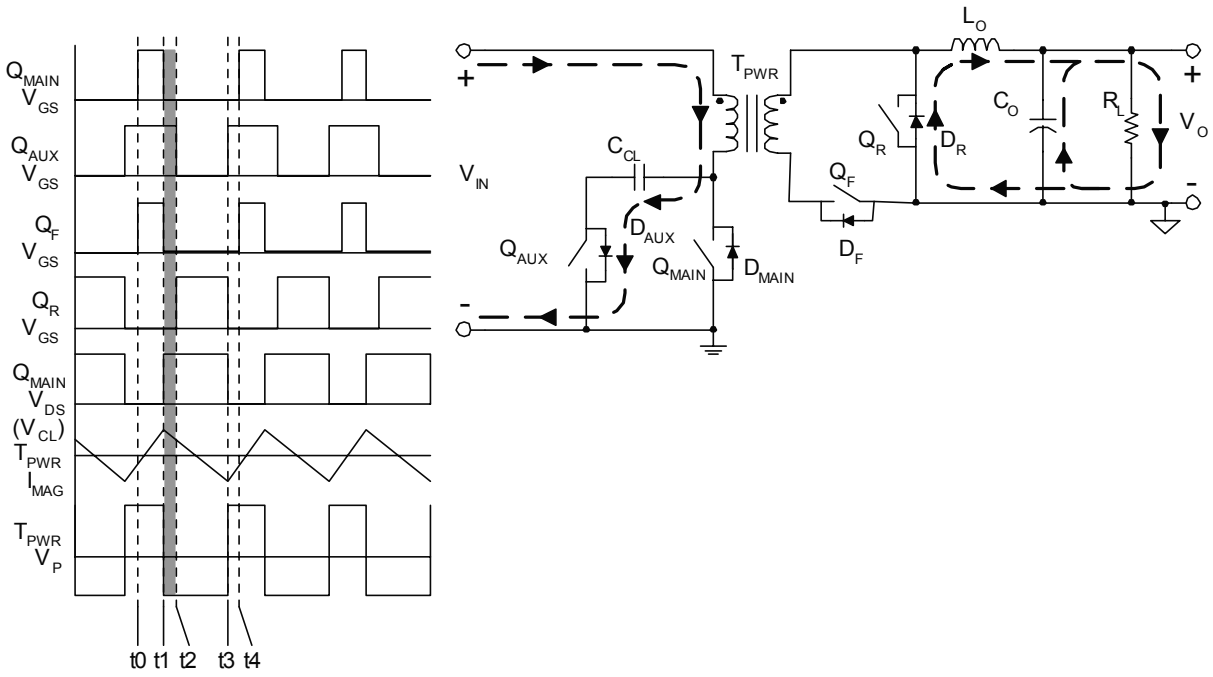


Figure 2. t1 → t2: Resonant Interval

2.3 t2 → t3: Active Clamp

This is the active clamp state where the transformer primary is reset. Although the schematic of Figure 3 shows an immediate reversal of the primary current, the transition from positive to negative current flow is actually smooth and had really begun during the previous state when the magnetizing current had reached its maximum positive peak value. On the primary side, Q_{AUX} is now fully turned-on as the difference between the input voltage, V_{IN}, and the clamp capacitor voltage is now applied across the transformer primary. Q_{AUX} is subject to minimal conduction loss as only the magnetizing current is flowing through the channel resistance. Conversely, on the secondary side, Q_R is carrying the full load current through its channel resistance and is experiencing high conduction loss.

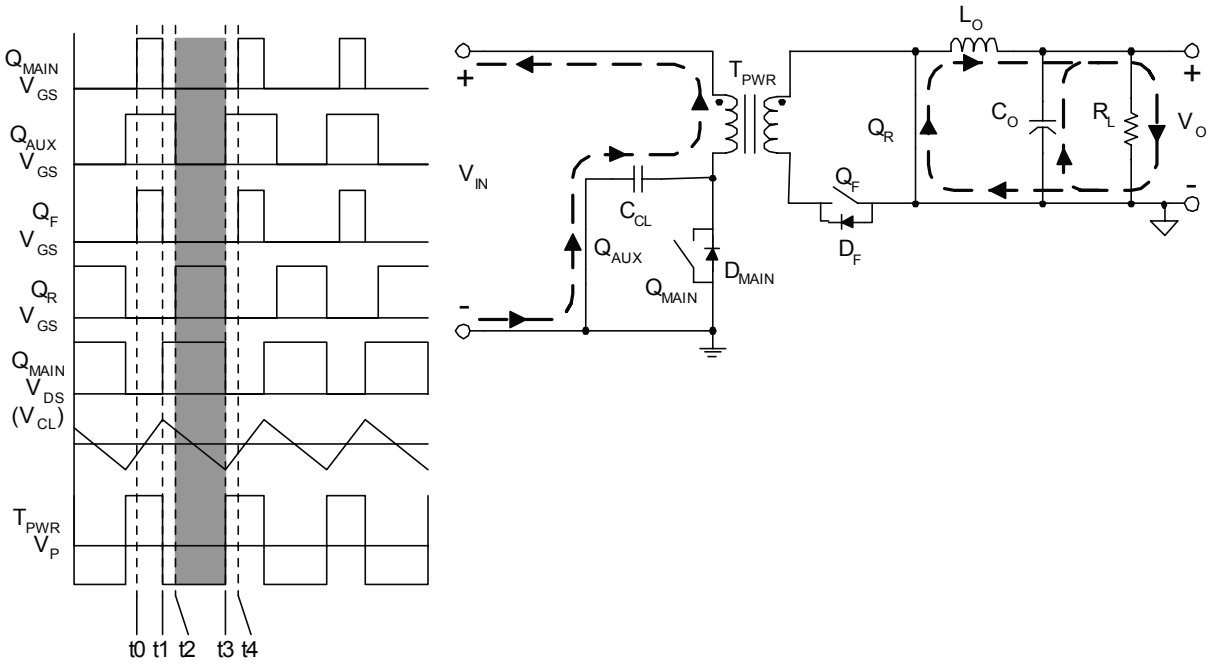


Figure 3. t2 → t3: Active Clamp Reset Interval

2.4 t3 → t4: Resonant

This is the second of two resonant states occurring within one full switching cycle. During this state Q_{AUX} has turned off under ZVS and the primary current remains continuous as it is diverted through the body diode, D_{MAIN}, of Q_{MAIN}. Again, the primary current is shown flowing negative but it is during this switching state that the current actually begins to make the transition to reverse direction. This is supported by the magnetizing current waveform which is shown at its maximum negative peak value. The body diode of Q_{MAIN} begins to conduct setting up the conditions for Q_{MAIN} to turn on under ZVS. It should be noted that under certain conditions Q_{MAIN} may not experience ZVS at turn-on. This shall be further explained in Section 4.4. On the secondary side, D_R begins to conduct just before Q_R turn-off. Therefore Q_R turns off under ZVS, but similar to the t1→t2 state also experiences unavoidable power loss due to body-diode conduction. At the completion of t4, the switching cycle reverts back to the t0→t1 state and the sequence repeats.

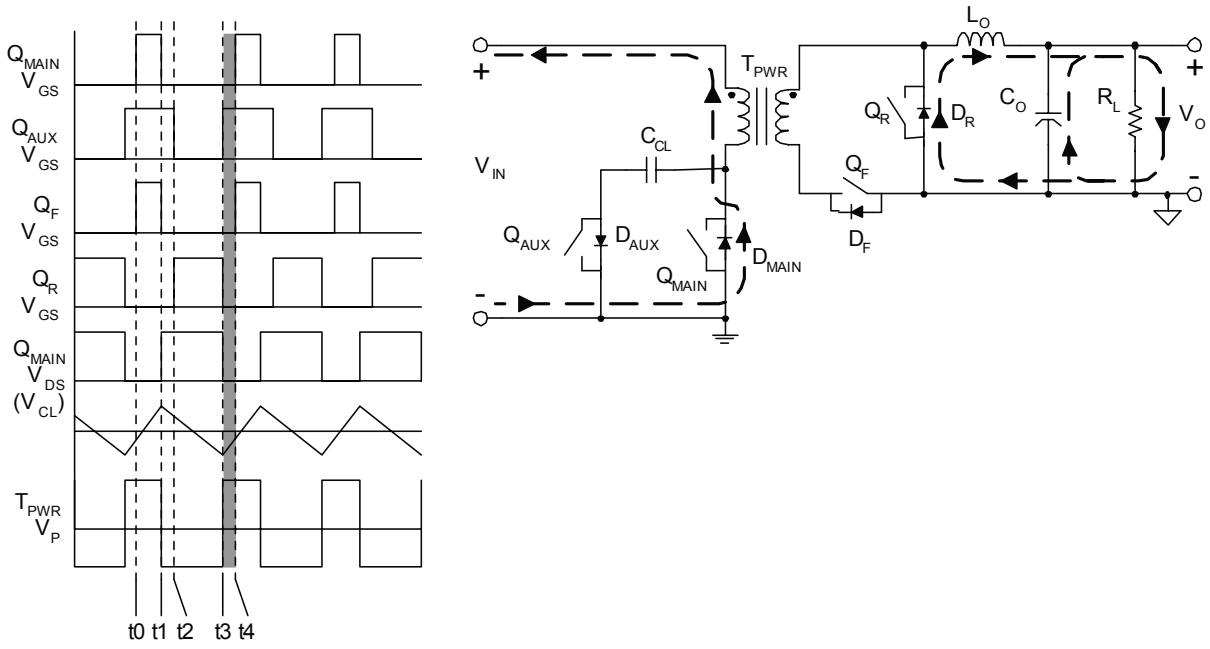


Figure 4. t3 → t4: Resonant Interval

3 DESIGN SPECIFICATIONS

To demonstrate the benefits of the UCC2891 Active Clamp PWM controller, a 100 W forward converter capable of delivering up to 30 A at 3.3 V output is designed. The converter must operate from a telecom input voltage of 36 V<V_{IN}<72 V. Some of the key electrical design specifications are listed in Table 1. Mechanically, a target of fitting the design within an industry standard half-brick has also been imposed.

Table 1. UCC2891 Design Example Specifications

Parameter	Symbol	Min	Typ	Max	Units
Input Voltage Range	V_{IN}	31	48	72	V
Input Turn-On Voltage	V_{ON}		35		
Input Turn-Off Voltage	V_{OFF}		34		
Full Load Efficiency	η	85%	90%		
Duty Cycle	D			0.6	
Output Voltage	V_O	3.135		3.465	V
Output Voltage Ripple	$\Delta V_{O(RIP)}$		33		mVpp
Output Load Current	I_O	0		30	A
Output Current Limit	I_{LIM}			32	
Switching Frequency	F_{SW}	275		325	kHz
Control Loop Bandwidth	BW	5		10	
Phase Margin	φ_M	30		60	Degrees
Ambient Temperature	T_A		25	40	°C

4 POWER STAGE DESIGN

A top-level diagram of the critical components that make up the active clamp forward converter power stage is shown in Figure 5.

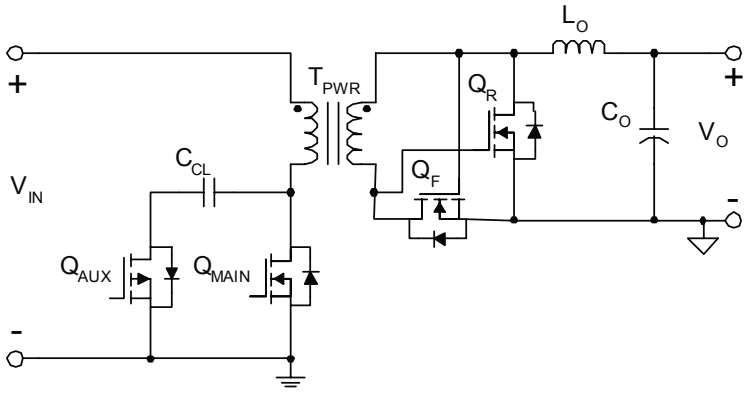


Figure 5. Active Clamp Forward Converter Power Stage

The active clamp portion of the power stage consists of the auxiliary (AUX) switch, Q_{AUX}, and the clamp capacitor, C_{CL}. Because Q_{AUX} is referenced to the primary side ground, this is referred to as a low-side clamp configuration. The details of the active clamp components are discussed in section 4.3.

For a 3.3 V output with 30 A of output current, synchronous rectification is used on the output side to maintain high efficiency especially at maximum load current. For ease of use and simplicity, self-driven synchronous rectification is chosen as shown by the forward rectifier, Q_F and the reverse rectifier, Q_R.

The power stage design begins with selecting the secondary side output components.

4.1 Output Power Stage Design

The maximum duty cycle for a forward converter using a third winding reset scheme is normally limited to 50 percent. RCD clamp and resonant reset forward converters can slightly exceed 50 percent, but the active clamp reset can easily push the maximum duty cycle to 60 percent and has even been used as high as 70 percent in some lower voltage applications. For this example the maximum duty cycle, during normal operation, is limited to 60 percent at 36V input. At 72 V input the duty cycle is approximately 30 percent.

The output inductor, L_O, can be calculated by first assuming a maximum allowable inductor ripple current, ΔI_{LO}.

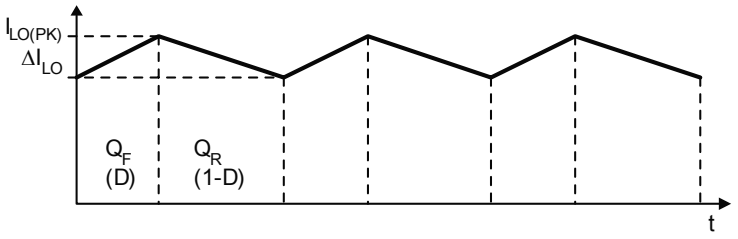


Figure 6. Output Inductor Current Waveform

4.1.1 Output Inductor

Assuming a peak-to-peak inductor ripple current equal to 15 percent of the maximum output current, Faraday's Law (1) can be applied to solve for L_O, as given by (2).

$$L_O = \left(\frac{V_O}{0.15 \times I_{O(MAX)} \times F_{sw}} \right) \times \left(1 - D_{MIN}\right) \quad (1)$$

$$L_O = \left(\frac{3.3V}{0.15 \times 30A \times \left(275 \times 10^3 Hz\right)} \right) \times \left(1 - 0.3\right) = 1.87 \mu H \quad (2)$$

Rounding up results in less ripple current through the inductor, while rounding down allows more ripple current and a smaller inductor value. Bear in mind, that as ΔI_{LO} is allowed to increase, the RMS ripple current into the output capacitor increases, as does any switching loss experienced by the output rectifiers. These are the trade-offs that must be looked at when deciding on the optimal value of L_O. For this design, off the shelf (OTS) planar magnetics are used because of their low mechanical profile and repeatable design characteristics. The PA0373 from Pulse is a 2 µH planar design rated at 30 Adc, with a saturation current rating of 35 A. The PA0373 also includes a 1:4 (main to auxiliary) coupled winding that can be used for a primary referenced bootstrap bias, V_{BOOT}.

Using (3), the actual value of ΔI_{LO} (4) can be back-calculated for the chosen value of L_O equal to 2 µH.

$$\Delta I_{LO} = \left(\frac{V_O}{L_O \times F_{SW}} \right) \times \left(1 - D_{MIN}\right) \quad (3)$$

$$\Delta I_{LO} = \left(\frac{3.3V}{2 \times 10^{-6} H \times \left(275 \times 10^3 Hz\right)} \right) \times \left(1 - 0.3\right) = 4.2 A_{PP} \quad (4)$$

A current of 4.2 A_{PP} translates to 14 percent of the total load current, which is more than acceptable in terms of allowable inductor ripple current. Using (5) the maximum RMS inductor current is calculated as 30.1 A_{RMS}, which is nearly equal to the maximum load current. Nonetheless, for higher values of ΔI_{LO} this calculation can serve as a design check to assure that the output inductor is not operating near saturation.

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{\Delta I_{LO}^2}{3}} = \sqrt{30A^2 + \frac{4.2A^2}{3}} = 30.1A_{RMS} \quad (5)$$

4.1.2 Bootstrap Bias Supply

During the freewheeling period when Q_R is conducting, the voltage across the output inductor is simply the regulated output voltage. And since the PA0373 uses a 1:4 (N_{BOOT}) coupled winding, an expression can be written relating V_{OUT} to V_{BOOT}.

$$V_O \times (1 - D) = \frac{V_{BOOT} + V_{D(BOOT)}}{N_{BOOT}} \times (1 - D) \quad (6)$$

Solving (6) for V_{BOOT} gives:

$$V_{BOOT} = (N_{BOOT} \times V_O) - V_{D(BOOT)} \quad (7)$$

Applying (7) and assuming a Schottky diode drop of 0.5 V for $V_{D(BOOT)}$, the approximate value of V_{BOOT} is 12.7 V as given by (8). For different values of V_{OUT} and V_{BOOT}, (6) can be rearranged to solve for a different required turns ratio on the coupled inductor, L_{BOOT}.

$$V_{BOOT} = (4 \times 3.3V) - 0.5V = 12.7V \quad (8)$$

The coupled winding technique, shown in Figure 7, works well under normal steady state conditions, however notice from (7) that the actual value of V_{BOOT} is dependant upon V_{OUT}. During abnormal operation such as over-current or short circuit current conditions, V_{OUT} is no longer in regulation causing the converter to operate in a hiccup mode as V_{BOOT} drops below the undervoltage lockout threshold of the PWM controller. If the PWM must remain fully functional during fault conditions where V_{OUT} drops out of regulation, then a separate regulated bias voltage must be derived and dedicated to maintaining V_{BOOT} above the UCC2891 undervoltage lockout threshold.

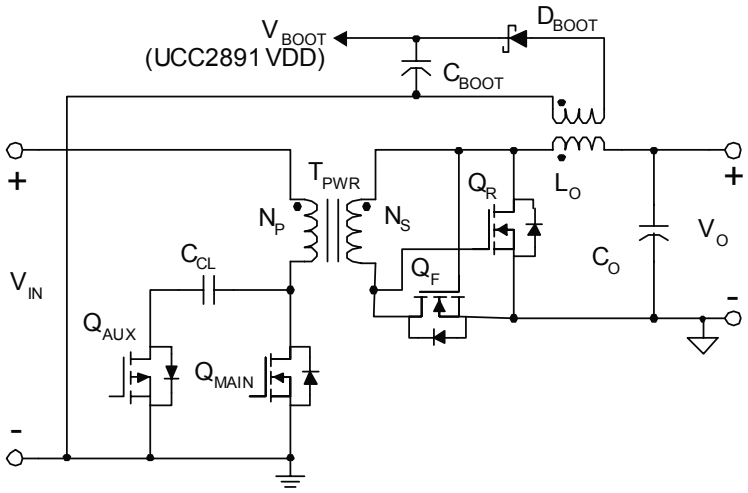


Figure 7. UCC2891 Bootstrap Bias Supply

From the UCC2891 data sheet, the minimum start-up voltage is 12.5 V, and the maximum start-up current is 500 µA. This information can be used to size the bootstrap capacitor according to (9).

$$C_{BOOT} = I_{START} \times \left(\frac{\left(1 - D_{MIN}\right)}{F_{SW} \times \Delta V} \right) \tag{9}$$

Substituting known values into (9) and solving gives:

$$C_{BOOT} = 500 \times 10^{-6} A \times \left(\frac{\left(1 - 0.3\right)}{\left(275 \times 10^{3} Hz\right) \times \left(12.7V - 12.5V\right)} \right) = 6.4 \times 10^{-9} F \approx 10nF \tag{10}$$

4.1.3 Output Capacitor

The output capacitor is chosen based upon many application specific variables such as cost, size, functionality and availability. This example determines the minimum output capacitance based upon an allowable output ripple voltage equal to 1 percent of the regulated output voltage, or roughly 33 mV_{pp}. Having already calculated the inductor ripple current from (4), the minimum output capacitance is calculated from (11) and is 58 µF as shown in (12).

$$C_{O(MIN)} = \frac{\Delta I_{LO}}{8 \times F_{SW} \times \Delta V_{O(Rip)}} \tag{11}$$

$$C_{O(MIN)} = \frac{4.2 A_{pp}}{8 \times \left(275 \times 10^{3} Hz\right) \times \left(33 \times 10^{-3} V\right)} = 58 \mu F \tag{12}$$

The capacitance value given by (12) only affects the capacitive component of the output ripple voltage, and the final selected value is dominated by $R_{ESR(OUT)}$ and transient considerations. Limiting the output ripple voltage to 33 mVpp, the total $R_{ESR(OUT)}$ of the output capacitor needs to be less than (13) as given by (14).

$$R_{ESR(OUT)} \le \frac{\Delta V_{O(RIP)}}{\Delta I_{LO}} \quad (13)$$

$$R_{ESR(OUT)} \le \frac{33\times10^{-3}V_{pp}}{4.2A_{pp}} = 8m\Omega \quad (14)$$

If transient response is a design consideration, then the selection of output capacitance can be derived from examining the transient voltage overshoot, V_{OS}, that can be tolerated during a step change in output load current. By equating the inductive energy with the capacitive energy, C_O can be derived as shown by (15).

$$C_O = \frac{L_O \times I_{STEP}^2}{V_{OS}^2} = \frac{L_O \times \left(I_{STEP(MAX)}^2 - I_{STEP(MIN)}^2\right)}{\left(V_{OS(MAX)}^2 - V_{OS(MIN)}^2\right)} \quad (15)$$

For a load step change from no load to 50 percent of full load and limiting the transient voltage overshoot to 3 percent of the regulated output voltage, C_O is calculated to be 672 µF as shown in (16).

$$C_O = \frac{L_O \times I_{STEP}^2}{V_{OS}^2} = \frac{\left(2\times10^{-6}H\right)\times\left(15A^2 - 0A^2\right)}{\left(3.4V^2 - 3.3V^2\right)} = 672\mu F \quad (16)$$

Two 330 µF, 6.3 V POSCAP capacitors are placed in parallel with a 10 µF ceramic capacitor as a good trade off between transient performance, small size and cost. The 6TPD330M POSCAP from Sanyo has a maximum $R_{ESR(OUT)}$ of 10 mΩ and a maximum ripple current rating of 4.4 A_{RMS}.

From (15), notice that C_O is proportional to L_O, which is also dependant upon F_{SW} and ΔI_{LO}. As a side note, this is the reason that interleaved power stages are so popular. The ripple cancellation effect reduces ΔI_{LO} allowing much higher frequency operation which in turn reduces L_O. A smaller value of L_O results in a smaller value of C_O, which greatly reduces the L_OC_O time constant of the power stage allowing for extremely fast transient response. For applications, such as intermediate bus converters, where transient response may be less of a concern, C_O can be selected solely based upon the result of (12) and (14).

4.1.4 Synchronous Rectifiers

There are many considerations for appropriately choosing MOSFETs used in self-driven synchronous rectifier applications. In a self-driven application the MOSFET gate-to-source voltage is ideally derived directly from the transformer secondary. As a result, the gate drive voltage is not regulated but instead varies as a function of the input voltage and transformer reset voltage, divided by the transformer turns ratio. If the input voltage range is wider than two to one, self driven synchronous rectification may not be an option and a control driven solution should instead be considered. Therefore, a good starting point is to perform a rough calculation to determine what the transformer turns ratio needs to be and then based upon the input voltage range, the variation in synchronous rectifier gate drive voltage can be calculated. By writing an equation for the volt-seconds balance across the output inductor an equation for the minimum secondary voltage, $V_{S(MIN)}$, is given by (17).

$$V_{S(MIN)} = \frac{V_O}{D_{MAX} - \left(\frac{t_{R(QMAIN)} + t_{F(QMAIN)} + t_{DELAY}}{T_{SW}} \right)} \quad (17)$$

Since the value for the rise and fall time of Q_{MAIN} and the delay time (as shown in Figure 2 and Figure 4) are not yet known, a worst case value of 3 percent of the minimum total period can initially be assumed and used to solve (18).

$$V_{S(MIN)} = \frac{3.3V}{0.6 - \left(\frac{109 \times 10^{-9} s}{3.64 \times 10^{-6} s} \right)} = 5.79V \quad (18)$$

Knowing the minimum input voltage, the result of (18) can now be used to calculate the primary to secondary transformer turns ratio as given in (19).

$$N = \frac{N_P}{N_S} = \frac{V_{IN(MIN)}}{V_{S(MIN)}} = \frac{36V}{5.79V} = 6.2 \approx 6 \quad (19)$$

Rounding (19) down to the next lowest integer results in a turns ratio of 6, assuring that the minimum secondary voltage is greater than the result determined by (18). As was mentioned previously, the gate-to-source voltage of the synchronous MOSFETs is not regulated, so the next step is to determine how much the V_{GS} of each MOSFET varies for a turns ratio of 6 over the full input voltage range.

The V_{GS} of Q_F varies proportionally with the input voltage divided down by the transformer turns ratio. For 36 V<V_{IN}<72 V, the gate-to-source voltage of Q_F varies between 6 V<$V_{GS(QF)}$<12 V, which is sufficient to fully enhance even a standard MOSFET. For the reverse MOSFET, Q_R, the gate-to-source voltage is derived from the transformer reset voltage divided down by the transformer turns ratio. Unique to the active clamp topology is the fact that the reset voltage is non-linear, and this is further discussed in Section 4.3. For 36 V<V_{IN}<72 V, the gate-to-source voltage of Q_R varies between 8 V<$V_{GS(QR)}$<5 V.

Selection of appropriate MOSFETs also depends upon knowing the RMS current and maximum drain-to-source voltage. From the schematic shown in Figure 5 it is apparent that the V_{GS} of Q_F is the same as the V_{DS} of Q_R, and the V_{GS} of Q_R is the same as the V_{DS} of Q_F. Therefore having already calculated what the V_{GS} is for each MOSFET, the V_{DS} is also now known.

Referring back to the inductor current waveform shown in Figure 6, the peak current seen by Q_F and Q_R can be calculated by (20).

$$I_{LO(PK)} = I_{O(MAX)} + \frac{\Delta I_{LO}}{2} = 30A + \frac{4.2A}{2} = 32.1A_{PK} \quad (20)$$

Q_F must be rated to withstand the peak current, as defined by (20) and the RMS current, as defined by (21), during the power transfer interval.

$$I_{QF(RMS)} = I_{O(MAX)} \times \sqrt{D_{MAX}} = 30A \times \sqrt{0.6} = 23.24A_{RMS} \quad (21)$$

Conversely, the freewheeling MOSFET, Q_R, must be rated to carry the maximum RMS current, as defined by (22), during the active clamp reset interval.

$$I_{QR(RMS)} = I_{O(MAX)} \times \sqrt{1 - D_{MIN}} = 30A \times \sqrt{1 - 0.3} = 25.1A_{RMS} \quad (22)$$

Because the duty cycle is close to 0.5, the maximum RMS currents are nearly equal for each MOSFET, so the same device can be used for Q_F and Q_R. The calculated parameters for each MOSFET are summarized in Table 2, and then used to specify the necessary parameters (with 20% margin added).

Table 2. Synchronous Rectifier MOSFET Specifications

PARAMETER	Q_F	Q_R
CALCULATED PARAMETERS		
V_{GS}	6V<V_{GS}<12V	8V<V_{GS}<5V
V_{DS}	8V<V_{DS}<5V	6V<V_{DS}<12V
I_D (I_{RMS})	23.24A	25.1A
SPECIFIED PARAMETERS		
$V_{GS(MAX)}$	15V	15V
$V_{DS(MAX)}$	15V	15V
$I_{D(MAX)}$ (I_{RMS})	30A	30A
$R_{DS(ON)}$	Extremely Low	Extremely Low
Q_G	Average	Average
Number of MOSFETs[1]	2	3

Notes: 1. As determined by equations (31) and (36).

During turn-off the synchronous rectifiers of an active clamp forward converter switch at near zero voltage. During turn-on, Q_F experiences some switching loss, but Q_R turns-on under ZVS conditions. Because of the high levels of average current each device must carry, a MOSFET with extremely low on resistance should be selected. However, Q_F may still experience some switching loss, so it is desirable not to blindly select the absolute lowest $R_{DS(ON)}$ device, but still pay close attention to the gate charge characteristic.

The HAT2165 device from Renesas has an $R_{DS(ON)}$ and Q_G of 2.5 mΩ and 80 nC specified at 12 V V_{GS}. The absolute maximum electrical ratings for the HAT2165 are V_{DS}=30 V, V_{GS}=±20 V and I_D=55 A. The device is available in a low profile LFPAK package which is a thermally enhanced version of an industry standard SO8 package. The junction to ambient thermal impedance is approximately 60 °C/W when the LFPAK is mounted on a 40 mm x 40 mm, 1 oz copper pad. Designing for an ambient environment, T_A, of 40 °C, and placing a design limit on the maximum allowable junction temperature equal to 75 percent of the absolute maximum junction temperature, the maximum power dissipation that can be tolerated within a single LFPAK can be estimated by (23).

$$P_{QF(LIMIT)} = \frac{T_{j(MAX)} - T_A}{\theta_{jA}} = \frac{\left(0.75 \times 150^\circ C\right) - 40^\circ C}{60^\circ C/W} = 1.25W/MOSFET \quad (23)$$

A quick calculation of the total power dissipated should be done to determine how many parallel MOSFETs must be used for Q_F and Q_R, in order to maintain a maximum power dissipation of 1.25 W per MOSFET.

4.1.4.1 Q_F Power Loss Calculations

All of the following Q_F calculations are performed under the worst case operating conditions of minimum V_{IN}, maximum D and maximum I_O. For the switching loss calculation of (26), the rise time, $t_{R(QF)}$, can be approximated by (24), assuming that the sink resistance between the transformer winding and the gate of Q_F is less than 3 Ω, and at minimum V_{IN}, V_{GS} is equal to 6 V. From the manufacturer's data sheet, the gate charge, Q_G of the HAT2165 is approximately 80 nC. Since this device turns off under ZVS, the fall time is neglected.

$$t_{R(QF)} \approx \frac{Q_G \times R_{QF}}{V_{GS(QF)}} = \frac{80nC \times 3\Omega}{6V} = 40ns \quad (24)$$

$$P_{SW(QF)} = \frac{V_{DS(MAX)} \times \left(I_{O(MAX)} - \frac{\Delta I_{LO}}{2} \right) \times t_{R(QF)} \times F_{SW}}{2} \quad (25)$$

$$P_{SW(QF)} = \frac{5V \times \left(30A - \frac{4.2A}{2} \right) \times \left(40 \times 10^{-9} s \right) \times \left(300 \times 10^{3} Hz \right)}{2} = 837mW \quad (26)$$

And since the Q_F synchronous rectifier is turning off at near ZVS, there is some body-diode conduction loss at turn-off. For the purpose of loss estimation only, a worst case body-diode conduction time of 50 ns is a reasonable estimate as applied to (27).

$$P_{BD(QF)} = V_F \times I_{QF(RMS)} \times F_{SW} \times t_{BD(QF)} = 1V \times 23.24A \times \left(300 \times 10^{3} Hz \right) \times \left(50 \times 10^{-9} s \right) = 350mW \quad (27)$$

The conduction losses due to RMS current flowing through the MOSFET channel resistance are straight forward as given by (28).

$$P_{C(QF)} = I^2_{QF(RMS)} \times R_{DS(ON)} = 23.24A^2 \times \left(2.5 \times 10^{-3} \Omega \right) = 1.35W \quad (28)$$

There are also some small but additional losses associated with charging and discharging the MOSFET gate capacitance, but most of this loss is recovered to the output load when self-driven synchronous rectification is used. For applications using control driven synchronous rectification, these same losses are dissipated in the MOSFET driver as long as the driver impedance is much greater than the internal MOSFET impedance. For this example, gate charge losses are therefore neglected for the purpose of sizing the Q_F and Q_R MOSFETs.

The maximum power loss for a single Q_F, HAT2165 LFPAK MOSFET is estimated by (30).

$$P_{QF(MAX)} = P_{SW(QF)} + P_{BD(QF)} + P_{C(QF)} \quad (29)$$

$$P_{QF(MAX)} = 837mW + 350mW + 1.35W = 2.54W \quad (30)$$

2.54 W of power dissipation would result in a junction temperature of 192 °C, far exceeding the 150 °C limit. The number of parallel Q_F MOSFETs required maintaining the 112 °C junction temperature design limit is given by (31).

$$QF_{NUM} = \frac{P_{QF(MAX)}}{P_{QF(LIMIT)}} = \frac{2.54W}{1.25W} = 2.03 \approx 2 \quad (31)$$

For a higher design safety margin, Q_F would ideally be rounded up to the next highest whole number, but since the result of (31) is only slightly greater than 2, two parallel MOSFETs are used for Q_F. Also, when switching MOSFETs are connected in parallel, the total on resistance is reduced, but the required gate charge is increased. Therefore in some cases the total power dissipated between parallel connected MOSFETs may increase, while the power dissipated per device should decrease. A more exact solution can be found by recalculating (24) through (30) for the number of MOSFETs determined from (31).

4.1.4.2 Q_R Power Loss Calculations

All of the following Q_R calculations are performed under the worst case operating conditions of maximum V_{IN}, minimum D and maximum I_O. Since the Q_R synchronous rectifier is turning on and off under ZVS conditions, switching losses are neglected. However, there is greater body-diode conduction loss than for the Q_F case. For the purpose of loss estimation only, a worst case body-diode conduction time of 150 ns is a reasonable estimate as applied to (32).

$$P_{BD(QR)} = V_F \times I_{QR(RMS)} \times F_{SW} \times t_{BD(QR)} = 1V \times 25.1A \times \left(300 \times 10^3 Hz\right) \times \left(150 \times 10^{-9} s\right) = 1.13W \quad (32)$$

The conduction losses due to RMS current flowing through the MOSFET channel resistance are straight forward as given by (33).

$$P_{C(QR)} = I^2_{QR(RMS)} \times R_{DS(ON)} = 25.1A^2 \times \left(2.5 \times 10^{-3} \Omega\right) = 1.58W \quad (33)$$

The maximum power loss estimate for a single Q_R, HAT2165 LFPAK MOSFET is estimated by (35).

$$P_{QR(MAX)} = P_{BD(QR)} + P_{C(QR)} \quad (34)$$

$$P_{QR(MAX)} = 1.13W + 1.58W = 2.71W \quad (35)$$

The number of parallel Q_R MOSFETs required maintaining the 112 °C junction temperature design limit is given by (36).

$$QR_{NUM} = \frac{P_{QR(MAX)}}{P_{QR(LIMIT)}} = \frac{2.71W}{1.25W} = 2.17 \approx 3 \quad (36)$$

Body-diode conduction losses are the second highest source of power dissipation in a synchronous rectifier. In a self-driven application, the body-diode conduction time associated with Q_R can vary greatly. Therefore a cautious design approach would be to use three parallel MOSFETs for Q_R. This allows for the real possibility that the conduction time may increase under certain conditions, or that the switching frequency increases slightly beyond the nominal value of 300 kHz, resulting in additional power dissipation in Q_R.

4.2 Power Transformer Considerations

For simplicity, the PA0810 OTS planar transformer from Pulse was chosen. Rated up to 140 W and measuring less than 10 mm high, the PA0810 is a good choice for module power applications requiring low-profile passive components. The PA0810 uses two primary windings of six turns each, and two single turn secondary windings. As determined from (19), a turns ratio of six must be maintained by connecting the two primary windings in parallel and the two secondary windings in parallel. This reduces the dc winding resistance by half, greatly reducing the I^2R conduction losses.

Since the PA0810 is part of a configurable family of planar transformers, its design and construction may not be optimal for all situations. Many applications might demand more than is possible from an OTS transformer solution, such as smaller size, fewer windings, increased primary to secondary isolation or higher efficiency.

At 300 kHz the transformer losses are dominated by core loss, occurring from time varying flux swing through the transformer's BH curve and conduction loss, resulting from the RMS current flowing through the planar windings. The flux swing, ΔB, is first determined from (37) containing a constant specific to the effective area of the PA0810 core geometry ((37) is found in the manufacturer's data sheet).

$$\Delta B = \frac{179211.46 \times V_{IN(MIN)} \times D_{MAX}}{F_{SW(kHz)} \times N_P} \quad (37)$$

$$\Delta B = \frac{179211.46 \times 36V \times 0.6}{300 \times 6} = 2{,}150G \quad (38)$$

The result of (38) can now be applied to (39) (also available in the manufacturer's data sheet) to determine the core loss.

$$P_{CORE} = 1.59 \cdot 10^{-13} \times \Delta B^{2.5} \times F_{SW(kHz)}^{1.8} = 1.59 \cdot 10^{-13} \times 2150^{2.5} \times 300^{1.8} = 0.98W \quad (39)$$

The copper losses are a result of RMS currents flowing through the primary and secondary windings. The average current through the secondary was defined previously by (21) and the average primary current (42) is made up of the primary magnetizing current (40) and peak current (41).

$$I_{MAG} = \frac{V_{IN(MIN)} \times D_{MAX}}{F_{SW} \times L_{MAG}} = \frac{36V \times 0.6}{\left(300 \times 10^3 Hz\right) \times \left(65 \times 10^{-6} H\right)} = 1.1A \quad (40)$$

$$I_{PRI(PK)} = \left(\frac{I_{LO(PK)}}{N}\right) + I_{MAG} = \left(\frac{32.1A}{6}\right) + 1.1A = 6.45A_{PK} \quad (41)$$

$$I_{PRI(RMS)} = \frac{I_{QF(RMS)}}{N} + \frac{I_{MAG}}{2} = \frac{23.24A}{6} + \frac{1.1A}{2} = 4.42A \quad (42)$$

From the manufacturer's data sheet, the DC resistances of the transformer primary and secondary (paralleled windings) are given as 11.25 mΩ and 0.875 mΩ respectively. These values can now be used along with the known transformer RMS currents to calculate the conduction losses as given by (44).

$$P_{CU} = \left(I_{PRI(RMS)}^2 \times R_{DC(PRI)}\right) + \left(I_{QF(RMS)}^2 \times R_{DC(SEC)}\right) \quad (43)$$

$$P_{CU} = \left(4.42A^2 \times 11.25 \times 10^{-3}\Omega\right) + \left(23.24A^2 \times 0.875 \times 10^{-3}\Omega\right) = 0.69W \quad (44)$$

The maximum transformer power loss can now be calculated by (45).

$$P_{T(PWR)} = P_{CORE} + P_{CU} = 0.98W + 0.69W = 1.67W \quad (45)$$

From the temperature curves given in the manufacturer's data sheet, 1.67 W of total power loss results in approximately 40 °C rise above ambient temperature. Therefore the maximum anticipated temperature of the transformer is approximately 80 °C, as given by (46).

$$T_{T(PWR)} = \Delta T_{T(PWR)} + T_A = 40^\circ C + 40^\circ C = 80^\circ C \quad (46)$$

4.3 Active Clamp Circuit

From Figure 5, whenever Q_{AUX}, is conducting, the difference between the clamp voltage and the input voltage is applied across the transformer magnetizing inductance, and this is referred to as the transformer reset period. Specific to the low-side clamp is the fact that Q_{AUX} must be a P-channel device only because of the direction of the body-diode. It is also worthy to note that Q_{AUX} carries only the transformer magnetizing current, which has a very small average value compared to the reflected load current. For this reason, specifying a low gate charge MOSFET should be a primary consideration with low $R_{DS(ON)}$ being only a secondary concern. Q_{AUX} must also be rated to withstand the full clamp voltage as given by Figure 8. For this application, the IRF6216 from international Rectifier is chosen.

Neglecting the effect of leakage inductance, the transfer function for the low-side clamp can be derived by applying the principle of volt-seconds balance across the transformer magnetizing inductance.

$$D \times V_{IN} = (1 - D) \times V_{CL} - (1 - D) \times V_{IN} \quad (47)$$

Simplifying (47) for the clamp voltage, V_{CL}, gives:

$$V_{CL} = \left(\frac{1}{1 - D}\right) \times V_{IN} \quad (48)$$

It is interesting to note that the transfer function given in (48) is also the same transfer function for a non-isolated boost converter and this is why the low-side clamp is commonly referred to as a boost type clamp.

The result of (48) describes the transfer function between the input voltage and the clamp voltage. However, notice from Figure 1 that whenever Q_{AUX} is conducting, the clamp voltage is applied directly across the drain-to-source junction of Q_{MAIN}, and not the transformer primary magnetizing inductance. Therefore (48) can be extended and written to include the drain-to-source voltage stress on Q_{MAIN}.

$$V_{DS(QMAIN)} = V_{CL} = \left(\frac{D}{1 - D}\right) \times V_{IN} \quad (49)$$

During the transformer reset period, the dot polarity on the transformer primary reverses, so the voltage applied to the primary is now defined as:

$$V_{RESET} = V_{CL} - V_{IN} \quad (50)$$

If the expression for V_{CL} from (48) is substituted into (50) and simplified, a transfer function relating the input voltage to the reset voltage can be shown as:

$$V_{RESET} = \left(\frac{D}{1-D}\right) \times V_{IN} \quad (51)$$

Furthermore, the duty cycle, D, of a single-ended forward converter is defined as the ratio of the output voltage to the input voltage multiplied by the transformer turns ratio, N.

$$D = \left(\frac{V_O}{V_{IN}}\right) \times N \quad (52)$$

Substituting (52) into (49) and (51) and simplifying gives expressions for V_{CL} and V_{RESET} in terms of V_{IN}, V_{OUT} and N, as shown in (53) and (54).

$$V_{DS(QMAIN)} = V_{CL} = \frac{V_{IN}^2}{V_{IN} - N \times V_O} \quad (53)$$

$$V_{RESET} = \frac{V_O \times V_{IN} \times N}{V_{IN} - N \times V_O} \quad (54)$$

The results of (53) and (54) can now be used to graphically show how the clamp voltage and transformer reset voltage vary with input voltage for a fixed value of V_{OUT} and a fixed transformer turns ratio, N. Using a value of 4 V for V_{OUT} (3.3 V plus some additional voltage drop), the graphical results of (53) are first plotted in Figure 8. Also shown in Figure 8 is the effect that varying the transformer turns ratio (varying D) has on the primary MOSFET drain-to-source voltage stress.

Figure 8 shows a drastic variation in the Q_{MAIN} MOSFET voltage stress during minimum input voltage (maximum duty cycle, D). For this reason the UCC2891, shown in Figure 10, provides the capability of precisely clamping the maximum duty cycle. The consequence could be destructive voltage levels applied to the primary MOSFET or having to over specify the maximum MOSFET voltage rating. Figure 9 shows that for a typical forward converter operating over the full telecom input voltage (36 V<V_{IN}<75 V), a turns ratio of N=6 results in 110 V of applied drain-to-source voltage at V_{IN}=36 V and V_{IN}=75 V. The MOSFET voltage shown in Figure 8 is also the voltage seen by the clamp capacitor, C_{CL}. As such, the clamp capacitor must be appropriately chosen to withstand the full clamp voltage plus any additional de-rating voltage. Having chosen a turns ratio of 6, the transformer reset voltage, $V_{RESET,}$ given by (54) can also be plotted against varying input voltage and is shown in Figure 9.

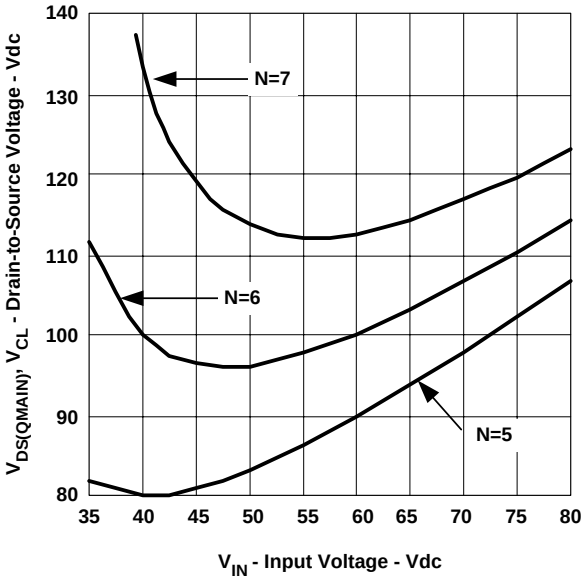


Figure 8.
Q_{MAIN} Drain-to-Source Voltage
vs. Input Voltage

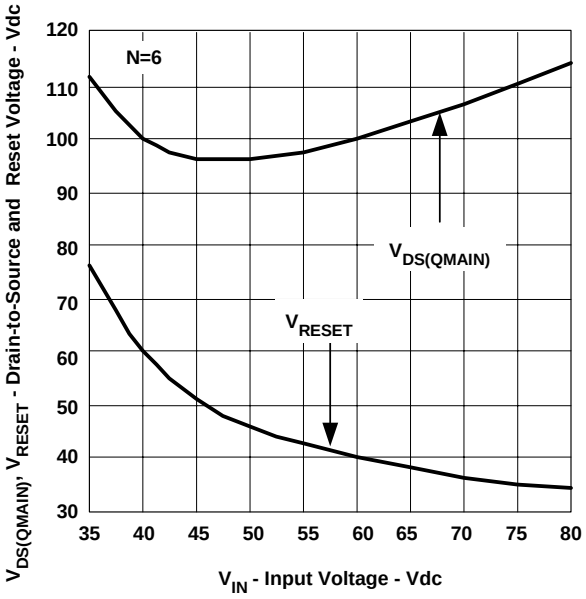


Figure 9.
Drain-to-Source Voltage and Reset Voltage
vs. Input Voltage

4.3.1 Low-Side Clamp Gate Drive

Since it has already been established that Q_{AUX} must be a ground referenced P-channel device, a negative gate drive voltage is required to fully turn this device on. However, the UCC2891 does not produce output voltage levels below ground reference. Using a gate drive circuit applied to the low-side clamp, the P-channel MOSFET can be directly driven from the UCC2891 as shown in Figure 10.

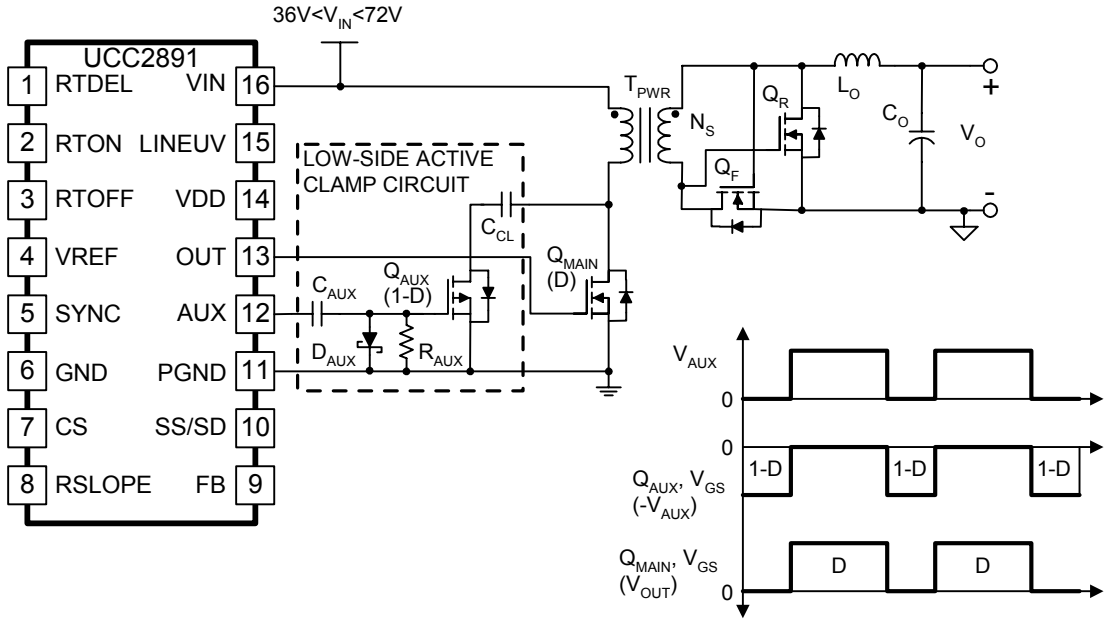


Figure 10. Low-Side Clamp and Gate Drive Circuit

The first time the UCC2891 AUX voltage goes positive, the Schottky diode, D_{AUX}, is forward biased and the capacitor, C_{AUX}, is charged to $-V_{AUX}$ volts. The capacitor voltage then discharges through R_{AUX}. If the time constant of R_{AUX} and C_{AUX} in (55) is much greater than the PWM period, then the voltage across C_{AUX} remains relatively constant and the resultant gate to source voltage seen at Q_{AUX} is $-V_{AUX}$ with a peak positive value of zero volts. Therefore, V_{AUX} is effectively shifted below ground and is now adequate for driving the gate of the ground referenced P-channel MOSFET, Q_{AUX}.

$$R_{AUX} \times C_{AUX} \cong \frac{100}{F_{SW}} \qquad (55)$$

The value of C_{AUX} is determined by arbitrarily choosing R_{AUX} to be 1KΩ, and solving (56).

$$C_{AUX} = \frac{100}{\left(1\times10^{3}\,\Omega\right)\times\left(300\times10^{3}\,Hz\right)} = 0.33\mu F \qquad (56)$$

4.3.2 Selecting The Clamp Capacitor

The first consideration for sizing the clamp capacitor is to know what the appropriate voltage rating must be over the full range of V_{IN} (shown in Figure 8).

The value of the clamp capacitor is primarily chosen based on the amount of allowable ripple voltage that can be tolerated. Also, it is assumed that the value of the capacitor is large enough to approximate the clamp voltage as a constant voltage source. However, according to (53) V_{CL} changes with input voltage. Whenever a line transient or sudden change in duty cycle is commanded, it takes some finite amount of time for the clamp voltage, and therefore the transformer reset voltage, to adapt. Larger capacitor values result in less voltage ripple but also introduces a transient response limitation. Smaller capacitor values result in faster transient response, at the cost of higher voltage ripple. Ideally the clamp capacitor should be selected to allow some voltage ripple, but not so much as to add additional drain-to-source voltage stress to Q_{MAIN}. Allow approximately 20 percent voltage ripple while paying close attention to V_{DS} of Q_{MAIN}.

A simplified method for approximating C_{CL}, is to solve for C_{CL} such that the resonant time constant is much greater than the maximum off-time. While additional factors such as the power stage time constant and control loop bandwidth also affect transient response, this approach, stated in (57), assures that transient performance is not compromised, at least from the active clamp circuit point of view.

$$2 \times \pi \times \sqrt{L_{MAG} \times C_{CL}} > t_{OFF(MAX)} \tag{57}$$

By solving for (57) for C_{CL}, and multiplying the result by a factor of 10 to assure that the inequality of (57) holds true, (57) can be rewritten as (58), expressing C_{CL} in terms of known design parameters:

$$C_{CL} > 10 \times \left(\frac{(1 - D_{MIN})^2}{L_{MAG} \times (2 \times \pi \times F_{SW})^2} \right) \tag{58}$$

Once C_{CL} is calculated by (59), the final design value may vary slightly after the clamp capacitor ripple voltage is measured in circuit.

$$C_{CL} > \frac{10 \times (1 - 0.3)^2}{(65 \times 10^{-6} H) \times (2 \times \pi \times (300 \times 10^3 Hz))^2} = 21.22 \times 10^{-9} F \approx 22nF \tag{59}$$

4.4 Primary MOSFET (Q_{MAIN}) Selection

Since the clamp voltage has already been determined from (53), the drain-to-source voltage stress of Q_{MAIN} is also known. Figure 8 shows that the maximum voltage stress over the full input range should be limited to 110 V. Also, the drain current of Q_{MAIN} is known from (41) and (42). The maximum RMS drain current occurs at minimum input voltage and maximum load current and is 4.42 A as given by (42). Therefore selecting a MOSFET with a 150 V V_{DS} rating and an I_D rating of at least 6.45 A insures a greater than 35 percent design safety margin. The Si7846DP from Vishay Siliconix is a 150 V, 6.7 A, N-channel MOSFET available in thermally enhanced SO8 PowerPAK™ package.

From the manufacturer's data sheet, the total gate charge is approximately 35 nC and the expected on-resistance is 41 mΩ for a 12 V applied gate drive.

Using the $I_{PRI(RMS)}$ current from (42), the conduction loss due to primary current flowing through the channel resistance of Q_{MAIN} is determined from (60).

$$P_{C(QMAIN)} = I_{PRI(RMS)}^2 \times R_{DS(QMAIN)} = 4.42A^2 \times \left(41 \times 10^{-3}\Omega\right) = 0.8W \qquad (60)$$

As explained in Section 4.4.1, Q_{MAIN} always turns off under ZVS, but may still be subject to some turn-on losses, as represented by (62). Typically ZVS at turn-on is lost at some minimum load current, estimated to be 40 percent of the maximum load current for this case. Above 12 A (40 percent maximum load), it is assumed that Q_{MAIN} experiences ZVS at turn-on and turn-off.

$$P_{SW(QMAIN)} = \frac{V_{CL} \times \left(0.4 \times \left(I_{PRI(PK)} - \frac{I_{MAG}}{2}\right)\right) \times F_{SW} \times Q_{G(QMAIN)}}{2 \times I_{G(QMAIN)}} \qquad (61)$$

$$P_{SW(QMAIN)} = \frac{110V \times \left(0.4 \times \left(6.45A - \frac{1.1A}{2}\right)\right) \times 300 \times 10^3 Hz \times 35 \times 10^{-9} C}{2 \times 2A} = 0.68W \qquad (62)$$

NOTE: If Q_{MAIN} does not turn on under ZVS conditions for a load current greater than 12 A, then the value of 0.68 W calculated by (62) may increase, possibly resulting in a higher actual junction temperature. Careful ZVS measurements should be made once the design is built and tested.

The third contributor to power loss in Q_{MAIN} is due to the charging and discharging of the MOSFET output capacitance, $C_{OSS(QMAIN)}$. For lower voltage applications this is sometimes neglected, however notice from (63) that the power loss is proportional to the square of the voltage. For the low-side active clamp forward converter, the maximum drain-to-source voltage (V_{CL}=110 V) is seen at minimum and maximum V_{IN}. Because the clamp voltage and the MOSFET $C_{OSS(QMAIN)}$ are both non-linear variables, estimating these losses can be difficult. From the manufacturer's curves $C_{OSS(QMAIN)}$ appears more predictable between 60 V and 120 V, and so a value of 150 pF is used.

$$P_{COSS(QMAIN)} = \frac{C_{OSS(QMAIN)} \times V_{CL}^2 \times F_{SW}}{2} = \frac{\left(150 \times 10^{-12} F\right) \times 110V^2 \times 300 \times 10^3 Hz}{2} = 0.27W \qquad (63)$$

The total losses in Q_{MAIN} can now be calculated by (64)

$$P_{QMAIN(MAX)} = P_{C(QMAIN)} + P_{SW(QMAIN)} + P_{COSS(QMAIN)} = 0.8W + 0.68W + 0.27W = 1.75W \quad (64)$$

A quick check of the maximum junction temperature of Q_{MAIN} is calculated to be 131 °C as shown in (65).

$$T_j = \left(R_{\theta jA} \times P_{QMAIN(MAX)}\right) + T_A = \left(52^\circ C/W \times 1.75W\right) + 40^\circ C = 131^\circ C \quad (65)$$

131 °C is slightly higher than 75 percent (113 °C) of the absolute maximum junction temperature of 150 °C. Therefore careful attention must be paid to Q_{MAIN}, especially under extreme conditions such as maximum input voltage, maximum load current, or any operating mode that forces Q_{MAIN} out of ZVS. When laying out the PCB, placing additional copper area under the drain tab of the Q_{MAIN} PowerPAK™ also helps to lower the junction temperature.

4.4.1 Primary MOSFET (Q_{MAIN}) Zvs Considerations

The ability to ZVS Q_{MAIN} is one of the primary motivations for using the active clamp. Detailing the conditions for ZVS first requires an understanding of the contributing parasitic elements as shown in Figure 11.

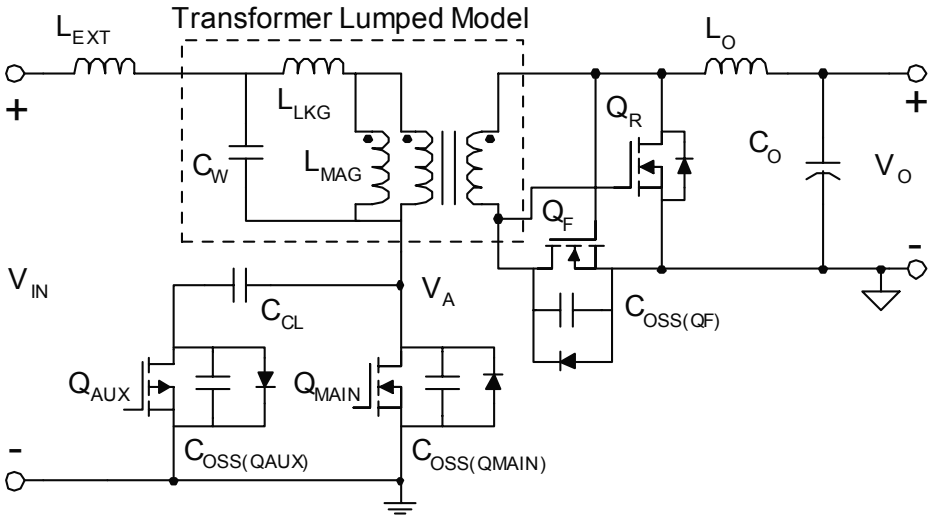
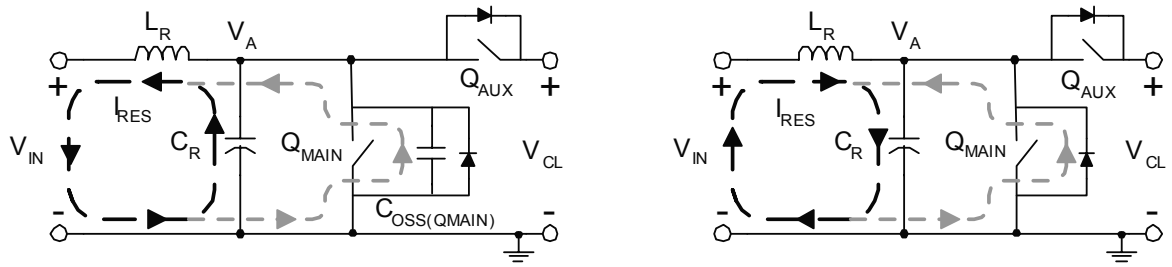


Figure 11. Active Clamp Power Stage with Parasitic Elements

The conditions for ZVS are that the drain-to-source voltage must be zero prior to Q_{MAIN} switching either on or off. This condition is achieved when the voltage at node V_A, shown In Figure 12, is resonantly driven to zero volts within the set time interval shown in Figure 2 (Q_{MAIN} turn-off) or Figure 4 (Q_{MAIN} turn-on). Therefore, for the purpose of ZVS, the circuit of Figure 11 can be reduced to a simple resonant circuit as shown in Figure 12.



t1→t2: Q_{MAIN} turn-off t3→t4: Q_{MAIN} turn-on

Figure 12. Simplified ZVS Resonant Circuit

During the t1→t2 interval, Q_{MAIN} has just turned off and Q_{AUX} is about to turn on. As $C_{OSS(QMAIN)}$ is charged to V_A, the body-diode of Q_{MAIN} is reverse biased and the current that was previously flowing through the channel resistance of Q_{MAIN} is now diverted to $C_{OSS(QMAIN)}$. Some of this current is also diverted to the output capacitance of Q_{AUX}, but more important is the fact that this current naturally charges in the same direction as the resonant current flowing out of V_A. Because the two currents are additive, Q_{MAIN} always turns off under ZVS regardless of the amount of current charging $C_{OSS(QMAIN)}$.

During the t3→t4 interval, Q_{MAIN} is about to turn on and Q_{AUX} has just turned off. Notice that the resonant current, I_{RES}, required to drive V_A to zero volts is opposed by the current necessary for Q_{MAIN} ZVS. Because these two currents are opposed with respect to V_A, Q_{MAIN} experiences ZVS only at turn-on under specific operating conditions. Referring to Figure 11 and Figure 12, the resonant inductance is first defined by (66) and no external inductance, L_{EXT}, is initially assumed. The resonant capacitance is defined by (68).

$$L_R = L_{LKG} + L_{MAG} + L_{EXT} \tag{66}$$

$$L_R = \left(190 \times 10^{-9}\, H\right) + \left(65 \times 10^{-6}\, H\right) + 0 = 65.19\,\mu H \tag{67}$$

$$C_R = \frac{4}{3} \times \left(C_{OSS(QMAIN)} + C_{OSS(QAUX)} + \frac{C_{OSS(QF)}}{N^2} \right) + C_W \tag{68}$$

$$C_R = \frac{4}{3} \times \left(\left(150 \times 10^{-12}\, F\right) + \left(30 \times 10^{-12}\, F\right) + \frac{2 \times \left(1200 \times 10^{-12}\, F\right)}{6^2} \right) + \left(90 \times 10^{-12}\, F\right) = 420\ pF \tag{69}$$

The main limitation for Q_{MAIN} turning on under ZVS is the ability to store enough inductive energy to fully discharge the resonant capacitor. This requirement can be checked mathematically to determine if an external inductor added in series with the transformer primary should be considered.

$$\frac{1}{2} \times L_{MAG} \times {I_{MAG}}^2 + \frac{1}{2} \times L_{LKG} \times \left(\frac{I_O}{N}\right)^2 > \frac{1}{2} \times C_R \times \left(V_{IN} + V_{CL}\right)^2 \tag{70}$$

As I_{OUT} approaches zero, the ZVS turn-on conditions for Q_{MAIN} are entirely dependant upon the magnetizing current. Therefore, under no load conditions (I_{OUT}=0 A), (70) can be reduced and solved for I_{MAG} by (71).

$$I_{MAG} > \sqrt{\frac{C_R \times \left(V_{IN} + V_{CL}\right)^2}{L_{MAG}}} \quad (71)$$

Since I_{MAG} has already been determined by (40), the result can be used to see if the inequality given by (71) is met.

$$I_{MAG} > \sqrt{\frac{\left(420 \times 10^{-12} F\right) \times \left(72V + 110V\right)^2}{65 \times 10^{-6} H}} = 0.463A \quad (72)$$

From (40), I_{MAG} is equal to 1.1 A which is greater than 0.463 A, so we can expect that Q_{MAIN} should experience ZVS down to near zero load current. If it turned out that there were not enough magnetizing current to overcome the resonant current required by C_R, then the transformer design can be reconsidered in an effort to reduce the magnetizing inductance. Another option would be to solve (74) for L_{EXT}, and then add the appropriate external inductance to meet the ZVS conditions for a given minimum load current.

$$\frac{1}{2} \times L_{MAG} \times {I_{MAG}}^2 + \frac{1}{2} \times L_{LKG} \times \left(\frac{I_O}{N}\right)^2 + \frac{1}{2} \times L_{EXT} \times \left(\frac{I_O}{N}\right)^2 > \frac{1}{2} \times C_R \times \left(V_{IN} + V_{CL}\right)^2 \quad (73)$$

$$L_{EXT} > \frac{C_R \times \left(V_{IN} + V_{CL}\right)^2 - L_{MAG} \times {I_{MAG}}^2}{\left(\frac{I_O}{N}\right)^2} - L_{LKG} \quad (74)$$

From the resonant inductance and capacitance, the resonant frequency is determined from (75) which can then used to calculate the amount of delay time necessary for the ZVS resonant transition to occur. The delay time calculated from (78) is used to program the UCC2891.

$$\omega_R = \frac{\pi}{\sqrt{L_R \times C_R}} \quad (75)$$

$$\omega_R = \frac{\pi}{\sqrt{\left(65.19 \times 10^{-6} H\right) \times \left(420 \times 10^{-12} F\right)}} = 19 \times 10^6 \frac{Rad}{s} \quad (76)$$

$$t_{DELAY} = \frac{\pi}{2 \times \omega_R} \quad (77)$$

$$t_{DELAY} = \frac{\pi \cdot Rad}{2 \times \left(19 \times 10^6 Rad / s\right)} = 82.7 \times 10^{-9} s \approx 100ns \quad (78)$$

4.5 Input Capacitance

The active clamp forward converter is a buck derived power topology with a pulsed AC input current, high in di/dt content, as shown in Figure 13.

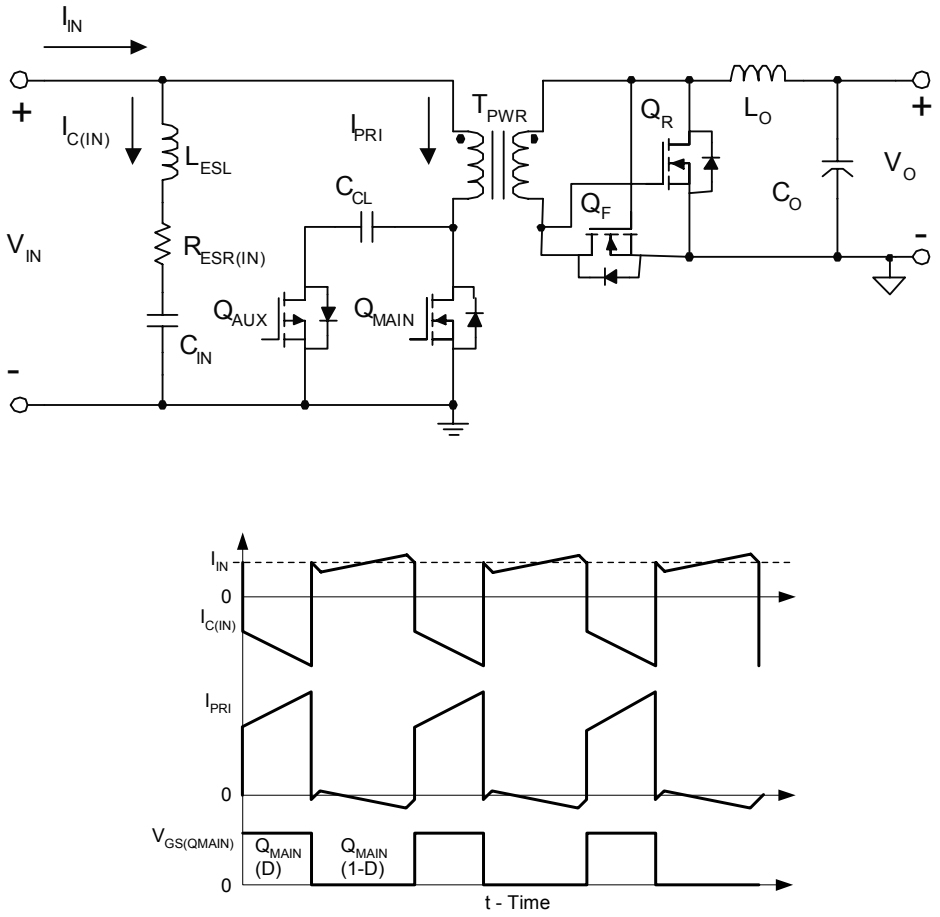


Figure 13. Primary Power Stage Current Waveforms

The input capacitor of Figure 13 is shown along with its equivalent parasitic series resistance and series inductance, which both can contribute to overall input ripple voltage. Analogous to the output capacitor, the purpose of the input capacitor is to provide high frequency filtering so that the input voltage is as close as possible to a pure DC source with low associated voltage ripple and noise.

The first thing to determine for choosing the input capacitor is the maximum RMS current. The RMS capacitor current is derived from the $I_{C(IN)}$ waveform shown in Figure 13 and can be expressed by (79). Unique to the active clamp rest technique is the magnetizing current shown in the I_{PRI} waveform during the off-time (1-D) of Q_{MAIN}. As can be seen by (79), this has a small but non-negligible effect on the RMS capacitor current. For a forward converter not using active clamp reset, this term would not exist since I_{PRI} is clamped to zero during the reset period.

$$I_{C(IN)} = \sqrt{\left[\left(I_{IN} - I_{PRI(RMS)}\right)\times D\right]^2 + \left[\left(I_{IN} + I_{MAG}\right)\times\left(1-D\right)\right]^2} \quad (79)$$

The only constant term in (79) is I_{MAG}. To express (79) in terms of known values, the maximum input current, I_{IN}, can be estimated by (80), and if the resonant transition delay is neglected, the duty cycle, D, can be closely approximated by (52).

$$I_{IN} = \frac{V_O \times I_{O(MAX)}}{\eta \times V_{IN}} \quad (80)$$

$$I_{PRI(RMS)} = \frac{I_{O(MAX)}}{N} \times \sqrt{D} = I_{O(MAX)} \times \sqrt{\frac{V_O \times N}{V_{IN}}} \quad (81)$$

Therefore (79) can now be rewritten as shown in (82) where all of the variables are now known.

$$I_{C(IN)} = \sqrt{\left(\left(\frac{V_O \times I_{O(MAX)}}{\eta \times V_{IN}} - \left(\frac{I_{O(MAX)}}{N} \times \sqrt{\frac{V_O \times N}{V_{IN}}}\right)\right) \times \left(\frac{V_O \times N}{V_{IN}}\right)\right)^2 + \left(\left(\frac{V_O \times I_{O(MAX)}}{\eta \times V_{IN}} + I_{MAG}\right) \times \left(1 - \frac{V_O \times N}{V_{IN}}\right)\right)^2} \quad (82)$$

Using the full load efficiency, η, of 0.85, the result of (82) can now easily be plotted against the full range of V_{IN} as shown in Figure 14.

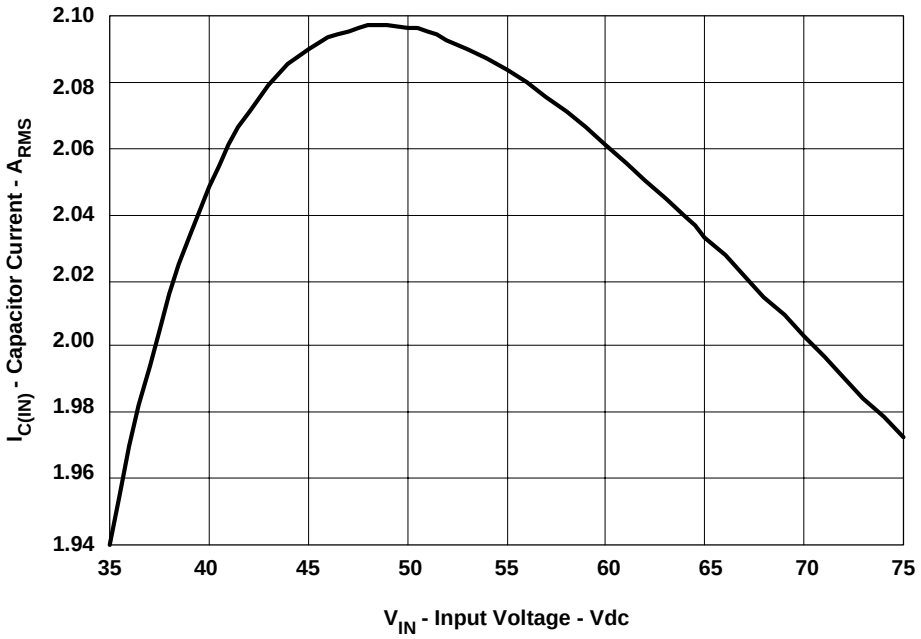


Figure 14. Input Capacitor Current vs. Input Voltage

Applying a 25 percent design margin, the input capacitance should be rated to handle at least 2.63 A_{RMS} capacitor current.

For initially choosing the input capacitor it is assumed that the change in ripple voltage is capacitive dominant, although at higher frequency operation L_{ESL} and $R_{ESR(IN)}$ can dominate over C_{IN}. The minimum required input capacitance that would limit the voltage ripple to 5 percent of the minimum input voltage is given by (83).

$$C_{IN(MIN)} = \frac{I_{IN} + I_{MAG}}{0.05 \times V_{IN}} \times t_{OFF} = \frac{I_{IN} + I_{MAG}}{F_{SW} \times (0.05 \times V_{IN})} \times (1 - D) \quad (83)$$

Substituting (80) into (83) and simplifying gives an expression for $C_{IN(MIN)}$ in terms of known design parameters as shown in (84). At minimum V_{IN}, maximum D and maximum I_{OUT}, and adding an additional 25 percent design margin, the minimum required capacitance value is determined to be 4 µF as shown in (85).

$$C_{IN(MIN)} = \frac{V_O \times I_{O(MAX)} + I_{MAG} \times \eta \times V_{IN(MIN)}}{\eta \times V_{IN(MIN)} \times F_{SW} \times (0.05 \times V_{IN(MIN)})} \times (1 - D_{MAX}) \quad (84)$$

$$C_{IN(MIN)} = \frac{1.25 \times (3.3V \times 30A + 1.1A \times 0.85 \times 36V)}{0.85 \times 36V \times 300 \times 10^3 Hz \times (0.05 \times 36V)} \times (1 - 0.6) = 4\mu F \quad (85)$$

Because the amount of input ripple voltage is large compared to the capacitor ripple current, the $R_{ESR(IN)}$ of the input capacitor is less of a concern than for the output capacitor. Nonetheless, the minimum required $R_{ESR(IN)}$ should still be checked by (86).

$$R_{ESR(IN)} < \frac{0.05 \times V_{IN(MIN)}}{\left(I_{PRI(PK)} + \left(\frac{I_{MAG}}{2}\right)\right)} = \frac{0.05 \times 36V}{\left(6.45A + \left(\frac{1.1A}{2}\right)\right)} = 257m\Omega \quad (86)$$

For a maximum V_{IN} of 72 V, multilayer ceramic is the most viable capacitor choice. Using two or more parallel ceramic capacitors easily satisfies the $R_{ESR(IN)}$ requirement from (86) while also introducing minimal parasitic inductance. The C4532X7R2A225 is a 2.2 µF, 100 V multilayer ceramic capacitor from TDK rated for 2.5 A_{RMS} at 300 kHz, with an $R_{ESR(IN)}$ of 4 mΩ. Three parallel capacitors are chosen giving a total input capacitance of 6.6 µF.

4.6 Current Sensing

The UCC2891/3 has a current sense threshold of 0.75 V, while the UCC2892/4 has a current sense threshold of 1.27 V. The goal of current mode control is to modulate the on time of Q_{MAIN} based upon the error voltage and the current flowing in the output inductor. Because the output current is so high, current sensing is done on the primary side where the RMS load current is reduced by the transformer turns ratio. Primary side current sensing can be done using either a small current sense resistor placed in series with the source of Q_{MAIN} or a current sense transformer. When designing for high efficiency, the total losses associated with each approach should be considered.

The resistive current sensing approach is shown in Figure 15, along with the approximate voltage waveform seen across the current sense resistor.

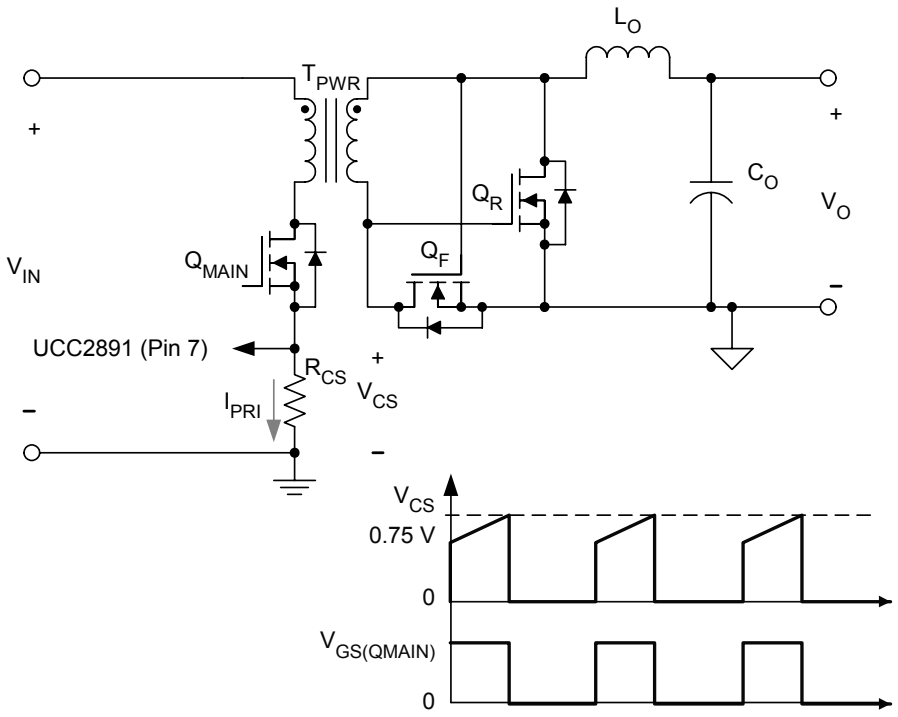


Figure 15. UCC2891 Resistive Current Sensing

From (41), the peak primary current is 6.45 A for I_{OUT}=30 A, but for setting the current limit, the peak primary current is equal to 6.78 A corresponding to I_{LIM}=32 A. The value of R_{CS} is given by (87).

$$R_{CS} = \frac{V_{CS}}{I_{PRI(CL\_PK)}} = \frac{0.75V}{6.78A} = 0.11\Omega \quad (87)$$

Using the primary RMS current of 4.42 A from (42), the maximum power dissipated in the nominal current sense resistor is given by (88).

$$P_{RCS} = I_{PRI(RMS)}{}^2 \times R_{CS} = 4.42A^2 \times 0.128\Omega = 2.5W \quad (88)$$

Dissipating 2.5 W in the current sense resistor would result in an overall efficiency penalty of 2%. The impact of this approach should be compared to using a current sense transformer as shown in Figure 16.

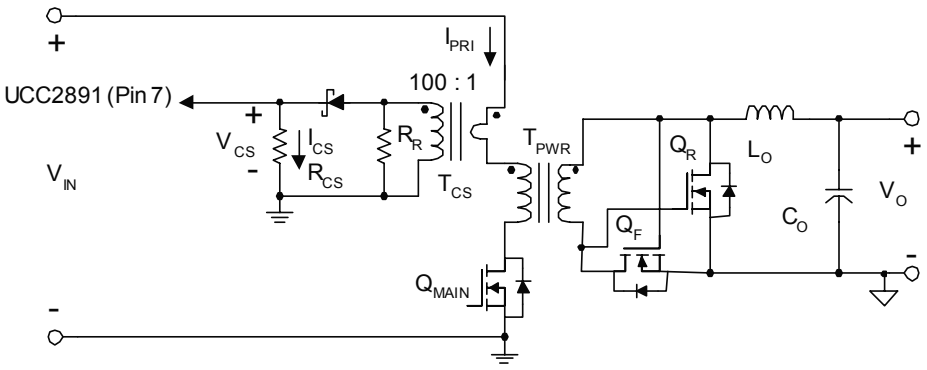


Figure 16. Current Sensing with a Current Sense Transformer

Consider the current sense transformer, T_{CS}, shown in Figure 16. The current flowing through R_{CS} is the primary current, I_{PRI}, reduced by the current sense transformer turns ratio. For a current transformer turns ratio of 100 to 1, I_{CS} during peak current limit is determined by (89).

$$I_{CS(CL\_pk)} = I_{PRI(CL\_PK)} \times \frac{1}{N_{CS}} = \frac{6.78A}{100} = 67.8mA \quad (89)$$

And from $I_{CS(CL\_PK)}$, the current sensing resistor is calculated by (90).

$$R_{CS} = \frac{V_{CS}}{I_{CS(CL\_PK)}} = \frac{0.75V}{67.8 \times 10^{-3} A} = 11\Omega \quad (90)$$

Using the primary RMS current of 4.42 A from (42), the maximum power dissipated in the 11 Ω current sense resistor is given by (91).

$$P_{RCS} = \left(\frac{I_{PRI(RMS)}}{N_{CS}} \right)^2 \times R_{CS} = \left(\frac{4.42A}{100} \right)^2 \times 11\Omega = 21.5mW \quad (91)$$

For T_{CS}, the P8208 100:1 current sense transformer from Pulse is rated to handle up to 10 A of primary current, and has a maximum height of less than 5 mm. The largest contribution of power dissipation comes from the primary current flowing through the single turn dc resistance. For the P8208, the dc resistances are 6 mΩ for the single turn primary and 5.5 Ω for the 100 turn secondary. The current sense transformer conduction losses are given by (92) and (93).

$$P_{TCS(PRI)} = I_{PRI(RMS)}{}^2 \times R_{PRI} = 4.42A^2 \times 6 \times 10^{-3}\Omega = 117.2mW \quad (92)$$

$$P_{TCS(SEC)} = \left(\frac{I_{PRI(RMS)}}{N_{CS}} \right)^2 \times R_{SEC} = \left(\frac{4.42A}{100} \right)^2 \times 5.5\Omega = 10.7mW \quad (93)$$

The Schottky rectifier used in the sensing circuit of Figure 16, also adds a small amount of power dissipation as a product of the RMS current and diode voltage drop when the diode is conducting. Assuming a forward voltage drop, V_F, of 0.6 V, the power dissipated in the diode can be approximated by (94).

$$P_{CS(DIODE)} = V_F \times \left(\frac{I_{PRI(RMS)}}{N_{CS}} \right) = 0.6V \times \left(\frac{4.42A}{100} \right) = 26.5mW \quad (94)$$

The final component to consider is R_R, which is used to reset the current sense transformer during the off-time. Since R_{CS} is much smaller than R_R, the secondary RMS current always flows to R_{CS} when the diode is conducting. When the current sense diode is non-conducting, R_R is present to maintain current flowing in the transformer secondary necessary for reset. Therefore the reset volt-seconds are determined by the value of R_R. R_R should be selected such that the transformer reset time is shorter than the minimum reset time of the power transformer, T_{PWR}. Increasing R_R has the effect of reducing the reset time but increasing the reset voltage, causing additional voltage stress to the current sensing diode. For minimal voltage stress on the current sense diode, an approximation for R_R is given by (95).

$$R_R = \frac{(V_{CS} + V_D) \times D_{MAX} \times N_{CS}}{(1 - D_{MAX}) \times I_{MAG}} \quad (95)$$

$$R_R = \frac{(0.75V + 0.6V) \times 0.6 \times 100}{(1 - 0.6) \times 1.1A} = 184\Omega \quad (96)$$

The total power dissipated using the current sense transformer can now be determined by (97).

$$P_{TCS} = P_{RCS} + P_{TCS(PRI)} + P_{TCS(SEC)} + P_{CS(DIODE)} \quad (97)$$

$$P_{TCS} = 21.5mW + 117.2mW + 10.7mW + 26.5mW = 175.9mW \quad (98)$$

Comparing the result of (98) to (88), the power dissipated using the current sense transformer technique of Figure 16 results in only 175.9 mW of total power dissipation compared to 2.5 W when a current sense resistor is used in series with the Q_{MAIN} MOSFET source. This is almost always the case for low input voltage, high current design applications and even for some off-line applications it may be worthwhile to compare the losses for each of the two current sensing techniques.

4.7 Summary Of Power Stage Losses

The total full load power dissipation (from a 100 W load) in only the power stage is summarized in Figure 17 and is estimated to be approximately 9.9 W, resulting in an estimated full load efficiency of 91 percent. The power estimate of Figure 17 neglects the losses in the input and output capacitors, as well as the loss in the Q_{AUX} MOSFET, but these are assumed to be minimal within the scope of this estimation.

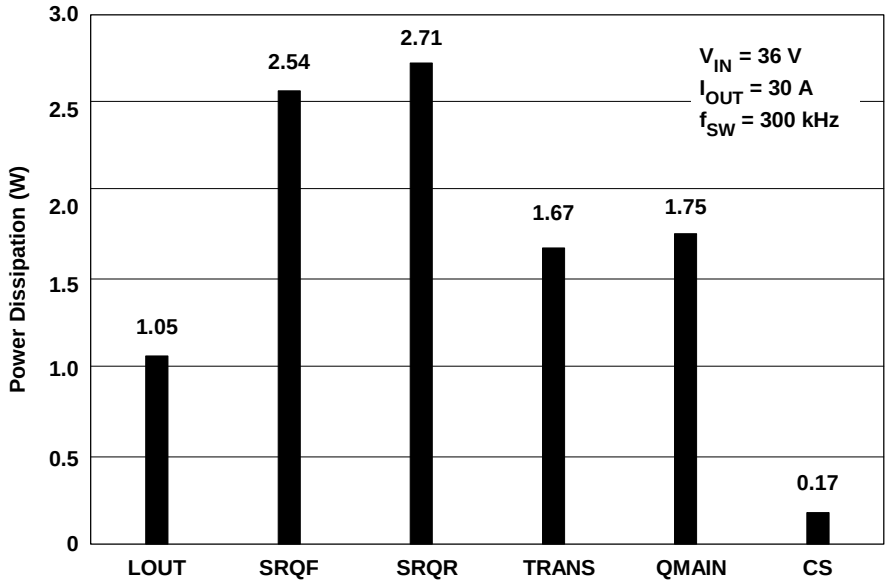


Figure 17. Power Stage Loss Estimate

5 OPTOCOUPLER VOLTAGE FEEDBACK

The UCC2891 PWM controller modulates the duty cycle using current mode control (CMC). The current sense information is derived from the primary side as discussed in the previous section. However, the dc error signal necessary for the voltage loop portion must be fed back from the secondary side to the primary side. Crossing the isolation boundary can be accomplished by using magnetic feedback or optocoupler feedback. Since the output inductor already provides the primary referenced bootstrap bias, adding a second coupled winding to gather the error voltage feedback signal is not desirable for this example. Therefore to keep all the component choices OTS, an optocoupler is used and is configured as shown in Figure 18.

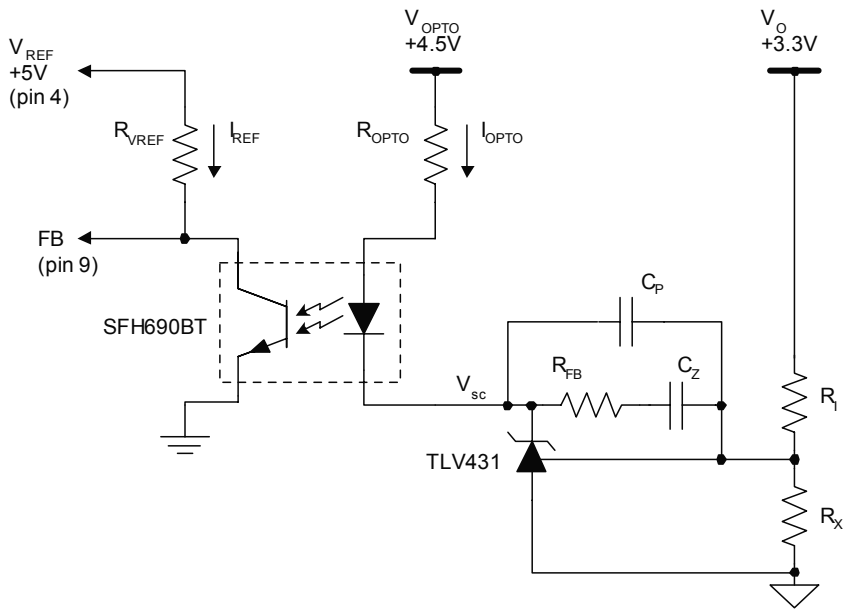


Figure 18. Optocoupler Feedback and Secondary Side Compensator

The recommended usable voltage at the FB pin of the UCC2891 is within the range of 1.25 V<V_{FB}<4.5 V. When V_{FB} is less then 1.25 V the UCC2891 operates in a pulse skipping mode. Since the input voltage for this example is only varying over a 2:1 range, it is possible to avoid the pulse skipping mode, during normal operation, by limiting the minimum V_{FB} to within 1.5 V. Therefore over the full 2:1 V_{IN} range, the FB voltage can be expected to change proportionally within the range of 1.5 V<V_{FB}<3.0 V. The next consideration is that the reference voltage of the UCC2891 can only source 5 mA of current. Since V_{REF} is used as the pull-up voltage for the optocoupler output, the maximum allowable I_{REF} is design limited to 2 mA.

$$R_{VREF} = \frac{V_{REF} - V_{FB(MIN)}}{I_{REF(MAX)}} = \frac{5V - 1.5V}{2mA} = 1.75K\Omega \quad (99)$$

$$I_{REF(MIN)} = \frac{V_{REF} - V_{FB(MAX)}}{R_{VREF}} = \frac{5V - 3V}{1.75K\Omega} = 1.1mA \quad (100)$$

The SFH690BT has a Current Transfer Ratio (CTR) between 100 percent and 300 percent. If the optocoupler is biased for the minimum CTR of 100 percent, then the current, I_{OPTO}, should be equal to the result of (101).

$$I_{OPTO(MIN)} = \frac{I_{REF(MIN)}}{CTR_{(MIN)}} = \frac{1.1mA}{1} = 1.1mA \quad (101)$$

Since the TLV431 can sink up to 25 mA of cathode current, there is plenty of headroom for driving the optocoupler. In order to minimize the DC gain of the optocoupler, 20 percent of the maximum TLV431 current is allowed. The optocoupler biasing resistor, R_{OPTO}, can be determined from (102). V_{OPTO} is selected based upon the minimum transformer secondary voltage of 6 V minus 1.5 V of headroom for a simple series pass regulator design.

$$R_{OPTO} = \frac{V_{OPTO} - V_F - V_{SC}}{I_{TLV431}} = \frac{4.5V - 1.3V - 1.24V}{5mA} = 392\Omega \quad (102)$$

Based on the selected biasing resistors and the minimum CTR, the minimum gain of the optocoupler is given by (103).

$$G_{OPTO} = \left(\frac{R_{VREF}}{R_{OPTO}}\right) \times CTR_{\min} = \left(\frac{1.75K\Omega}{392\Omega}\right) \times 1 = 4.46 = 13dB \quad (103)$$

Once the circuit is built and tested the overall control loop needs to be optimized. Since the gain of the optocoupler is part of the overall converter gain, the optocoupler biasing resistors may be adjusted to optimize the PWM feed back voltage.

6 COMPENSATING THE FEEDBACK LOOP

The overall control loop is shown in Figure 19. The loop consists of five gain blocks denoted by K, Gcl(s), Gf(s), Gc(s) and Gopto(s). K represents the primary side of the converter and consists of the current sensing circuit, slope compensation and feedback voltage all used as controlling inputs to the PWM comparator. The UCC2891 includes slope compensation circuitry that is internal to the control IC but externally programmable by a single resistor from R_{SLOPE} to ground reference.

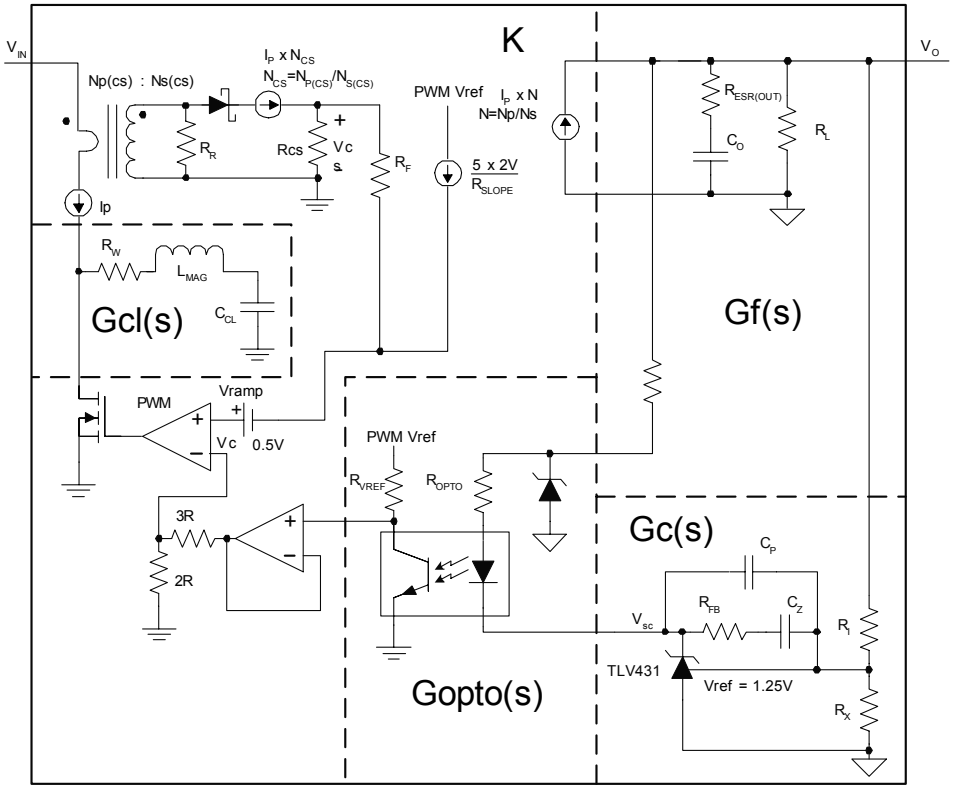


Figure 19. UCC2891 Control Schematic

Gcl(s) is the second order resonance effect formed between the transformer primary magnetizing inductance and clamp capacitor. Gf(s) is the secondary side of the power stage shown with the output inductor removed. Because the output inductor current is one of the control variables, the double pole effect normally seen in voltage mode controlled converters is removed thus simplifying the compensation. Gc(s) is the secondary side compensator using a TLV431 set up in a type 2 configuration. Because of its low cost, the TLV431 is a very popular choice for use as the error amplifier. Gopto(s) is the optocoupler gain block as described in the previous section. The varying TLV431 cathode voltage sets the diode current of the optocoupler. The gain and CTR of the optocoupler determine the emitter current seen on the primary side. The varying emitter current is then used to set the dc control voltage seen by the UCC2891. Inside the UCC2891, the feedback voltage is buffered and divided down by 2/5 before appearing at the inverting input of the PWM comparator.

From the control schematic of Figure 19, a simplified gain block diagram is shown in Figure 20. With the exception of Gc(s), the components that make up each block are known and can now be used to define the control to output transfer, Gco(s).

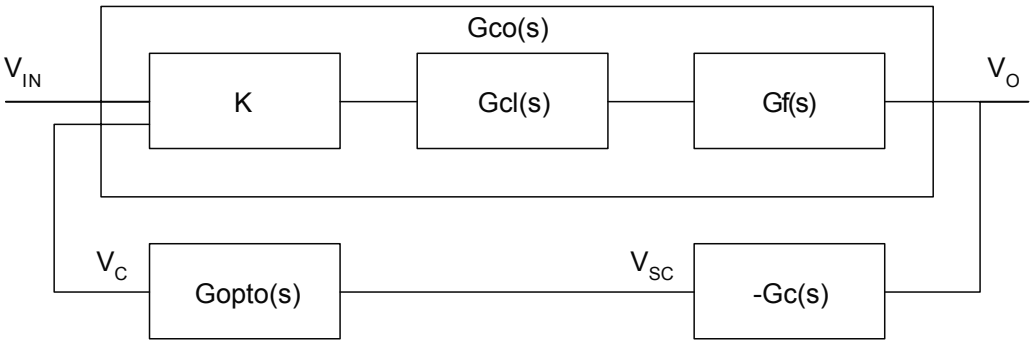


Figure 20. UCC2891 Simplified Control Block Diagram

The gain constant K is simplified and defined by (104). The additional voltage placed on the current sense pin due to slope compensation also has a small negligible effect on K, but it is omitted here for simplification.

$$K = \frac{\Delta V_O}{\Delta V_C} = \frac{N \times R_L}{\frac{R_{CS}}{N_{CS}}} = \frac{N \times N_{CS} \times V_O}{I_{O(MAX)} \times R_{CS}} \quad (104)$$

Unique to the active clamp operating in peak CMC, is a double pole resonant effect occurring between the transformer magnetizing inductance and the clamp capacitor. This can impact the control loop design in some instances and is discussed in more detail in references [9] and [10].

$$Gcl(s) = \left(\frac{1}{L_{MAG} \times C_{CL}} \times \frac{1}{S^2 + S\left(\frac{R_W}{L_{MAG}}\right) + \frac{1}{L_{MAG} \times C_{CL}}} \right) \quad (105)$$

The transfer function, Gf(s), of the output filter is reduced to a first order system given by (106).

$$Gf(s) = \frac{S \times C_O \times R_{ESR(OUT)} + 1}{S \times (R_L + R_{ESR(OUT)}) \times C_O + 1} \quad (106)$$

As shown in Figure 20, the control to output gain of the system is given by (108).

$$Gco(s) = K \times Gcl(s) \times Gf(s) \quad (107)$$

$$Gco(s) = \left(\frac{N \times N_{CS} \times V_O}{I_{O(MAX)} \times R_{CS}} \right) \times \left(\frac{1}{L_{MAG} \times C_{CL}} \times \frac{1}{S^2 + S \times \left(\frac{R_W}{L_{MAG}} \right) + \frac{1}{L_{MAG} \times C_{CL}}} \right) \times \left(\frac{S \times C_O \times R_{ESR(OUT)} + 1}{S \times (R_L + R_{ESR(OUT)}) \times C_O + 1} \right) \quad (108)$$

From (103), the dc gain of the optocoupler, Gopto, has already been calculated as 13 dB. However the optocoupler also exhibits a single pole roll off occurring at roughly 1 kHz, and can be combined with Gopto to give (109), which represents the uncompensated feedback. Since the small signal response of an optocoupler is not specified within the manufacturer's data sheet and can vary for a given application, it should be measured in circuit to validate the assumptions used in the control loop model.

$$Gopto(s) = \frac{Gopto}{1 + S \times \left(\frac{1}{2 \times \pi \times 1kHz} \right)} \quad (109)$$

For a forward converter operating in peak CMC, a type 2 compensation network is generally used and is shown in the Gc(s) section of Figure 19. For the CMC active clamp forward converter this compensation scheme can be used when the overall crossover frequency is designed to be at least one decade before the Gcl(s) resonant frequency defined by (110).

$$F_{CL} = \frac{1}{2 \times \pi \times \sqrt{L_{MAG} \times C_{CL}}} = \frac{1}{2 \times \pi \times \sqrt{65\mu H \times 22nF}} = 133kHz \quad (110)$$

$$F_O \le \frac{F_{CL}}{10} \quad (111)$$

From (111) the crossover frequency, F_0, of the control loop is selected to be 7 kHz. For wider bandwidth requirements, the single pole roll-off of the optocoupler limits the amount of phase boost that a type 2 compensation network can provide. In these instances an additional zero would have to be introduced into the loop, implying a type three compensation network. The frequency response for each block of the control to output, Gco(s), gain and phase are shown individually and added together in Figure 21 and Figure 22.

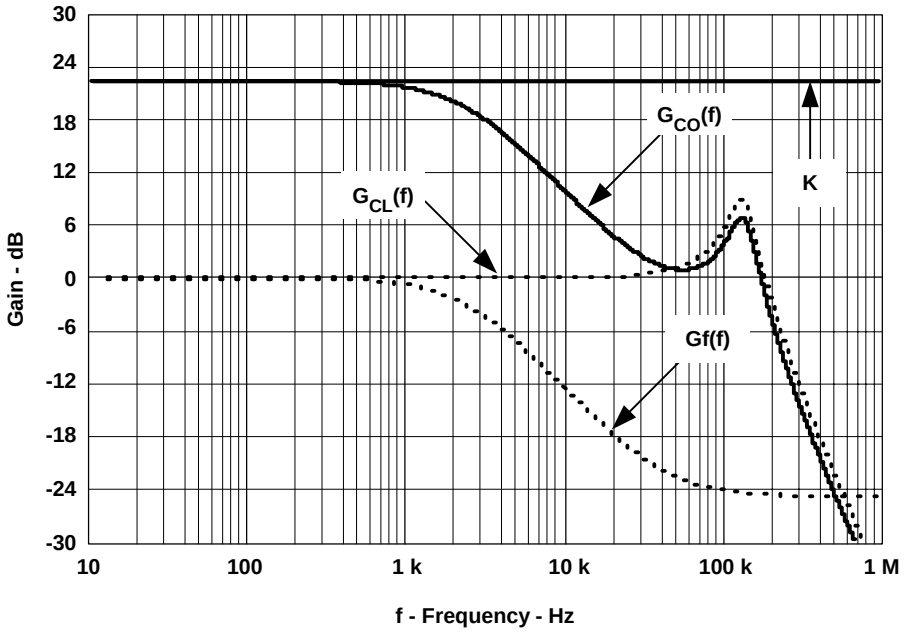


Figure 21. Open Loop Control to Output Gain

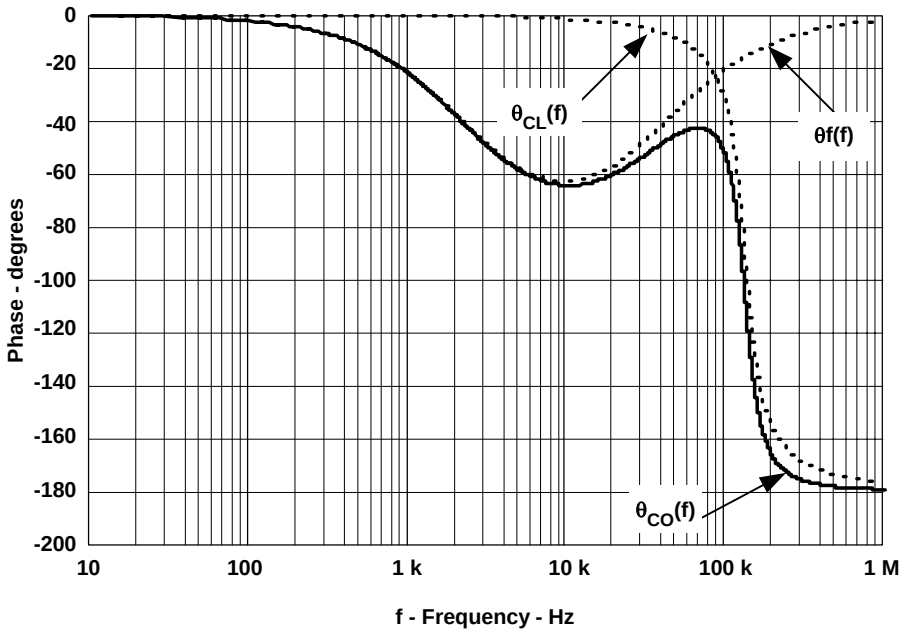


Figure 22. Open Loop Control to Output Phase

By plotting (109) and adding the result to Gco(s), the total closed loop uncompensated gain and phase are now known and the compensation network that makes up Gc(s) in Figure 19 can now be designed as follows. From Figure 23, the uncompensated overall gain is about 7.6 dB at F_0=7 kHz. The compensator needs to be designed to have a -7.6 dB gain at the crossover frequency. The required absolute gain at F_0 is given by (112).

$$gc(F_0) = 10^{\frac{-1\times[Gco(F_0)+Gopto(F_0)]}{20}} = 10^{\frac{-1\times(7.6dB)}{20}} = 0.417 \qquad (112)$$

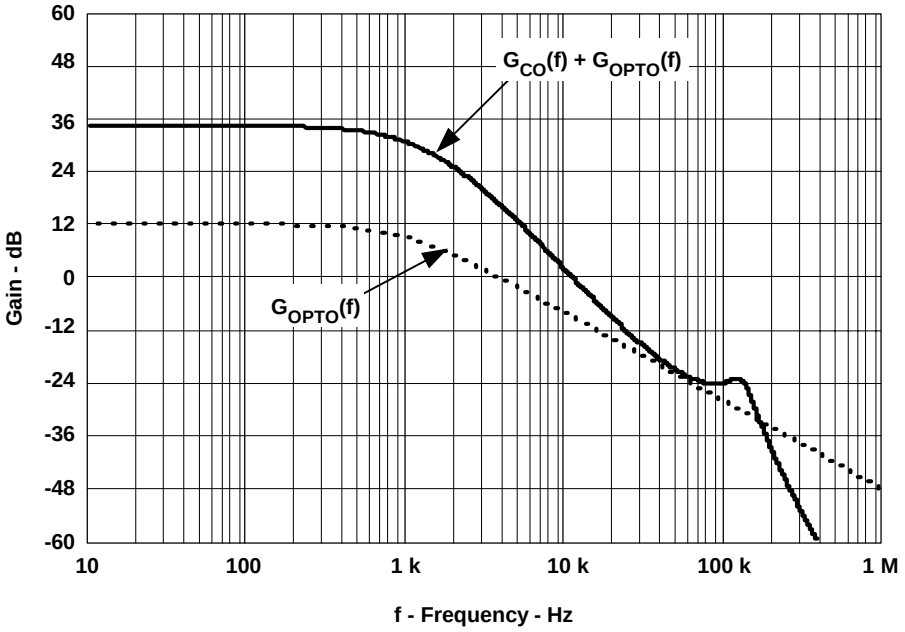


Figure 23. Closed Loop Uncompensated Gain

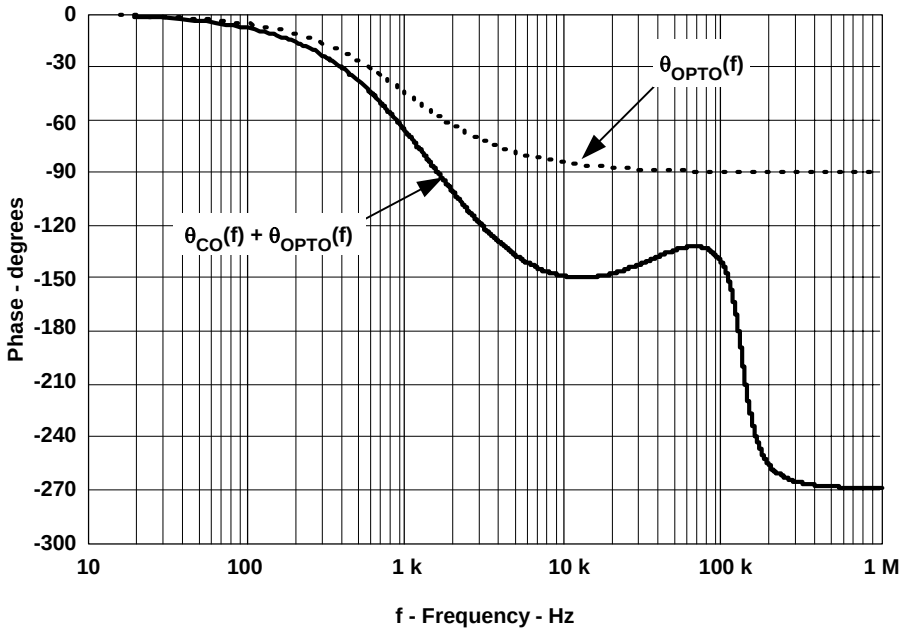


Figure 24. Closed Loop Uncompensated Phase

If R_X is arbitrarily chosen to be 17.4 KΩ, then R_I can be calculated from (113). Actual component values used in the final design are shown to the right of each result.

$$R_I = R_X \times \frac{V_O - V_{REF}}{V_{REF}} = 17.4K\Omega \times \frac{3.3V - 1.25V}{1.25V} = 28.54K\Omega \rightarrow 28.7K\Omega \quad (113)$$

The feedback resistor, R_{FB}, is chosen to provide the required negative gain at F_0 and is calculated from (114).

$$R_{FB} = gc(F_0) \times R_I = 0.417 \times 28.7K\Omega = 11.96K\Omega \rightarrow 10K\Omega \quad (114)$$

The pole formed by R_{FB} and C_P is used to compensate for $R_{ESR(OUT)}$ of the output capacitor. It is placed at the highest anticipated $R_{ESR(OUT)}$ of the output capacitance, which is 6mΩ. C_P is then calculated according to (115).

$$C_P = \frac{C_O \times R_{ESR(OUT)}}{R_{FB}} = \frac{660\mu F \times 6m\Omega}{10K\Omega} = 396pF \rightarrow 330pF \quad (115)$$

The zero formed by R_{FB} and C_Z is used to provide additional phase boost at F_0, and compensate for the low frequency pole seen by the output capacitor and load resistance. C_Z is determined from (116).

$$C_Z = \frac{V_O \times C_O}{R_{FB} \times I_{O(MAX)}} = \frac{3.3V \times 660\mu F}{10K\Omega \times 30A} = 7.2nF \rightarrow 82nF \quad (116)$$

The final component values tested in the actual design were only slightly changed from calculated values and are shown for completeness in Figure 25.

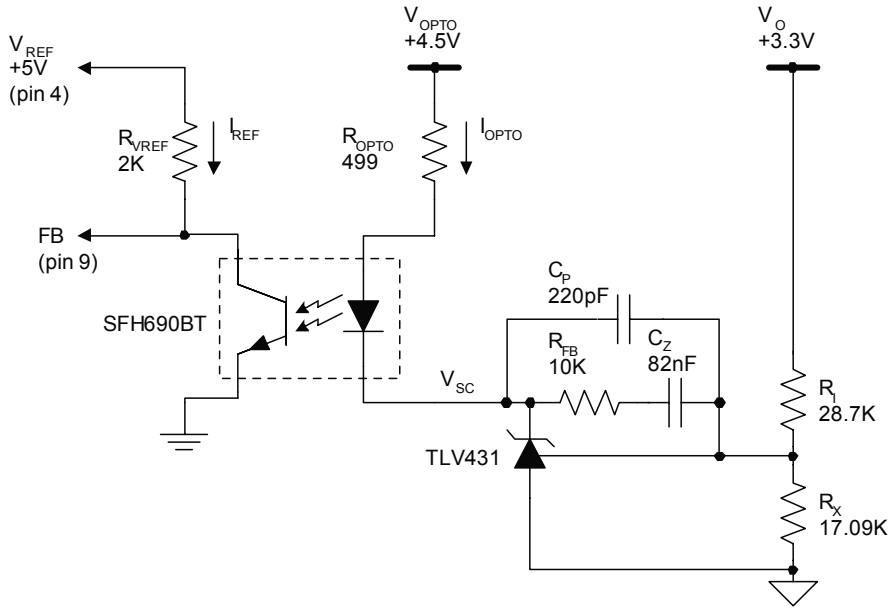


Figure 25. Type 2 Compensator (Final Component Design Values Shown)

The calculated gain and phase responses of the compensated TLV431 are shown in Figure 26. At F_0=7 kHz, the compensator has a gain of -7.6 dB. Also shown in Figure 26, is a dotted line indicating the maximum gain bandwidth product (GBW) of the open loop TLV431. For this design, the compensated network is well below the GBW limit, but it should be noted nonetheless. Figure 26 shows the phase compensator boost of nearly 90 degrees at the crossover frequency.

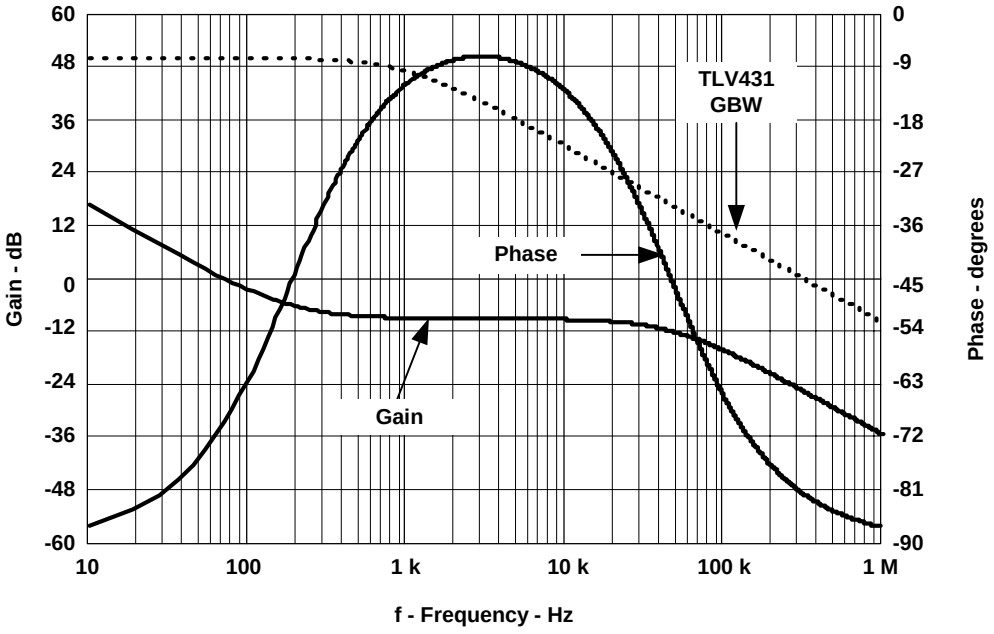


Figure 26. Type 2 Compensator Gain and Phase

With the circuit of Figure 25 introduced into the design, the calculated total closed loop gain and phase responses are shown in Figure 27. From the loop gain response of Figure 27, the crossover frequency of 7 kHz is achieved with about 50 dB of low frequency gain. The double pole response of the active clamp circuit can also be seen around 133 kHz. The effective phase boost of the compensator can be seen starting at around 100 Hz. However, due to the effect of the optocoupler phase shift, the compensator it is unable to fully contribute the amount of phase shown in Figure 26. The result is a drastic reduction in phase margin and is modeled here to be about 30 degrees. Normally, the compensation would be revisited in an effort to achieve greater than 40 degrees of phase margin. In this case the actual phase margin measured in the final circuit proved to be greater than 45 degrees over the full range of V_{IN} and I_{OUT}. This indicates that the optocoupler phase shift was not as close to the crossover frequency as originally assumed.

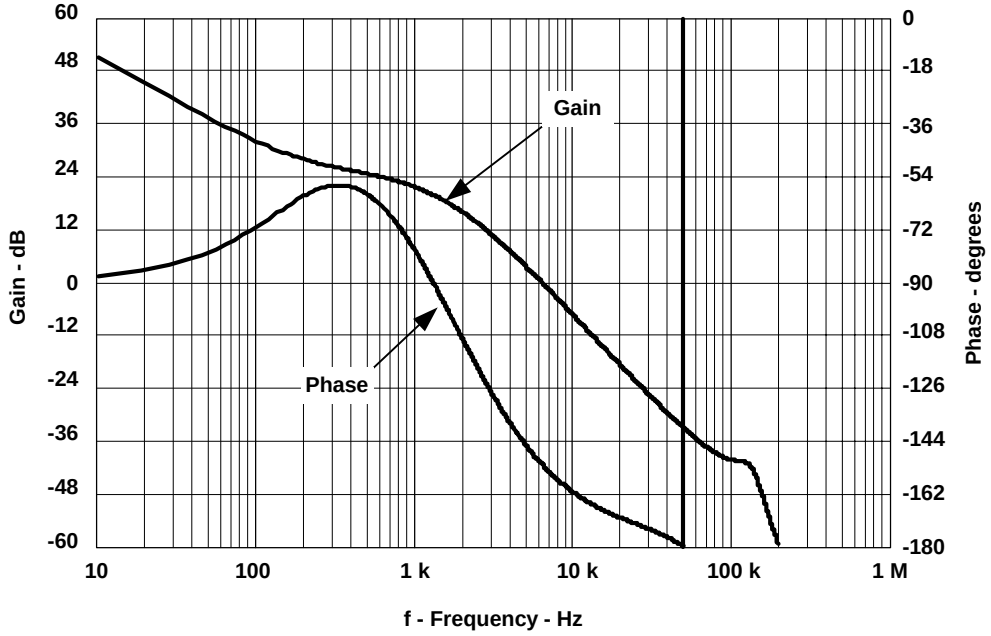


Figure 27. Calculated Total Overall Loop Gain and Phase

7 PROGRAMMING THE UCC2891 PWM CONTROL IC

Using design information from the power stage, the PWM controller can now be set up. This is generally the final step in completing the power converter design. The following design equations are intended to complement the step by step, set up procedure shown in the application section of references [1] and [2]. Actual component values used in the design are shown to the right of each result.

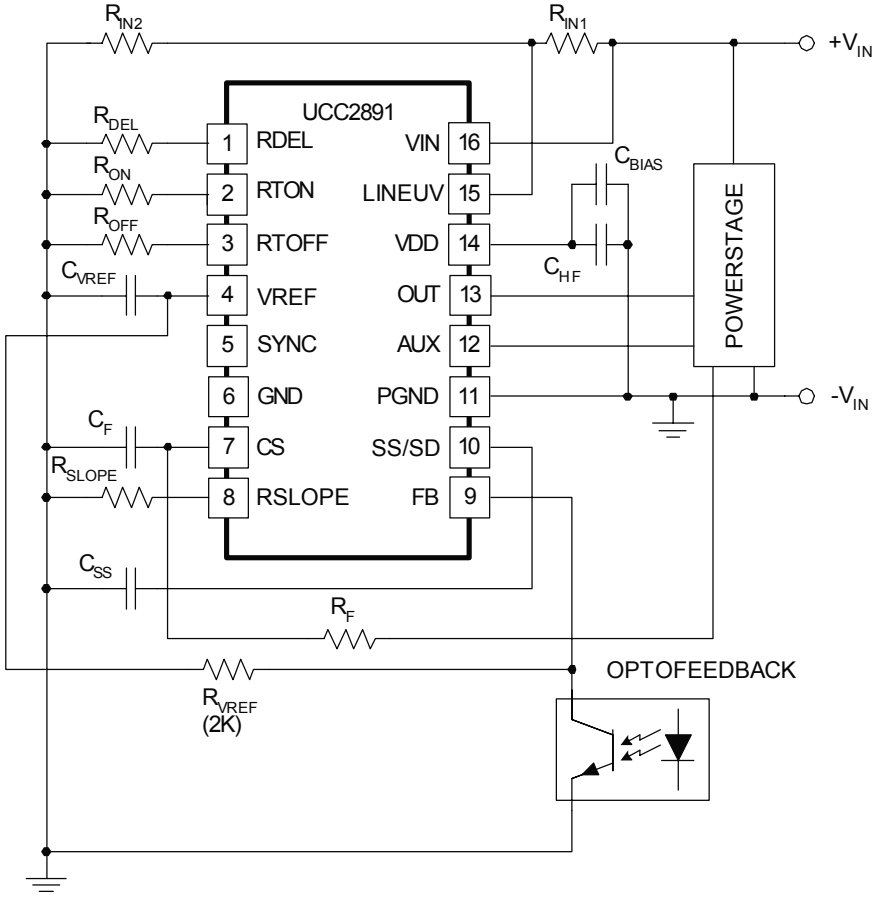


Figure 28. UCC2891 Set Up Diagram

7.1 Step 1. Oscillator

The oscillator frequency and maximum duty cycle clamp are set by R_{ON} and R_{OFF} according to (117) and (118).

$$R_{ON} = \frac{t_{ON}}{37.33\times10^{-12}} = \frac{D_{MAX}}{F_{SW}\times37.33\times10^{-12}} = \frac{0.65}{300kHz\times37.33\times10^{-12}} = 58K\Omega \rightarrow 57.6K\Omega \quad (117)$$

$$R_{OFF} = \frac{t_{OFF}}{16\times10^{-12}} = \frac{1-D_{MAX}}{F_{SW}\times16\times10^{-12}} = \frac{1-0.65}{300kHz\times16\times10^{-12}} = 72.9K\Omega \rightarrow 76.8K\Omega \quad (118)$$

7.2 Step 2. Soft Start

The soft start capacitor is set according to a desired soft start time applied to (119) below. For this example a soft start time of 40 ms is arbitrarily chosen.

$$C_{SS} = \frac{2.5V \times 0.43 \times t_{SS}}{R_{ON} \times (4.5V - 1.25V)} = \frac{2.5V \times 0.43 \times 40ms}{57.6K\Omega \times (4.5V - 1.25V)} = 229nF \rightarrow 0.22\mu F \quad (119)$$

7.3 Step 3. VDD Bypass Requirements

First the high frequency filter capacitor is calculated based on gate charge parameters of Q_{MAIN} and Q_{AUX}. Assuming that the switching frequency ripple should be kept below 100 mV across C_{HF}, its value can be approximated by (120). From (61), $Q_{G(QMAIN)}$ is 35 nC, and from the IRF6216 AUX MOSFET data sheet, $Q_{G(AUX)}$ is also 35 nC.

$$C_{HF} = \frac{Q_{G(QMAIN)} + Q_{G(QAUX)}}{0.1V} = \frac{35nC + 35nC}{0.1V} = 700nF \rightarrow 1\mu F \quad (120)$$

C_{BIAS} is determined based upon the amount of energy storage defined by t_{SS} and the turn-on (13.5V) and turn-off (8V) thresholds of the PWM controllers UVLO circuit monitoring the voltage at pin 14. In addition, the bias current of the PWM controller and RMS gate drive current of Q_{MAIN} and Q_{AUX} must also be known. From the UCC2891 data sheet, the peak driver currents are given as $I_{G(QMAIN)} = I_{G(QAUX)} = 2$ A and $I_{DD(MAX)} = 3$ mA. Therefore, the power consumption during start up can be estimated by (122).

$$P_{BIAS} = \begin{pmatrix} I_{DD(MAX)} + F_{SW} \times \left(\left(I_{G(QMAIN)} \times t_{R(QMAIN)} \right) + \left(I_{G(QAUX)} \times t_{R(QAUX)} \right) \right) \\ + \left(\left(Q_{G(QMAIN)} + Q_{G(QAUX)} \right) \times F_{SW} \right) \end{pmatrix} \times V_{DD} \quad (121)$$

$$P_{BIAS} = \begin{pmatrix} 3mA + 300kHz \times \left((2A \times 20ns) + (2A \times 20ns) \right) + \\ \left((35nC + 35nC) \times 300kHz \right) \end{pmatrix} \times 12V = 144mW \quad (122)$$

For the desired soft start time of 40 ms, the minimum value of C_{BIAS} can now be calculated by (123).

$$C_{BIAS} > \frac{2 \times P_{BIAS} \times t_{SS}}{(13.5V^2 - 8.5V^2)} = \frac{2 \times 144mW \times 40ms}{(13.5V^2 - 8.5V^2)} = 97uF \rightarrow (2)47\mu F \quad (123)$$

Using 2 parallel 47µF capacitors for C_{BIAS} should be close enough weighing a trade off between soft start time and total required capacitance.

7.4 Step 4. Delay Programming

The resistor, R_{DEL}, sets the turn-on delay between both gate drive signals. The delay time is identical for each switching transition, between OUT (pin13) turning off and AUX (pin14) turning on as well as between AUX turning off and OUT turning on. Using the t_{DELAY} result from (78), the value of R_{DEL} is given by (124).

$$R_{DEL} = (t_{DELAY} - 50ns) \times 0.87 \times 10^{11} \Omega \cdot s^{-1} = (100ns - 50ns) \times 0.87 \times 10^{11} \Omega \cdot s^{-1} = 3.33K\Omega \rightarrow 8.45K\Omega \quad (124)$$

Once the design is optimized it is important to remember that increasing t_{DELAY} beyond 100 ns allows more time to achieve ZVS but results in less available duty cycle, which can effect low line regulation.

7.5 Step 5. Input Voltage Monitoring

The amount of hysteresis current fed back to the LINEUV comparator is first calculated by (125).

$$I_{HYST} = \frac{2.5V}{R_{DEL}} \times 0.05 = \frac{2.5V}{3.33K\Omega} \times 0.05 = 37.5\mu A \quad (125)$$

The amount of hysteresis voltage is specified by the difference between V_{ON} and V_{OFF} in Table 1, and is used to calculate R_{IN1} from (126).

$$R_{IN1} = \frac{V_{ON} - V_{OFF}}{I_{HYST}} = \frac{35V - 34V}{37.5\mu A} = 26.6K\Omega \rightarrow 26.7K\Omega \quad (126)$$

The low-side resistor of the LINEUV divider is now easily calculated from (127).

$$R_{IN2} = R_{IN1} \times \frac{1.27V}{V_{OFF} - 1.27V} = 26.7K\Omega \times \frac{1.27V}{31V - 1.27V} = 1.1K\Omega \rightarrow 1K\Omega \quad (127)$$

7.6 Step 6. Current Sense Filtering and Slope Compensation

The UCC2891 PWM controller uses an internal slope compensation scheme that is externally programmable by appropriately selecting two resistors, R_F and R_{SLOPE}. The current sense filter resistor, R_F, is selected based upon the chosen corner frequency of the low pass filter formed by R_F and C_F. As a starting point, a general rule of thumb is to select the corner frequency to be 10 times the switching frequency. Also, C_F should be chosen between the recommended limits of 47 pF≤C_F≤270 pF. Arbitrarily picking C_F equal to 100 pF, R_F can be determined from (128).

$$R_F = \frac{1}{2 \times \pi \times (10 \times F_{SW}) \times C_F} = \frac{1}{2 \times \pi \times (10 \times 300kHz) \times 100pF} = 530\Omega \approx 536\Omega \rightarrow 1.82K\Omega \quad (128)$$

A closest standard resistor value of 536 Ω is chosen for R_F. The output inductor current slope must now be defined as it is reflected from the secondary, back to the primary and then translated to a voltage slope seen across the current sense resistor, R_{CS}. When a current sense transformer is used, the voltage equivalent compensation ramp can be determined from (130).

$$\frac{dV_L}{dt} = \frac{\left(V_{IN(MIN)} \times N_S - V_O \times N_P\right) \times N_S \times R_{CS}}{N_P{}^2 \times L \times N_{CS}} \quad (129)$$

$$\frac{dV_L}{dt} = \frac{\left(36V \times 1 - 3.3V \times 6\right) \times 1 \times 12.7\Omega}{6^2 \times 2\mu H \times 100} = 0.027\frac{V}{\mu s} \quad (130)$$

For applications that do not use a current sense transformer, (129) can still be applied by making the N_{CS} term equal to one. Using the calculated values of R_F and dV_L/dt, R_{SLOPE} can now be determined from (132).

$$R_{SLOPE} = \frac{5 \times 2V \times R_F}{\left(\frac{D_{MAX}}{F_{SW}}\right) \times m \times \left(\frac{dV_L}{dt}\right)} \quad (131)$$

From (131), all of the variables are now known except for m which is a dimensionless number indicating the amount of desired slope compensation. Typical values of m are between 0.5≤m≤1, where 0.5 is the minimum amount of slope compensation necessary to assure stability for peak CMC. As m is increased beyond 1, peak CMC behaves more towards voltage mode control (VMC). A good starting point is to design for m=0.75.

$$R_{SLOPE} = \frac{5 \times 2V \times 536\Omega}{\left(\frac{0.65}{300kHz}\right) \times 0.75 \times \left(0.027\frac{V}{\mu s}\right)} = 122K\Omega \rightarrow 158K\Omega \quad (132)$$

8 SCHEMATIC and BILL of MATERIAL (BOM)

The schematic diagram for the design example is shown in Figure 29. Component values shown may differ slightly from calculated values. Also shown in Table 3 is the BOM listing each manufacturer and component part number corresponding to the schematic shown in Figure 29.

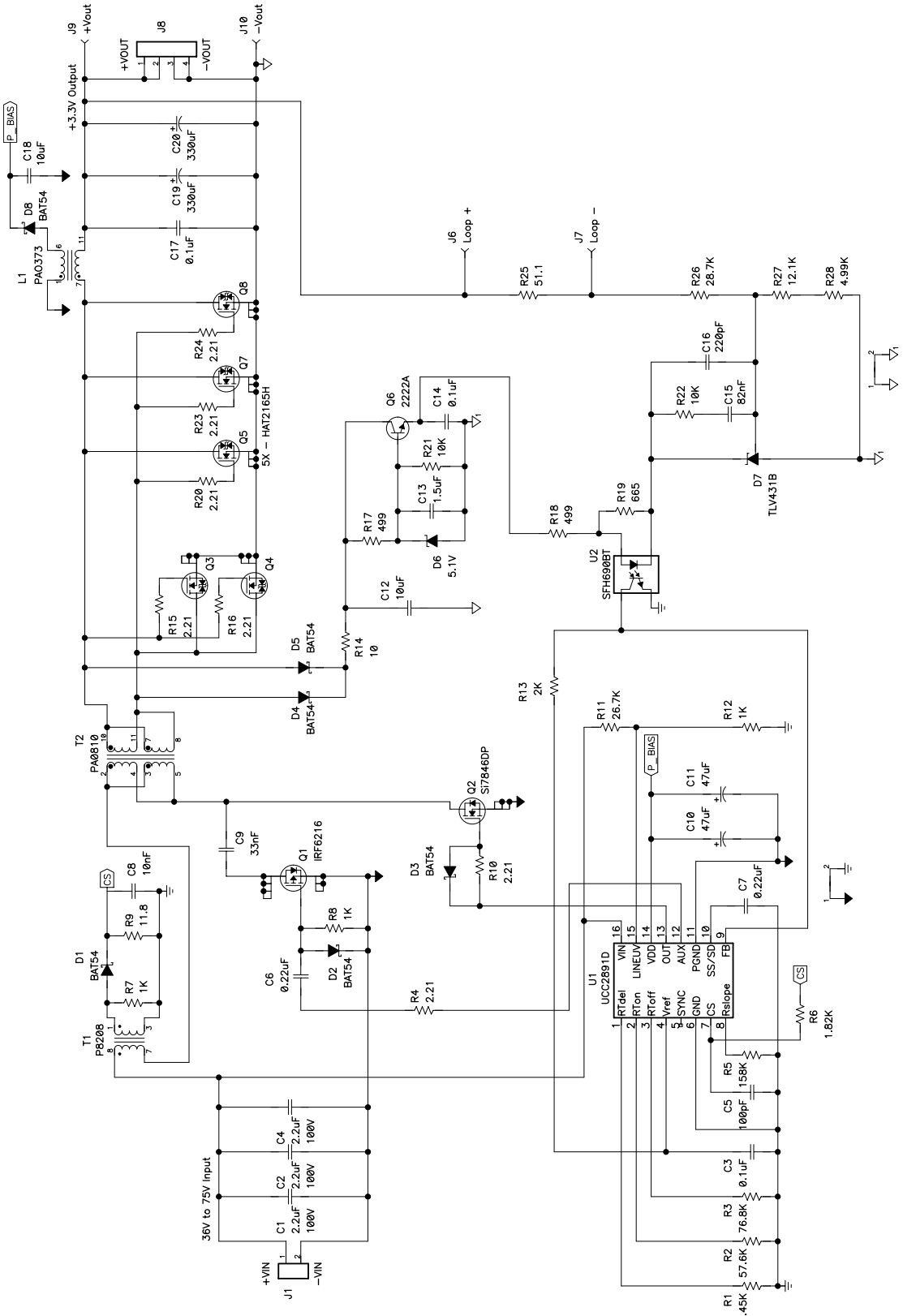


Figure 29. UCC2891 Design Example Schematic

Table 3. UCC2891 Design Example List of Materials

RefDes	QTY	Description	SIZE	MFR	PART NUMBER
C1, C2, C4	3	Capacitor, ceramic, 2.2 µF, 100-V, X7R, 20%	1812	TDK	C4532X7R2A225M
C3, C14, C17	3	Capacitor, ceramic, 0.1-µF, 50-V, X7R, 20%	805	Vishay	VJ0805Y104MXAA
C5	1	Capacitor, ceramic, 100-pF, 50-V, NPO, 10%	805	Vishay	VJ0805A101KXAA
C6, C7	2	Capacitor, ceramic, 0.22-µF, 50-V, X7R, 20%	805	TDK	C2012X7R1H224M
C8	1	Capacitor, ceramic, 10-nF, 50-V, X7R, 20%	805	Vishay	VJ0805Y103MXAA
C9	1	Capacitor, ceramic, 33-nF, 100-V, X7R, 20%	805	Vishay	VJ0805Y333MXBA
C10, C11	2	Capacitor, tantalum chip, 47-µF, 16V	C	Vishay	595D476X9016C2T
C12, C18	2	Capacitor, ceramic, 10-uF, 16-V, X5R, 20%	1206	TDK	C3216X5R1C106M
C13	1	Capacitor, ceramic, 1.5-µF, 10-V, X5R, 20%	805	TDK	C2012X5R1A155M
C15	1	Capacitor, ceramic, 82-nF, 50-V, X7R, 10%	805	Vishay	VJ0805Y823KXAA
C16	1	Capacitor, ceramic, 220-pF, 50-V, NPO, 10%	805	Vishay	VJ0805A221KXAA
C19, C20	2	Capacitor, POSCAP, 330-µF, 6.3-V, 20%	7343 (D)	Sanyo	6TPD330M
D1, D2, D3, D4, D5, D8	6	Diode, schottky, 200-mA, 30-V	SOT23	Vishay	BAT54
D6	1	Diode, zener, 5.1-V, 350-mW	SOT23	Vishay	BZX84C5V1
D7	1	Adjustable precision shunt regulator, 0.5%	SOT23	ON Semi	TLV431BSN1T1
J1	1	Terminal block, 2-pin, 15-A, 5.1 mm	0.40 x 0.35	OST	ED500/2DS
J6, J7, J9, J10	4	Printed circuit pin, 0.043 Hole, 0.3 Length	0.043	Mill-Max	3103-1-00-15-00-00-0X-0
J8	1	Terminal block, 4-pin, 15-A, 5.1mm	0.80 x 0.35	OST	ED500/4DS
L1	1	Inductor, 2 µH, 1 primary, 1 secondary	Planar	Pulse	PA0373
Q1	1	MOSFET, P-channel, 150-V, 2.2-A, 240-mΩ	SO8	IR	IRF6216
Q2	1	MOSFET, N-channel, 150-V, 6.7-A, 50- mΩ	Power Pak S08	Vishay	Si7846DP
Q3, Q4, Q5, Q7, Q8	5	MOSFET, N-channel, 30-V, 55-A, 2.5- mΩ	LFPAK	Renesas	HAT2165H
Q6	1	Bipolar, NPN, 40-V, 600-mA, 225-mW	SOT23	Vishay	MMBT2222A
R1	1	Resistor, chip, 8.45K-Ω, 1/10W, 1%	805	Vishay	CRCW0805-8451-F
R2	1	Resistor, chip, 57.6K-Ω, 1/10W, 1%	805	Vishay	CRCW0805-5762-F
R3	1	Resistor, chip, 76.8K-Ω, 1/10W, 1%	805	Vishay	CRCW0805-7682-F
R4, R10, R15, R16, R20, R23, R24	7	Resistor, chip, 2.21-Ω, 1/10W, 1%	805	Vishay	CRCW0805-2R21-F
R5	1	Resistor, chip, 158K-Ω, 1/10W, 1%	805	Vishay	CRCW0805-1583-F
R6	1	Resistor, chip, 1.82K-Ω, 1/10W, 1%	805	Vishay	CRCW0805-1821-F
R7, R8, R12	3	Resistor, chip, 1K-Ω, 1/10W, 1%	805	Vishay	CRCW0805-1001-F

RefDes	QTY	Description	SIZE	MFR	PART NUMBER
R9	1	Resistor, chip, 11.8 Ω, 1/10W, 1%	805	Vishay	CRCW0805-11R8-F
R11	1	Resistor, chip, 26.7 kΩ, 1/10W, 1%	805	Vishay	CRCW0805-2672-F
R13	1	Resistor, chip, 2 kΩ, 1/10W, 1%	805	Vishay	CRCW0805-2001-F
R14	1	Resistor, chip, 10 Ω, 1/10W, 1%	805	Vishay	CRCW0805-10R0-F
R17, R18	2	Resistor, chip, 499 Ω, 1/10W, 1%	805	Vishay	CRCW0805-4990-F
R19	1	Resistor, chip, 665 Ω, 1/10W, 1%	805	Vishay	CRCW0805-6650-F
R21, R22	2	Resistor, chip, 10 kΩ, 1/10W, 1%	805	Vishay	CRCW0805-1002-F
R25	1	Resistor, chip, 51.1 Ω, 1/10W, 1%	805	Vishay	CRCW0805-51R1-F
R26	1	Resistor, chip, 28.7 kΩ, 1/10W, 1%	805	Vishay	CRCW0805-2872-F
R27	1	Resistor, chip, 12.1 kΩ, 1/10W, 1%	805	Vishay	CRCW0805-1212-F
R28	1	Resistor, chip, 4.99 kΩ, 1/10W, 1%	805	Vishay	CRCW0805-4991-F
T1	1	Transformer, current sense, 10-A, 1:100	SMD	Pulse	P8208
T2	1	Transformer, high frequency planar	Planar	Pulse	PA0810
U1	1	IC, current mode active clamp PWM controller	SO16	TI	UCC2891D
U2	1	IC, phototransistor, CTR 100%-300%	SOP4	Vishay	SFH690BT

9 UCC2891 DESIGN EXAMPLE PERFORMANCE DATA

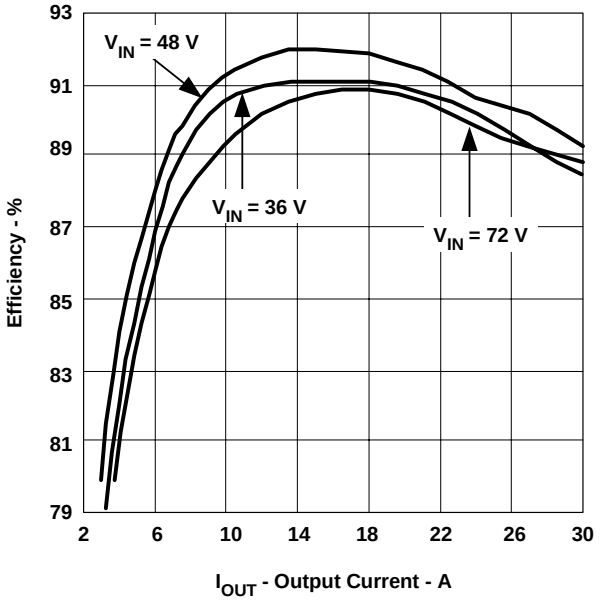


Figure 30.
Efficiency vs. Output Current

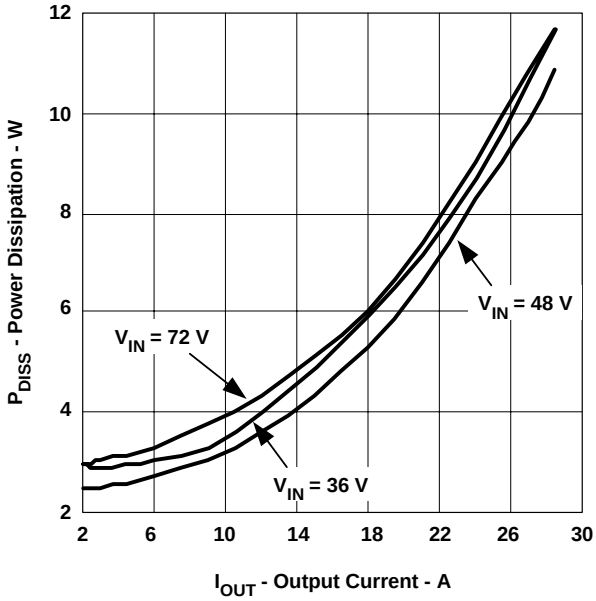


Figure 31.
Power Dissipation vs. Output Current

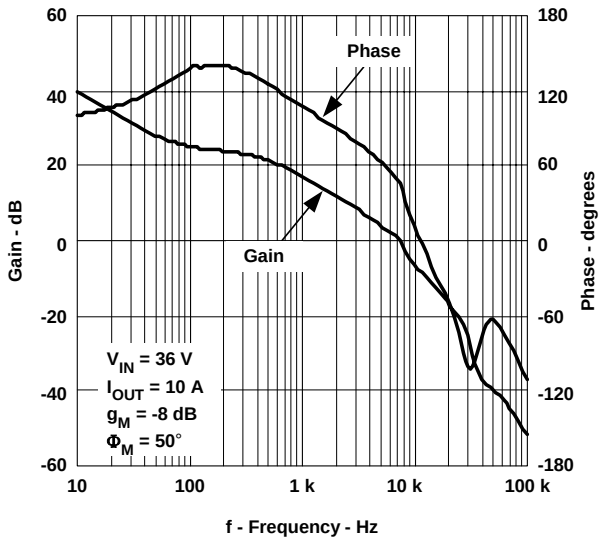


Figure 32.
Gain and Phase vs. Frequency

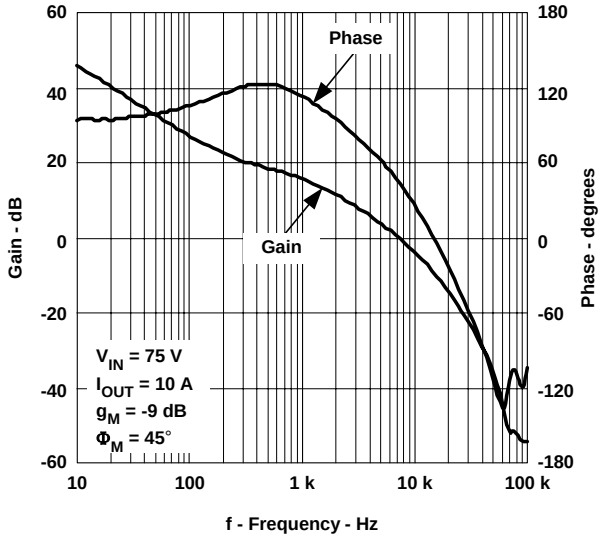


Figure 33.
Gain and Phase vs. Frequency

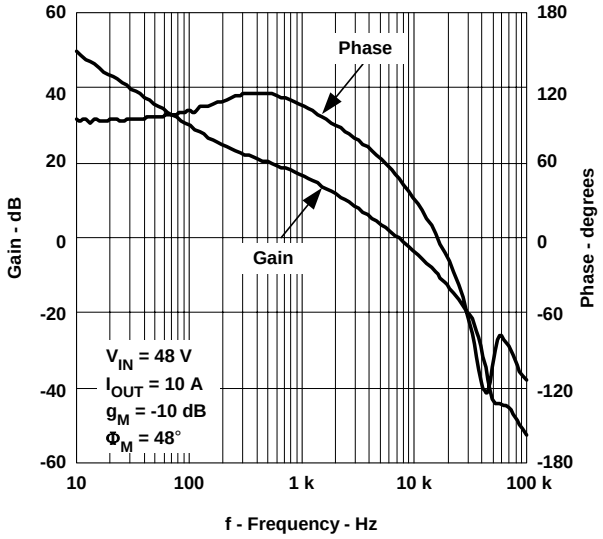


Figure 34.
Gain and Phase vs. Frequency

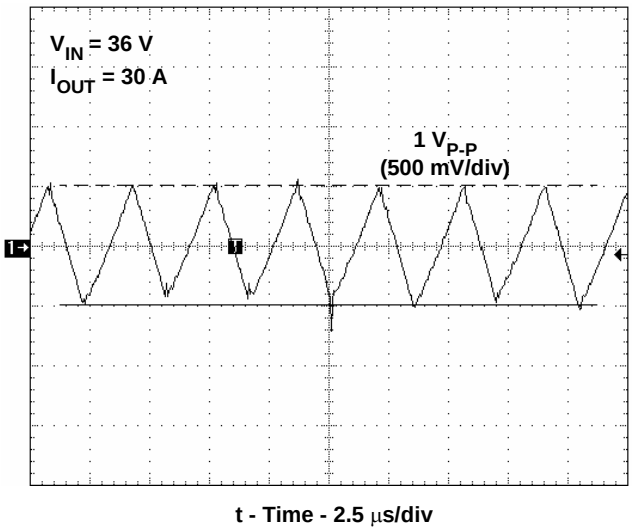


Figure 35. Input Ripple Voltage

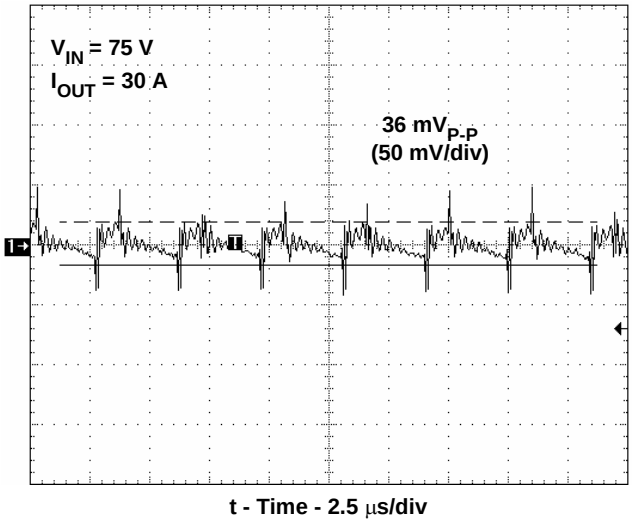


Figure 36. Output Ripple Voltage

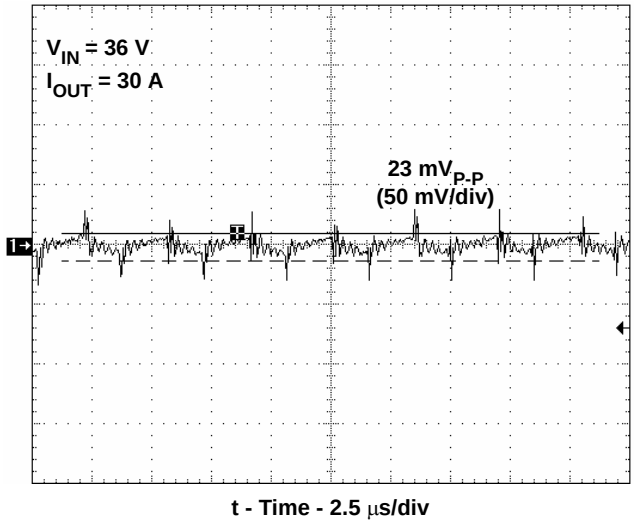


Figure 37. Output Ripple Voltage

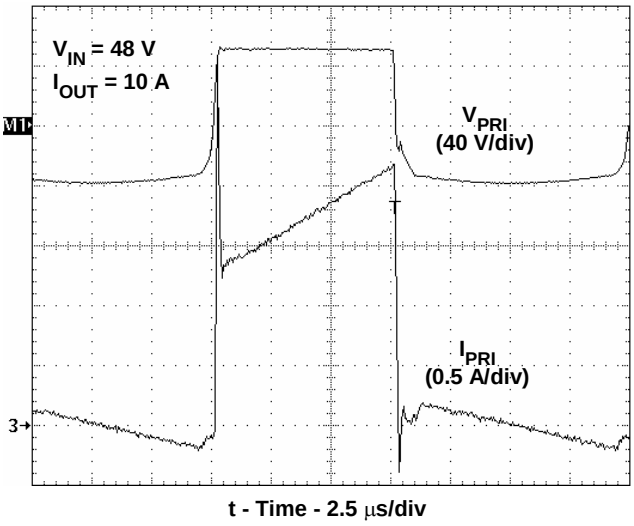


Figure 38. Transformer Primary

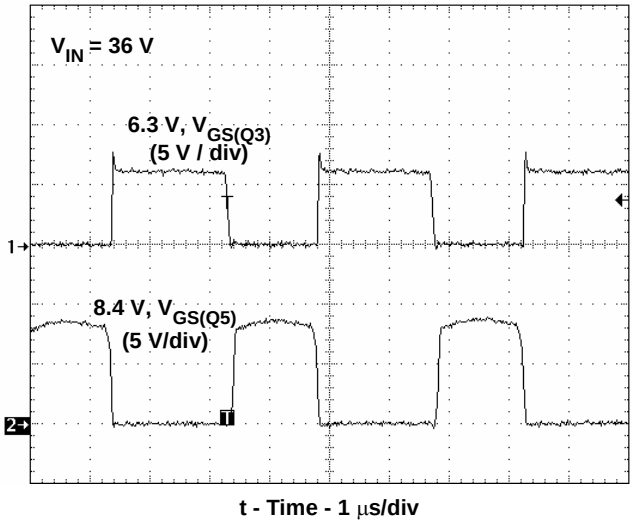


Figure 39. SR Gate Drive (VIN = 36 V)

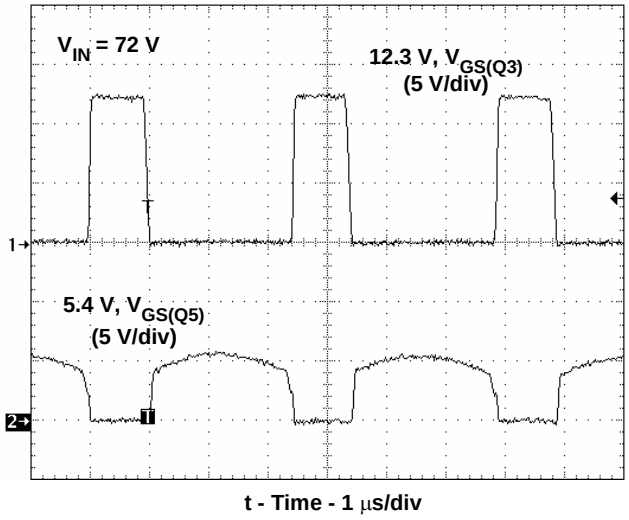


Figure 41. SR Gate Drive (VIN = 72 V)

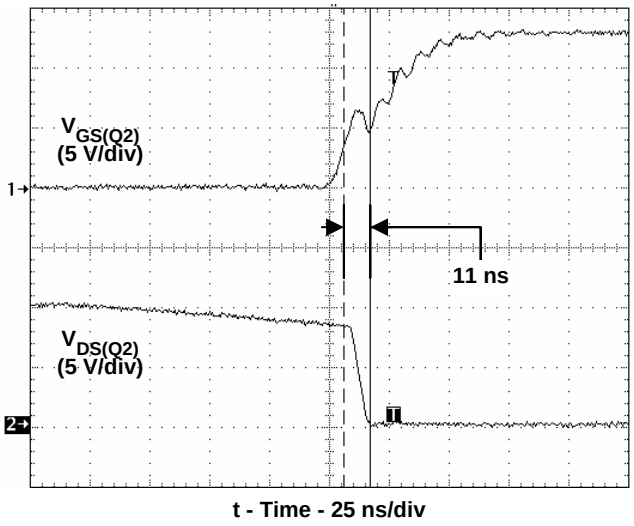


Figure 40. Main MOSFET (Q2) Turn-On

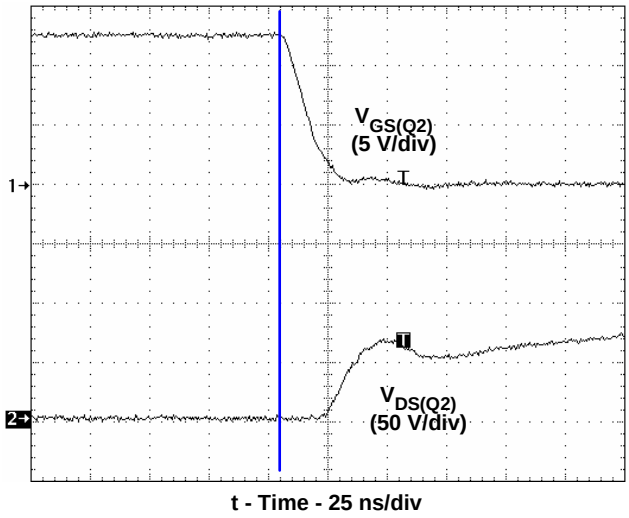


Figure 42. Main MOSFET (Q2) Turn-Off

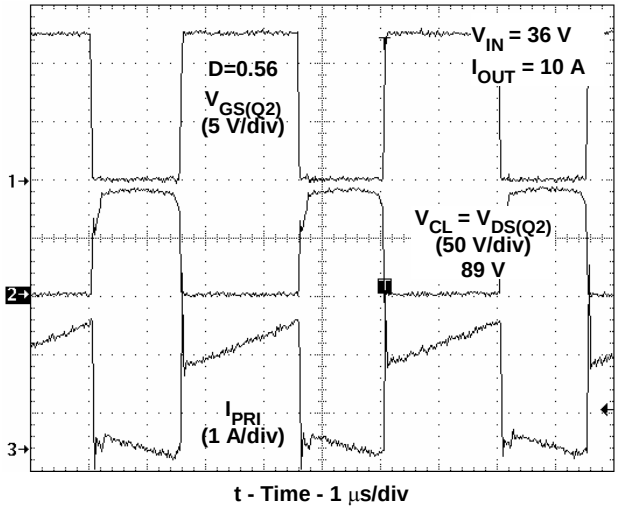


Figure 43. Primary Waveforms

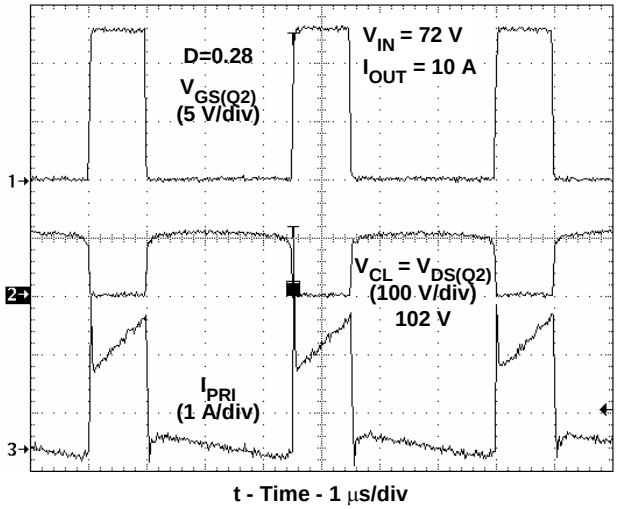


Figure 44. Primary Waveforms

10 SUGGESTED DESIGN IMPROVEMENTS

Once the design was built and tested, several areas of improvement were noticed and have been noted below. Component reference designations in the following notes refer to the schematic of Figure 29.

10.1 Main MOSFET ZVS

From Figure 40, the main MOSFET, Q_2 was shown not to switch at zero voltage as indicated by the 11ns overlap between V_{GS} and V_{DS}. Increasing the delay time, adding an external inductor in series with the transformer primary and adding a saturable reactor in series with the transformer secondary each had no effect on moving the turn-on voltage closer to ZVS. It is believed that the forward synchronous MOSFET (Q_3, Q_4) is conducting for a portion of the dead-time period when ZVS should be occurring. During the set delay period, the resonant energy is circulating through the transformer primary. If the secondary is energized for even a brief portion of the ZVS period, then the stored resonant inductive energy necessary for discharging the resonant capacitance is lost as it is inadvertently coupled to the secondary. This seems to be a natural consequence of using self driven SR in the active clamp forward converter. A possible design improvement might be to drive both synchronous rectifiers with a control driven solution instead of a transformer driven approach.

10.2 Soft Start of V_{OUT}

The output voltage was found to overshoot during initial turn-on only. When power is initially transferred from the primary to the secondary, there is a brief period of time required for the converter secondary side to charge the optocoupler biasing circuitry and TLV431 feedback circuitry. During this time the converter output starts to rise, but since the TLV431 can only sink current, the PWM is not yet receiving any feedback voltage from the secondary. For low output voltage designs this is a problem since the converter output rises quickly to the regulation point (and beyond) before the feedback circuitry is fully operational. To prevent this overshoot it is necessary to control the rate of rise of the output from the secondary side as well as through the primary side soft start. Start up performance is improved when the feedback circuitry is pre-biased but this requires a dedicated secondary side voltage that must be regulating prior to the UCC2891 converter. The TLV431 is a popular choice for feedback compensation, but it may not be the best choice for low voltage converters. A better approach may be to use an operational amplifier with a precision voltage reference. This solution would outperform the TLV431 because the error amplifier can now source current necessary to drive the optocoupler. Improved secondary side control during start-up is another advantage since the rise rate of the reference voltage could also be independently controlled.

10.3 Power Stage Efficiency Improvement

Using OTS components has the advantage of simplifying the design procedure. However, when choices are limited to OTS components only, the design of the power stage may sometimes not be optimal, particularly in the area of magnetic components. For this example, the transformer was found to have enough headroom to lower the switching frequency down to about 250kHz without approaching saturation. The efficiency for this design example operating at 250 kHz is shown in Figure 45, and compared to 300 kHz operation in Figure 46.

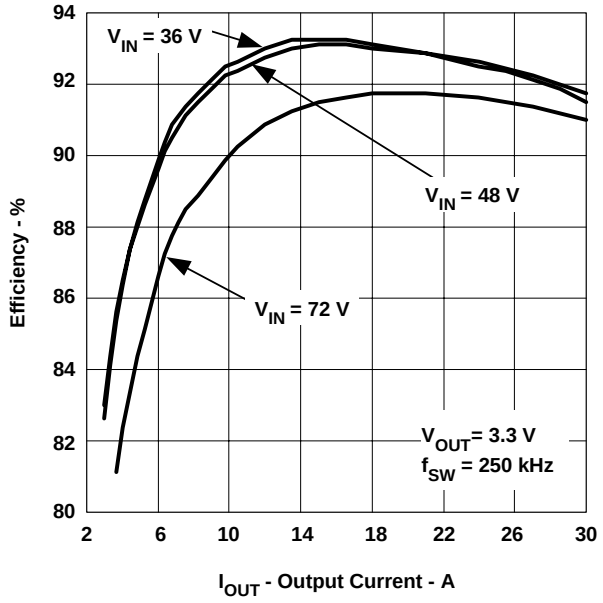


Figure 45. Efficiency vs. Output Current

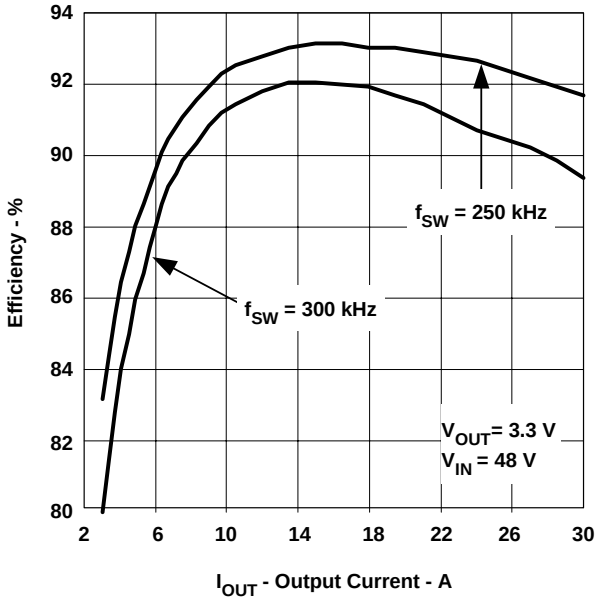


Figure 46. Efficiency vs. Output Current

11 CONCLUSION

A step by step design procedure of a 3.3 V, 100 W active clamp forward converter operating in peak CMC has been show. The design example is based upon using the UCC2891 Active Clamp PWM Current Mode controller, however the power stage design procedure is applicable to any low-side active clamp forward converter. The concept of ZVS has been explained as it applies to the active clamp forward topology. The details of the major component losses within the power stage have also been examined. Although the final design was unable to fully ZVS the main MOSFET, efficiencies greater than 90 percent over a wide range of V_{IN} and I_{OUT} have been claimed. ZVS design solutions and converter performance improvements have also been presented.

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