FIVE to TEN SERIES CELL LITHIUM-ION OR LITHIUM-POLYMER BATTERY PROTECTION AND AFE IC

FEATURES

- 5-,6-,7-,8-,9-, or 10 Series Cell Protection
- PMOS FET Drive for Charge and Discharge FETs
- Capable of operation with 1mΩ Sense Resistor
- Supply Voltage Range from 7.0V to 50V
- Low Supply Current of 150 μA Typical
- Integrated 5.0V 25-mA LDO
- Integrated 3.3V 25-mA LDO

Stand Alone Mode

- Pack protection control and recovery
- Individual cell monitoring
- Integrated cell balancing
- Programmable Threshold and Delay time for
  - Over Voltage
  - Under Voltage
  - Over Current in Discharge
  - Short Circuit in Discharge
- Fixed Over Temperature Protection

Host Control Mode

- I^2C Interface to Host Controller
- Analog interface for Host cell measurement and system Charge/Discharge current
- Host controlled protection recovery
- Host controlled cell balancing

APPLICATIONS

- Cordless Power Tools
- Power Assisted bicycle and scooter
- UPS
- Medical equipments

DESCRIPTION

The bq77PL900 is a five to ten series cell lithium-ion battery pack protector. With the integrated I^2C communication interface it is also suitable as an analog front end (AFE) that incorporates two LDOs, one of 5.0V @ 25mA and a second of 3.3V @ 25mA to power a Host controller.

The bq77PL900 integrates a voltage translation system to extract battery parameters such as individual cell voltages and charge/discharge current. Other parameters such as voltage protection thresholds and detection delay time can be programmed by using the internal EEPROM which increases the flexibility of the battery management system.

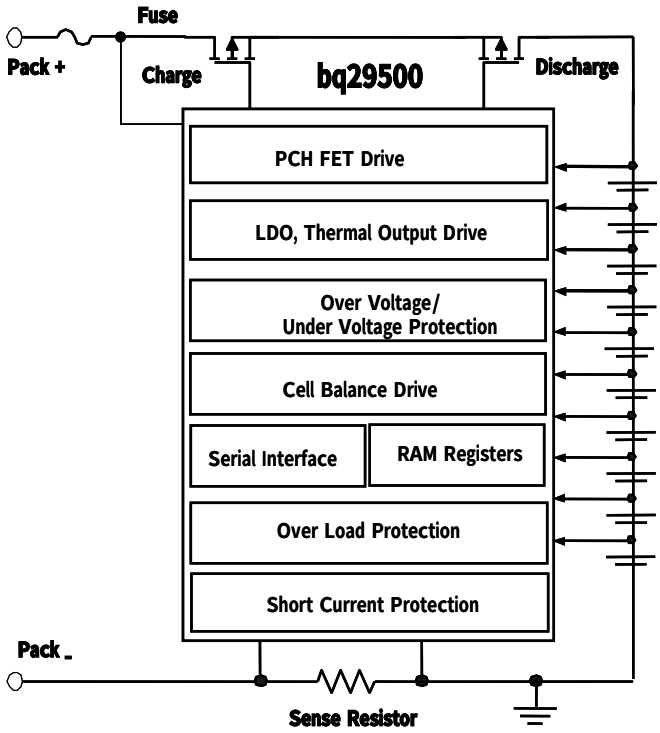
The bq77PL900 primarily acts as a Stand Alone battery protection system (Stand Alone Mode). It can be combined with a micro controller to offer fuel gauge or other battery management capabilities to the Host system (Host Control Mode).

The bq77PL900 provides full safety protection for over voltage, under voltage, over current in discharge and short circuit in discharge conditions. In safety conditions the bq77PL900 turns off the FET drive autonomously dependant on the internal EEPROM threshold and timing configuration setting. No external components are needed to configure the protection features.

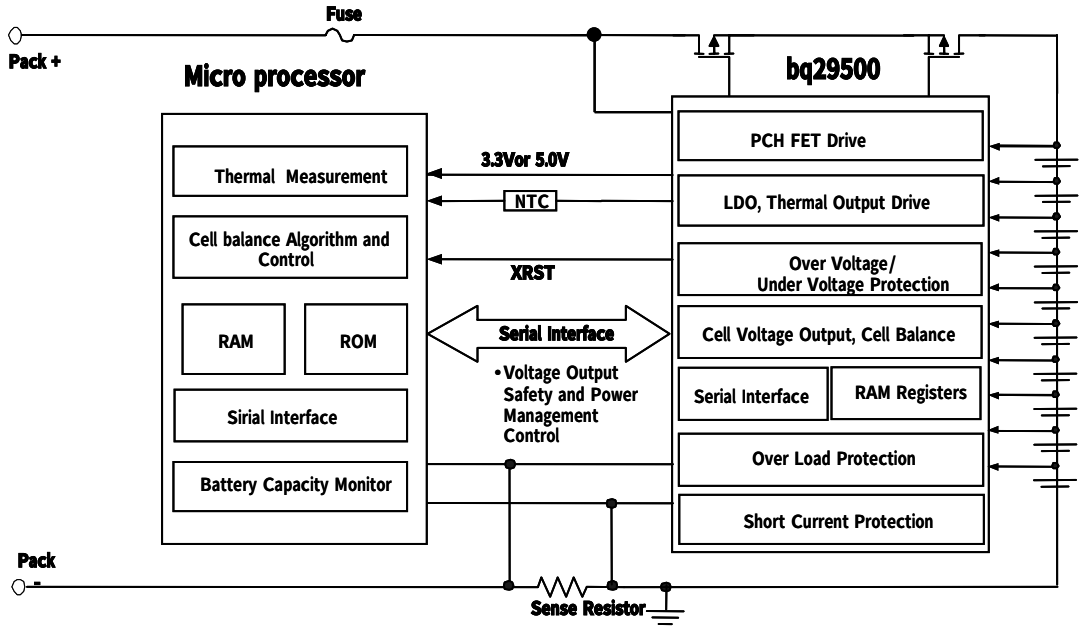
The analog outputs allow the host to observe individual cell voltages and charge/discharge current. Cell balancing of each cell can be performed autonomously or the host can control it via a cell bypass path integrated into the bq77PL900, which can be enabled via the internal control register accessible via the I^2C like interface. The maximum bypass current is set via an external series resistor and internal FET on resistance (typ. 400Ω). Optionally, external bypass cell balance FETs could

1 TYPICAL IMPLEMENTATION

1.1 Stand Alone Mode



1.2 Host Control Mode



2 PIN DETAILS

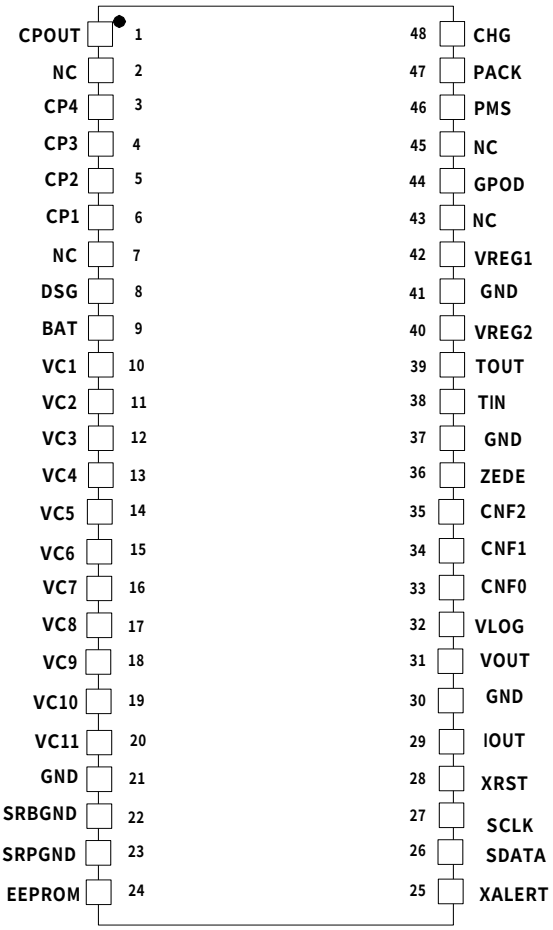
2.1 Pin Descriptions

Pin #	Name	Description
1	CPOUT	Charge pump output and Internal power source.
2	NC	No Connect (not electrically connected)
3	CP4	Charge pump capacitor 1 connection terminal(GND)
4	CP3	Charge pump capacitor 1 connection terminal
5	CP2	Charge pump capacitor 2 connection terminal
6	CP1	Charge pump capacitor 2 connection terminal
7	NC	No Connect (not electrically connected)
8	DSG	Discharge FET gate drive
9	BAT	Power supply voltage
10	VC1	Sense voltage input terminal for most positive cell, balance current input for most positive cell and battery stack measurement input

Pin #	Name	Description
11	VC2	Sense voltage input terminal for second most positive cell, balance current input for second most positive cell and return balance current for most positive cell.
12	VC3	Sense voltage input terminal for third most positive cell, balance current input for third most positive cell and return balance current for second most positive cell.
13	VC4	Sense voltage input terminal for fourth positive cell, balance current input for fourth positive cell and return balance current for third most positive cell.
14	VC5	Sense voltage input terminal for fifth positive cell, balance current input for fifth positive cell and return balance current for fourth most positive cell.
15	VC6	Sense voltage input terminal for sixth positive cell, balance current input for sixth positive cell and return balance current for fifth most positive cell.
16	VC7	Sense voltage input terminal for seventh positive cell, balance current input for seventh positive cell and return balance current for sixth most positive cell.
17	VC8	Sense voltage input terminal for eighth positive cell, balance current input for eighth positive cell and return balance current for seventh most positive cell.
18	VC9	Sense voltage input terminal for ninth positive cell, balance current input for ninth positive cell and return balance current for eighth most positive cell.
19	VC10	Sense voltage input terminal for tenth positive cell, balance current input for tenth positive cell and return balance current for ninth most positive cell.
20	VC11	Sense voltage input terminal for most negative cell, return balance current for least positive cell.
21	GND	Power supply ground
22	SRBGND	Current sense terminal(Connect Battery to cell's GND)
23	SRPGND	Current sense positive terminal when discharging relative to SRNGND, Current sense negative terminal when charging relative to SRGND,. (Connect to Pack GND)
24	EEPROM	Active high EEPROM write enable pin. During normal operation should be connected to GND
25	XALERT	Open-drain output used to indicate status register change. With an internal 100kΩ pull-up to VREG1or VREG2
26	SDATA	Open-drain bi-directional serial interface data with an internal 10kΩ pull-up to V_{LOG}
27	SCLK	Open-drain bi-directional serial interface clock with an internal 10kΩ pull-up to V_{LOG}
28	XRST	Power on reset output. Active low open-drain output for micro processor
29	IOUT	Amplifier output for charge/discharge current measurement
30	GND	Power supply ground
31	VOUT	Amplifier output for cell voltage measurement
32	VLOG	Data I/O voltage set by connecting either VREG1 or VREG2
33	CNF0	Used cell for number determination in combination with CNF1 and CNF2
34	CNF1	Used cell for number determination in combination with CNF0 and CNF2
35	CNF2	Used cell for number determination in combination with CNF0 and CNF1
36	ZEDE	Protection delay test pin. Minimizes protection delay times when connected to VLOG. Programmed delay times used when pulled to GND, normal operation.

Pin #	Name	Description
37	GND	Power supply ground
38	TIN	Temperature sensing input
39	TOUT	Thermistor bias current source
40	VREG2	Integrated 3.3V regulator output
41	GND	Should be connected system GND, not power supply GND
42	VREG1	Integrated 5.0V regulator output
43	NC	No Connect (not electrically connected)
44	GPOD	General purpose N-CH FET open drain output
45	NC	No Connect (not electrically connected)
46	PMS	Determines CHG output state for zero volt charge
47	PACK	PACK positive terminal and alternative power source
48	CHG	Charge FET gate drive

2.2 Pin Out Diagrams



Package Dissipation Ratings

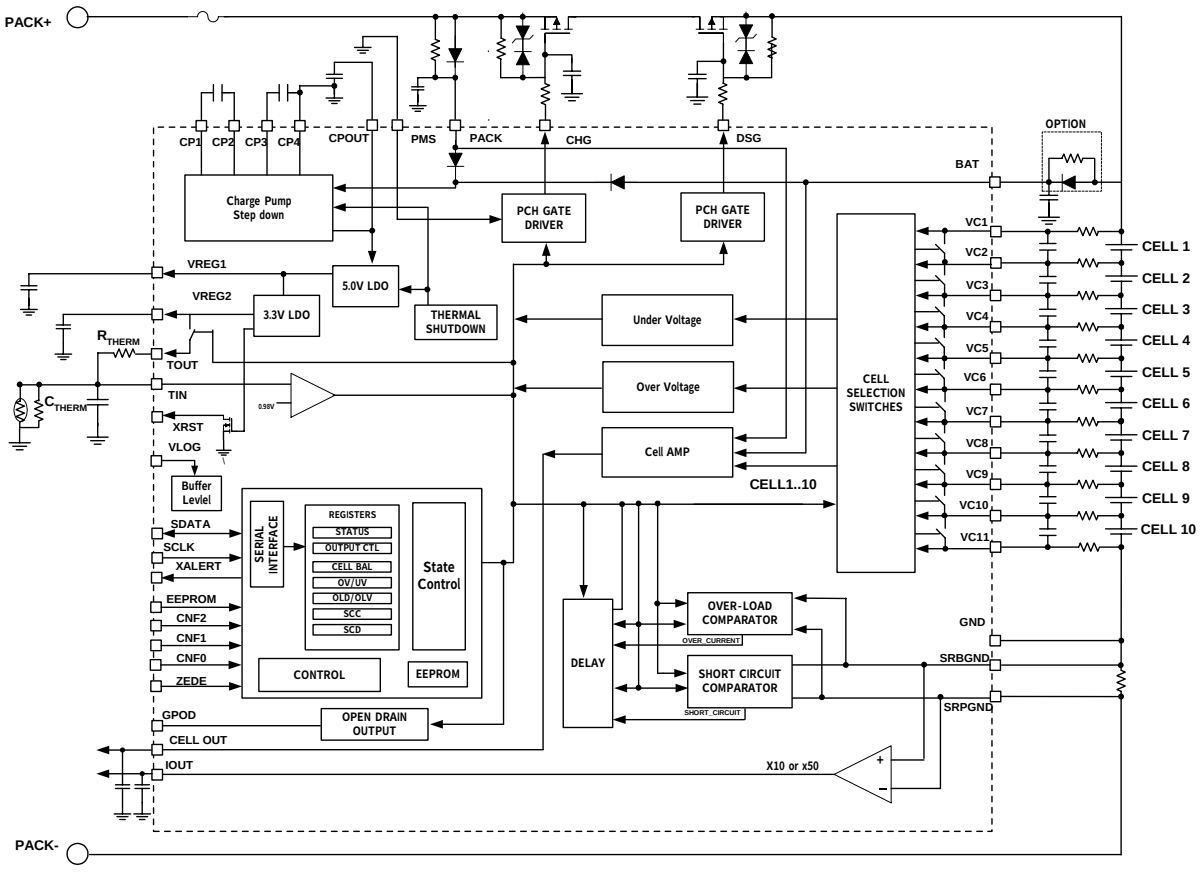
PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A \geq 70°C$	$T_A = 85°C$ POWER RATING	$T_A = 100°C$ POWER RATING
DL	1388mW	11.1mW/°C	720mW	555mW

3 ORDERING INFORMATION

T_A	PACKAGED
	SSOP48
-40°C to 100°C	bq77PL900DL

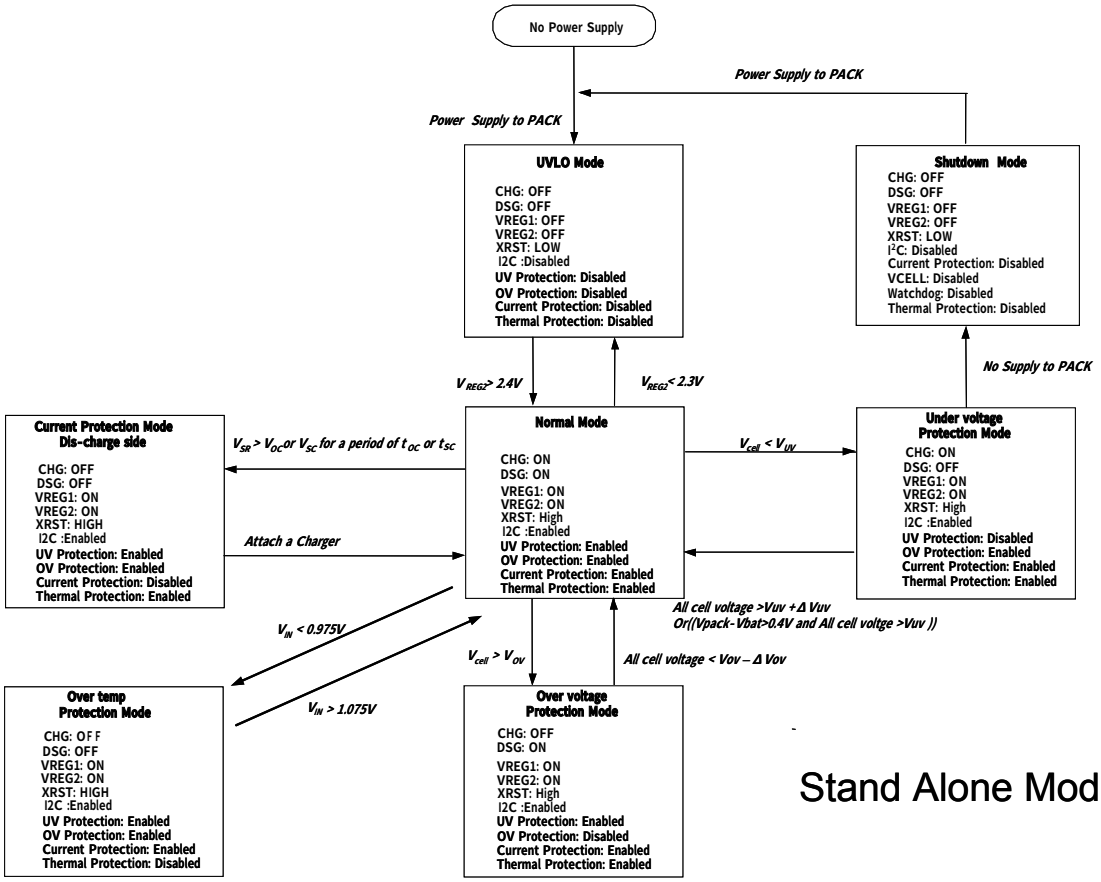
(1) The bq77PL900 can be ordered in tape and reel by adding the suffix R to the orderable part number, i.e., bq77PL900DLR.

FUNCTIONAL BLOCK DIAGRAM



4 SAFETY STATE OVERVIEW

4.1 Stand Alone Mode

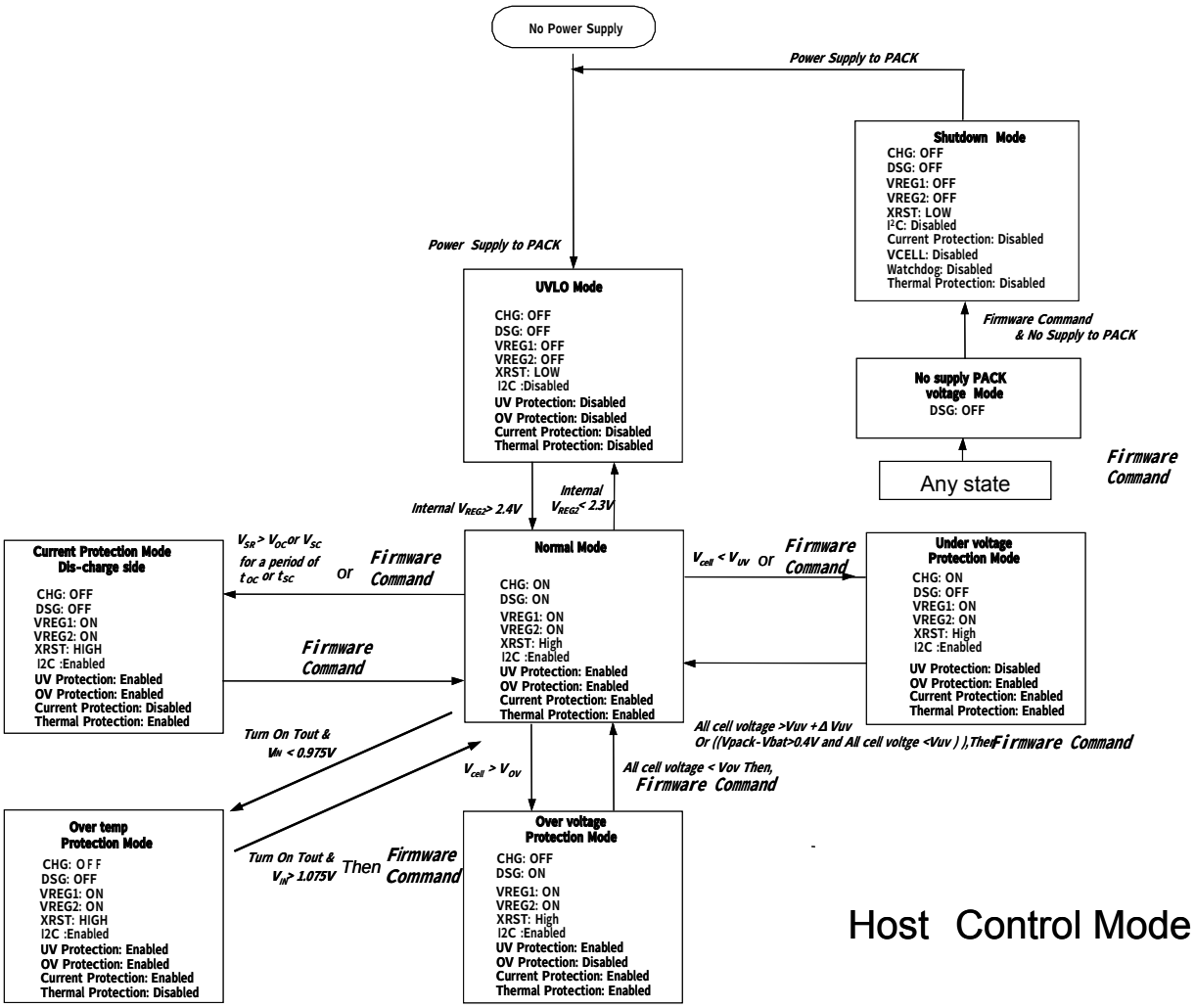


Stand Alone Mode

4.2 Stand Alone STATUS bit, XALERT and FET Transition Summary

MODE TRANSITION	STATUS BIT	XALERT	FET ACTIVITY
Normal to Current Protection	SCD or OCD = 1	H to L	DSG and CHG off
Current Protection to Normal	SCD or OCD = 0	L to H	DSG and CHG on
Normal to Over Voltage Protection	OVP = 1	H to L	CHG off
Over Voltage Protection to Normal	OVP = 0	L to H	CHG on
Normal to Under Voltage Protection (When VAPCK goes down to 0V, move to shutdown mode)	UVP = 1	H to L	DSG off
Under Voltage Protection to Normal	UVP = 0	L to H	DSG on
Normal to Over temperature	OVT=1	H to L	DSG and CHG off
Over temperature to Normal	OVT=0	L to H	DSG and CHG on

4.3 Host Mode



4.4 Host Control Summary

MODE TRANSITION		Function and Firm ware Procedure
Normal to Current protection		Vsr > Voc or Vsc for period of toc or tsc Automatically, DSG and CHG turn off , SCD or OCD status changes=1, XALERT=L
Current protection to Normal		1.Send commands to transition LTCLR from 0 to 1 to 0 2. Read status bit. XALERT would change to H. 3.Set CHG and DSG FET ON to enable normal operation
Normal to Over voltage protection		Vcell > Vov for period of tov Automatically, CHG turns off, UV status changes=1,XALERT=L
Over voltage protection to Normal		1.Confirm the OVP protection status is cleared 2. Send command LTCLR from 1 to 0 3. Read status bit. XALERT would change to H. 4.Set CHG FET ON to enable normal operation
Normal to Undervoltage protection	UVFET_DIS=0	Vcell < Vuv for period of tuv Automatically, DSG turns off, UV status changes=1,XALERT=L
	UVFET_DIS=1	1.Vcell < Vuv or for period of tuv, UV status changes=1,XALERT=L 2. Send commands to turn off DSG .
Under voltage protection to Normal	UVFET_DIS=X	1.Confirm the OVP protection status is cleared 2. Send command LTCLR from 1 to 0 3.Set DSG FET ON to enable normal operation 4. Read status bit. XALERT would change to H.
Normal to Over temperature		1. Send commands to turn on TOUT 2. If TIN voltage <0.975V, DSG and CHG turn off , OVTEMP status changes=1,XALERT=L
Over temperature to Normal		1. Send commands to turn on TOUT (To return to Normal mode, bq77PL900 needs to acknowledge Vth > 1.075V) 2.Send commands to transition LTCLR from 1 to 0 3.Set CHG and DSG FET ON 4. Read status bit. XALERT would change to H.
Any mode to Shut down		1.Set DSG FET OFF 2. Wait PACK voltage goes down to 0V 3.SET shut down bit to “1”

ABSOLUTE MAXIMUM RATINGS

Over operating free–air temperature range (unless otherwise noted)†

Supply voltage range, V_{MAX}	BAT, PACK	-0.3 to 60V
Input voltage range, V_{IN}	VC1~ VC10	-0.3 to 60V
	VC11	0.3 to 5.0V
	VCn to VCn+1, n=1 to 10	-0.3 to 6.0V
	PMS	-0.3 to 60V
	SRP, SRN	–0.5 to 1.0V
	SDATA, SCLK, EEPROM, VLOG, ZEDE, CNF0, CNF1, CNF2, TIN	-0.3 V to 7.0 V
Output voltage range, V_O	CHG	PACK-20 to 60v
	DSG	BAT-20 to 60v
	TOUT, VOUT, IOUT, XRST, XALERT, SDATA, SCLK	-0.3 V to 7.0 V
	CP1, CP2, CP3, CP4, CPOUT, GPOD	-0.3 to 60V
Current for cell balancing, I_{CB}		10mA
Storage temperature range, T_{STG}		–65 to 150°C
Lead temperature (soldering, 10 s), T_{SOLDER}		300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

Note 1: All voltages are with respect to ground of this device except VCn-VC(n+1), where n=1 to 10 cell voltage

5 RECOMMENDED OPERATING CONDITIONS

PARAMETER				MIN	NOM	MAX	UNIT
Supply Voltage		PACK, BAT		7.0		50	V
$V_{I(STARTUP)}$		Start up voltage PACK		7.5			V
V_{LOG}	Logic supply voltage			0.8*V_{REG2}		1.2*V_{REG1}	V
V_I	Input voltage range	VC1 to VC10		0		BAT	V
		VC11		0		0.5	
		SRP, SRN		-0.3		0.5	
		VCn – VC(n+1), (n=1 to 10)		0		5.0	
		PACK, BAT				50	
V_{IH}	Logic level input voltage high	SCLK, SDATA, EEPROM, VLOG (VLOG = VREG1 or VREG2)		0.8*V_{LOG}		V_{LOG}	
V_{IL}	Logic level input voltage low			0		0.2*V_{LOG}	
V_O	Output voltage range	XALERT, SDATA				V_{LOG}	V
		VOUT, IOUT	VGAIN=High		1.2		
			VGAIN=Low		0.975		

PARAMETER			MIN	NOM	MAX	UNIT
		GPOD			45	V
R_{VCX}				400		Ω
C_{REG1}	External 5.0V REG capacitor		2.2			µF
C_{REG2}	External 3.3V REG capacitor		2.2			µF
C_{CP1}, C_{CP2}	Charge pump flying capacitor		1.0			µF
C_{CPOUT}	Charge pump output capacitor		4.7			µF
C_{VOUT}	Output capacitance		0.1			µF
C_{IOUT}	Output capacitance		0.1			µF
I_{OL}		GPOD, XRST			1	mA
f_{SCLK}	Input Frequency	SCLK			100	KHz
	EEPROM number of writes				3	
T_{OPR}	Operating Temperature		-25		85	°C
T_{FUNC}	Functional Temperature		-40		100	°C

6 ELECTRICAL CHARACTERISTICS

6.1 Supply Current

BAT=PACK= 7V to 50V, T_A = -25 ºC to 85ºC, Typical values stated where T_A = 25ºC and BAT=PACK= 36V (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	NOM	MAX	UNIT
I_{CC1}	Supply current 1	No load at REG1, REG2, TOUT, SCLK, SDIN, XALERT CELLAMP, CURRENTAMP=off CHG, DSG= on, Cell balance = off I_{REG1} = I_{REG2} =0mA,Charge pump =off (1) , BAT=PACK= 35V	T_A = 25°C		500	750	µA
			T_A=-40°C to 100°C			850	
I_{CC2}	Supply current 2	No load at REG1, REG2, TOUT, SCLK, SDIN, XALERT CELLAMP, CURRENTAMP=on CHG, DSG= on, Cell balance = off I_{REG1} = I_{REG2} =0mA, Charge pump =off, BAT=PACK= 35V	T_A = 25°C		750	950	µA
			T_A=-40°C to 100°C			1250	
$I_{SHUTDOWN}$	Shutdown Mode	CHG, DSG = off, VREG1= VREG2=off, PACK = 0V, BAT = 35V	T_A=-40°C to 100°C		0.1	1.0	µA

Note 1: Charge pump starts working when (I_{REG33} + I_{REG5}) > 3.0mA

6.2 VREG1, Integrated 5.0V LDO

BAT=PACK= 7V to 50V, T_A = -25 ºC to 85ºC, Typical values stated where T_A = 25ºC and BAT=PACK= 36V (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	NOM	MAX	UNIT
$V_{(REG1)}$	Output voltage	8.5V < PACK or BAT ≤ 50V, I_{OUT} ≤ 25mA	T_A=-40°C to 100°C	4.55	5.0	5.45	V
		7.0V < PACK or BAT ≤ 8.5V, I_{OUT} ≤ 3mA		4.55	5.0	5.45	V
$\Delta V_{(REG1)}$	Output temperature drift	PACK or BAT=50V I_{OUT} = 2mA, T_A = 25°C			±0.2		%
$\Delta V_{(REG1LINE)}$	Line regulation	10V ≤ PACK or BAT≤ 50V, I_{OUT}=2mA, T_A = 25°C			10	20	mV
$\Delta V_{(REG1LOAD)}$	Load regulation	PACK or BAT = 36V, 0.2mA ≤ I_{OUT} ≤ 2mA, T_A = 25°C			7	15	mV
		PACK or BAT = 36V, 0.2mA ≤ I_{OUT} ≤ 25mA, T_A = 25°C			40	100	mV
$I_{REG1MAX}$	Curent limit	PACK or BAT = 36V, VREG1 = 4.5V ,T_A = 25°C		35	75	125	mA
		PACK or BAT = 36V, VREG1 = 0V ,T_A = 25°C		5	20	35	mA

6.3 VREG2, Integrated 3.3V LDO

BAT=PACK= 7V to 50V, T_A = -25 ºC to 85ºC, Typical values stated where T_A = 25ºC and BAT=PACK= 36V (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	NOM	MAX	UNIT
$V_{(REG2)}$	Output voltage	7.0V < PACK or BAT ≤ 50V, I_{OUT} ≤ 25mA	T_A=-40°C to 100°C	3.05	3.3	3.55	V
		7.0V < PACK or BAT ≤ 50V, I_{OUT} = 0.2mA	T_A=-40°C to 100°C	-2%	3.3	+2%	V
$\Delta V_{(REG2)}$	Output temperature drift	PACK or BAT = 50V I_{OUT} = 2mA,	T_A=-40°C to 100°C		±0.2		%
$\Delta V_{(REG2)}$	Line regulation	7.0V ≤ PACK or BAT≤ 50V, I_{OUT}=2mA, T_A=25°C			10	20	mV
$\Delta V_{(REG2)}$	Load regulation	PACK or BAT=36V, 0.2mA ≤ I_{OUT} ≤ 2mA, T_A=25°C			7	15	mV
		PACK or BAT=36V, 0.2mA ≤I_{OUT} ≤ 25mA, T_A=25°C			40	100	mV
$I_{REG2MAX}$	Current limit	PACK or BAT = 36V, VREG2 = 3.0V ,T_A=25°C		25	50	100	mA
		PACK or BAT = 36V, VREG2 = 0.0V ,T_A=25°C		10	20	30	mA

6.4 TOUT, Thermistor Power Supply

BAT=PACK= 7V to 50V, T_A = -25 ºC to 85ºC, Typical values stated where T_A = 25ºC and BAT=PACK= 36V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
V_{TOUT}		I_{OUT} = 0mA, T_A = -40°C to 100°C	3.05		3.55	V
$RDS_{(ON)}$	Pass-element series resistance	I_{OUT} = -1mA at TOUT pin, $RDS_{(ON)}$ = (V_{REG2} – V_{TOUT}) / 1mA, T_A = -40°C to 100°C, I_{reg2}=-0.2mA		50	100	Ω
V_{TINS}	Thermistor sense voltage	T_A=-40°C to 100°C	-5%	0.975	+5%	V
$V_{TINSHYS}$	Thermistor sense hysteresis voltage	T_A=-40°C to 100°C	50	100	150	mV

6.5 Thermal Shutdown

BAT=PACK= 7V to 50V, T_A = -25 ºC to 85ºC, Typical values stated where T_A = 25ºC and BAT=PACK= 36V (unless otherwise noted)

ARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
T_{therm}	Shutdown threshold	PACK or BAT = 36V (1)	TBD	150	TBD	ºC

Note 1: Not 100% tested, guaranteed by design up to 125ºC

6.6 PMS, Pre-charge Mode Select Disable

BAT=PACK= 7V to 50V, T_A = -25 ºC to 85ºC, Typical values stated where T_A = 25ºC and BAT=PACK= 36V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
$V_{PMSDISABLE}$	PMS disable threshold of BAT	PACK = PMS=20V, VREG2=0V, CHG=ON ->OFF	8	13	16	V

6.7 POR, Power On Reset

BAT=PACK= 7V to 50V, T_A = -25 ºC to 85ºC, Typical values stated where T_A = 25ºC and BAT=PACK= 36V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
V_{POR-}	Negative-going voltage input	VLOG=VREG1(5.0V)V	3.85	4.05	4.25	V
		VLOG=VREG2(3.3V)V	2.55	2.65	2.75	V
V_{POR_HYS}	Positive-going hystersis	VLOG = 3.3V	50	150	250	mv
		VLOG = 5.0V	100	250	400	mV
t_{RST}	Reset delay time		1		5	ms

6.8 Cell Voltage Monitor

BAT=PACK= 7V to 50V, T_A = -25 ºC to 85ºC, Typical values stated where T_A = 25ºC and BAT=PACK= 36V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
$V_{CELL\ OUT}$	CELL output	V_{Cn}– V_{Cn+1}= 0V , 20V ≤ BAT ≤50V, VGAIN=Low	TBD	0.975	TBD	V

		V_{Cn}– V_{Cn+1}= 0V , 20V ≤ BAT ≤50V, VGAIN=High	TBD	1.200	TBD	
		V_{Cn}– V_{Cn+1} = 4.5V , 20V ≤ BAT ≤50V		0.3		
REF 1	CELL output	Mode (Note1), 20V ≤ BAT or PACK ≤50V, VGAIN =Low	-2%	0.975	+2%	V
REF 2	CELL output	Mode (Note2), 20V ≤ BAT or PACK ≤50V, VGAIN =High	-2%	1.200	+2%	V
PACK	CELL output	Mode (Note3)	-5%	PACK/50	+5%	V
BAT	CELL output	Mode (Note4)	-5%	BAT/50	+5%	V
CMRR	Common Mode Rejection	CELL max to CELL min, 20V ≤ BAT ≤50V	40			dB
K1	CELL scale factor 1	K={CELL output (VC11=0.0 V, VC10=4.5V) -CELL output (VC11=VC10=0.0V)} / 4.5 (Note5)	0.147	0.150	0.153	
		K={CELL output (VC2=40.5V, VC1=45.0V) -CELL output (VC2=VC1=40.5V)} / 4.5 (Note5)	0.147	0.150	0.153	
K2	CELL scale factor 2	K={CELL output (VC11=0.0V, VC10=4.5V) -CELL output (VC11=VC10=0.0V)} / 4.5 (Note6)	0.197	0.201	0.205	
		K={CELL output (VC2=40.5V, VC1=45.0V) -CELL output (VC2=VC1=40.5V)} / 4.5 (Note6)	0.197	0.201	0.205	
$I_{VCELLOUT}$	Drive current	V_{Cn}– V_{Cn+1}= 0V , Vcell = 0V Ta=-40 to 100°C	12	18		µA
V_{ICR}	CELL output offset error	CELL output (VC2=45.0V, VC1=45.0V) -CELL output (VC2=VC1=0.0V)		-1		mV
R_{BAL}	Cell Balance internal resistance	$RDS_{(ON)}$ for internal FET switch at V_{DS} = 2.0V, BAT=PACK= 35V	-50%	400	+50%	Ω

Note 1 : STATE_CONTROL [VGAIN] = 0, FUNCTION_CONTROL [VAEN] = 1, CELL_SEL[CAL2] = 0,[CAL0] =1, [CAL0] = 1
Note 2 : STATE_CONTROL [VGAIN] = 1, FUNCTION_CONTROL [VAEN] = 1, CELL_SEL[CAL2] = 0,[CAL0] =1, [CAL0] = 1
Note 3 : STATE_CONTROL [VGAIN] = X, FUNCTION_CONTROL [PACK]=1,[VAEN] = 1,
Note 4 : STATE_CONTROL [VGAIN] = X, FUNCTION_CONTROL [BAT]=1,[VAEN] = 1,
Note 5 : STATE_CONTROL [VGAIN] = 0, FUNCTION_CONTROL [VAEN] = 1, CELL_SEL[CAL2] = 0,[CAL0] =0, [CAL0] = 0
Note 6 : STATE_CONTROL [VGAIN] = 1, FUNCTION_CONTROL [VAEN] = 1, CELL_SEL[CAL2] = 0,[CAL0] =0, [CAL0] = 0

6.9 Current Monitor

BAT=PACK= 7V to 50V, T_A = -25 ºC to 85ºC, Typical values stated where T_A = 25ºC and BAT=PACK= 36V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
V_{CELL_OFF}	Input offset voltage	VSRP = VSRN = 0V (Note 1)		1.2		V
$V_{IOUT\_OFF\_DRIFT}$	Input offset voltage drift	VSRP = VSRN = 0V (Note 1)	-3		3	mV
DC gain	Low	(Note 2) -100mV < SRP < +100mV	-2%	10	+2%	
DC gain	High	(Note 3) -20mV < SRP < +20mV	-2%	50	+2%	
$I_{IOUTOUT}$	Drive current	V_{IOUT}= 0.0V T_A=-40 to 100ºC	12	18		µA

Note 1 : STATE_CONTROL [IGAIN] = X, FUNCTION_CONTROL [IAEN] = 1, [IACAL] = 1
Note 2 : STATE_CONTROL [IGAIN] = 0, FUNCTION_CONTROL [IAEN] = 1, [IACAL] = 0

Note 3: STATE_CONTROL [IGAIN] = 1, FUNCTION_CONTROL [IAEN] = 1, [IACAL] = 0

6.10 Battery Protection Thresholds

BAT=PACK= 7V to 50V, T_A = -25 ºC to 85ºC, Typical values stated where T_A = 25ºC and BAT=PACK= 36V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
V_{OV}	OV detection threshold range	Default	4.15		4.50	V
ΔV_{OV}	OV detection threshold program step			50		mV
V_{OVH}	OV detection hysteresis voltage range	Default	0.1		0.4	V
ΔV_{OVH}	OV detection hysteresis program step			0.1		V
V_{UV}	UV detection threshold range	Default	1.40		2.90	V
ΔV_{UV}	UV detection threshold program step			100		mV
V_{UVH}	UV detection hysteresis voltage	Default	0.2		1.2	V
ΔV_{UVH}	UV detection threshold program step			200		mV
V_{OCDT}	OCD detection threshold range	Default	10		85	mV
ΔV_{OCDT}	OCD detection threshold program step			5.0		mV
V_{SCDT}	SCD detection threshold range	Default	60		135	mV
ΔV_{SCDT}	SCD detection threshold program step			5.0		mV
V_{OV_acr}	OV detection threshold accuracy	Default (T_A = 0 to 85℃)	-50	0	+50	mV
V_{UV_acr}	UV detection threshold accuracy	Default	-100	0	+100	mV
V_{OCD_acr}	OCD detection threshold accuracy	Default	-20	0	+20	%
V_{SCD_acr}	SCD detection threshold accuracy	Default	-20	0	+20	%

6.11 Battery Protection Delay Times

BAT=PACK= 7V to 50V, T_A = -25 ºC to 85ºC, Typical values stated where T_A = 25ºC and BAT=PACK= 36V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
t_{OV}	OV detection delay time range	Default	500		2250	ms
Δt_{OV}	OV detection delay time step			250		ms
t_{UV}	UV detection delay time range	Default	0		8000	ms
Δt_{UV}	UV detection delay time step		1.25		1000	ms
t_{OCD}	OCD detection delay time range	Default	20		1600	ms
Δt_{OCD}	OCD detection delay time step		20		100	ms
t_{SCD}	SCD detection delay time range	Default	0		900	µs
Δt_{SCD}	SCD detection threshold program step			60		µs
t_{OV_acr}	OV detection delay time accuracy	Default	-15	0	15	%
t_{UV_acr}	UV detection delay time accuracy	Default	-15	0	15	%
t_{OC_acr}	OC detection delay time accuracy	Default	-15	0	15	%
V_{SCD_acr}	SC detection delay time accuracy	t_{SCD} Max	-15	0	15	%
t_{SRC}	OC/SC recovery timing at Stand Alone Mode		-15	12.8sec	15	%

6.12 Battery Protection Recovery

BAT=PACK= 7V to 50V, T_A = -25 ºC to 85ºC, Typical values stated where T_A = 25ºC and BAT=PACK= 36V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
V_{RECSC}	SC,OC recovery voltage		1.0	1.4	2.0	V
V_{RECUV}	Under voltage recover voltage	V_{RECUV}= V_{PACK}- V_{BAT} , V_{UV}+V_{UVH} >V_{CELL}> V_{UV}	0.05	0.1	0.3	V

FET Drive

BAT=PACK= 7V to 50V, T_A = -25 ºC to 85ºC, Typical values stated where T_A = 25ºC and BAT=PACK= 36V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(FETON)}$	Output voltage, charge, and discharge FETs on	$V_{O(FETONDSG)}$ = $V_{(BAT)}$-$V_{(DSG)}$, V_{GS} connect 1MΩ, BAT=PACK= 35V		8	12	16	V
		$V_{O(FETONCHG)}$ = $V_{(PACK}$-$V_{(CHG)}$, V_{GS} connect 1MΩ, BAT=PACK= 35V		8	12	16	
$V_{(FETOFF)}$	Output voltage, charge and discharge FETs off	$V_{O(FETOFFDSG)}$ = $V_{(PACK)}$-$V_{(DSG)}$, BAT=PACK= 35V				0.2	V
		$V_{O(FETOFFCHG)}$ = $V_{(BAT)}$-$V_{(CHG)}$, BAT=PACK= 35V				0.2	
t_r	Rise time	C_L = 20nF , BAT=PACK= 35V	V_{DSG}: 10% to 90%		5	15	µs
			V_{CHG}: 10% to 90%		5	15	
t_f	Fall time	C_L = 20nF , BAT=PACK= 35V	V_{DSG} : 90% to 10%		90	140	µs
			V_{CHG}: 90% to 10%		90	140	

6.13 Logic

BAT=PACK= 7V to 50V, T_A = -25 ºC to 85ºC, Typical values stated where T_A = 25ºC and BAT=PACK= 36V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
V_{OL}	Logic level output voltage	XALERT, I_{OUT} = 200µA, T_A = -40°C to 100°C			0.4	V
		SDATA, SCLK, XRST. I_{OUT} =1mA, T_A = -40°C to 100°C			0.4	
		GPOD, I_{OUT} =1mA, T_A = -40°C to 100°C			0.6	
I_{LEAK}	Leakage current	GPOD V_{OUT} = 1V, T_A = -40°C to 100°C			1.0	µA
V_{IH}	SCLK (hysteresis input)	Hysteresis		400		mV
R_{UP}	Pull up resistance	XALERT T_A = -40°C to 100°C	60	100	200	KΩ
		DATA, SCLK, T_A = -40°C to 100°C	6	10	20	
		XRST T_A = -40°C to 100°C	1	3	6	
I_{DOWN}	Pull down current	CNF0, CNF1, CNF2 = VREG2		2	4	µA

6.14 I²C Compatible Interface

BAT=PACK= 7V to 50V, T_A = -25 ºC to 85ºC, Typical values stated where T_A = 25ºC and BAT=PACK= 36V (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
t_r	SCLK、SDATA Rise Time		1000	ns
t_f	SCLK 、SDATA Fall Time		300	ns
$t_{w(H)}$	SCLK Pulse Width High	4.0		µs
$t_{w(L)}$	SCLK Pulse Width Low	4.7		µs
$t_{su(STA)}$	Setup time for START condition	4.7		µs
$t_{h(STA)}$	START condition hold time after which first clock pulse is generated	4.0		µs
$t_{su(DAT)}$	Data setup time	250		ns
$t_{h(DAT)}$	Data hold time	0		µs
$t_{su(STOP)}$	Setup time for STOP condition	4.0		µs
$t_{su(BUF)}$	Time the bus must be free before new transmission can start	4.7		µs
t_V	Clock Low to Data Out Valid		900	ns
$t_{h(CH)}$	Data Out Hold Time After Clock Low	0		ns
f_{SCL}	Clock Frequency	0	100	kHz

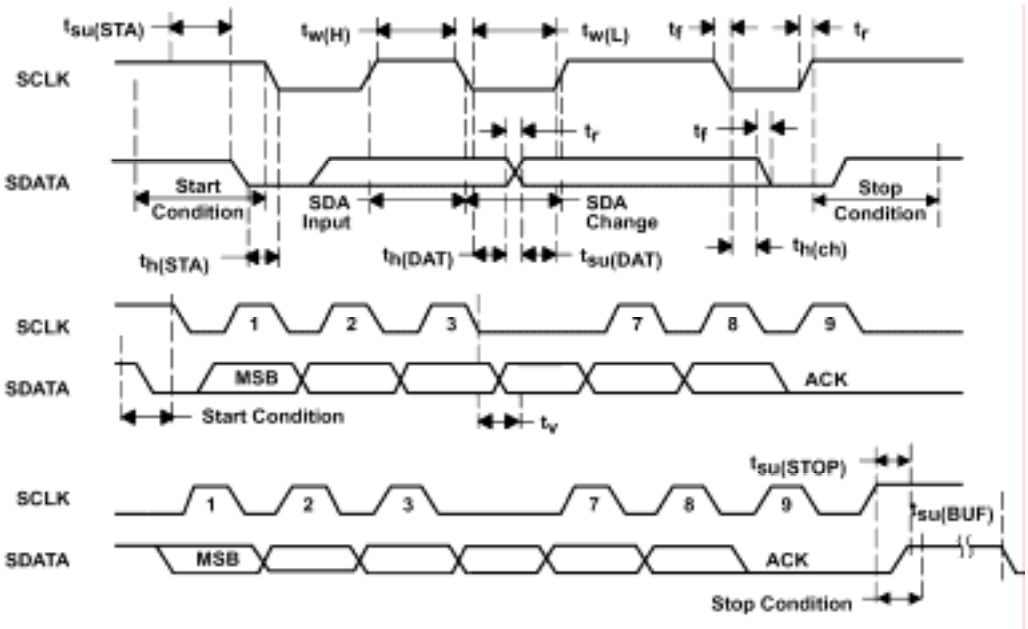


Figure 1: I2C like I/F timing char

7 GENERAL OPERATIONAL OVERVIEW

7.1 Stand Alone Mode and Host Control ModeThe bq77PL900 has two operational modes, 'Stand Alone Mode' and 'Host Control Mode'. The mode is switched by *STATE_CONTROL [HOST]*. In Stand Alone Mode, the battery protection is managed by the bq77PL900 without the need for any external control. In this mode the CHG and DSG FETs are driven ON and OFF automatically and cell balancing is processed by a fixed algorithm if enabled by OCDELAY[CBEN]). In this mode, I^2C communication is enabled and a host can read the registers and set *STATE_CONTROL [HOST]* but can not control any output or function such as Vcell AMP enable. In Host Control Mode, a Host controller can obtain battery information such as voltage and current from the bq77PL900 analog interface. This allows the Host such as a micro controller to calculate remaining capacity or implement an alternative cell balancing algorithm. In this mode, the bq77PL900 still detects cell protection faults and acts appropriately although the recovery method is different from that in Stand Alone mode. The Host controller has control over the recovery method and FET action after the protection state has been entered. The following table contains further details of the protection action differences.

Table 1: Stand Alone Mode and Host Control Mode Protection Summary

<table>
<tr><th>FUNCTION</th><th>MODE</th><th>Stand Alone Mode (HOST=L)</th><th>Host Control Mode (HOST=H)</th></tr>
<tr><td rowspan="2">OV Protection</td><td>Detection</td><td rowspan="9">Automatic

The bq77PL900 detects and recover from protection states and controls the FETs</td><td>Automatic
The bq77PL900 detects an OV voltage and turns OFF CHG FET. Need to turn off cell balancing for correct voltage detection</td></tr>
<tr><td>Recovery</td><td>Host-Control</td></tr>
<tr><td rowspan="2">UV Protection</td><td>Detection</td><td>Host-Control
The bq77PL900 detects a UV voltage but no FET action is taken. Need to turn off cell balancing for correct voltage detection</td></tr>
<tr><td>Recovery</td><td>Host-Control</td></tr>
<tr><td rowspan="2">OCD /SCD Protection</td><td>Detection</td><td>Automatic
The bq77PL900 detects OCD and turns CHG and DSG FETs OFF</td></tr>
<tr><td>Recovery</td><td>Host-Control</td></tr>
<tr><td rowspan="2">Over Temp Protection</td><td>Detection</td><td>Host needs to turn ON</td></tr>
<tr><td>Recovery</td><td>Host-Control</td></tr>
<tr><td>CHG/DSG FET Control</td><td>---</td><td>Automatic
Host can't drive the FET</td><td>Host control
bq77PL900 can't release from protection state automatically</td></tr>
<tr><td>Cell balancing</td><td>---</td><td>CBEN=1: Automatic
CBEN=0: No function</td><td>Host Control
The Host can balance any cells at any time
CBEN=Don't Care</td></tr>
<tr><td>Zerovolt charge1</td><td>PMS = High
ZVC=X</td><td>Automatic
(0V charge current flows thorough CHG FET)</td><td>Automatic</td></tr>
</table>

Zerovolt charge2	PMS = Low, ZVC=0	**No support 0V charge**	**Host-Control** Host should control pre-charge FET by using GPOD pin
Zerovolt charge3	PMS = Low, ZVC=1	**Automatic (0V charge current flows thorough FET that is driven by GPOD)**	

7.2 Normal Operation Mode

When all cell voltages are with in the range of V_{UV} to V_{OV}, and the CHG and DSG FETs are turned ON, the cells are charged and discharged at any time.

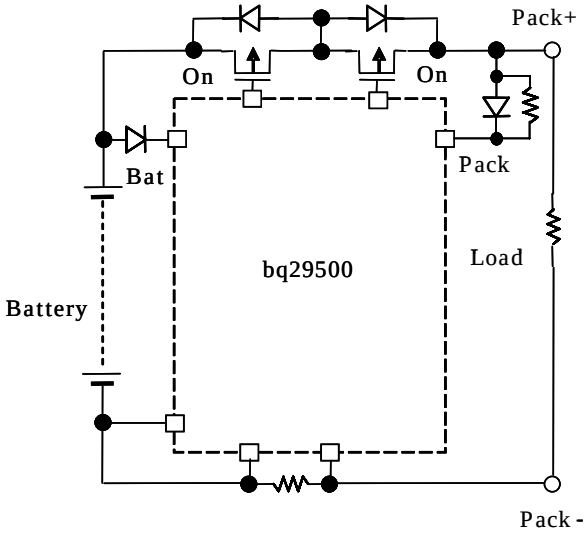


Figure 2: Normal Operation Mode

7.3 Battery Protection

The bq77PL900 fully integrates battery protection circuits including cell over voltage, under voltage, over current in discharge and short circuit in discharge detection. Each detection voltage can be adjusted by programming the integrated EEPROM. Also, the detection delay time can be programmed per the following table.

CAUTION: Only a maximum of 3 programming cycles per byte should performed to ensure data stability.

Table 2: Detection Voltage, Detection Delay Time Summary

PARAMETER		MIN	MAX	STEP	BITS
Over Voltage	Voltage	4.150V	4.500 V	50.0 mV	3
	Delay	0.5s	2.25s	0.25s	3
	Hysteresis	100mV	400mV	50mV	2

Under Voltage	Voltage	1.400V	2.900V	100.0mV	4
	Delay	0ms	30ms	1.25-10ms	4
		1s	8s	1s	
	Hysteresis	100mV	1200mV	0.2V,0.4V	2
Over Current In Discharge	Voltage	10 mV	85mV	5.0 mV	4
	Delay	20ms	16000ms	20ms or 100ms	5
Short Circuit in Discharge	Voltage	60mV	135 mV	5.0 mV	4
	Delay	0 µs	900µs	60 µs	4

7.3.1 Cell Over Voltage and Cell Under Voltage detection

Cell Over Voltage and Cell Under Voltage detection circuit consists of a S/H (sample and hold) circuit and 2 comparators.
S/H period is about 120us for each cell, S/H is performed sequentially on each cell. Once all of cells are checked, the bq77PL900 waits about 50mS for next S/H.

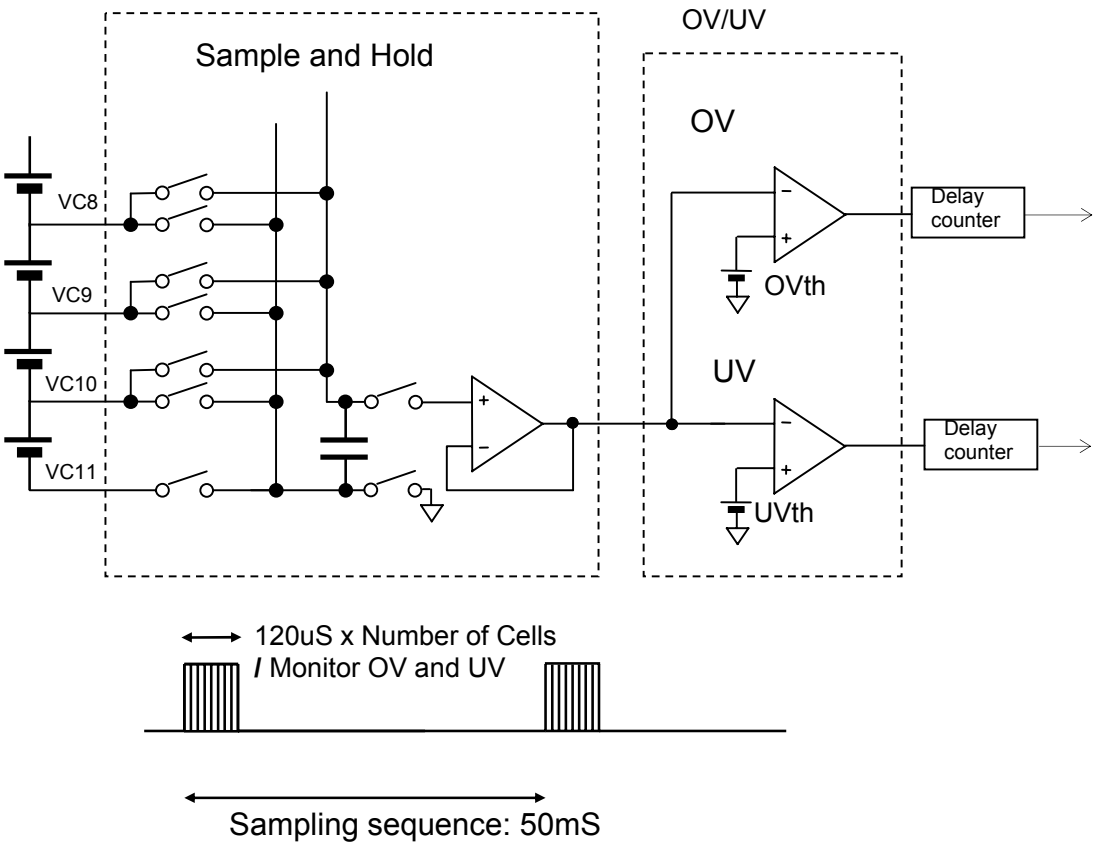


Figure 3: Cell Voltage Monitoring Circuit

7.3.2 Cell Over Voltage Detection and Recovery

Cell over voltage detection is the same as Host Control mode for the FET OFF sate but the recovery conditions are different. The CHG FET is turned OFF if any one of the cell voltages remains higher than V_{OV} for a period greater than t_{OV}. As a result, the cells are protected from an over charge condition. Also XLAERT changes from High to Low. Both V_{OV} and t_{OV} can be programmed in internal EEPROM.

7.3.2.1 Recovery in Host Control Mode

The recovery condition is as followings. (i) all cell voltage become lower than V_{OV}(ΔV_{OVH} is ignored). Additionally, the Host needs to send a sequence of firmware commands to the bq77PL900 to turn ON the CHG FET. The Firm ware command sequence to turn ON the CHG FET is as follows. (i) Host must toggle LTCLR from 0 to 1 and then back to 0. (ii)Then set the CHG control bit to 1.
To reset XLAERT high the host needs to read the Status register.
Figure 4 illustrates circuit schematic in over voltage protection mode in Host Control Mode. Figurer45 illustrates the timing chart of protection mode.

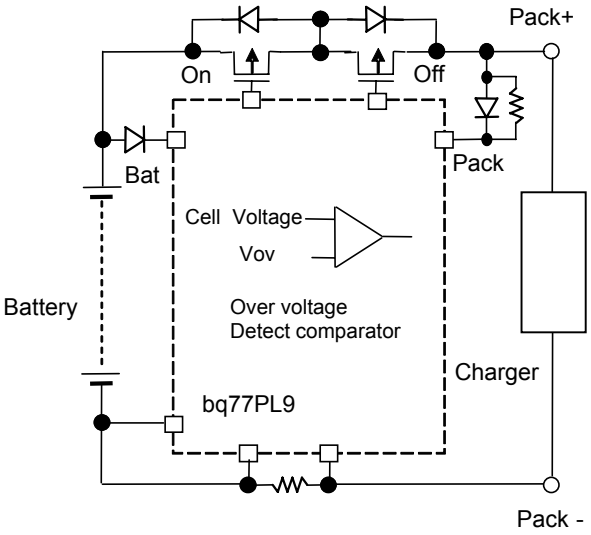


Figure 4: Over Voltage in Host Control Mode

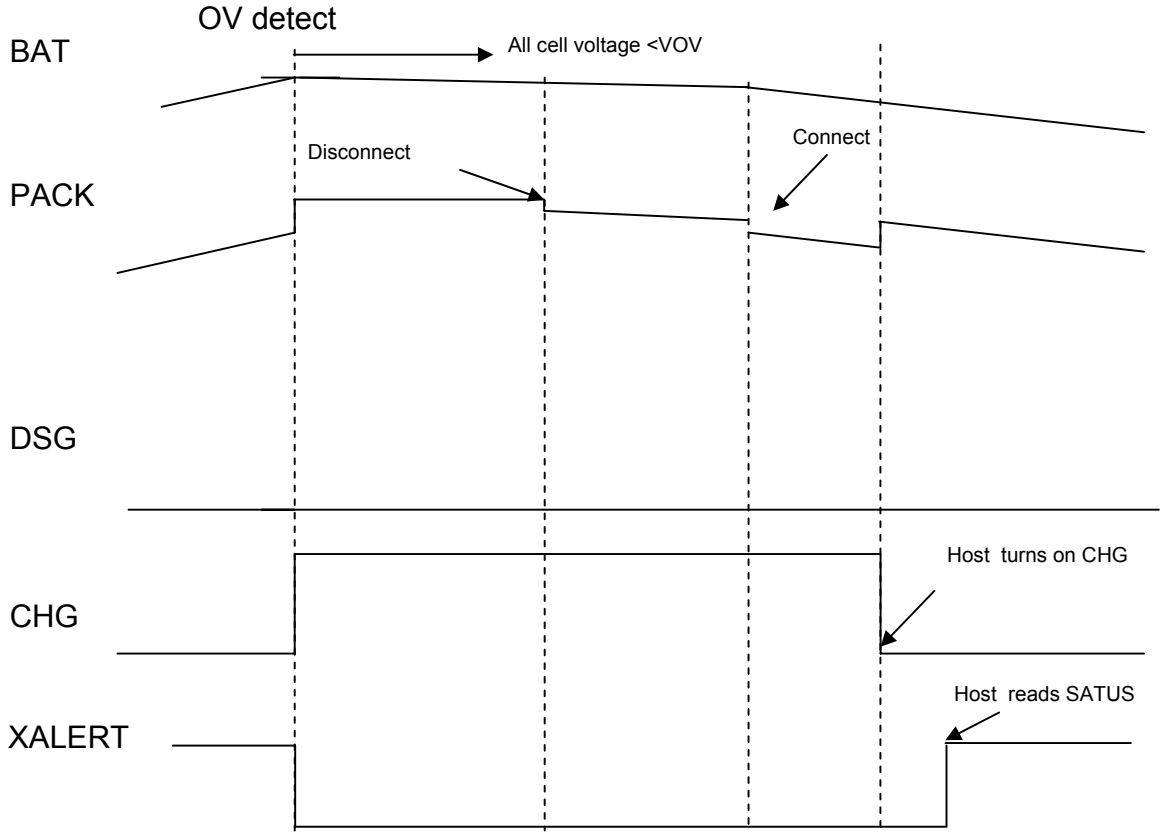


Figure 5: OV and OV recovery timing in Host Control Mode

7.3.2.2 Recovery in Stand Alone Mode

The recovery condition occurs when all cell voltage becomes lower than (V_{OV}-ΔV_{OVH}). Figure 6 illustrates circuit schematic in over voltage protection mode in Stand Alone Mode. Figure 7 illustrates the timing chart of protection mode.

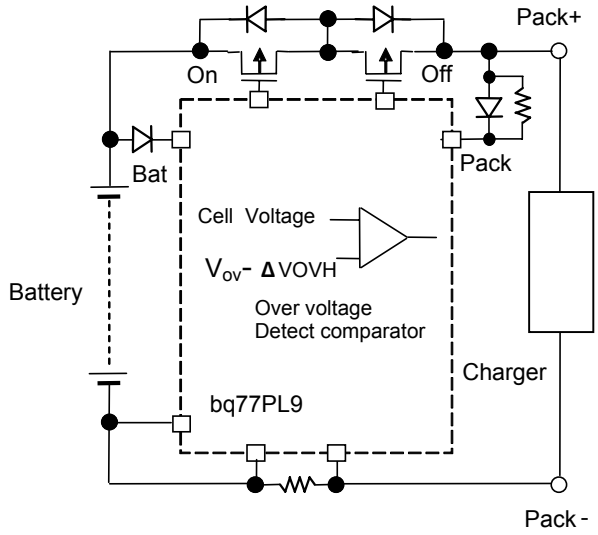


Figure6. Cell over voltage protection mode in Stand Alone Mode

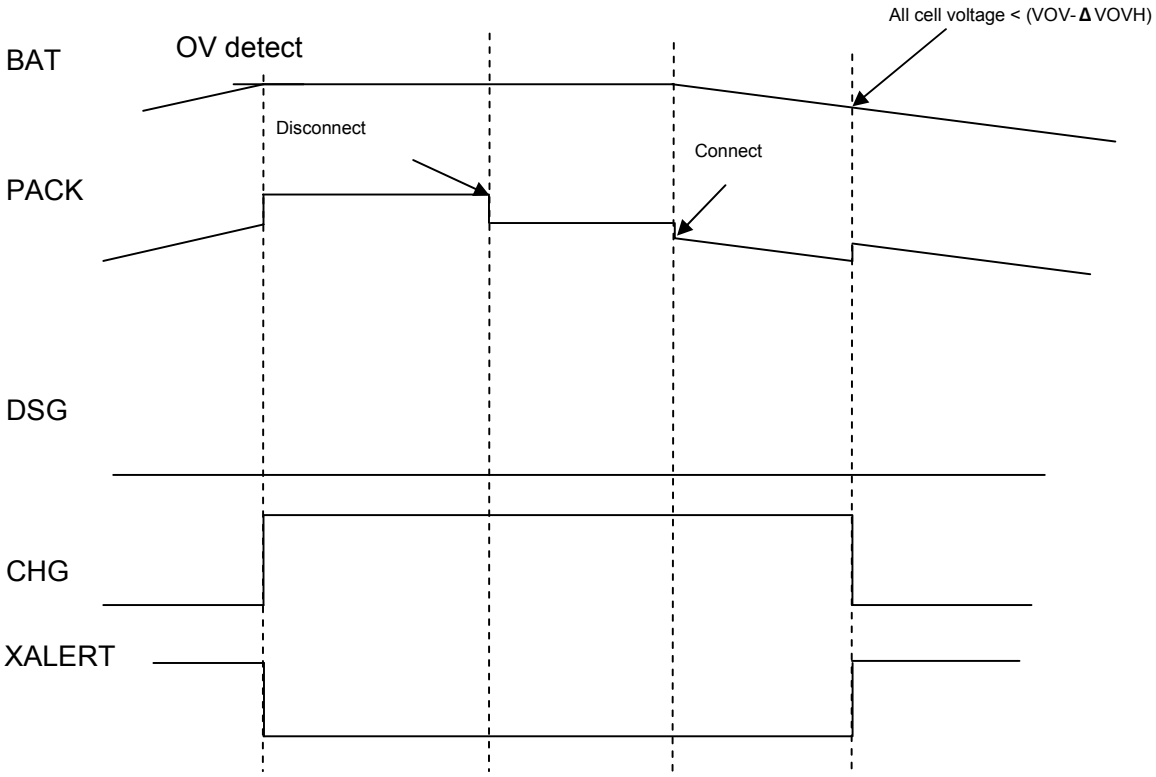


Figure 7: OV and OV recover timing in Stand Alone Mode

7.3.3 Cell Under Voltage Detection and Recovery

When any one of the cell voltages falls below V_{UV}, for a period of $t_{UV,}$ bq77PL900 enters under voltage mode.

At this time the DSG FET is turned OFF and XALERT driven low. Both V_{UV} and t_{UV} can be programmed in internal EEPROM.

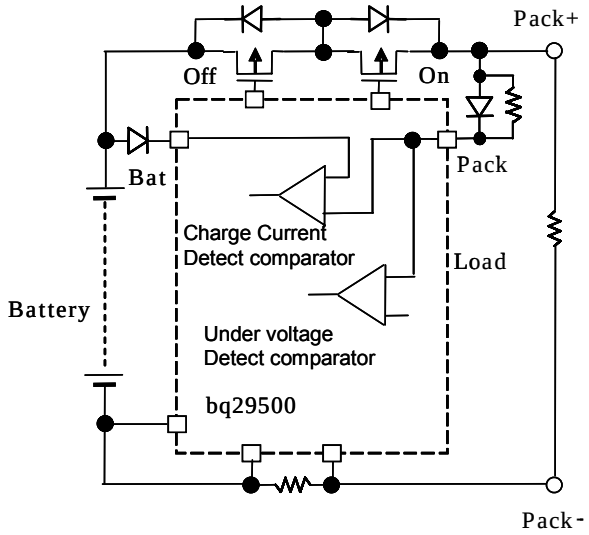


Figure 8: Cell under voltage protection mode at Host Control Mode and Stand Alone Mode(attaching a Charger)

7.3.3.1 In Host Control Mode

Cell under voltage protection recovery conditions are when (i) all cell voltage become higher than (V_{UV}+ΔV_{UVH}) or (ii) all cell voltages are higher than V_{UV} AND a charger is connected between PACK+ and PACK- noting that PACK+ voltage must be higher than BAT due to the diode forward voltage.
The bq77PL900 monitors the difference of voltage between PACK+ and BAT voltage. When a difference higher than 0.4V(typ), it is interpreted that a charger has been connected.
Figure 8 illustrates circuit schematic in under voltage protection mode.
In some applications, it is required to not turn OFF the DSG FET suddenly. In these cases, by setting ***UVLEVLE [UVFET_DIS]*** =1, only XALERT is driven low in response to entering an under voltage condition. The host can turn OFF the DSG FET to protect under voltage condition.
When the bq77PL900 recovery condition is satisfied, the host needs to send a sequence of firmware commands to the bq77PL900.The firmware command sequence to turn ON the DSG FET is as following. (i)Host must toggle LTCLR from 0 to 1 and back to 0, (ii)Then set the DSG ON bit to 1. Then Host can then read the status register to reset XALERT high.
Figurer9 and Figure10 illustrate the timing chart of protection mode.

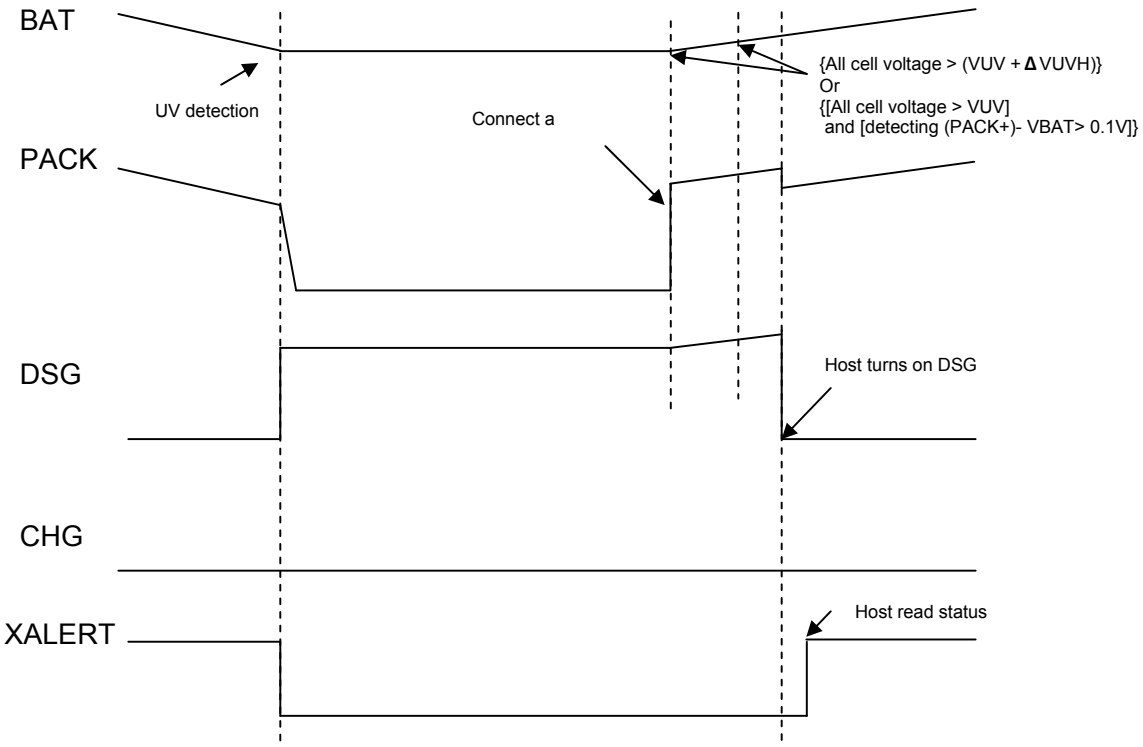


Figure 9: UV and UV recovery timing Host Control Mode (UVFET_DIS=0)

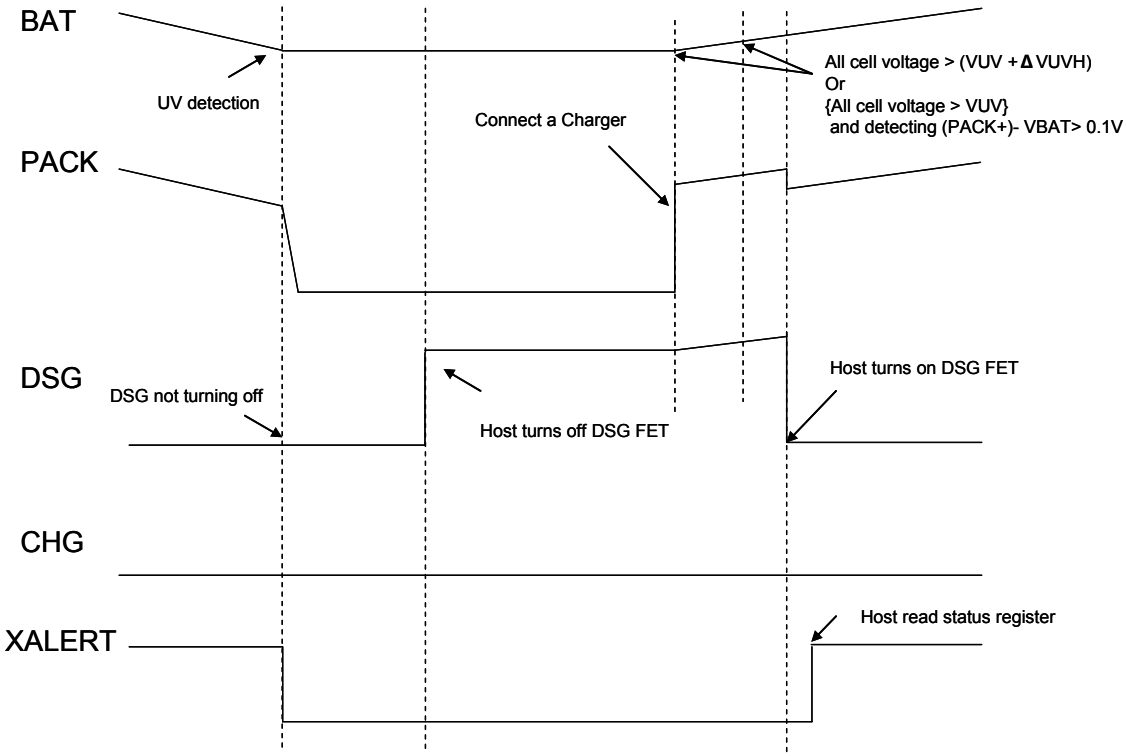


Figure 10: UV and UV recovery timing Host Control Mode (UVFET_DIS=1)

7.3.3.2 In Stand Alone Mode

On detection on entry to under voltage mode the bq77PL900 moves to the SHUTDOWN power mode. When a charger is attached, the bq77PL900 wakes up from shutdown mode. If cell voltages are lower than the under voltage condition, the DSG FET is turned OFF and XALERT driven low. During periods when a charger is attached the bq77PL900 never changes to shutdown mode.
When the under voltage recovery condition is satisfied, the DSG FET turns ON and XLAERT is reset high.

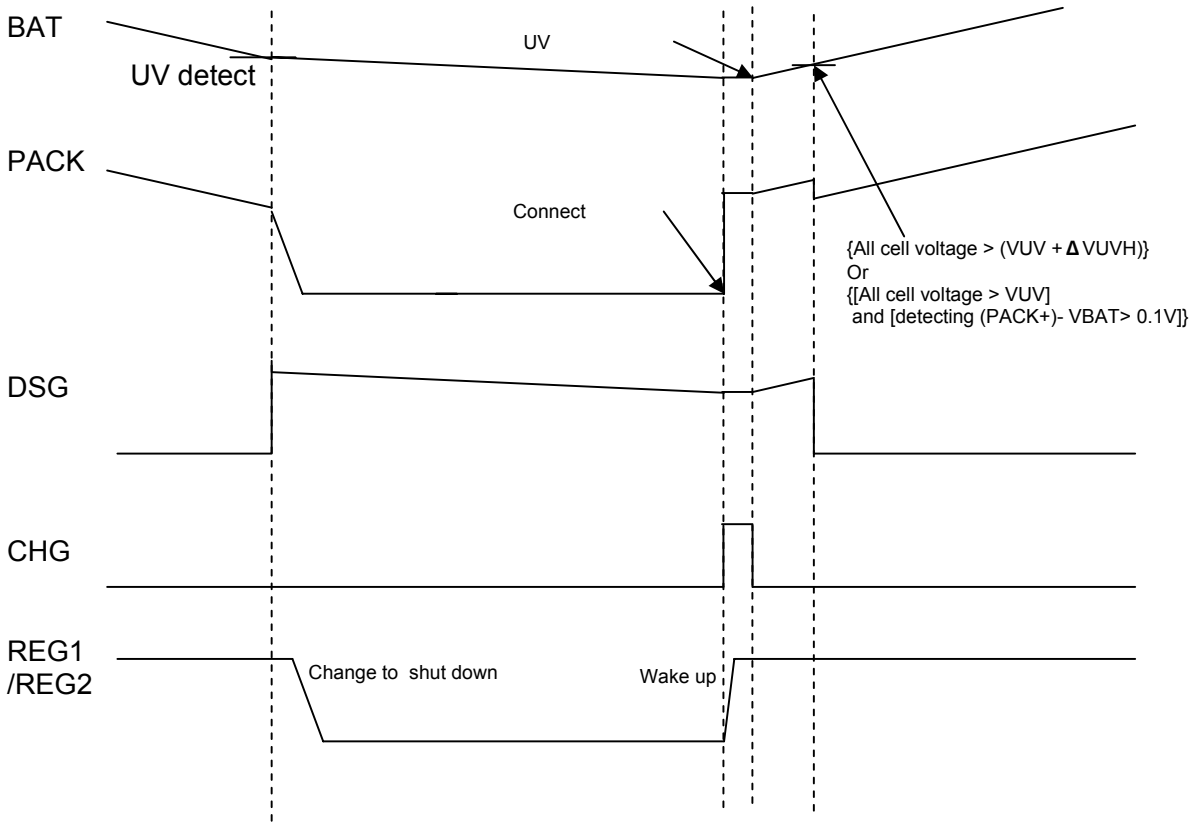


Figure 11: UV and UV recovery in Stand Alone Mode

7.3.4 Over Current in Discharge (OCD) Detection

The over current in discharge detection feature detects abnormal currents in the discharge direction via measuring the voltage across the sense resistor (V_{OCD}) and is used to protect the pass FETs, cells and any other inline components from abnormal discharge current conditions. The detection circuit also incorporates a blanking delay period (t_{OCD}) before turning OFF the pass FETs. Both V_{OCD} and t_{OCD} can be programmed in internal EEPROM.

7.3.5 Short Circuit in Discharge (SCD) Detection

The short circuit in discharge detections feature detects severe discharge current via measuring the voltage across the sense resistor (V_{SCD}) and is used to protect the pass FETs, cells and any other inline components from severe current conditions. The detection circuit also incorporates a blanking delay period (t_{SCD}) before turning OFF the pass FETs. Both V_{SCD} and t_{SCD} can be programmed in internal EEPROM.

7.3.6 Over Current in Discharge and Short Circuit in Discharge Recovery

In Host control mode, the Host needs to send a sequence of firmware commands to the bq77PL900. The firmware command sequence to turn ON the DSG and CHG FETs is as follows. (i)Host must toggle LTCLR from 0 to 1 and back to 0, (ii)Then set 1 the DSG and CHG control bits to 1.To reset XALERT high the STATUS register needs to be read

In Stand Alone Mode, the bq77PL900 has two methods to recover from Over Current and Short Circuit conditions by setting SOR bit of OCD_CFG.

SOR = 0, Recover comparator is active after 12.8sec. An internal comparator monitors the PACK+ voltage and when the PACK+ voltage reaches V_{RECSC}, the over current in discharge recovers. When the bq77PL900 detects attaching a charger, the DSG and CHG FETs turn ON and XLAERT reset High.

SOR = 1, after 12.8sec, the bq77PL900 automatically recovers from OC and SC. The DSG and CHG FETs turn ON and XLAERT is reset high. If the OC or SC condition is still present, OC and SC will be detected again and the recovery/detection cycle continues until the fault is removed.

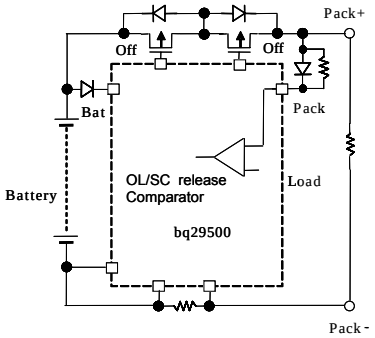


Figure 12: Over Current and Short Circuit protection modes

Table 3: Detection and Recovery Condition Summary (Stand Alone Mode)

	CELL OVER VOLTAGE	CELL UNDER VOLTAGE	OVER CURRENT IN DISCHARGE	SHORT CIRCUIT IN DISCHARGE
Detection condition	Any Cell Voltage > V_{OV}	Any Cell Voltage < V_{UV}	(V_{SRP} - V_{SRN}) > V_{OCD}	(V_{SRP} - V_{SRN}) > V_{SCD}
CHG FET	ON → OFF	ON	ON →OFF	ON →OFF
DSG FET	ON	ON →OFF	ON →OFF	ON →OFF
Recovery Condition 1	All cell voltage < (V_{OV} - ΔV_{OVH})	All cell voltage > (V_{UV} +ΔV_{UVH})	SOR=0: Attach a charger SOR=1:OC condition is released	SOR=0: Attach a charger SOR=1: SC condition is released
Recovery Condition 2		All cell voltage > V_{UV} AND PACK+ - V_{BAT} >0.1V		
CHG FET	OFF →ON	ON	OFF → ON	OFF → ON
DSG FET	ON	OFF →ON	OFF →ON	OFF →ON

Table 4: Detection and Recovery Condition Summary (Host Control Mode)

	CELL OVER VOLTAGE	CELL UNDER VOLTAGE	OVER CURRENT IN DISCHARGE	SHORT CIRCUIT IN DISCHARGE
Detection condition	Any Cell Voltage > V_{OV}	Any Cell Voltage < V_{UV}	(V_{SRP} - V_{SRN}) > V_{OCD}	(V_{SRP} - V_{SRN}) > V_{SCD}
CHG FET	ON → OFF	ON	ON →OFF	ON →OFF
DSG FET	ON	ON →OFF	ON →OFF	ON →OFF
Recovery Condition 1	All cell voltage < V_{OV} (ignore the hysteresis)	All cell voltage > (V_{UV} +ΔV_{UVH})	None	None
Recovery Condition 2		All cell voltage > V_{UV} AND VPACK- VBAT >0.1V		
CHG FET(1)	OFF →ON	ON	OFF → ON	OFF → ON
DSG FET(1)	On	OFF →ON	OFF →ON	OFF →ON

Notes 1: Host is required to set and clear LTCLR, then turn on the FETs.

7.4 Low Drop Out Regulators (REG1 and REG2)

The bq77PL900 has two Low Drop Out (LDO) regulators that provides power to both internal and external circuitry. The inputs for these regulators can be derived from the PACK or BAT terminals (see Initialization for further details). The output of REG1 is typically 5.0 V with the minimum output capacitance for stable operation with 2.2μF and is also internally current limited. During normal operation, the regulator limits output current to typically 25mA. The output of REG2 is typically 3.3 V with the minimum output capacitance for stable operation with 2.2μF and is also internally current limited.

Until the internal regulator circuit is correctly powered, the DSG and CHG FETs are driven OFF.

7.5 Initialization

From a shutdown situation the bq77PL900 requires a voltage greater that the Start Up Voltage ($V_{STARTUP}$) applied to the PACK pin to enable its integrated regulator and provide the regulators power source. Once the REG1 and REG2 outputs become stable, the power source of the regulator is switched to BAT.

After the regulators have started they will then continue to operate through the BAT input. If the BAT input is below the minimum operating range then the bq77PL900 will not operate until the supply to the PACK input is applied.

If the voltage at REG2 falls the internal circuit will turn off the CHG and DSG FETs and disable all controllable functions including the REG1, REG2 and TOUT outputs.

7.6 5 to 10 Series Cell Configuration

Unused cell inputs are required to be shorted to the upper most voltage connected terminal. For example, in a 5-cell configuration VC1 to VC5 are shorted to VC6. In a 9-cell configuration VC1 is shorted to VC2.

CNF0, CNF1, CNF2 pins should be connected to VLOG = logic 1 (through 10kΩ resistance) or GND = logic 0 (directly) according to the desired cell configuration as seen below.

Table 5: Cell Configuration

CNF2 PIN	CNF1 PIN	CNF0 PIN	CELL CONFIGURATION
0	0	0	10 cell
0	0	1	9 cell
0	1	0	8 cell
0	1	1	7 cell
1	0	0	6 cell
1	0	1	5 cell
All Other Combinations			10Cell

7.7 Delay Time Zero

The ZEDE pin enables the EEPROM programmed detection delay times when connected with GND (normal operation). The detection delay time is set to 0 when this pin is connected with VLOG. This is typically used in battery manufacturing test only.

7.8 Cell Voltage Measurement

The cell voltage is translated to allow a Host controller to measure individual series elements of the battery. The series element voltage is presented on the VOUT terminal. The cell voltage amplifier gain can be selected as one of the following two equations. VOUT voltage gain is selected by *STATE_CONTROL [VGAIN]*. VOUT is internally connected to ground when disabled.

$$V_{OUT}\,1 = 0.975 - \{ (\text{Cell Voltage}) \times 0.15 \} \quad \text{when (VGAIN = 0)}$$

or

$$V_{OUT}\,2 = 1.200 - \{ (\text{Cell Voltage}) \times 0.20 \} \quad \text{when (VGAIN = 1)}$$

The total pack voltage can also be monitored. The pack voltage output is enabled or disabled by *FUNCTION_CONTROL [PACK].*

$$V_{OUT}\,3 = (\text{Total pack voltage}) \times 0.02 \text{ when (PACK = 1)}$$

The total pack voltage can also be monitored. The bat voltage output is enabled or disabled by *FUNCTION_CONTROL [BAT].*

$$V_{OUT}\,4 = (\text{Total Battery voltage}) \times 0.02 \text{ when (BAT = 1)}$$

7.9 Cell Voltage Measurement Calibration

The bq77PL900 Cell Voltage monitor consists of a S/H (sample and hold) circuit and differential amplifier.

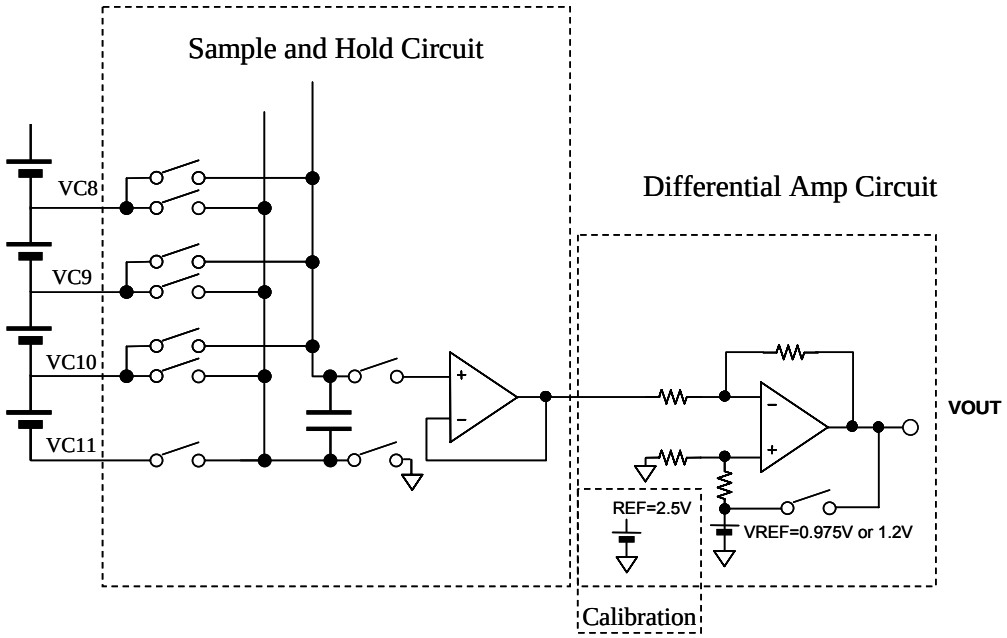


Figure 13: Cell Voltage Monitoring Circuit

To calibrate the VCELL output, it needs to measure a 2.5v signal, but 2.5V is beyond the ADC input range of most Analog to Digital converters used in these applications. The bq77PL900 is designed to measure the 2.5V through differential amplifier first which is where the calibration step starts from.

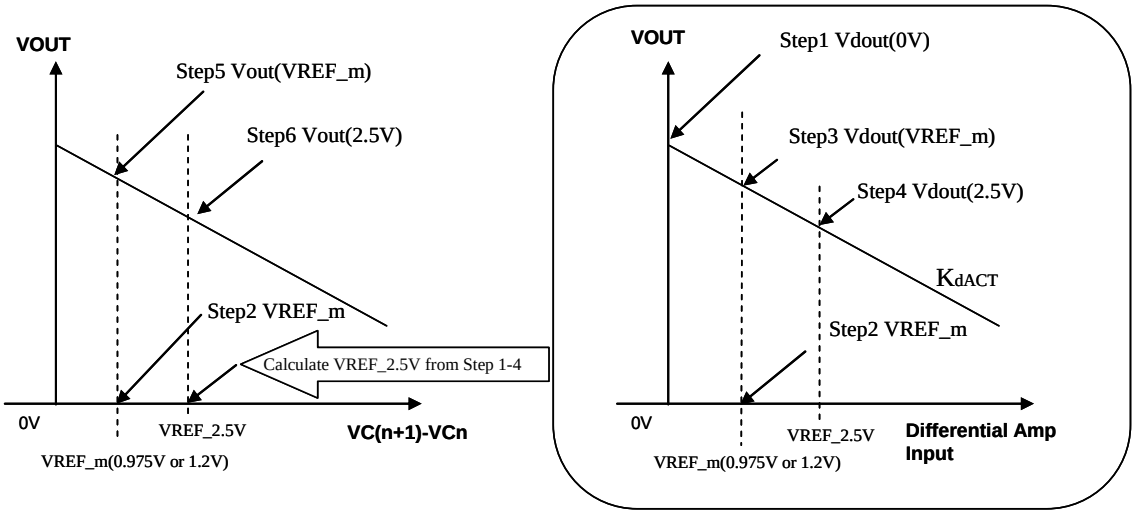


Figure 14: Calibration Method

7.9.1 Step 1

Set CAL2=0,CAL1=0, CAL0=1, CELL[4:1]=0, VAEN=1
Measure the output voltage of differential amp at 0V input(both input of differential amp are connected GND). The output voltage includes the offset and represented by

$Vd_{OUT}(0V)$ = measured output voltage of differential amplifier at 0V input
(This value includes an offset voltage(V_{OS})and a reference voltage)

7.9.2 Step 2

Set CAL2=0, CAL1=1, CAL0=1, VAEN=1
VREF is trimmed to 0.975V or 1.2V within +-2%. Then measure internal reference voltage VREF from VOUT directly

VREF_m = measured reference voltage(0.975V or 1.2V)

7.9.3 Step 3

Set CAL2=0, CAL1=1, CAL0=0, CELL[4:1]=0, VAEN=1
Measure scaled REF voltage through differential amp.

$Vd_{OUT}(VREF\_m)$ = The output voltage includes the scale factor error and offset
$=VREF+(1+K)* V_{OS} – K * VREF$
$= VREF\_m + (1 + Kd_{ACT}) * V_{OS} – Kd_{ACT} * VREF\_m$
Where $VREF\_m+ (1 + Kd_{ACT}) * V_{OS} =Vd_{OUT}(0V)$

$Kd_{ACT} =(Vd_{OUT}(0V) – Vd_{OUT}(VREF\_m)) / VREF\_m$
=(measured value @step1 – measured value@step3)/ measured value@step2

Calibrated differential voltage is calculated by:
$Vdout = VREF+(1+K)* V_{OS} – K * Vdin$
$= Vd_{OUT}(0V) – Kd_{ACT} * Vdin$
Where Vdin= input voltage of differential amp

7.9.4 Step 4

Set CAL2=1, CAL1=0, CAL0=0, CELL[4:1]=0, VAEN=1
Measure scaled REF(2.5V) though differential amp,
In case of bq-GG, it can not measure 2.5V direct, because of it's ADC input voltage is 1.0V.
So to measure the 2.5V internal reference voltage, using differential amp is a method to turn down the measurement value.

Vdout(2.5V) = measured differential amp output voltage at 2.5V input

Already, differential amp calibration was done by step1,2 and 3.
So VREF_2.5V is presented by
$VREF\_2.5V= \{ Vd_{OUT}(0V)- Vdout(2.5V)\}/ Kd_{ACT}$

7.9.5 Step 5

Set CAL2=1,CAL1=0, CAL0=1, CELL2=0, CELL1=0, VAEN=1

Vout(0.975V or 1.2V) = Measure scaled REF(0.975V or 1.2V) output voltage S/H and differential amplifier.

7.9.6 Step 6

Set CAL2=1, CAL1=1, CAL0=0, CELL[4:1]=0, VAEN=1

Vout(2.5V) = Measure scaled REF(2.5V) output voltage S/H and differential amp.

Scale factor

K_{ACT} =(V_{OUT}(2.5V) – V_{OUT}(0.975Vor1.2V) /(VREF_2.5V-VREF_m)

Vout(0V)= V_{OUT}(2.5V) – K_{ACT} *VREF_2.5V

Or

Vout(0V)= V_{OUT}(0.975Vor1.2V) – K_{ACT} *VREF_m

Cell voltage is calculated by below

VCn – VC(n+1) = { Vout(0V) – V_{OUT}} / K_{ACT}

7.10 Current Monitor

Discharge and charge current is translated to allow a Host controller to accurately measure current which can then be used for additional safety features or calculating the remaining capacity of the battery. The sense resistor voltage is converted per the equation below. The typical offset voltage is V_{CELL_OFF}(1.20V typical) although can be presented on the IOUT pin for measurement if required.

The output voltage increases when current is positive (discharging) and decreases when current is negative (charging).

$$V_{CURR} = 1.20 + (I_{PACK} \times R_{SENSE}) \times (IGAIN)$$

Where

State_Contorl [IGAIN] = 1 then IGAIN = 50

State_Contorl [IGAIN] = 0 then IGAIN = 10

The current monitor amplifier can present the offset voltage as shown in table 6. The IOUT pin is enabled or disabled by *FUNCTION_CONTROL [IACAL, IAEN]* and has a default state of OFF. IOUT is internally connected to ground when disabled

Table 6: IACAL and IAEN Configuration

IACAL	IAEN	CONDITION
0	1	NORMAL
1	1	OFFSET
X	0	OFF

7.11 Cell Balance Control

The integrated cell balance FETs allow a bypass path to be enabled for any one series element. The purpose of this bypass path is to reduce the current into any one cell during charging to bring the series elements to the same voltage. Series resistors placed between the input pins and the positive series element nodes limits the bypass current value. Series input resistors between 500Ω and 1kΩ are recommended for effective cell balancing.

In Host Control Mode, individual series element selection is made via *CELL_BALANCE [CBAL1, CBAL2, CBAL3, CBAL4, CBAL5, CBAL6, CBAL7, CBAL8] and FUNCTION_CONTROL [CBAL9, CBAL10]*.

In Stand Alone mode, cell balancing works as shown in the figure below. When a certain cell (Cell A) voltage reaches cell over voltage, the battery charging stops and then cell balance starts working at ta. The Cell A voltage decreases by the bypass current until the voltage reaches (V_{OV} -ΔV_{OVH}). Cell B voltage doesn't change during the period because cell balancing works only for the cell that reached V_{OV}. At tb, battery charging starts again. Cell A and Cell B have been charged in this period until Cell A voltage reaches V_{OV} again. The voltage difference between Cell A and Cell B becomes smaller when the bq77PL900 repeats the above cycle. The bq77PL900 stops cell balance when cell over voltage protection has released.

bq77PL900 is designed to prevent cell balancing on adjacent cells or on every other cells. For example, if cell over voltage happened to Cell 8 and Cell 7 (Cell7 is next to Cell8 and higher) and Cell3(Cell3 is not next to Cell8 and Cell7), cell balance starts for Cell8 and Cell3 at first. When Cell8 voltage is back to normal voltage, cell balance starts for Cell7.

While the bq77PL900 monitors the over voltage and under voltage, Cell balance automatically will be turn off. This configuration is supported for both modes (Host control and Stand Alone mode).

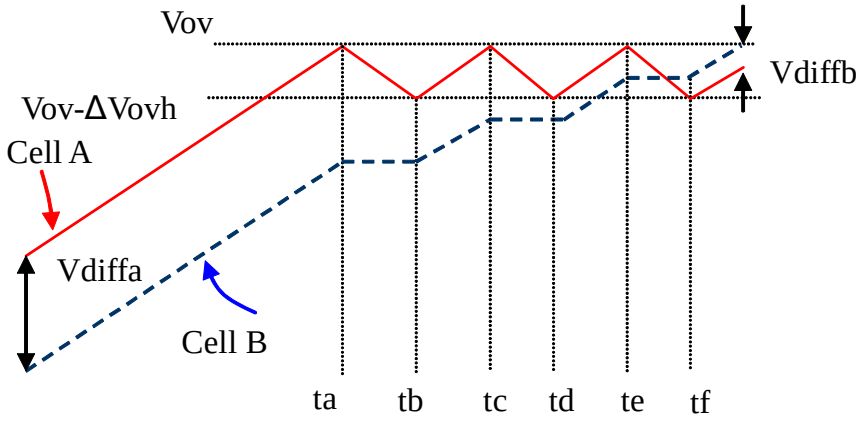


Figure 15: Cell Balancing timing chart (Automatic)

7.12 Thermistor Drive Circuit (TOUT), Thermistor Input (TIN)

The TOUT pin is powered by REG2 and can be enabled via *FUNCTION_CONTROL [TOUT]* to drive an external thermistor and is default OFF. A 10kΩ 25ºC NTC (eg: Semitec 103AT) thermistor is typical. The maximum output impedance is 100Ω.

The bq77PL900 monitors the battery temperature as shown below. A voltage divided by the NTC thermistor and reference resistor is connected to TIN. The bq77PL900 compares the TIN voltage with the internal reference voltage (0.975V) and when $V_{TIN} < V_{REF}$ the bq77PL900 turns OFF the CHG and DSG FETs and sets *STATUS [OVTEMP]*.

In Host Control Mode, the host should enable and disable the TOUT.

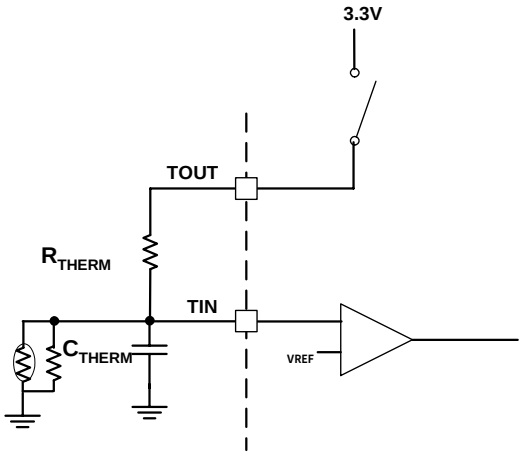


Figure 16: Temperature Monitoring Circuit

7.13 General Purpose Open Drain Drive (GPOD)

The GPOD output is enabled or disabled by *OUTPUT_CONTROL [GPOD]* and has a default state of OFF.

In Stand Alone Mode, this pin is used for driving the 0V/Pre-charge FET for zero voltage battery charging by OCD_CFG *[ZVC]=1*

7.14 Alerting the Host (XALERT)

In both modes the XALERT pin is available and is driven low when faults are detected. The method to clear the XALERT pin is different between Stand Alone Mode and Host Control Mode. In Stand Alone Mode, XLAERT is cleared when all of faults are cleared. In Host Control Mode, the host has to toggle (from “0”, set to “1” then reset to “0”) *OUTPUT_CONTROL [LTCLR]* and then read the *STATUS* register.

7.15 Alerting the Host (LTCLR)

In Host Control Mode, when a protection fault occurs, the state is latched. The fault flag is un latched by toggling (from “0”, set to “1” then reset to “0”) *OUTPUT_CONTROL [LTCLR]*. The OCD, SCD, OV and UV bits are unlatched by this function. Now the FETs can be controlled by programming the *OUTPUT_CONTROL* register and the XALERT output can be cleared by reading the *STATUS* register. During detecting an over voltage or under voltage faults, LTCTR changes are ignored. After a period of 1ms, it needs to send a LTCLR command.

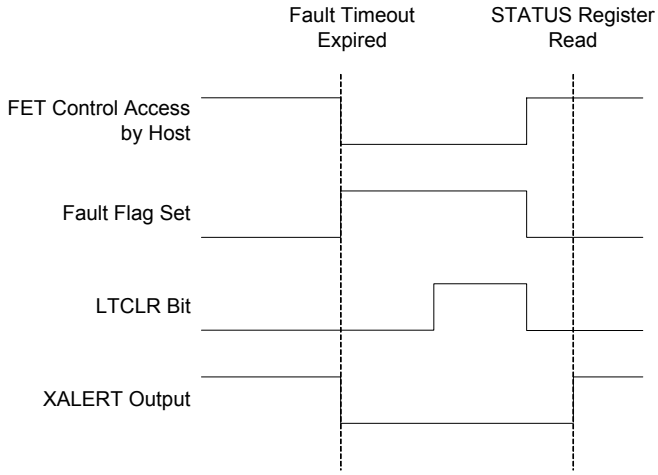


Figure 17: LTCLR and XLAERT Clear Timing (Host Control Mode)

7.16 POR

The XRST open drain output pin will be triggered on activation of the VREG1 or VREG2 output. This holds the Host controller in reset for t_{RST} allowing the V_{VREG1} or V_{VREG2} to stabilize before the host controller is released from reset.

The XRST output and monitoring voltage is supplied by the source of VLOG. When VLOG is connected to VREG1, the XRST output level is V_{VREG1} and monitors activation of the VREG1. When VLOG is connected to VREG2, the XRST output level is V_{VREG2} and monitors activation of the VREG2.

When V_{VREG1} or V_{VREG2} voltage is below the output specifications, XRST will be active low(0.8x VLOG).

When V_{BAT} is below 7.0V, VREG1 and VREG2 will stop, then XRST will go low. If a Host has a problem with a sudden Reset signal, it is recommended monitoring the Battery voltage to avoid it, eg: burnout detection.

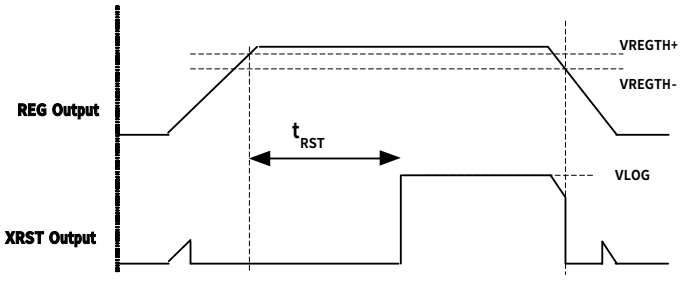


Figure 18: XRST Timing Chart – Power Up and Power down

7.17 EEPROM Write Sequence

The bq77PL900 has integrated configuration EEPROM for OV, UV, OCD and SCD thresholds and delays. The appropriate configuration data is programmed to the configuration registers and then 0xe2 is sent to the EEPROM register to enable the programming supply voltage. By driving the EEPROM pin (set high and then low), the data is written to the EEPROM.

When Supplying BAT, care should be taken not to exceed VCn – VC(n+1), (n=1 to 10) >5.0V. If BAT and VC1 is connected on board, we recommend that all of cell balance FETs be ON where each input voltage is divided with internal cell balance ON resistance.

The recommended voltage at BAT or PACK for EEPROM writing is 20V. When Supplying VBAT, care is needed to ensure VBAT does not exceed the “VCn – VC(n+1), (n=1 to 10) absolute max voltage”. If BAT and VC1 are connected on board, we recommend supplying 7.5V to activate the bq77PL900 and turns ON all of cell balance FETs.

Then increase the power supply up to 20V. By this method, each input Voltage is divided with internal cell balance ON resistance.

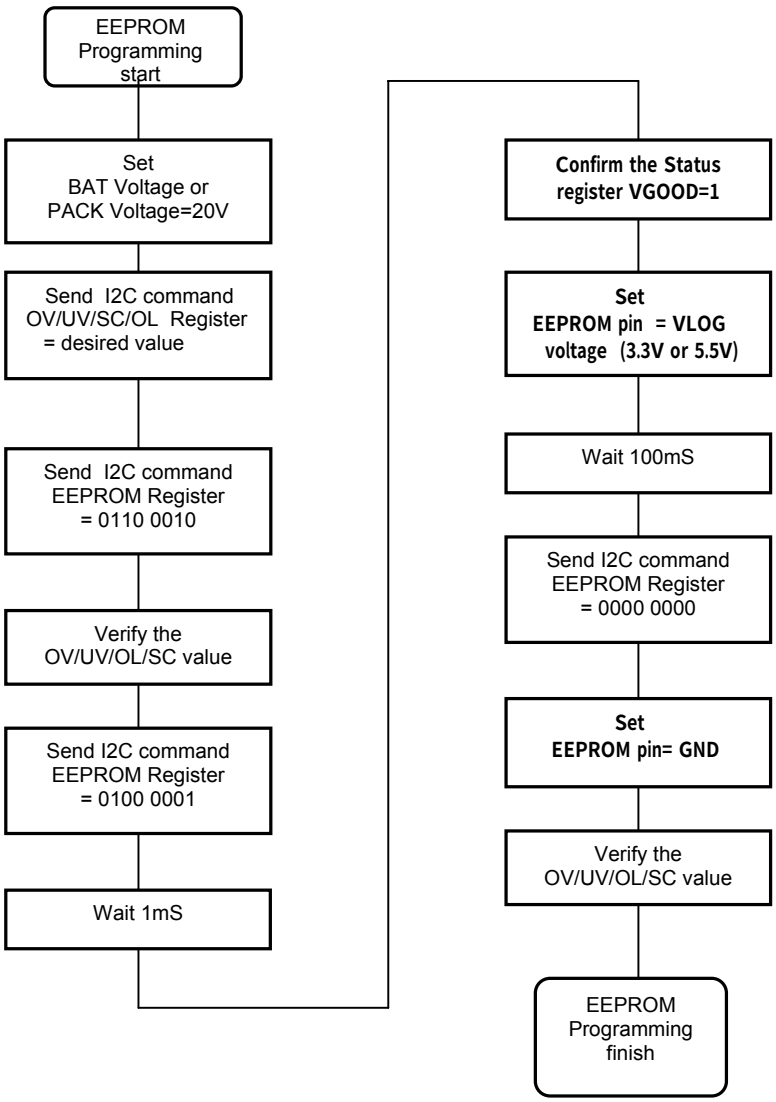


Figure 19: EEPROM Data Writing Flow Chart

7.18 Power Modes

The bq77PL900 has two power modes, Normal and shutdown. The following table outlines the operational functions during two power modes.

Table 7: Power Modes

POWER MODE	TO ENTER NORMAL MODE	MODE DESCRIPTION
Normal		The battery is in normal operation with protection, power management and battery monitoring functions available and operating. The supply current of this mode varies as the Host can enable and disable various features.
Shutdown	Add supply at the V_{PACK} < V_{WAKE}	When under voltage is detected in Stand Alone Mode, or Shutdown command at Host Control Mode , The bq77PL900 goes shut down, All outputs and interfaces are OFF and memory is not valid.

7.18.1 Shutdown Mode

In Host Control Mode the bq77PL900 enters shutdown mode when it receives the shutdown command, *STATE_CONTROL [SHDN]* set. First the DSG FET will be turned OFF and then after the Pack voltage goes to 0V, the bq77PL900 enters to shut down mode which stops all functions of bq77PL900.

In Stand Alone Mode the bq77PL900 enters shutdown when the battery voltage falls, and UV is detected. It turns the DSG FET OFF and after the Pack voltage goes to 0V, the bq77PL900 enters to shut down mode which stops all functions.

7.18.2 Exit From Shutdown

If a voltage greater than $V_{STARTUP}$ is applied to the PACK pin then the bq77PL900 will exit from shutdown and enter to normal mode.

7.19 Parity check

The bq77PL900 uses EEPROM for storage of protection thresholds and delay times etc… The EEPROM is also used to store internal trimming data. For safety reasons, the bq77PL900 is uses a column parity error checking scheme. If the column parity bit is changed from the written then *OUT_CONTROL [PFALT]* is set to 1 and XALERT driven low. In Stand alone mode, both DSG and CHG outputs are driven high turning OFF the DSG and CHG FETs. And GPOD output is turned off, too.
In Host Control Mode, only *OUT_CONTROL [PFALT]* and XALERT output are changed, so allowing the micro processor host to control bq77PL900's operation.

7.20 Communications

The I²C like communications provides read and write access to the bq77PL900 data area. The data is clocked via separate data (SDATA) and clock (SCLK) pins. The bq77PL900 acts as a slave device and does not generate clock pulses. Communication to the bq77PL900 can be provided from GPIO pins of a Host controller. The slave address for the bq29550 is 7 bits and the value is 0010 000

	(MSB)		I2C Address +R/W bit				(LSB)
	(MSB)		I2C Address			(LSB)	
Write	0	0	1	0	0	0	0
Read							1

The bq77PL900 does NOT have the following functions compatible with the I²C specification.

- The bq77PL900 is always regarded as a slave
- The bq77PL900 does not support the General Code of the I²C specification and therefore will not return an ACK but may return a NACK.
- The bq77PL900 does not support the Address Auto Increment, which allows continuous reading and writing.
- The bq77PL900 will allow data to written or read from the same location without re-sending the location address.

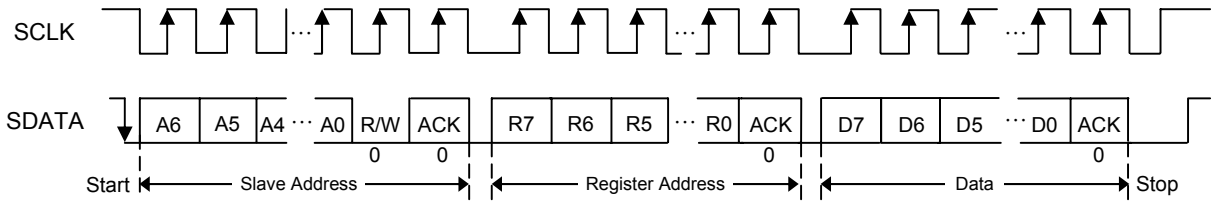


Figure 20: I²C-Bus Write to bq77PL900

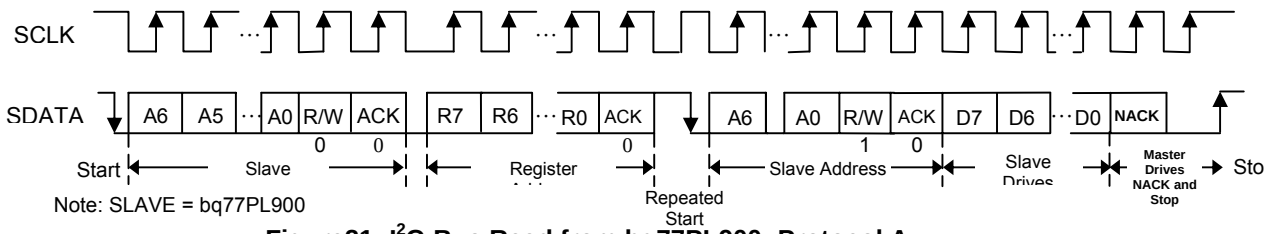


Figure21: I²C-Bus Read from bq77PL900: Protocol A

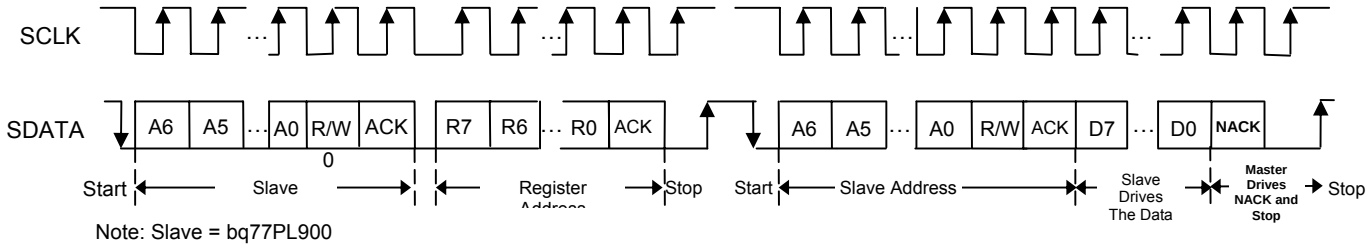


Figure22: I²C-Bus Read from bq77PL900: Protocol B

7.21 Register Set

The bq77PL900 has 12 addressable registers. These registers provide status, control, and configuration information for the battery protection system.

Table 8: Register Descriptions

NAME	Test Pin	ADDR	MEMORY TYPE	R/W	DESCRIPTION
STATUS	X	0x00	Read	R	Status register
OUTPUT_CONTROL	X	0x01	RAM	R/W	Output pin control from system Host Control Mode and external pin status
STATE_CONTROL	X	0x02	RAM	R/W	State control from system Host and external pin status.
FUNCTION_CONTROL	X	0x03	RAM	R/W	Function control from system Host and external pin status.
CELL BALANCE	X	0x04	RAM	R/W	Battery cell select for balance bypass
CELL _SEL	X	0x05	RAM	R/W	Battery cell select for balance bypass and for analog output voltage
OV CFG	X	0x06	EEPROM	R/W*	Over voltage level and delay time register
UV LEVEL	X	0x07	EEPROM	R/W*	Under voltage level register
OCV & UV DELAY	X	0x08	EEPROM	R/W*	Over load voltage level and Under voltage delay time register
OCDELAY	X	0x09	EEPROM	R/W*	Over load delay time register
SCD CFG	X	0x0a	EEPROM	R/W*	Short Circuit in discharge current level and delay time register
EEPROM	X	0x0b	RAM	R/W	EEPROM read and write enable register

Table 9: Register Map

NAME	I2C ADDR	B7	B6	B5	B4	B3	B2	B1	B0
STATUS	0x00	CHG	DSG	VGOOD	OVTEMP	UV	OV	OCD	SCD
OUTPUT_CONTROL	0x01	FS	PFALT	0	0	GPOD	CHG	DSG	LTCLR
STATE_CONTROL	0x02	IGAIN	VGAIN	0	0	0	0	HOST	SHDN
FUNCTION_CONTROL (Cell(9,10)Balance Register)	0x03	CBAL10	CBAL9	TOUT	BAT	PACK	IACAL	IAEN	VAEN
CELL BALANCE	0x04	CBAL8	CBAL7	CBAL6	CBAL5	CBAL4	CBAL3	CBAL2	CBAL1
CELL _SEL	0x05	0	CAL2	CAL1	CAL0	CELL4	CELL3	CELL2	CELL1
OV_CFG	0x06	OVD2	OVD1	OVD0	OVH1	OVH0	OV2	OV1	OV0
UV_CFG	0x07	0	UVFET_DIS	UVH1	UVH0	UV3	UV2	UV1	UV0
OCV&UV_DELAY	0x08	UVD3	UVD2	UVD1	UVD0	OCD3	OCD2	OCD1	OCD0
OCD_CFG	0x09	CBEN	ZVC	SOR	OCDD4	OCDD3	OCDD2	OCDD1	OCDD0
SCD_CFG	0x0a	SCDD3	SCDD2	SCDD1	SCDD0	SCD3	SCD2	SCD1	SCD0

EEPROM	Read –writing data(0x62)	0x0b	0	1	1	0	0	0	1	0
	Writing(0x41)		0	1	0	0	0	0	0	1
	Reading (except above)		0	0	0	0	0	0	0	0

7.21.1 Registore control

0x01 to 0x05 should be controlled during Host Control Mode.

7.21.2 STATUS: Status Regsiter

STATUS REGISTER (0x00)							
7	6	5	4	3	2	1	0
CHG	DSG	VGOOD	OVTEMP	UV	OV	OCD	SCD

The STATUS register provides information about the current state of the bq77PL900.

STATUS b0 (SCD): This bit indicates a short circuit in discharge condition.
0 = Current is below the short circuit in discharge threshold (default)
1 = Current is greater than or equal to the short circuit in discharge threshold

STATUS b1 (OCD): This bit indicates an over load condition.
0 = Current is less than or equal to the over load threshold (default).
1 = Current is greater than over load threshold.

STATUS b2 (OV): This bit indicates an over voltage condition.
0 = Voltage is less than or equal to the over voltage threshold (default).
1 = Voltage is greater than over voltage threshold.

STATUS b3 (UV): This bit indicates a under voltage condition.
0 = Voltage is greater than or equal to the under voltage threshold (default).
1 = Voltage is less than under voltage threshold.

STATUS b4 (OVTEMP): This bit indicates an over temperature condition.
0 = Temperature is lower than or equal to the over temperature threshold (default).
1 = Temperature is higher than over the temperature threshold

STATUS b5 (VGOOD): This bit indicates a valid EEPROM power supply voltage condition.
0 = Voltage is smaller than prescribed EEPROM power supply voltage. (default).
1 = Voltage is greater than or equal to the prescribed EEPROM power supply voltage

STATUS b6 (DSG): This bit reports the external discharge FET state
0 = Discharge FET is off
1 = Discharge FET is on
STATUS b7 (CHG): This bit reports the external charge FET state
0 = Charge FET is off
1 = Charge FET is on

OUTPUT_CONTROL: Output Control Regsiter

OUTPUT _CONTROL REGISTER (0x01)							
7	6	5	4	3	2	1	0
FS	PFALT	0	0	GPOD	CHG	DSG	LTCLR

The OUPTUT_CONTROL register controls some of the outputs of the bq77PL900 and can show the state of the external pin corresponding to the control.

OUTPUT_ CONTROL b0 (LTCLR): When a fault is latched this bit will release the fault latch when toggled.0 = (default)

0->1 ->0 clears the fault latches allowing STATUS to be cleared on its next read

OUTPUT_ CONTROL b1 (DSG): This bit controls the external discharge FET.

0 = Discharge FET is OFF in Host Control Mode .

1 = Discharge FET is ON in Host Control Mode .

OUTPUT_ CONTROL b2 (CHG): This bit controls the external charge FET.

0 = Charge FET is OFF in Host Control Mode .

1 = Charge FET is ON in Host Control Mode .

OUTPUT_CONTROL b3 (GPOD): This bit enables or disables the GPOD output

0 = GPOD output is high impedance (default)

1 = GPOD output is active (GND)

OUTPUT_CONTROL b6 (PFALT): This bit indicates a parity error of EEPROMs.This bit is read only.

0 = No parity error (default)

1 = A parity error happen

OUTPUT_CONTROL b7 (FS): This bit select Under voltage detection sampling time

0 = Sampling time is 50ms/cell (typ) (default).

1 = Sampling time is 100us/cell (typ)

OUTPUT_CONTROL b6-b4: These bits are not used and should be set to 0.

7.21.3 STATE_CONTROL: State Control Register

STATE_CONTROL REGISTER (0x02)							
7	6	5	4	3	2	1	0
IGAIN	VGAIN	0	0	0	0	HOST	SHDN

The STATE_CONTROL register controls the states of the bq77PL900.

STATE_CONTROL b0 (SHDN): This bit enables or disables the shut down mode in Host mode

0 = Disable shut down mode (default)

1 = Enable shut down mode(if PACK voltage =0V)

STATE_CONTROL b1 (HOST): This bit select mode Stand Alone Mode or Host control.

0 = Stand Alone Mode (default)

1 = Host Control Mode

STATE_CONTROL b6 (VGAIN): This bit controls the cell amplifier scale.

0 = SCALE 0.15 (default)

1 = SCALE 0.20

STATE_CONTROL b7 (IGAIN): This bit controls the current monitor amplifier gain.

0 = GAIN 10 (default)

1 = GAIN 50

STATE_CONTROL b5-b2: These bits are not used and should be set to 0.

7.21.4 FUNCTION_CONTROL: Function Control Register, (Cell (9, 10) Balance Register)

FUNCTION CONTROL REGISTER (0x03)							
7	6	5	4	3	2	1	0
CBAL10	CBAL9	TOUT	BAT	PACK	IACAL	IAEN	VAEN

The FUNCTION_CONTROL register controls some features of the bq77PL900.

FUNCTION_ CONTROL b0 (VAEN): This bit controls the internal cell voltage amplifier

0 = Disable cell voltage amplifier (default).

1 = Enable cell voltage amplifier

FUNCTION _CONTROL b1 (IAEN): This bit controls the internal current monitor amplifier

0 = Disable current monitor amplifier (default).

1 = Enable curent monitor amplifier

FUNCTION_CONTROL b2 (IACAL): This bit controls the internal current monitor amplifier offset voltage output

0 = Disable offset voltage output (default)

1 = Enable offset voltage output

FUNCTION_CONTROL b3 (PACK): When VAEN=1, PACK input is divided by 50 and presented on VCELL

0 = Disable pack total voltage output (default)

1 = Enable pack total voltage output

FUNCTION_ CONTROL b4 (BAT): When VAEN=1, BAT input is divided by 50 and presented on VCELL.

0 = Disable pack total voltage output (default)

1 = Enable pack total voltage output

This bit priority is higher than PACK(b3).

FUNCTION _CONTROL b5 (TOUT): This bit controls the power to the thermistor.
0 = Thermistor power is off in Host Control Mode (default)
1 = Thermistor power is on in Host Control Mode .

FUNCTION _CONTROL b7-b6 (CELL10-9): This bit enables or disables the cell 9 and cell 10 balance charge bypass path
0 = disable bottom series cell 9 or cell 10 balance charge bypass path (default).
1 = enable bottom series cell 9 or cell 10 balance charge bypass path

7.21.5 CELL_BALANCE : Cell (1 to 8) Balance Register

CELL_BALANCE REGISTER (0x04)							
7	6	5	4	3	2	1	0
CBAL8	CBAL7	CBAL6	CELL5	CBAL4	CBAL3	CBAL2	CBAL1

The CELL_BALANCE register controls cell balancing of the bq77PL900.

CELL_BALANCE b7(CBAL8) : this bit enables VC3-VC4 cell balance charge bypass path
CELL_BALANCE b6(CBAL7) : this bit enables VC4-VC5 cell balance charge bypass path
CELL_BALANCE b5(CBAL6) : this bit enables VC5-VC6 cell balance charge bypass path
CELL_BALANCE b4(CBAL5) : this bit enables VC6-VC7 cell balance charge bypass path
CELL_BALANCE b3(CBAL4) : this bit enables VC7-VC8 cell balance charge bypass path
CELL_BALANCE b2(CBAL3) : this bit enables VC8-VC9 cell balance charge bypass path
CELL_BALANCE b1(CBAL2) : this bit enables VC9-VC10 cell balance charge bypass path
CELL_BALANCE b0(CBAL1) : this bit enables VC10-VC11 cell balance charge bypass path
0 = disable series cell balance charge bypass path (default).
1 = enable series cell balance charge bypass path

7.21.6 CELL_SEL : Cell Translation Selection and Cell Translation Status Register

CELL_SEL REGISTER (0x05)							
7	6	5	4	3	2	1	0
0	CAL2	CAL1	CAL0	CELL4	CELL3	CELL2	CELL1

The CELL_SEL register determines cell selection for voltage measurement and translation. The resister also determines operation mode of the cell voltage monitoring.

CELL_SEL b3-b0 (CELL4-1): These four bits select the series cell for voltage measurement translation.

CELL4	CELL3	CELL2	CELL1	SELECTED CELL
0	0	0	0	VC11-VC10, Bottom series element (Default)
0	0	0	1	VC10-VC9, Second lowest series element
0	0	1	0	VC9-VC8, Third lowest series element

0	0	1	1	VC8-VC7, 4th lowest series element
0	1	0	0	VC7-VC6, 5th lowest series element
0	1	0	1	VC6-VC5, 6th highest series element
0	1	1	0	VC5-VC4, 7th highest series element
0	1	1	1	VC4-VC3, 8th highest series element
1	0	0	0	VC3-VC2, 9th highest series element
1	0	0	1	VC2-VC1, Top series element
Other				VC11-VC10, Bottom series element

CELL_SEL b6-b4 (CAL2-0): These two bits determine the mode of the voltage monitor block.

CAL2	CAL1	CAL0	SELECTED MODE
0	0	0	Cell translation for selected cell (default)
0	0	1	Monitor offset of differential amp (both input of differential amp are connected GND)
0	1	0	Monitor the scaled V_{REF}(*1) value
0	1	1	Monitor the V_{REF}(*1)directly
1	0	0	Monitor the scaled 2.5V value to measured the 2.5V
1	0	1	Monitor the VC10= V_{REF}(*1), VC11=0V
1	1	0	Monitor the VC10=2.5V, VC11=0V
1	1	1	Monitor the VC9=2.5V, VC10=1.2V

(*1) When VGAIN=0, VREF = 0.975V, When VGAIN=1, VREF = 1.2V

CELL_SEL b7: These bits are not used and should be set to 0.

7.21.7 OV_CFG : Over Voltage Delay Time, Hysteresis and Threshold Configuration Register

OV CFG REGISTER (0x06)							
7	6	5	4	3	2	1	0
OVD2	OVD1	OVD0	OVH1	OVH0	OV2	OV1	OV0

The OV register determines cell over voltage threshold, hysteresis voltage and detection delay time.

OV_CFG b2-b0 (OV2-0) configuration bits with corresponding voltage threshold with a default of 000. Resolution is 50mV.

0x00	4.15V	0x02	4.25V	0x04	4.35V	0x06	4.45V
0x01	4.20V	0x03	4.30V	0x05	4.40V	0x07	4.50V

OV_CFG b4-b3 (OVH1-0) configuration bits with corresponding hysteresis voltage with a default of 00. Resolution is 100mV.

0x00	0.10V	0x01	0.20V	0x02	0.30V	0x03	0.0V

OV_CFG b7-b5 (OVD2-0) configuration buts with corresponding delay time for over voltage with a default of 000.Resolution is 250msec

0x00	0.50sec	0x02	1.00sec	0x04	1.50sec	0x06	2.00sec
0x01	0.75sec	0x03	1.25sec	0x05	1.75sec	0x07	2.25sec

7.21.8 UV_CFG : Under Voltage Hysteresis and Threshold Configuration Register

UV LEVEL REGISTER (0x07)							
7	6	5	4	3	2	1	0
0	UVFET _-DIS	UVH1	UVH0	UV3	UV2	UV1	UV0

The UV register determines cell under voltage threshold, hysteresis voltage and detection delay time.

UV_CFG b2-b0 (UV3-0) configuration bits with corresponding voltage threshold with a default of 000. Resolution is 100mV.

0x00	1.40V	0x04	1.80V	0x08	2.20V	0x0c	2.60V
0x01	1.50V	0x05	1.90V	0x09	2.30V	0x0d	2.70V
0x02	1.60V	0x06	2.00V	0x0a	2.40V	0x0e	2.80V
0x03	1.70V	0x07	2.10V	0x0b	2.50V	0x0f	2.90V

UV_CFG b5-b4 (UVH1-0) configuration bits with corresponding hysteresis voltage with a default of 00. Resolution is 200mV.

0x00	0.20V	0x01	0.40V	0x02	0.8V	0x03	1.20V

When the Under Voltage threshold and the hysteresis values are high then under voltage recovery may not occur. To avoid this, the following table should be used for assistance in configuration.

Table 10: Combination of UV release voltage vs. hysteresis

		Hystersis			
		0.2V	0.4V	0.8V	1.2V
Cell under voltage(V)	1.4	1.6	1.8	2.2	2.6
	1.5	1.7	1.9	2.3	2.7
	1.6	1.8	2	2.4	2.8
	1.7	1.9	2.1	2.5	2.9
	1.8	2	2.2	2.6	3
	1.9	2.1	2.3	2.7	3.1
	2	2.2	2.4	2.8	3.2
	2.1	2.3	2.5	2.9	3.3
	2.2	2.4	2.6	3	3.3
	2.3	2.5	2.7	3.1	3.3
	2.4	2.6	2.8	3.2	3.3
	2.5	2.7	2.9	3.3	3.3
	2.6	2.8	3	3.3	3.3
	2.7	2.9	3.1	3.3	3.3
	2.8	3	3.2	3.3	3.3
	2.9	3.1	3.3	3.3	3.3

UV_CFG b6 (UVFET_DIS): This bit disable automatically turn off DSG output, when UV is detected in Host Control Mode .

0 = DSG output change to OFF, when UV is detected (default).
1 = DSG output not change to OFF, when UV is detected.
But, UV of the status register will be change, even this bit =1

UV_CFG b7 : This bit should be set 0 so that bq77PL900 protect battery cell safety.

7.21.9 OC&UV_DELAY : Over Current and Under Voltage Delay Register

OC&UVDELAY REGISTER (0x08)							
7	6	5	4	3	2	1	0
UVD3	UVD2	UVD1	UVD0	OCD3	OCD2	OCD1	OCD0

The FUNCTION & OCDV CFG register determines over current in discharge voltage threshold and controls functions.

OC&UV_DELAY b3-b0 (OCD3-0) configuration bits with corresponding voltage threshold. Resolution is 5mV.

0x00	10 mV	0x04	30 mV	0x08	50 mV	0x0c	70 mV
0x01	15 mV	0x05	35 mV	0x09	55 mV	0x0c	75 mV
0x02	20 mV	0x06	40 mV	0x0a	60 mV	0x0e	80 mV
0x03	25 mV	0x07	45 mV	0x0b	65 mV	0x0f	85 mV

OC&UVDELAY b7-b4 (UVD3-0) configuration buts with corresponding delay time for under voltage with a default of 000. Resolution is 1.0sec at FS bit=0,.

OC&UVDELAY b7-b4 (UVD3-0)	FS bit (OUTPUT_CONTROL b7)	
	1	0
0x00	See Table Below	1s
0x01		2s
0x02		3s
0x03		4s
0x04		5s
0x05		6s
0x06		7s
0x07		8s
0x08	1s	1s
0x09	2s	2s
0x0a	3s	3s
0x0b	4s	4s
0x0c	5s	5s
0x0d	6s	6s
0x0e	7s	7s
0x0f	8s	8s

UVD<3:0>	Internal Count	Delay time (ms) ,FS =1					
		5Cell	6Cell	7Cell	8Cell	9Cell	10Cell
0x00	0	0	0	0	0	0	0
0x01	2	1.25	1.5	1.75	2	2.25	2.5
0x02	4	2.5	3	3.5	4	4.5	5
0x03	8	5	6	7	8	9	10
0x04	10	6.25	7.5	8.75	10	11.25	12.5
0x05	12	7.5	9	10.5	12	13.5	15
0x06	16	10	12	14	16	18	20
0x07	24	15	18	21	24	27	30

7.21.10 OCD_CFG : Over Current in Discharge Configuration Register

OCD_CFG REGISTER (0x09)							
7	6	5	4	3	2	1	0
CBEN	ZVC	SOR	OCDD4	OCDD3	OCDD2	OCDD1	OCDD0

The FUNCTION & OCD_CFG register determines Function and over load detection delay time.

OCD_CFG b4-b0 (OCDD4-0) configuration bits with corresponding delay time. Units are in ms and resolution is 20ms or 100ms

0x00	20msec	0x08	180msec	0x10	100msec	0x18	900msec
0x01	40msec	0x09	200msec	0x11	200msec	0x19	1000msec
0x02	60msec	0x0a	220msec	0x12	300msec	0x1a	1100msec
0x03	80msec	0x0b	240msec	0x13	400msec	0x1b	1200msec
0x04	100msec	0x0c	260msec	0x14	500msec	0x1c	1300msec
0x05	120msec	0x0d	280msec	0x15	600msec	0x1d	1400msec
0x06	140msec	0x0e	300msec	0x16	700msec	0x1e	1500msec
0x07	160msec	0x0f	320msec	0x17	800msec	0x1f	1600msec

OCD_CFG b5 (SOR): Recover condition from SC and OC with Stand Alone Mode
0 =Recover by attaching a Charger. Recover comparator is active after 12.8sec for OC/SC detection (default)
1 = Recover by SC/OC condition released. Recovery from OC/SC after 12.8sec.

OCD_CFG b6 (ZVC): This bit controls the 0V/Pre-charge of GPOD output
0 = Disable GPOD output 0V/Pre-charge mode with Stand Alone (default)
1 = Enable GPOD output 0V/Pre-charge mode with Stand Alone

OCD_CFG b7 (CBEN): This bit controls the cell balancing.
0 = Disable cell balancing function (default)
1 = Enable cell balancing function.

7.21.11 SCD_CFG : Short Circuit in Discharge Configuration Register

SCD_CFG REGISTER (0x0a)							
7	6	5	4	3	2	1	0
SCDD3	SCDD2	SCDD1	SCDD0	SCD3	SCD2	SCD1	SCD0

The SCD_CFG register determines short circuit voltage threshold and detection delay time.

SCD_CFG b3-b0 (SCD3-0): These lower nibble bits select the value of the short circuit in discharge voltage threshold with 0000 as the default, units in mV and a resolution of 5mV

0x00	60mV	0x04	80 mV	0x08	100 mV	0x0c	120 mV
0x01	65 mV	0x05	85 mV	0x09	105 mV	0x0d	125 mV
0x02	70 mV	0x06	90 mV	0x0a	110 mV	0x0e	130 mV
0x03	75 mV	0x07	95 mV	0x0b	115 mV	0x0f	135 mV

SCD_CFG b7-b4 (SCDD3-0): These upper nibble bits select the value of the short circuit in discharge delay time. 0000 is the default, units of μs and a resolution of 60μs.

0x00	0μsec	0x04	240μsec	0x08	480μsec	0x0c	720μsec
0x01	60μsec	0x05	300μsec	0x09	540μsec	0x0d	780μsec
0x02	120μsec	0x06	360μsec	0x0a	600μsec	0x0e	840μsec
0x03	180μsec	0x07	420μsec	0x0b	660μsec	0x0f	900μsec

7.21.12 EEPROM : EEPROM Write Enable and COnfiguratin Register

EEPROM REGISTER (0x0b)							
7	6	5	4	3	2	1	0
EEPROM7	EEPROM6	EEPROM5	EEPROM4	EEPROM3	EEPROM2	EEPROM1	EEPROM0

EEPROM b7-b0 (EEPROM7-0):

These bits enable data write to EEPROM(0x06-0x9a) with 01000001 (0x41).

Pre-writing data is available by setting these bits with 01100010 (0x62).

Default is 00000000 (0x00).

In order to charge cells, the CHG FET must be turned on to create a current path. When the battery voltage (V_{BAT}) is low and the CHG is ON, the pack voltage (V_{PACK}) is as low as the battery voltage. In cases where the level is below the supply voltage for the bq77PL900 is too low to operate, there are two configurations to provide appropriate 0 V/pre-charge function.

Common FET mode does not require a dedicated 0V/pre-charge FET. The CHG FET is ON. This method is suitable for a charger that has a 0V/pre-charge function. The second mode is to use a 0V/Pre-charge FET which establishes a dedicated 0V/pre-charge current path by using an additional open drain (GPOD output) for driving an external FET (PCHG FET). This configuration sustains the PACK+ voltage level. Any type of charger can be used with this configuration.

Table 11: 0V Charge Summary

PROTECTION MODE	0V CHARGE TYPE	DEMANDED CHARGE FUNCTION	APPLICATION CIRCUIT
Host Control Mode	Common FET (1)	Fast charge Pre-charge	PMS = PACK GPOD ouput not used
	0V/Pre-Charge FET(2)	Fast charge	PMS =GND GPOD output: Drives 0V-charge FET (PCHG FET).
Stand Alone Mode	Common FET (1)	Fast charge Pre-charge	PMS = PACK GPOD output not used.
	0V/Pre-Charge FET(2)	Fast charge	PMS = GND GPOD output: Drives 0V-charge FET (PCHG FET).

7.21.13 Common FET

In this mode the PMS pin is connected to PACK+. In this configuration, the charger must have a 0V/pre-charging function which is typically controlled as follows:

- The cell voltage is lower than certain constant voltage (normally about 3.0V/cell)
  - Apply 0V/Pre charging current.
- The cell voltage is higher than certain constant voltage (normally about 3.0V/cell)
  - Apply fast charging current.

When the charger is connected and V_{PMS} is greater than or equal to 0.7V the CHG FET is turned ON. The charging current flows through the CHG FET and the back diode of the DSG.

$V_{PACK+} = V_{BAT} + 0.7V$ (VF: forward voltage of a DSG-FET back diode)$+V_{DS}$(CHG-FET)

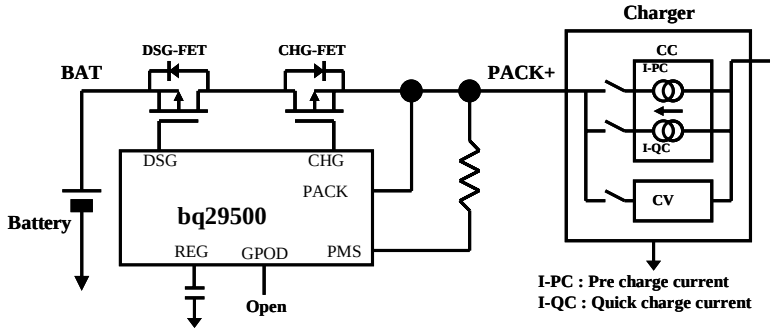


Figure 23: Common FET Circuit Diagram

When the PACK pin voltage is maintained at higher than 0.7V and the pre-charging current is maintained, the PACK voltage and BAT voltage are under the minimum bq77PL900 supply voltage so the bq77PL900 regulator is inactive.
When the BAT voltage rises and the PACK pin voltage reaches bq77PL900 minimum supply voltage, an internal 3.3V regulator is turned ON. Then, the CHG FET state is controlled by UVP and OVP functions. When the all the cell voltages reach fast charge voltage (about 3.0V per cell), the charger starts fast charging mode.

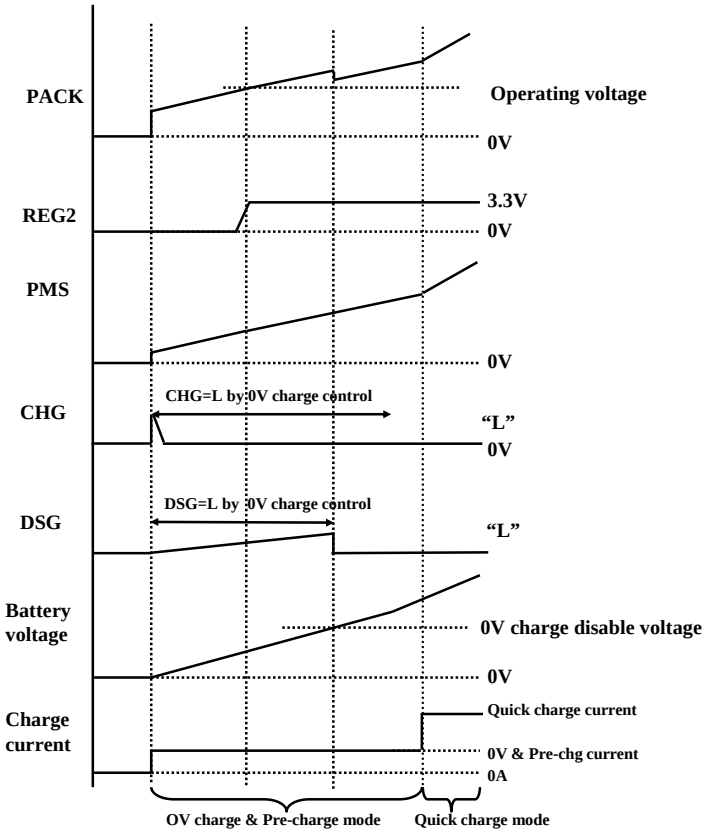


Figure 24: Signal Timing of Pins during 0 V/Pre-charging

7.21.14 0V/Pre-Charge FER in Host Control Mode

In this configuration, the charger doesn't need to support a pre-charge function. Thus, the Host controller and bq77PL900 must limit the fast charging current to a suitable 0V/Pre-charge level.
The PMS pin is connected to GND and a 0V/pre-charge current flow through a dedicated 0V/pre-charge FET (PCHG FET).

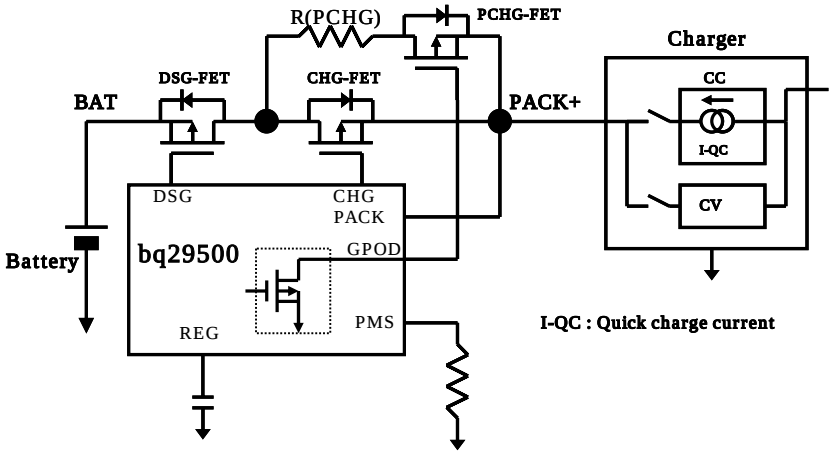


Figure 25 : 0V/Pre-charge FET circuit in Host Control Mode

The 0V/pre-charge FET is driven by the GPOD output. By set 1 at GPOD bit , then GPOD output turns ON, then the PCHG FET. The 0V/pre-charge current is limited by the 0V/pre-charge FET (PCHG FET) and a series resister (R(PCHG)) as below.

$$I_{0V/PCHG} = I_D = (V_{PACK+} - V_{BAT} - V_{DS}) / R_P$$

A load curve of the PCHG FET is shown below. When the gate – source voltage (V_{DS}) is high enough, the FET operates in the linear region and has low resistance. By approximating V_{DS} as 0V, the 0V/pre-charge current ($I_{0V/PCHG}$) is expressed as below.

$$I_{0V/PCHG} = (V_{PACK+} - V_{BAT}) / R_P$$

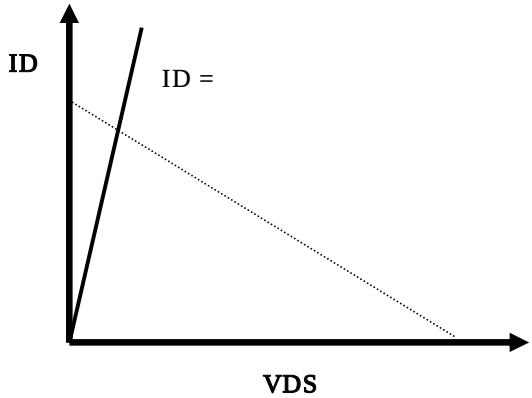


Figure 26 : 0V/PCHG FET ID and VDS characteristics

During the 0V/pre-charge, the CHG FET is turned OFF and the PCHG FET is turned ON. When the Host controller detects that all the cell voltage have reached the fast charge threshold, it then turns ON the CHG FET and turns OFF the PCHG FET. The signal timing is shown below.

The CHG, DSG and PCHG FETs are turned OFF when the charger is connected. Then, the charger applies its maximum output voltage (constant voltage mode output voltage) to the PACK+ pin. Then, the bq77PL900 3.3V regulator becomes active and supplies power to the Host controller. As the Host controller starts up, it turns on the GPOD output and the 0V/pre-charge current begins to flow.
In this configuration, attention is needed to control high power consumption at the PCHG FET and the series resistor (R_P). The highest power is consumed at 0V cell voltage (highest voltage between PACK+ and BAT pins) and it results in highest heat generation. For example, the power consumption in 10 series batteries with 42V fast charge voltage and 1K Ohms R_P is expressed as below.

$$I_{OV/PCHG} = (42V - 0.0V) / 1k\Omega = 42mA$$
$$(\text{Power Consumption at } R_P) = 42V \times 42mA = 1.6W$$

It is recommended to combine the resister (R_P) and the thermistor to reduce the consumption.
Once the cell voltage reaches the fast charge threshold, the host controller turns ON the CHG and DSG FETs and also turns OFF the PCHG FET.

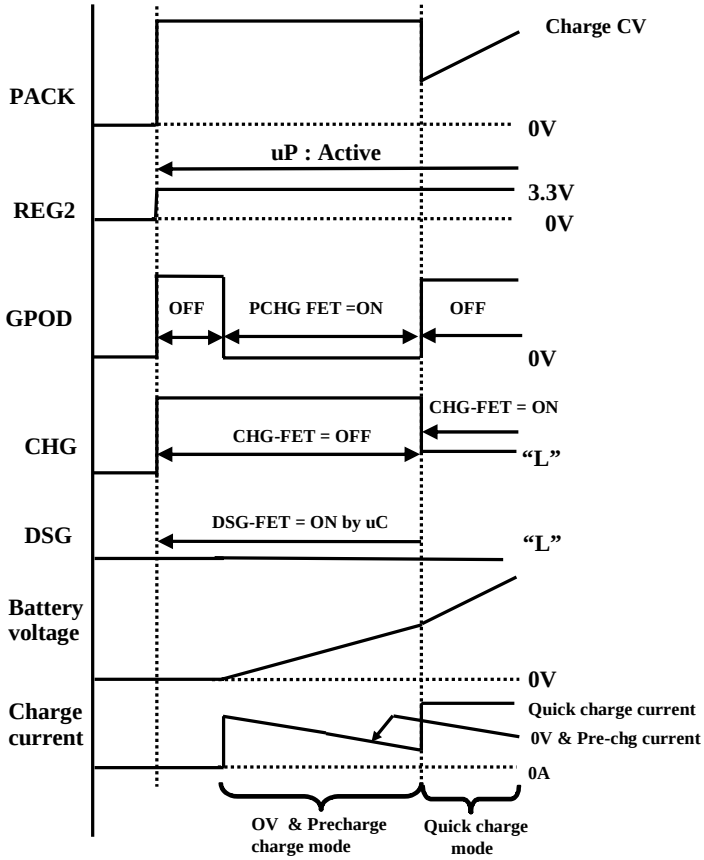


Figure 27 : Signal Timing of Pins during 0 V charging and pre-charging (Pre-charge FET) with Host Control Mode

7.21.15 0V/Pre-Charge FER in Stand Alone Mode

The circuit configuration is the same as 0/Pre-charge FET In Host Control Mode although in Stand Alone Mode the bq77PL900 automatically turns on GPOD output. When the battery voltage reaches “0V the charger disable voltage” (=PMS disable voltage), GPOD output is turned OFF, and then the DSG and CHG FETs are controlled by internal UV comparator function. To activate this mode, set *OCDELAY register [ZVC]*.

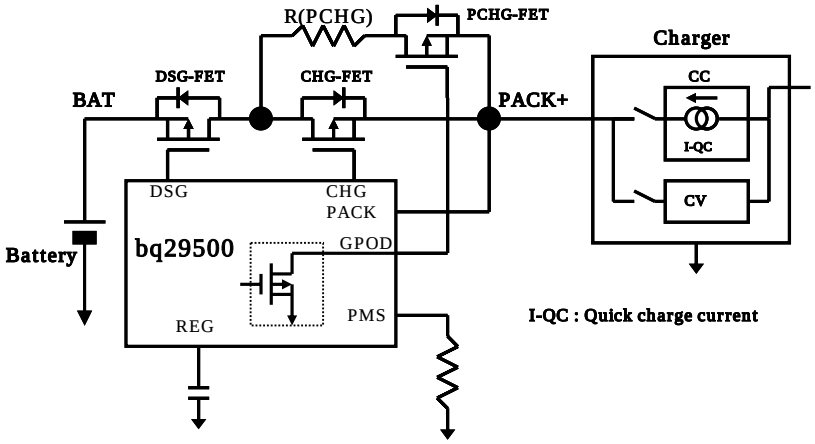


Figure 28 : 0V/Pre-charge FET Circuit Diagram In Stand Alone Mode

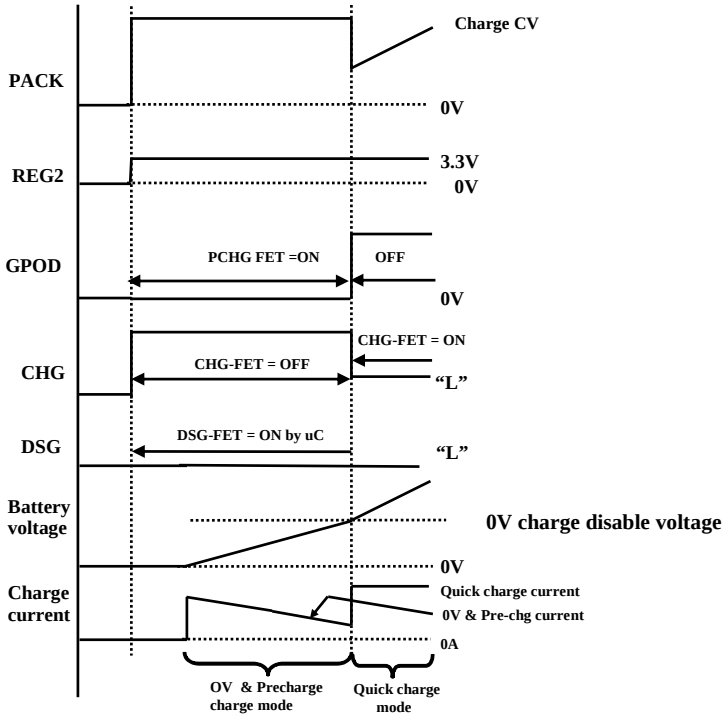
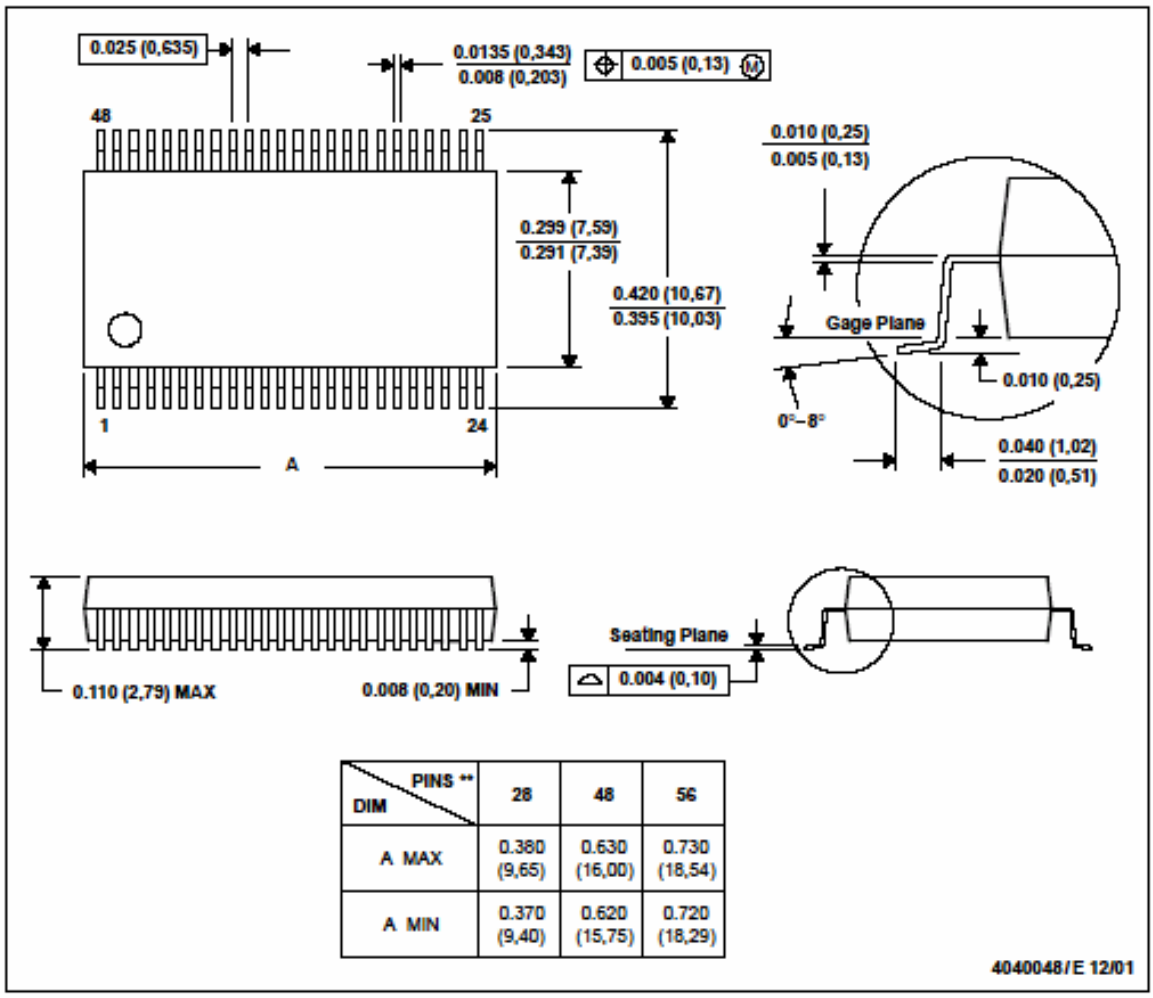


Figure 29: Signal Timing of Pins during 0V/Pre-charging (PCHG FET) In Stand Alone Mode

8 Mechanical Information

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048/E 12/01

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

9 Reference Schematic

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