UBA2071T; UBA2071TS

Half-bridge control IC for CCFL backlighting

Rev. 4.10 — August 2007 Objective data sheet

1. General description

The UBA2071 is a high voltage IC intended to drive Cold Cathode Fluorescent Lamps (CCFLs) for back-lighting applications. The IC contains a controller, level-shifter, bootstrap diode and drivers for the external half-bridge power switches.

The UBA2071 has a built in low frequency PWM generator which can be used to set the brightness level of the CCFLs. This PWM dimming can be synchronized with other ICs. The lamp current is controlled via an internal error amplifier.

The UBA2071 is designed to drive an half bridge with a supply voltage of up to 550V, so the inverter can be supplied directly from a 400V PFC bus.

The low voltage part of the IC needs little current, so it can be supplied by a dV/dt supply from the half bridge circuit that it drives.

2. Features

Suitable for operating in a very wide inverter supply voltage range (up to 550 V DC)
Integrated level-shifter
Integrated bootstrap diode
Lamp current control by modulating the high frequency oscillator
Over-voltage control
Over-current protection
Ignition failure detection
Hard-switching control
Arcing detection
Separate bidirectional pin for fault signaling
Brightness level adjustment through PWM dimming
Integrated PWM generator
Power-down mode
Communication pin for master / slave operation

3. Applications

LCD-backlighting, including LCD-TV and LCD-Monitor applications. The IC is intended to drive and control a half-bridge inverter with resonant load circuit for CCFLs, but can also drive an array of External Electrode Fluorescent Lamps (EEFLs).

4. Quick reference data

Table 1. Quick reference data.

T_{amb} = 25 °C; V_{VDD} = 12 V; R_{IREF} = 33 kΩ; V_{EN}=V_{VDD} and CPWM connected to a capacitor, unless otherwise specified. All voltages are measured with respect to signal ground (SGND, pin 10). SGND and PGND connected together. Currents are positive when flowing into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{HV}	Inverter supply voltage					550	V
V_{VDD}	IC supply voltage					14	V
I_{VDD}	IC standby current	disabled, V_{VDD}=11V			0.16		mA
I_{VDD}	IC supply current	oscillating, CF=100pF, GL and GH open			1.5		mA
$F_{S(min)}$	minimum output frequency		[1]	10		100	kHz
$F_{S(max)}/F_{S(min)}$	VCO frequency ratio				2.4		
$V_{IFB(reg)}$	current regulation reference level			1.2	1.25	1.3	V
$V_{VFB(ovref)}$	over voltage reference level			2.4	2.5	2.6	V
$T_{fault(stop)}$	fault time-out time	C_{CT} = 100nF		0.88	1.0	1.12	s
$I_{driver(source)}$	sourcing current of drivers	V_{GL}, V_{GH} = 4V		-105	-90	-75	mA
$R_{driver(sink)}$	sinking current of drivers	V_{GL}, V_{GH} = 2V		13.5	16.0	18.5	Ω
F_{PWM}	PWM dimming frequency		[1]	100		1000	Hz
D_{PWMd}	PWM generator duty cycle		[2]	12		100	%

[1] Can be set by external capacitor.

[2] PWMd is active low: A low level on the PWMd pin corresponds with lamps on. Example: D_{PWM}=20% means PWMd is during 20% of each cycle low and the lamps are 20% of the time on, resulting in a light output of 20%

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
UBA2071T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
UBA2071TS	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

6. Block diagram

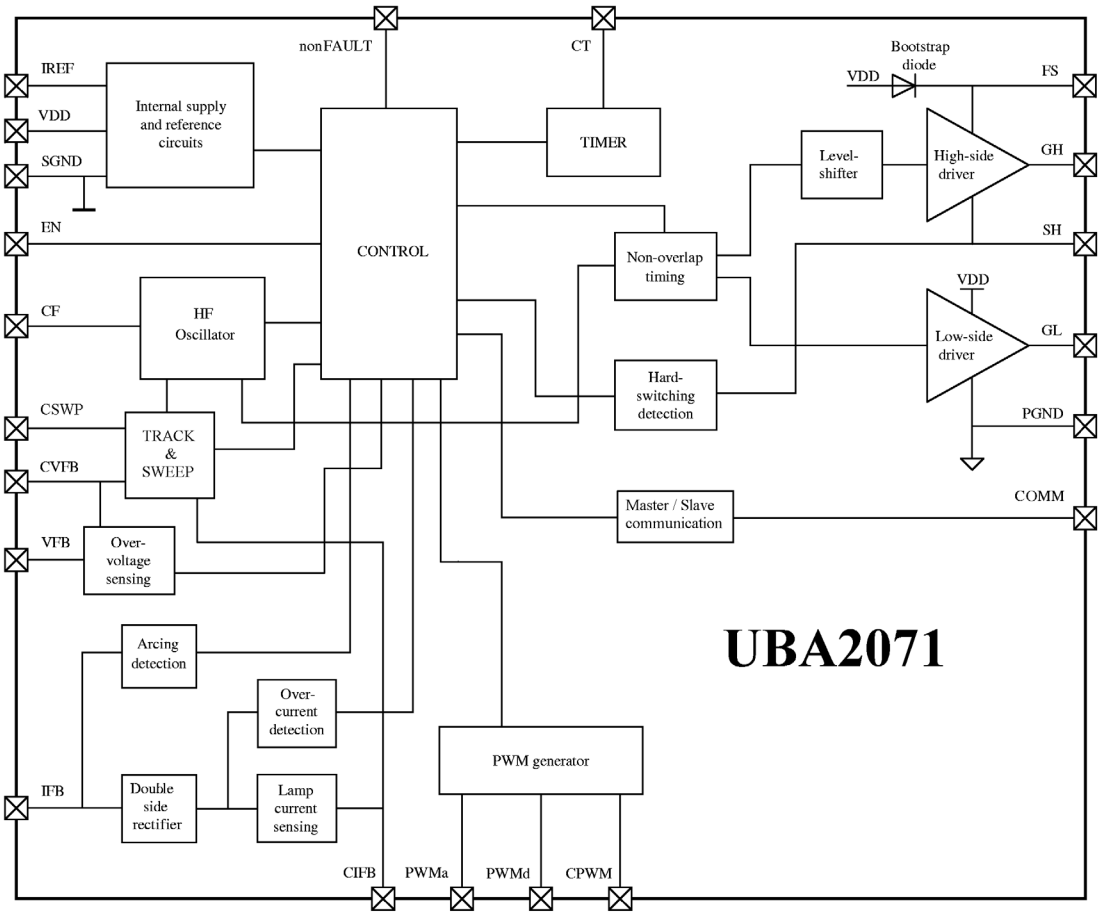


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

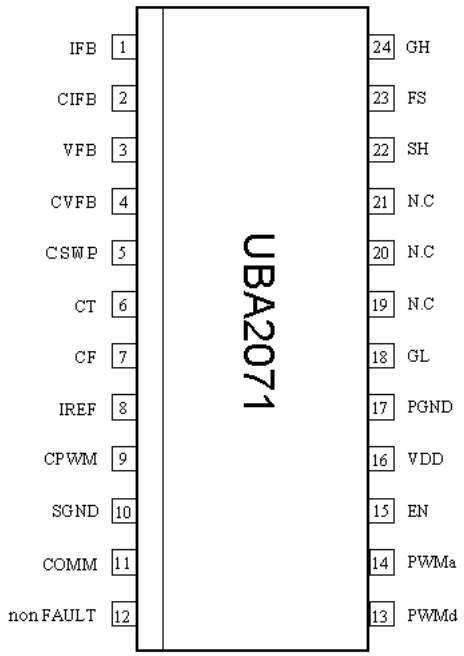


Fig 2. Pin assignment SO24 and SSOP24 package (top view)

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description	Function
IFB	1	current feedback input.	Input signal for the lamp current control loop. Should be connected to a voltage proportional to the lamp current.
CIFB	2	current regulation capacitor.	A capacitor must be connected between this pin and the signal ground. It sets the time constant of the lamp current control loop.
VFB	3	voltage feedback input	Input signal for the voltage control loop. Should be connected to a voltage proportional to the transformer output voltage
CVFB	4	voltage regulation capacitor	A capacitor must be connected between this pin and the signal ground. It sets the time constant of the voltage control loop.
CSWP	5	frequency sweep capacitor	A capacitor must be connected between this pin and the signal ground. It sets the time in which the HF frequency is swept up from regulation level to the maximum frequency and back during PWM dimming.
CT	6	fault timing capacitor	A capacitor must be connected between this pin and the signal ground. It sets the time that a fault condition is allowed before the IC shuts down itself.
CF	7	HF-oscillator timing capacitor	A capacitor must be connected between this pin and the signal ground. It sets the minimum switching frequency of the full bridge.
IREF	8	reference current output	A 33kΩ resistor must be connected between this pin and the signal ground. The IC uses it to make accurate internal currents.

Table 3: Pin description *…continued*

Symbol	Pin	Description	Function
CPWM	9	PWM timing capacitor	If a capacitor is connected between this pin and the signal ground, it sets the frequency of the PWM oscillator. If this pin is connected to signal ground the internal PWM oscillator is disabled.
SGND	10	signal ground	
COMM	11	master / slave communication	Via this pin the UBA2071 can communicate with a dedicated slave device.
nonFAULT	12	status signal input/output	The IC signals a fault condition to external circuits by pulling this pin low. Also external circuits can signal a fault condition to the IC by pulling this pin low.
PWMd	13	digital PWM dimming input/output	Digital output of internally generated PWM signal if a capacitor is connected to the CPWM-pin. Digital input of PWM signal if the CPWM-pin is connected to signal ground. *Note that the signal on the PWMd-pin is active low, so low voltage on the PWMd-pin means lamps are on.*
PWMa	14	analog PWM dimming input	The duty cycle of the internally generated PWM signal is proportional to the voltage on this pin.
EN	15	chip enable input	A low voltage on this pin will reset and shut down the IC
VDD	16	supply input	A buffer capacitor must be connected between this pin and power ground
PGND	17	power ground	return for the low side driver
GL	18	low-side driver output	Gate connection of the low side power switch
NC	19	not connected	HV spacer pin
NC	20	not connected	HV spacer pin
NC	21	not connected	HV spacer pin
SH	22	high-side source connection	Return for high side gate driver. Must be connected to the source of the high side half bridge power switch.
FS	23	floating supply output	A buffer capacitor must be connected between this pin and the SH-pin. This capacitor is charged when the low side power switch is on and supplies the high side driver.
GH	24	high-side driver output	Gate connection of the high side half bridge power switch

8. Functional description

The UBA2071 is designed to drive a half-bridge inverter (as shown in Figure 3) with a resonant load. The load consists typically of transformers with CCFLs.

The IC has an AC lamp current sense input (IFB). It regulates the lamp current by varying its switching frequency. The load is presumed to be inductive: higher frequency results in lower lamp current.

The UBA2071 includes a so called PWM dimming function. The IC switches the lamps on and off with a frequency lower than the lamp current frequency but higher then what the human eye can see. The light output of the lamps can be set by setting the ratio of the on- and off-time.

The IC has several protections.

The next chapters will descibe each function in more detail.

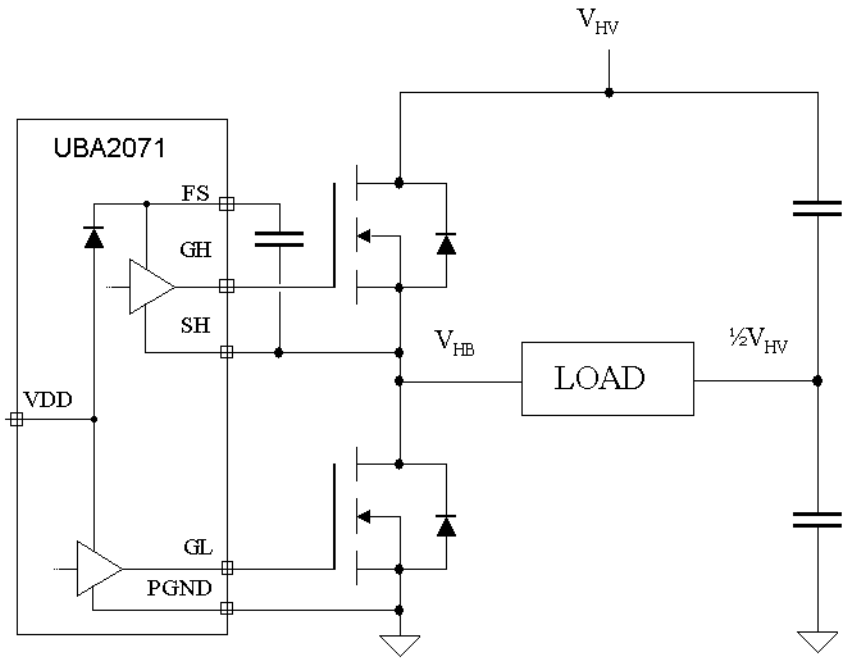


Fig 3. Basic half bridge inverter

8.1 Supply, Start-up and Under-Voltage Lock-Out (UVLO)

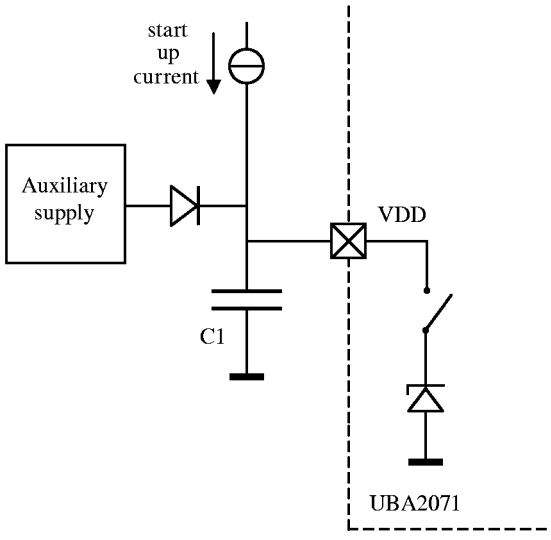


Fig 4. Supply configuration

The IC is supplied via the VDD-pin as shown in Figure 4. The auxiliary supply is either made by the inverter itself, using an auxiliary winding on the lamp transformer or a dV/dt supply, or is an fixed voltage supply available from any external circuit. A start up current source that can supply minimal $I_{VDD(start)}$ is needed for start up. This can be a resistor to the half-bridge supply voltage.

The IC starts up when the voltage at the VDD-pin comes above $V_{VDD(start)}$ and locks out (stops oscillating) when the voltage at the VDD-pin drops below $V_{VDD(stop)}$. The hysteresis between the start and stop levels allows the IC to be supplied by the supply buffer capacitor (C1 in Figure 4) until the auxiliary supply is settled. The auxiliary supply must not exceed the maximum voltage allowed on the VDD-pin and has to be above $V_{VDD(stop)}$.

8.2 VDD clamp

When the IC is disabled (EN-pin low) or in the stop state, the VDD clamp is activated. The VDD clamp is an internal active zener limiting the voltage to $V_{VDD(clamp)}$. It prevents the start up current source from charging the VDD buffer capacitor to a too high voltage. The maximum clamp current is stated in Table 4 .

The maximum current that is allowed to be delivered by the start up current source is determined by the clamp voltage $V_{VDD(clamp)}$ as stated in Table 6 and the maximum allowed VDD voltage as stated in Table 4.

Note that if the IC is supplied with a fixed voltage supply and the VDD voltage is above $V_{VDD(clamp,min)}$ then the supply current at VDD when the IC is in stop state or disabled can be higher then $I_{VDD(start)}$ due to current through the clamp.

8.3 Enable

The UBA2071 can be put in standby via the EN-pin. If the voltage on the EN-pin is below $V_{EN(low)}$, the IC will stop oscillating, and most parts of the internal circuits will shut down. When the voltage on the EN-pin comes above $V_{EN(high)}$, the IC will start up again.

8.4 The oscillator

The IC uses an internal voltage controlled saw-tooth oscillator (see Figure 5). Its frequency is inverse proportional to the capacitor connected to the CF-pin. The IC switches GL on and GH off during one oscillator period and GL off and GH on during the next oscillator period. This results in a load voltage frequency (called the switching frequency from here on) of half the oscillator frequency with 50% duty cycle.

The oscillator frequency is controlled via the charge current at the CF-pin. By changing the frequency the lamp current is controlled. It is also used to limit the transformer output voltage and to switch lamps on and off during PWM dimming.

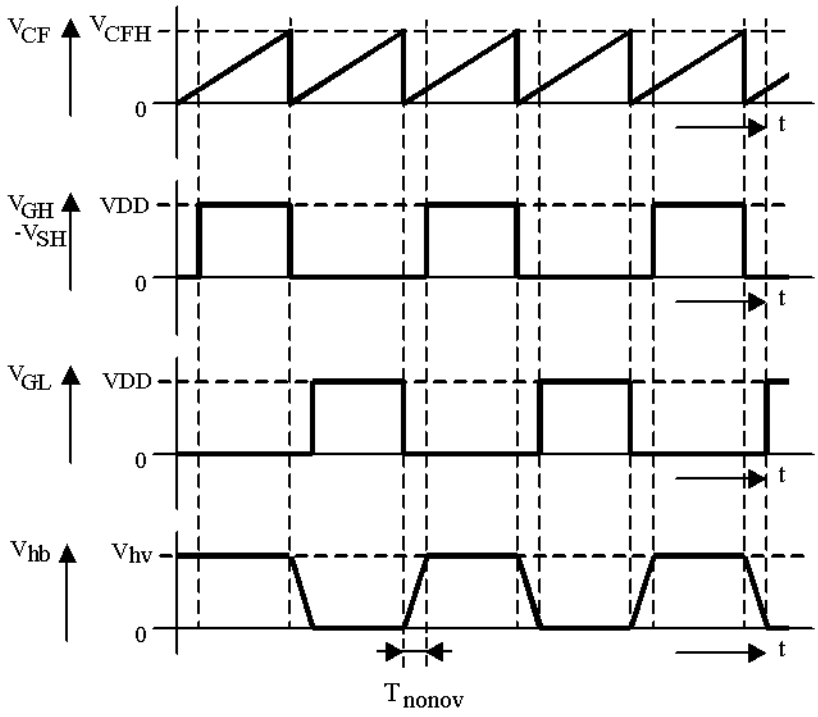


Fig 5. Oscillator, driver and half-bridge voltages

8.5 Non overlap

During each transition between the two states GL high /GH low and GL low /GH high, GL and GH will both be low for a fixed time T_{nonov} (the 'non-overlap time') to allow the half bridge point to be charged or discharged by the load current (presuming the load always has an inductive behavior), and thus enabling zero voltage switching (see also Figure 5).

8.6 Low- and high-side drivers

The low- and high-side drivers are identical. The output of each driver is connected to the equivalent gate of an external power MOSFET. The high-side driver is supplied by the bootstrap capacitor, which is charged from the VDD voltage via an internal diode when the low-side power MOSFETs is on. The low-side driver is directly supplied by the VDD voltage.

8.7 Lamp (re-)ignition

The IC starts at its maximum switching frequency $F_{s(max)}$. The lamp current and the lamp voltage control loops are enabled. The frequency is swept down towards the minimum frequency $F_{s(min)}$ (see Figure 7). During this initial ignition frequency sweep the lamp voltage will increase as the frequency comes closer to the resonant frequency of the unloaded resonance circuit. Once the ignition voltage V_{ign} is reached, the lamps will ignite and the lamp voltage will drop to the voltage of the loaded resonance curve (see Figure 6).

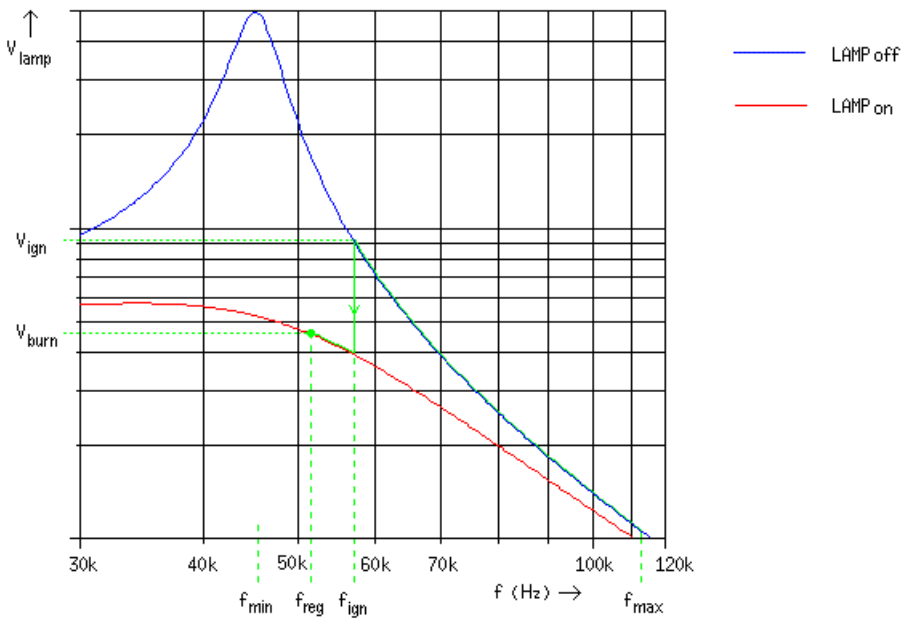


Fig 6. Initial ignition of fluorescent lamp via frequency sweep and load resonance.

Advantage of the sweep rather then a fixed ignition frequency is that sensitivity for spread in resonance frequency is much lower.

Once the lamps are ignited the frequency sweep-down continues, gradually increasing the lamp current (the resonance circuit should now still be inductive, so current increases as frequency drops) until the current regulation level is reached (at f_{reg}). The frequency will not reach f_{min} if the lamp current comes into regulation. Once it has been detected that the lamps are on PWM dimming is enabled. See Figure 7.

Initial ignition frequency sweep and PWM-generator are not synchronized. Once the regulation frequency is reached, PWM dimming can start anywhere in its cycle. A small internal PWM dimming enable delay time, $T_{PWM(delay)}$, allows the lamps to settle before PWM dimming starts.

At the start of the lamps off period of the PWM dimming, the switching frequency is swept up to f_{max}. This reduces the lamp voltage so the lamps go out. If f_{max} is reached, both GL and GH are made low, so both half bridge powers will be non-conducting (indicated by the dotted part of the switching frequency (F_S) line in Figure 7).

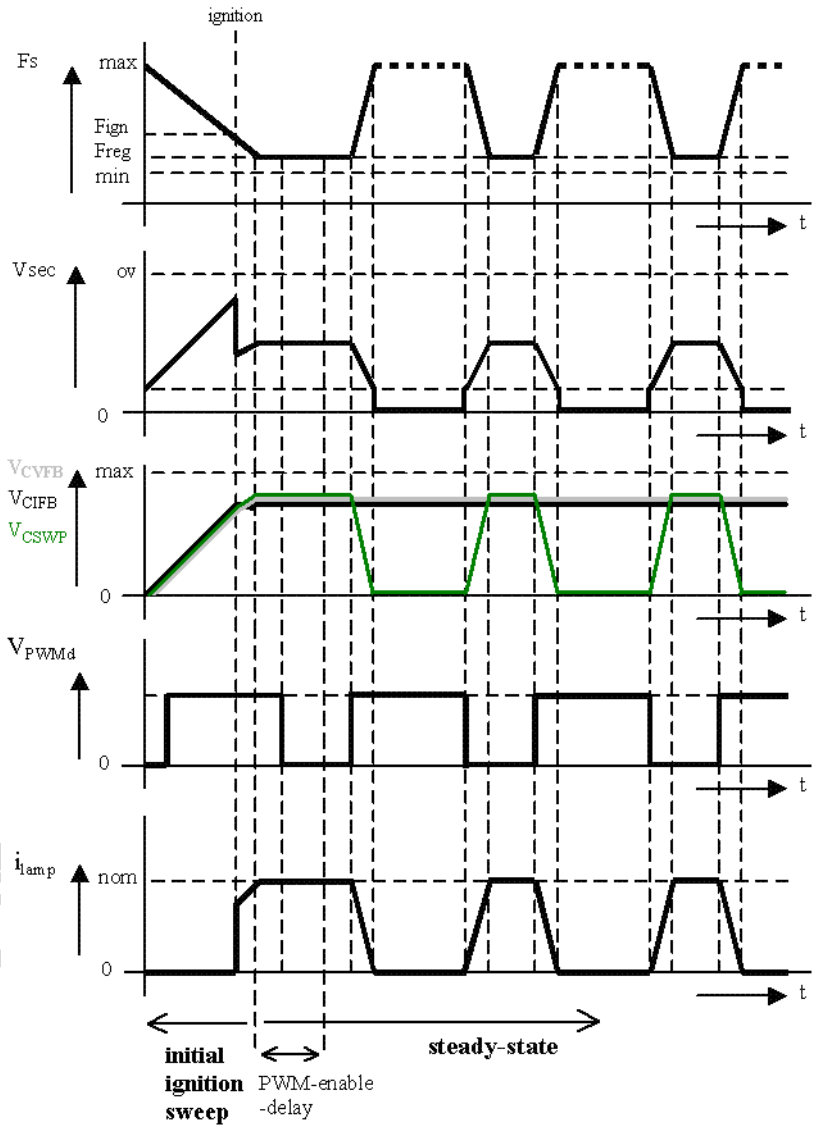


Fig 7. Initial ignition frequency sweep and PWM dimming frequency sweep signals

At the start of the lamps on period GI and GH start switching again and the frequency is swept back to the regulation frequency f_{reg}. The duration of the PWM frequency sweep is inverse proportional to the capacitor connected to the CSWP-pin.

8.8 Over voltage control

The over voltage control circuit is intended to prevent the transformer output voltage from exceeding its maximum rating. It can also be used to regulate the output voltage to the required lamp ignition voltage.

Under normal circumstances the capacitor at the CVFB-pin is charged by a constant bias current $I_{CVFB(charge)}$, thus the voltage on the CVFB-pin will increase resulting in a decrease of switching frequency. If the IC is in current regulation this bias current will flow away via a tracking circuit which makes the voltage on the CVFB-pin to follow the voltage on the CIFB-pin (see Figure 9).

When the voltage on the VFB-pin exceeds the OV reference level $V_{VFB(ovref)}$, not only an fault condition is signalled (for handling of fault conditions see Section 8.13), but also the bias current at the CVFB-pin changed to the discharge current $I_{CVFB(discharge)}$. As a result, the switching frequency increases and the output voltage of the transformer will decrease[1]. As soon as the voltage at the VFB-pin drops below the OV reference level, the CVFB capacitor is charged again and the output voltage of the transformer will increase again. Because the charging and discharging of the CVFB capacitor follows the ripple on the VFB voltage, the feedback gain of the voltage control loop is set by the ripple on the feedback signal.

The voltage at the CVFB-pin is limited by the oscillator circuit to $V_{CVFB(range)}$ when the minimum switching frequency $F_{s(min)}$ is reached (See Figure 8). This ensures an immediate frequency increase capability at over voltage detection.

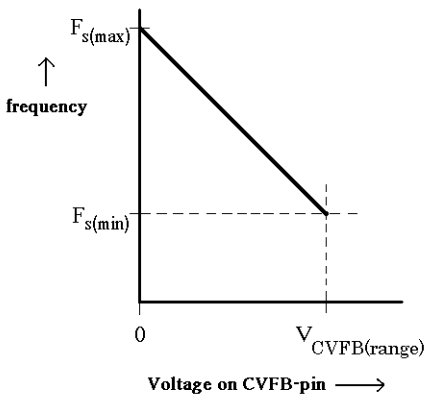


Fig 8. frequency function of CVFB voltage.

8.9 Lamp current control

The lamp current control is always active when the IC is on, except if the lamps are off during PWM dimming. The AC lamp current is sensed by an external resistor connected to the IFB-pin, see Figure 9. The resulting AC voltage on the IFB-pin is internally double-sided rectified (DSR), and compared to a reference level $V_{IFB(reg)}$ by an operational transconductance amplifier (OTA).

When the current is being regulated, switches S1 is closed (conducting). The output current of the OTA is fed into capacitor C1, which is connected to the CIFB-pin. So C1 is charged and discharged according to the voltage on the IFB-pin.

1. Presuming that the load impedance is in inductive region.

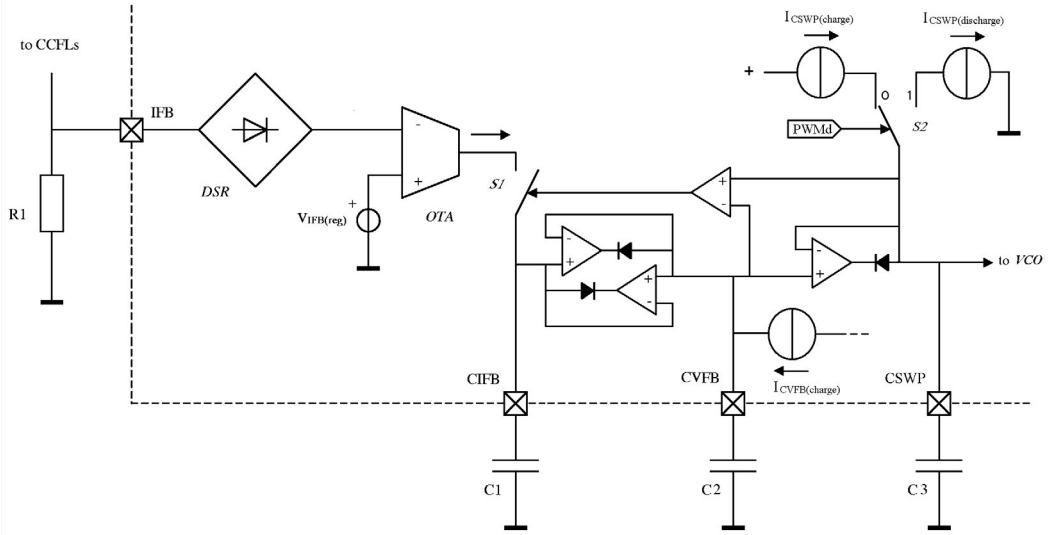


Fig 9. Lamp frequency control circuit

Under normal operating conditions, the voltage across capacitor C2, which is connected to the CVFB-pin, will follow the voltage on the CIFB-pin, and during the lamps on period of the PWM dimming, the voltage across C3, which is connected to the CSWP-pin, will follow the voltage on the CVFB pin, and thus also the voltage on the CIFB-pin.

The voltage on the CWP-pin is connected to the VCO input of the hf-oscillator and thus controls the switching frequency. Increasing the frequency will decrease the lamp current (presumed the load is inductive) and the other way round.

The advantage of having a separate current regulation loop timing capacitor pin CIFB next to the voltage regulation loop timing capacitor CVFB is that time constants for both loops can be set independent. The separate PWM dimming sweep timing capacitor pin CSWP makes it possible to set the PWM dimming sweep speed independent of the current and voltage regulation loops.

8.10 PWM dimming

PWM (Pulse Width Modulation) dimming is a method of reduce average lamp light output by switching the lamps on and off with a repetition rate (or PWM frequency) F_{PWM} high enough not to be seen by the human eye (but much lower then the inverter frequency F_S). By varying the lamps on to lamps off period ratio (called the duty cycle D_{PWM}) light output can be varied over a wide range.

The voltage at the CSWP-pin determines the actual switching frequency, it is inverse proportional to the switching frequency. During the lamps on period of the PWM dimming it follows the voltage at the CVFB-pin (the current $I_{CSWP(charge)}$ is drained by the tracking circuit between the CVFB-pin and the CSWP-pin).

During the lamps off period of the PWM dimming the lamp current control loop (Figure 9) is opened by opening switches S1. The voltage on the CSWP-pin is swept down and up again, thus sweeping up en down the frequency. This switches off the lamps and turns them on again (See also Figure 7). In the mean time the regulation level (the frequency at

which the lamp current was in regulation) is preserved in C1 and C2. Switch S1 is closed (conducting) again when the voltage on the CSWP-pin has reached the voltage on the CVFB-pin again.

The IC waits until the CSWP sweep-up (is frequency sweep down) has reached the current/voltage control level at the CVFB-pin again before sweeping down again. This prevents the lamps from going completely out when deep dimming is combined with a too large capacitor at the CSWP-pin.

After the switching frequency has reached F_{max}, both GL and GH are made low, so both half bridge powers will be non-conducting, see Figure 10 . This guarantees zero lamp current during the PWM-off period[2], while the CSWP frequency sweep acts as soft stop and soft re-start, of which the softness can be set by the value of the capacitor connected to the CSWP-pin.

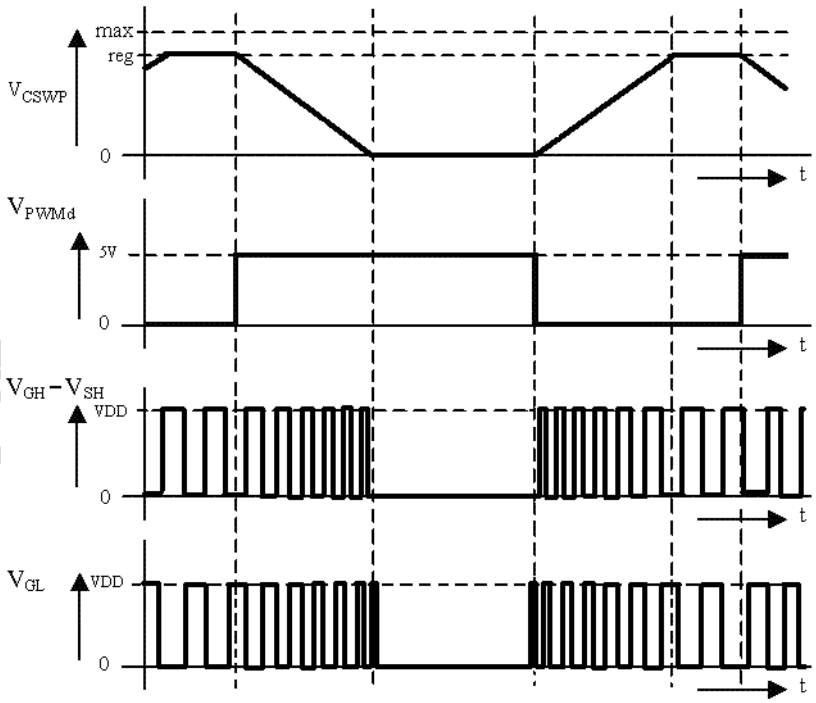


Fig 10. PWM dim cyclus waveforms

Three pins are available to configure the internal PWM generator: the CPWM-, PWMa-, and the PWMD-pin. The two possible PWM configurations are shown in Figure 11. In the analog or master mode the internal PWM generator is active and generating the PWM signal. This signal is put on the PWMd-pin, which is automatically configured as an output. The minimum duty cycle of the internal PWM generator is limited to $D_{PWM(min)}$.

2. Untill the ringing of voltage on the half-bridge point has died away, some (capacitive) current may still cause a light glow at the hot side of the lamps. Therefor it is advised to maximise the attinuation of the ringing circuit (made up by the transformer inductance and the dV/dt limiting capacitor).

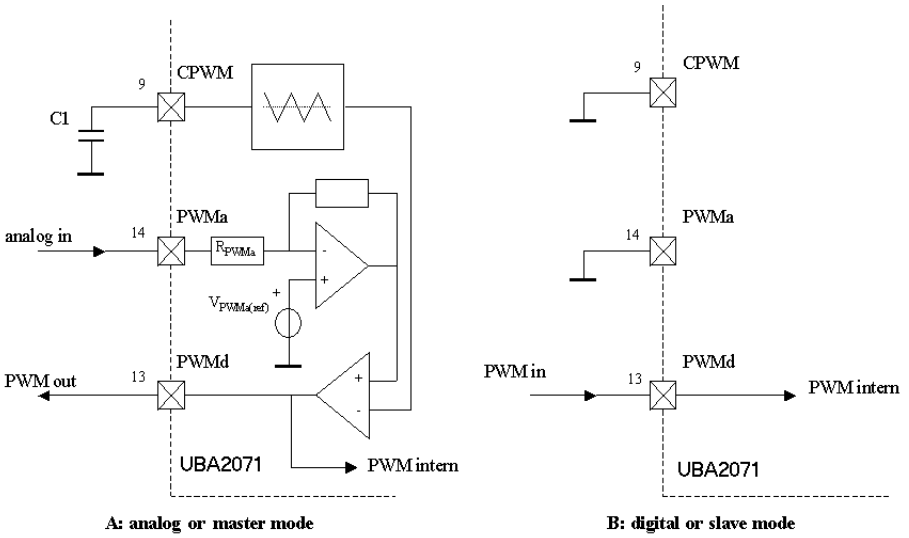


Fig 11. PWM dimming configurations

When the CPWM-pin is connected to ground the IC is put in digital or slave mode and the PWMd-pin is an input. The internal PWM generator is not used. The IC uses the PWM signal provided on the PWMd-pin.

PWM dimming of multiple ICs can be synchronized by configuring one IC as master and the others as slaves and connecting all PWMd-pins together.

The PWMd input/output is active low. A voltage below $V_{PWMD(low)}$ on the pin will turn the lamps on, while a voltage above $V_{PWMD(high)}$ will turn the lamps off.

The real lamp light output will be slightly less then the PWM duty cycle (unless the duty cycle is near $D_{PWM(max)}$) because of the phase shift sweep time (see Figure 12). The difference depends on the capacitor connected to the CSWP-pin.

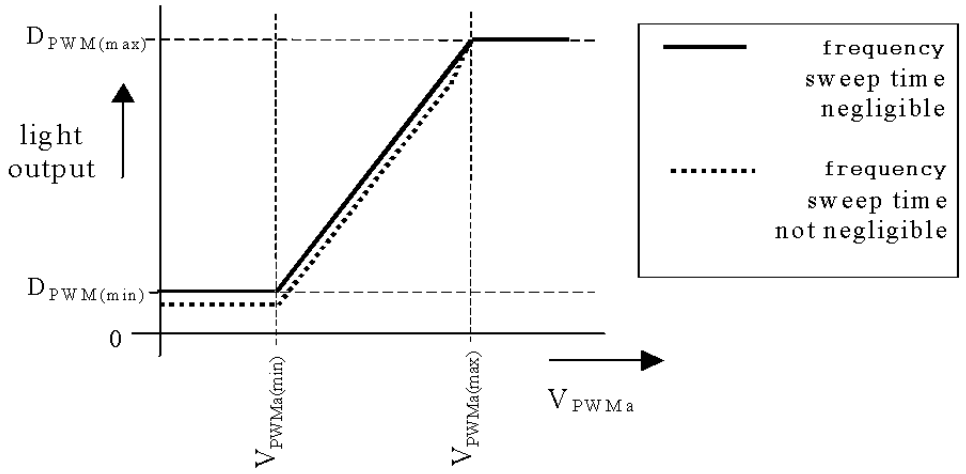


Fig 12. Light output as function of PWMa input voltage

PWM dimming is only enabled in normal mode, when no fault condition exists. The only exception is when an external detected fault condition is entered via the nonFAULT-pin, then PWM dimming remains active (see Figure 14).

8.11 The fault timer

The fault timer provides a delay in between the detection of a fault and the shut down of the IC (enter STOP-state). Its time is controlled by a capacitor at the CT-pin.

Any fault condition will start the timer. When the timer is activated, the capacitor at the CT-pin will be alternating charged and discharged (see Figure 13). These cycles are being counted by a four bit counter. After one cycle (the fault signalling delay $T_{fault(delay)}$) the nonFAULT-pin is activated (pulled low), to signal to any external circuit that there is a fault detected and the IC will stop if that fault continues. Once all bits of the counter are true (after 15.5 cycles) the fault time-out period $T_{fault(timeout)}$ is reached, and the IC will enter STOP-state.

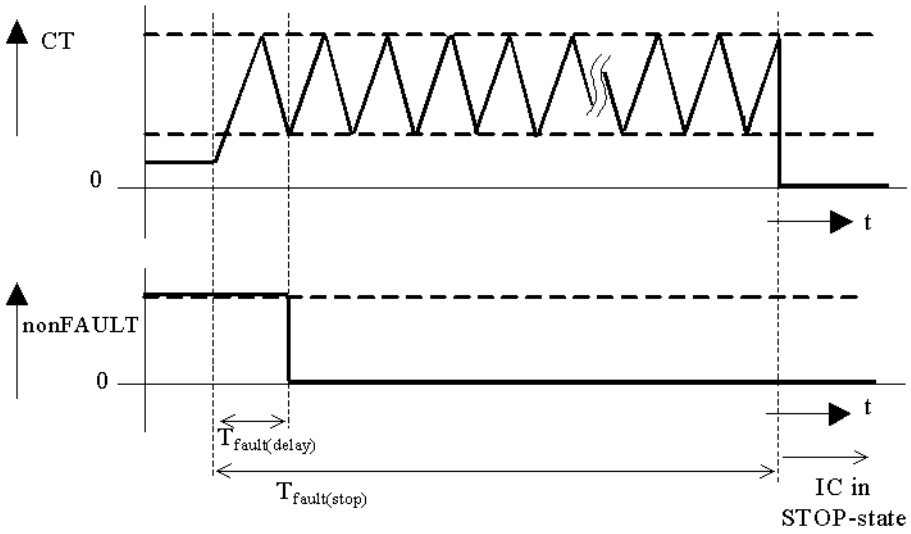


Fig 13. Fault timer waveforms

If the fault timer is inactive, the CT-pin voltage is one Vbe (≡0.7V). The CT-timer has a protection that prevents the IC to start-up if the CT-pin is shorted to GND.

8.12 Communication

The UBA2071 has a dedicated communication pin, the COMM-pin, for communicating with a slave half-bridge driver (like the UBA2073), for instance for use in a balanced half bridge driver configuration.

Via the COMM-pin, a clock signal and a signal to indicate that both half bridge powers are to be turned off are exported, and a fault signal is imported. The clock signal is a digital signal with a low level $V_{CLK(low)}$ and a high level $V_{CLK(high)}$. To signal that both half bridge powers should be turned off the voltage at the COMM-pin is raised $V_{COMM(off)}$.

The UBA2071 looks at the current drawn from the COMM-pin during the clock-high period for a hard-switching signal from the slave half-bridge driver. First a non-overlap time period T_{nonov} is discarded, to prevent capacitive load on the communication line to be seen as a signal, then the detected current is averaged over the clock-high period before being compared to the reference level $I_{HSDslave(ref)}$. The current value is sampled on the falling edge of the clock signal and hold during the clock-low period. The received signal is treated equal to an internal hard-switching detection (so PWM dimming will be disabled, switching frequency will be increased and fault-timer will be started).

When only the UBA2071 is used, this pin must be not connected.

8.13 Protections

All fault conditions and how they are processed in the IC can be found in Figure 14.

The UBA2071 includes internal over voltage (OV), over voltage extra (OVE), overcurrent (OC), bad contact or arcing (ARC), ignition failure (IF), open or shorted current feedback (IFB open/short), open or shorted voltage feedvack (VFB open/short) and hard switching (HS) protections. There are also two pins, the nonFAULT-pin and the COMM-pin via which a fault can be signalled to the IC by an external circuit.

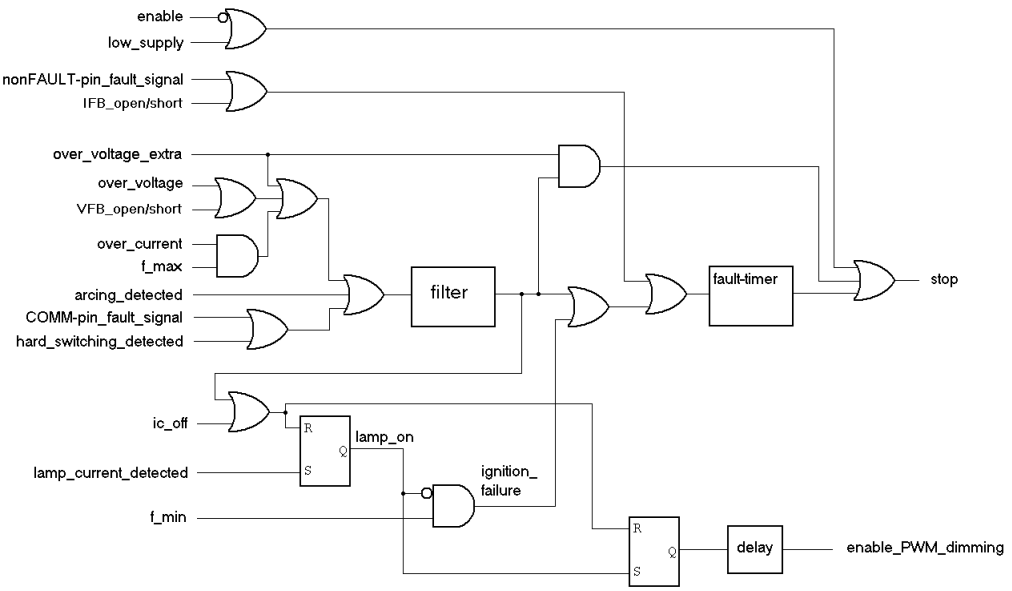


Fig 14. Simplified control schematic.

In the next sections each fault protection function will be explained.

8.13.1 Voltage feedback open or short protection

If the VFB-pin is left open or shorted to SGND, the voltage at the VFB-pin will drop below the VFB open/short protection thresshold $V_{VFB(OS)}$. As result the PWM dimming is disabled and the fault timer is started. Also to protect the inverter transformer(s) for overvoltage if the voltage feedback loop is broken, the frequency either stays at f_{max} or is increased by discharging the capacitor at the CVFB pin (by $I_{CVFB(discharge)}$).

8.13.2 Over voltage protection

The over voltage control (see Section 8.8) is intended to prevent the transformer output voltage from exceeding its maximum rating. Over voltage control level has to be at least at the required lamp ignition voltage, otherwise the lamps are not guaranteed to ignite.

Once the lamps are on, in steady state, the transformer output voltage will be usually about half the required ignition voltage. Thermal design of the transformers is based on this lower voltage, not on the ignition voltage were the over voltage control has to be above. Hence the circuit might not stay in over voltage regulation indefinitely. Therefor over voltage regulation is combined with over voltage protection.

When the voltage on the VFB-pin exceeds the OV reference level $V_{VFB(ovref)}$, not only CVFB is being discharge but also over voltage fault condition is signalled and PWM dimming is disabled and the fault timer is started. An internal latch makes the OV fault signal continuously high even if the voltage at the VFB-pin only exceeds $V_{VFB(ovref)}$ during part of the output period. So the peak of the voltage on the VFB-pin determines if an over voltage fault condition is seen. An internal filter prevents the over voltage fault condition to be resetted when the voltage at the VFB-pin drops below the OV reference level for only one or two hf cycles.

In order to avoid that OV fault condition at the nominal switching frequency (with the lamps operating normally), the voltage ripple on the VFB-pin must not be too large.

8.13.3 Hard switching protection

As the UBA2071 is intended to drive a half bridge at a high voltage, a feature is included to ensure zero voltage switching. The design of the resonant load should guarantee zero voltage switching under normal operating conditions. To prevent overheating due to high switching losses in case of any abnormal operating condition, hard-switching of the half-bridge is detected internally.

At the moment the high side switch is turned on, the voltage step at the SH-pin is measured. If it is above $V_{HS(thresshold)}$ then PWM dimming is disabled and the fault timer is started. Also the frequency is increased by discharging the capacitor at the CVFB pin (by $I_{CVFB(hs)}$).

8.13.4 Over voltage extra protection

Though the hard switching protection as described in Section 8.13.3 usually prevents the circuit from getting at the wrong side of the resonance curve of the load (were the load shows capacitive behavior), this might happen for instance when a lamp is suddenly disconnected. The parasitic capacitance of the lamp and its connection wire may make up a significant part of the resonance circuit capacitance, so if a lamp is suddenly disconnected the resonance frequency of the remaining load is suddenly higher, and the switching frequency might be at the capacitive side. Hard switching will occur and being detected,.The result is increase in switching frequency, which will make the situatie worse: the switching frequency comes closer to the resonance frequency of the remaining load, creating a higher and potentially destructive transformer secondary voltage.

The over voltage extra (OVE) protection prevents damage to the circuit by adding an extra over voltage protection level with quick response to that. When the voltage on the VFB-pin exceeds this OVE level $V_{VFB(ovextra)}$, an OVE fault condition is signalled. The IC will stop if this happens during a couple of subsequent hf cycles. The time it takes before the IC stops depends on the percentage of time the VFB-pin voltage exceeds the OVE level and if hard switching is detected also. Figure 15 shows typical shutdown response times in case over voltage and over voltage extra start being detected at the same moment and if over voltage, over voltage extra and hard switching start being detected at the same moment. The first parts of the curves are dashed because an internal filter makes that VFB needs to be above $V_{VFB(ovextra)}$ for at least about 1µs for the over voltage extra to react at all.

If normal over voltage fault was already present for more then about 840µs before over voltage extra detection started, or hard switching was already detected for more then about 55µs before over voltage extra detection started then the IC will shut down about 1µs after over voltage extra is detected.

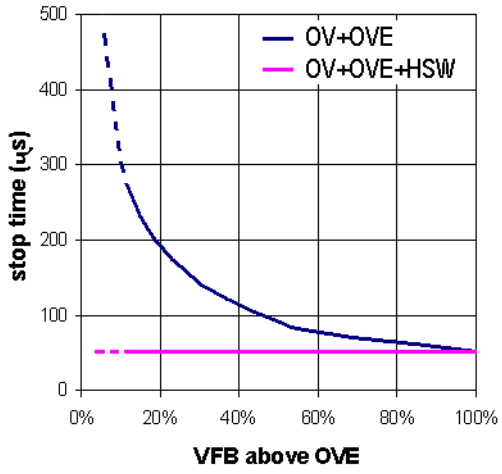


Fig 15. Shut down time at over voltage extra detection

8.13.5 Current feedback open or short protection

If the IFB-pin is left open or shorted to SGND, the absolute value[3] of the voltage at the IFB-pin will drop below the IFB open/short protection thresshold $V_{IFB(OS)}$ and the fault timer is started.

The IFB open/short protection looks only at the IFB-pin voltage if the voltage at the CSWP-pin is equal to the voltage at the CVFB-pin. During PWM dimming this is when the lamps are on and in current- or voltage-regulation (so not during PWM lamps of period and not during re-ignition frequency sweep). Also there's a built in activation delay to prevent the natural zero crossings of the current sense signal to activate the protection.

8.13.6 Over current detection

When the absolute value[4] of the voltage across the current sense resistor (connected to the IFB-pin) exceeds the OC reference level $V_{IFB(ocref)}$, and the IC is oscillating at $F_{s(max)}$, over-current is detected. As result PWM dimming is disabled and the fault timer is started.

8.13.7 Arcing detection

If arcing occurs, for instance due to a bad lamp connection, it causes repetitive short current spikes that can be seen as voltage spikes at the IFB input. The arcing detection circuit is directly connected to the IFB-pin, so it can only see spikes with a positive polarity. Usually that will be sufficient. It can detect spikes with amplitude above $V_{IFB(arcref)}$ and a duration longer then $T_{SPIKE(min)}$. Each spike will trigger an internal one-shot, which signals to the control circuits that arcing has been detected. When arcing is detected, PWM dimming is disabled and the fault timer is started.

3. The IFB-open/short comparator is behind the double side rectifier at the IFB-pin
4. The over current comparator is behind the double side rectifier at the IFB-pin

8.13.8 Ignition Failure (IF)

When the current control loop comes close to its regulation point, the lamps are presumed to be on (ignited). This is when the average double side rectified IFB-pin voltage is above $V_{IFB(lampon)}$. If the lamps are not on when the ignition sweep is finished (switching frequency has reached $F_{S(min)}$), then an ignition failure is detected, PWM dimming and is disabled and the fault timer is started.

8.13.9 The nonFAULT-pin

The nonFAULT-pin provides bidirectional signalling of the fault status between the IC and any external circuit. When no fault is detected, the voltage on the pin is pulled high by an internal current source.

An external circuit can signal to the IC that a fault has been detected by pulling down the pin. The IC will detect the current drawn from the pin and start the fault timer. To prevent interference with the PWM dimming, the IC will only look at the nonFAULT pin during the period that the lamp current regulation loop is closed (VCSWP=VCVFB).

When the IC detects a fault internal (as in Section 8.13.2 to Section 8.13.8), it signals this via the nonFAULT pin by pulling the pin down (after the fault signalling delay time $T_{fault(delay)}$). In this case the IC can not see anymore if there's an external detected fault, but that's no problem, because the fault timer is then already running.

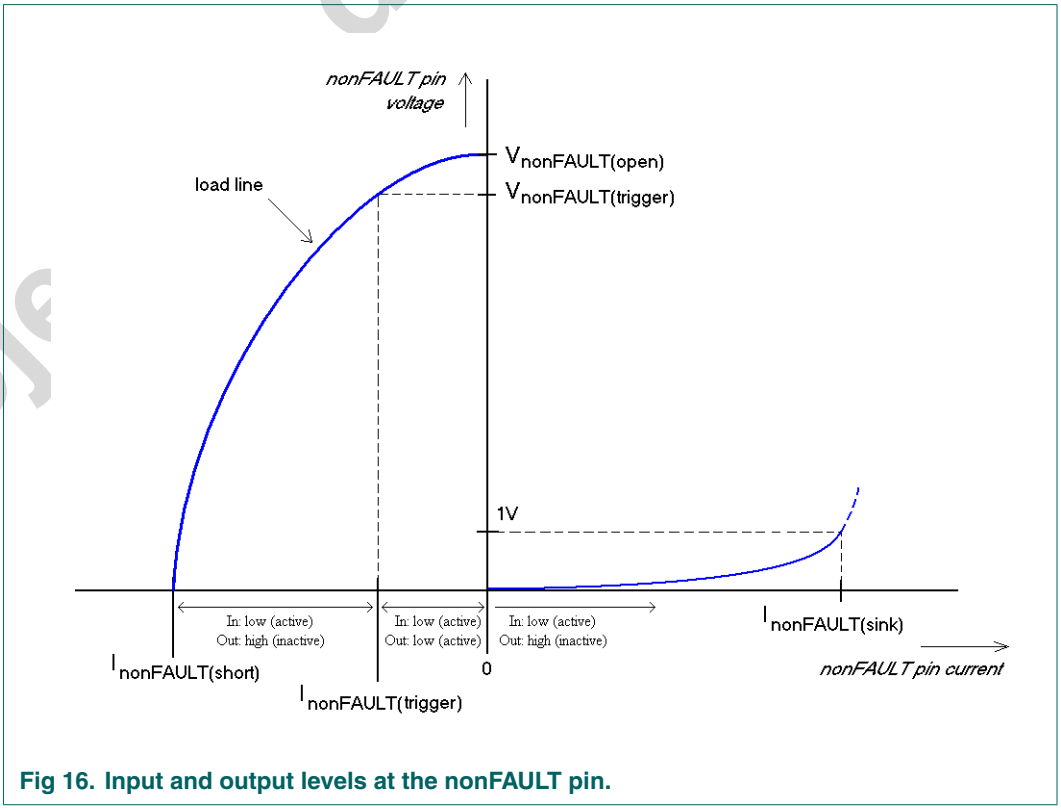


Fig 16. Input and output levels at the nonFAULT pin.

The signal from the IC is a voltage signal and the signal to the IC is a current signal. In this way a driving conflict is prevented. Also it leaves the possibility for the outside world to see the signal from the IC even while a fault condition is being signalled to the IC in the mean time, as illustrated in Figure 17.

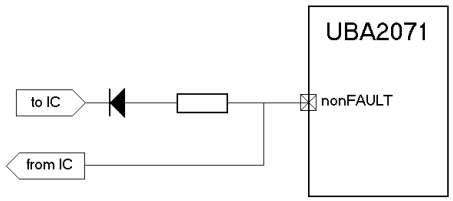


Fig 17. Splitting the nonFAULT pin signals to and from the IC.

8.13.10 Fault input via the COMM-pin

If a fault is signalled to the IC via the COMM-pin this fault is treated identical to 'hard switching detected' (see Section 8.13.3).

9. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to signal ground (pin 7); positive currents flow into the chip. The voltage ratings are valid provided other ratings are not violated.

Symbol	Parameter	Conditions	Min	Max	Unit
General					
R_{IREF}	reference resistor value on pin IREF		30	36	kΩ
SR	slew rate on pins FS, GH, and SH		–4	+4	V/ns
T_{amb}	ambient temperature		–25	+100	°C
T_j	junction temperature		–25	+125	°C
T_{stg}	storage temperature		–55	+150	°C
Voltages					
V_{FS}	voltage on pin FS	continuous	0	+570	V
		t < 0.5 s	0	+630	V
		with respect to V_{SH}	-0.3	+14	V
V_{GL}	voltage on pin GL		-0.3	+14	V
V_{GH}	voltage on pin GH	with respect to V_{SH}	-0.3	+14	V
V_{PGND}	voltage on pin PGND		-0.1	+0.1	V
V_{VDD}, V_{EN}	voltage on pins VDD and EN		-0.3	+14	V
V_{PWMa}, V_{PWMd}, $V_{nonFAULT}$	voltage on pins PWMa, PWMd, COMM and nonFAULT		-0.1	+5	V
V_{VFB}	voltage on pin VFB	continuous	-0.1	+5	V
		t<1ms	-0.1	+9	V
V_{IFB}	voltage on pin IFB	continuous	-5	+5	V
		t<1µs	-9	+9	V
Currents					
$I_{VDD(clamp)}$	clamp current on pin VDD	when disabled or in stop state	-	5	mA
ESD					

Table 4: Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to signal ground (pin 7); positive currents flow into the chip. The voltage ratings are valid provided other ratings are not violated.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{ESD}	electrostatic discharge voltage				
	human body model	IFB, CIFB, VFB, CVFB, CSWP, IREF, CT, CF, CPWM, nonFAULT, COMM, PWMa, PWMd, EN, VDD, GL	-2	+2	kV
		GH, FS, SH	-1	+1	kV
	machine model	all pins	-250	+250	V
Latch up					
	SNW-FQ-303	all pins			

10. Thermal characteristics

Table 5: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; SO24 package	80	K/W
		in free air; SSOP24 package	111	K/W

11. Characteristics

Table 6: Characteristics

T_{amb} = 25 °C; V_{VDD} = 12 V; R_{IREF} = 33 kΩ; V_{EN}=V_{VDD} and CPWM connected to a capacitor, unless otherwise specified. All voltages are measured with respect to signal ground (SGND, pin 10). SGND and PGND connected together.Currents are positive when flowing into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High voltage						
$I_{leakage}$	leakage current high voltage pins	V_{FS}, V_{GH}, and V_{SH} = 630 V; V_{VDD} = 0 V			5	µA
Start-up						
$V_{VDD(start)}$	VDD start-up voltage		11.7	12.1	12.5	V
$V_{VDD(stop)}$	VDD stop voltage		9.8	10.1	10.4	V
$V_{VDD(hys)}$	VDD start-stop hysteresis		1.8	2	2.2	V
$I_{VDD(start)}$	VDD start-up current	V_{VDD}=11V (non-oscillating)	0.13	0.16	0.19	mA
$V_{VDD(clamp,min)}$	VDD clamp voltage	EN pin grounded, I_{VDD} = 0.19mA	11			V
$V_{VDD(clamp)}$	VDD clamp voltage	EN pin grounded, I_{VDD} = 3mA	12.1		14.0	V
$V_{VDD(clamp)}$	VDD clamp voltage	EN pin grounded, I_{VDD} = 5 mA	12.5			V
Ignition						
$F_{s(max)}$ / $F_{s(min)}$	VCO frequency ratio		2.2	2.4	2.6	
$V_{CVFB(range)}$	VCO voltage range			2.5		V
$I_{CVFB(charge)}$	CVFB charge current	V_{VFB}=2V, V_{CVFB}=2V	-24	-21	-18	µA
$V_{IFB(lampon)}$	lamp on detection level			1.1		V
Normal operation						

Table 6: Characteristics *...continued*

T_{amb} = 25 °C; V_{VDD} = 12 V; R_{IREF} = 33 kΩ; V_{EN}=V_{VDD} and CPWM connected to a capacitor, unless otherwise specified. All voltages are measured with respect to signal ground (SGND, pin 10). SGND and PGND connected together.Currents are positive when flowing into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{supply}	supply current on pin VDD	oscillating at $F_{s(min)}$, C_{CF} = 100 pF	[3]	1.2	1.5	1.8	mA
$F_{s(min)}$	minimum switching frequency	C_{CF} = 100 pF	[4]	40.0	42.0	44.0	kHz
$F_{s(min)}$	minimum switching frequency		[4]	10		100	kHz
$V_{IFB(reg)}$	current regulation reference level			1.20	1.25	1.30	V
$V_{IFB(min)}$	minimum voltage of linear operating range				- 2.5		V
$V_{IFB(max)}$	maximum voltage of linear operating range				2.5		V
R_{IFB}	input impedance IFB pin	V_{IFB} = 1V			45		kΩ
R_{IFB}	input impedance IFB pin	V_{IFB} = -1V			24		kΩ
K_{IFB}	transconductance OTA			14	16.5	19	µA/V
Drivers							
$I_{driver(source)}$	sourcing current of drivers	V_{GL}, V_{GH} = 4V, V_{VDD} = V_{FS} =12V		-105	-90	-75	mA
$R_{driver(sink)}$	sinking resistance of drivers	V_{GL}, V_{GH} = 2V, V_{VDD} = V_{FS} =12V		13.5	16.0	18.5	Ω
T_{nonov}	non-overlap time			1.1	1.3	1.5	µs
V_{boot}	voltage drop bootstrap diode	I_{FS} = 5mA			1.5		V
PWM dimming							
$I_{supply(PWMoff)}$	supply current on pin VDD during drivers off period	C_{CF} = 100 pF, V_{PWMd}=0V, V_{CSWP}=0V		0.8	1.0	1.2	mA
$T_{PWM(delay)}$	PWM enable delay time			3	4	5	ms
F_{PWM}	PWM frequency			100		1000	Hz
F_{PWM}	PWM frequency	C_{CPWM} = 33 nF		308	324	340	Hz
$I_{CSWP(charge)}$	CSWP charge current	PWMd low, V_{CSWP} = 1V		-24	-21	-18	µA
$I_{CSWP(discharge)}$	CSWP discharge current	PWMd high, V_{CSWP} = 1V		18	21	24	µA
R_{PWMa}	input impedance PWMa pin				100		kΩ
$V_{PWMa(min)}$	input voltage on PWMa pin for minimum PWM duty cycle				1.24		V
$V_{PWMa(max)}$	input voltage on PWMa pin for maximum PWM duty cycle				3		V
$D_{PWM(min)}$	minimum PWM duty cycle		[5]		12		%
$D_{PWM(min)}$	minimum PWM duty cycle	CPWM pin connected to SGND	[5]		0		%
$D_{PWM(max)}$	maximum PWM duty cycle		[5]		100		%
$I_{PWMD(source)}$	source capability PWMd output	V_{PWMD}=3V			-1		mA
$I_{PWMD(sink)}$	sink capability PWMd output	V_{PWMD}=1V			1		mA
$V_{PWMD(high)}$	logic high input level on PWMd					1.7	V
$V_{PWMD(low)}$	logic low input level on PWMd			0.85			V
Communication (COMM-pin)							
$V_{CLK(low)}$	Clock low voltage	I_{COMM}=10µA		0	0.1	0.2	V
$I_{CLK(low)}$	Clock low sink capability	V_{COMM}=1.5V		2.6	3.3	4.0	mA

Table 6: Characteristics *...continued*

T_{amb} = 25 °C; V_{VDD} = 12 V; R_{IREF} = 33 kΩ; V_{EN}=V_{VDD} and CPWM connected to a capacitor, unless otherwise specified. All voltages are measured with respect to signal ground (SGND, pin 10). SGND and PGND connected together.Currents are positive when flowing into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CLK(high)}$	Clock high voltage	I_{COMM}=-10µA	4	4.3	4.6	V
$I_{CLK(high)}$	Clock high drive capability	V_{COMM}=2.5V	-4.0	-3.3	-2.6	mA
$V_{COMM(off)}$	Voltage on COMM pin telling slave driver IC to turn both half bridge switches off	PWMd=high		12		V
$I_{HSDslave(ref)}$	input trigger current of COMM pin	Clock=high, PWMd=low	-24	-30	-36	µA
Protections						
$V_{VFB(os)}$	VFB open/short detection level			100		mV
$V_{VFB(ovref)}$	over voltage reference level		2.40	2.50	2.60	V
$I_{CVFB(discharge)}$	CVFB discharge current	V_{VFB}<$V_{VFB(os)}$ or V_{VFB}>$V_{VFB(ovref)}$ VCVFB=2V	18	21	24	µA
$V_{VFB(ovextra)}$	over voltage extra level		2.9	3.0	3.1	V
$V_{IFB(os)}$	IFB open/short detection level			0.25		V
$V_{IFB(ocref)}$	over current reference level		2.65	3.0	3.3	V
$V_{HS(thresshold)}$	hard-switching detection level			56		V
$I_{CVFB(hs)}$	CVFB discharge current	hard switching detected, V_{CVFB}=2V	36	41	46	µA
$V_{IFB(arcref)}$	minimum detectable arcing spike amplitude			5		V
$T_{SPIKE(min)}$	minimum detectable arcing spike duration			200		ns
$T_{fault(delay)}$	fault output delay time	C_{CT} = 100 nF	0.063	0.069	0.075	s
$T_{fault(stop)}$	fault stop time	C_{CT} = 100 nF	0.88	1.00	1.12	s
$V_{nonFAULT(open)}$	open pin voltage on nonFAULT		4.7	5.0	5.3	V
$V_{nonFAULT(trigger)}$	input trigger voltage on pin nonFAULT		3.8	4.3	4.8	V
$I_{nonFAULT(trigger)}$	input trigger current of nonFAULT pin		-32	-27	-22	µA
$I_{nonFAULT(3V)}$	low input nonFAULT pin current	$V_{nonFAULT}$ = 3V	-220	-190	-160	µA
$I_{nonFAULT(short)}$	short circuit current on pin nonFAULT	$V_{nonFAULT}$ = 0V	-240	-205	-170	µA
$I_{nonFAULT(sink)}$	maximum low output current on pin nonFAULT	$V_{nonFAULT}$ = 1V	0.75	1	1.5	mA
Chip enable levels						
$V_{EN(high)}$	logic high level on pin EN				1.7	V
$V_{EN(low)}$	logic low level on pin EN		0.9			V

[3] GL and GH open.

[4] Given frequency is switching frequency of GL and GH. Sawtooth frequency on CF pin is twice as high.

[5] PWMd is active low: A low level on the PWMd pin corresponds with lamps on. Example: D_{PWM}=20% means PWMd is during 20% of each cycle low and the lamps are 20% of the time on, resulting in a light output of 20%

12. Application information

Figure 18 shows an example backlighting configuration, where the inverter is supplied from a high voltage DC source and the IC is supplied by means of a dV/dt supply (C8, C10, Z1 and D1). Two lamp are connected, each to the output of its own transformer. The leakage inductance of this transformer provides the ballast impedance for the lamp. An analogue voltage is converted to a PWM signal to provide for the desired brightness level. Lamp short detection is done via the lamp voltage sensing and D13, D23 and the nonFAULT pin.

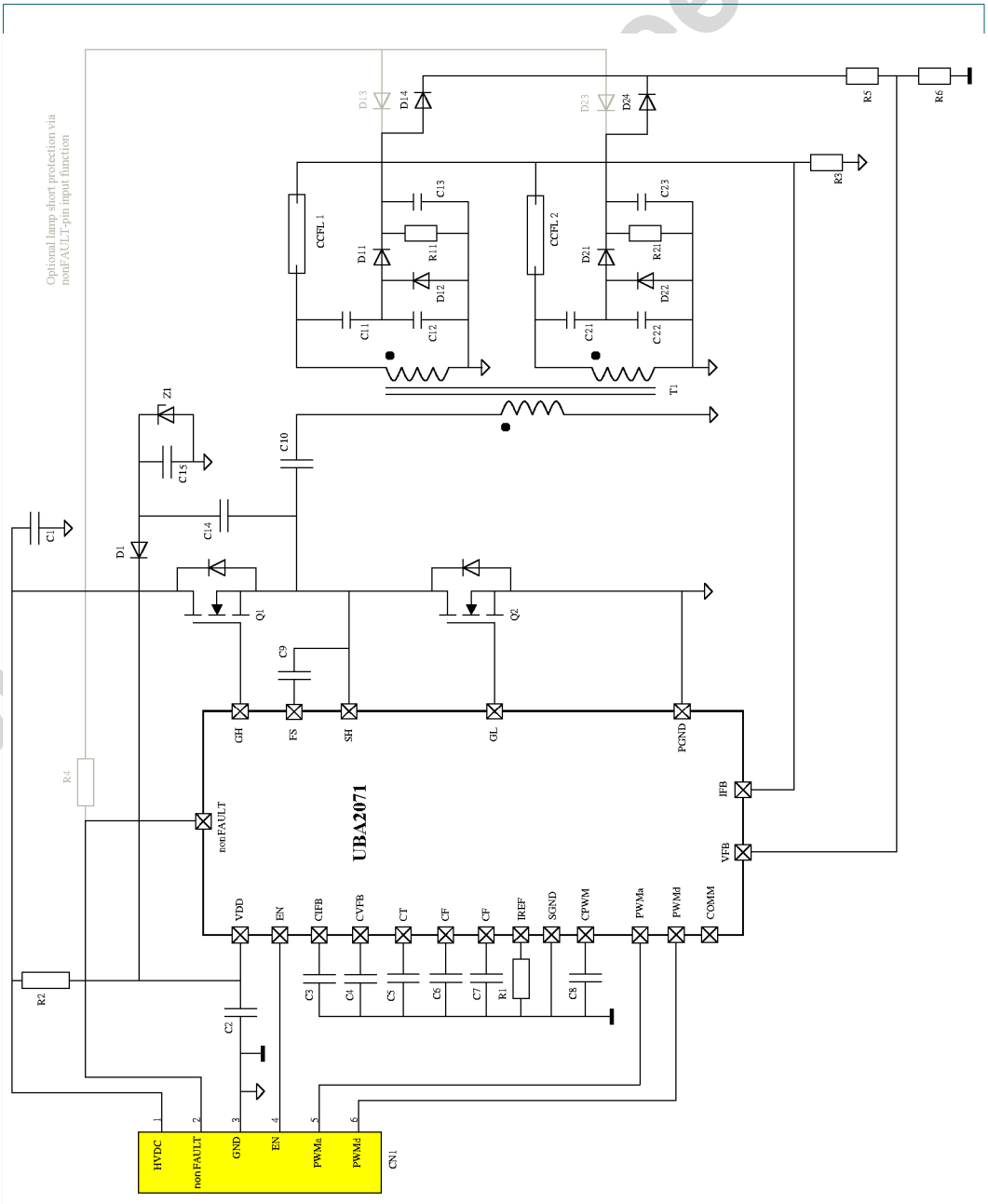


Fig 18. Example of single IC backlighting application

Figure 19 shows an example of a balanced application using one UBA2071 and one UBA2073.

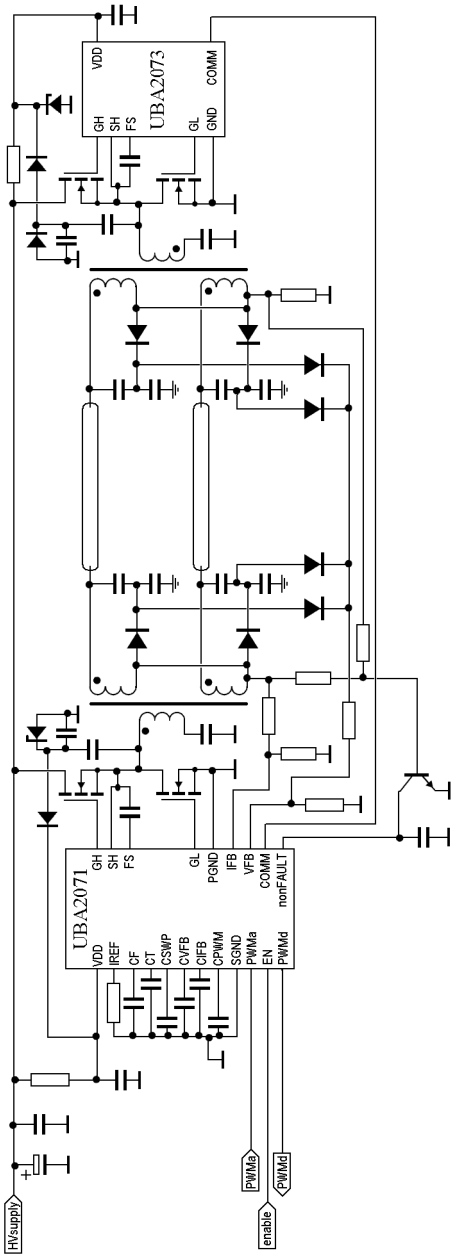


Fig 19. Example of balanced backlighting application

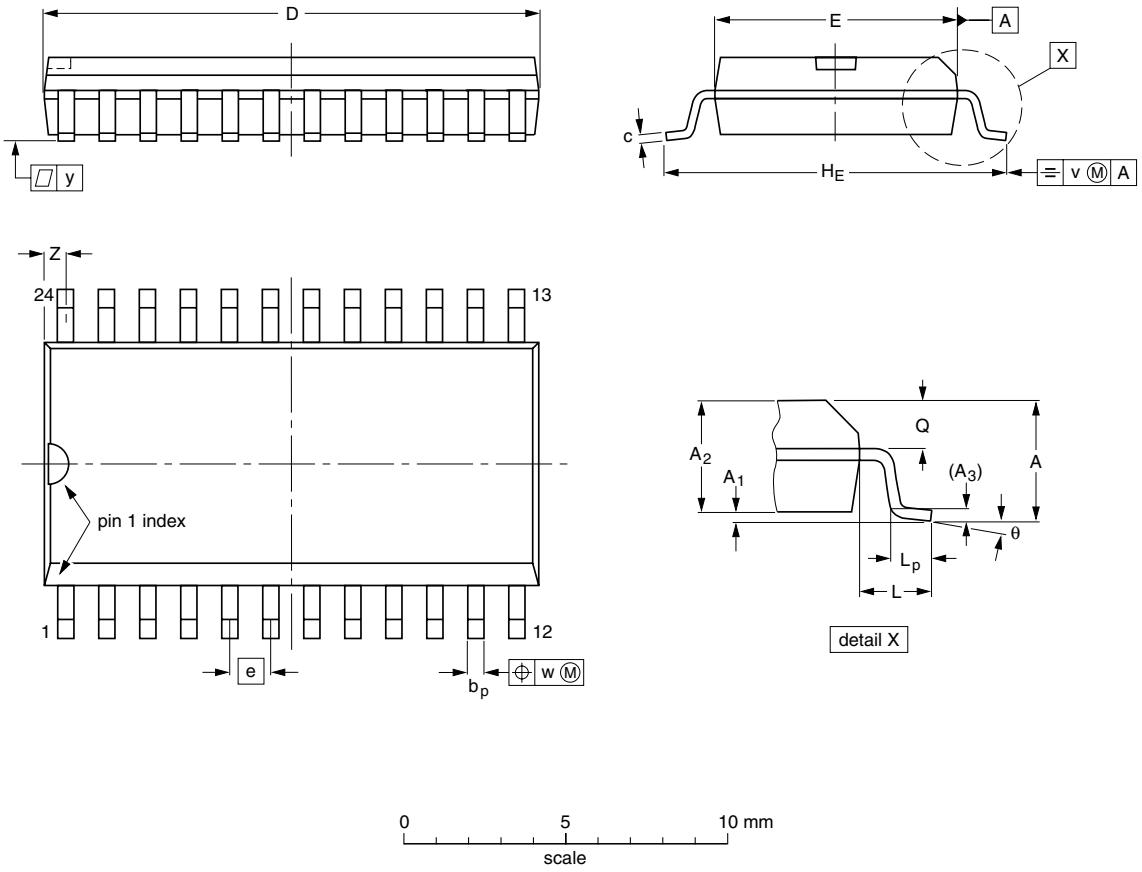
13. Test information

13.1 Quality information

The *General Quality Specification for Integrated Circuits, SNW-FQ-611* is applicable.

14. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

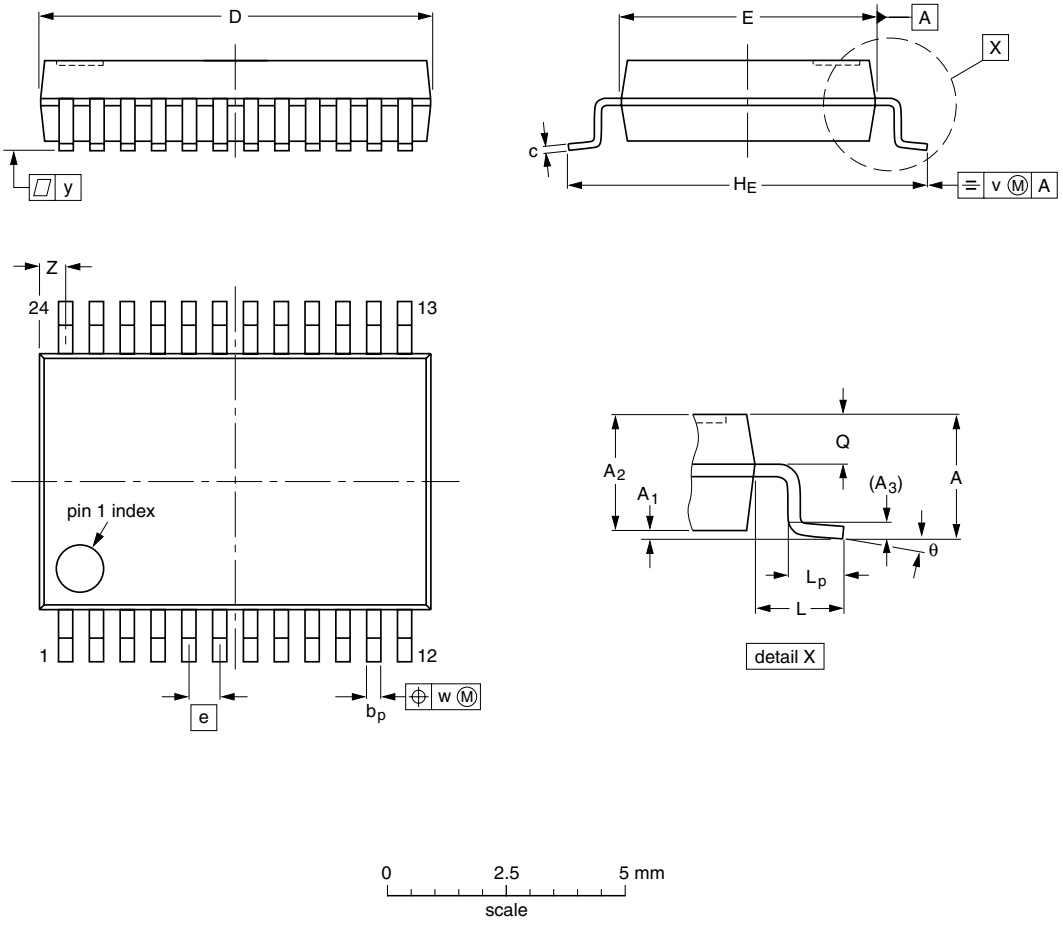
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 20. Package outline SO24 (SOT137-1)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

Fig 21. Package outline SSOP24 (SOT340-1)

15. Soldering

15.1 Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

15.2 Through-hole mount packages

15.2.1 Soldering by dipping or by solder wave

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

15.2.2 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

15.3 Surface mount packages

15.3.1 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all the BGA and SSOP-T packages

- for packages with a thickness ≥ 2.5 mm
- for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.

- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

15.3.2 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.3.3 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

15.4 Package related soldering information

Table 7: Suitability of IC packages for wave, reflow and dipping soldering methods

Mounting	Package[1]	Soldering method		
		Wave	Reflow[2]	Dipping
Through-hole mount	DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable[3]	–	suitable
Through-hole-surface mount	PMFP[4]	not suitable	not suitable	–
Surface mount	BGA, LBGA, LFBGA, SQFP, SSOP-T[5], TFBGA, VFBGA	not suitable	suitable	–
	DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[6]	suitable	–
	PLCC[7], SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended[7][8]	suitable	–
	SSOP, TSSOP, VSO, VSSOP	not recommended[9]	suitable	–

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[4] Hot bar soldering or manual soldering is suitable for PMFP packages.

[5] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[6] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[7] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[8] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[9] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

16. Revision history

Table 8: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
UBA2071_1	2005 07	Objective data	-	xxxx xxx xxxxx	-
UBA2071_2	2006 10	Objective data	-	xxxx xxx xxxxx	-
UBA2071_3	2007 03	Objective data	-	xxxx xxx xxxxx	-
UBA2071_4	2007 06	Objective data	-		

17. Legal information

17.1 Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

18. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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