Green mode PFC/Flyback-PWM Controller **SG6905**

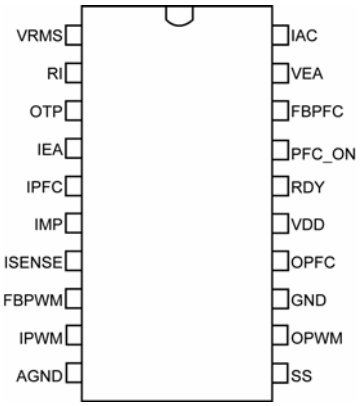
ABSTRACT

This application note shows a step-by-step design for a 300W power factor correction circuit. The equations also can be used for different output voltages and wattages.

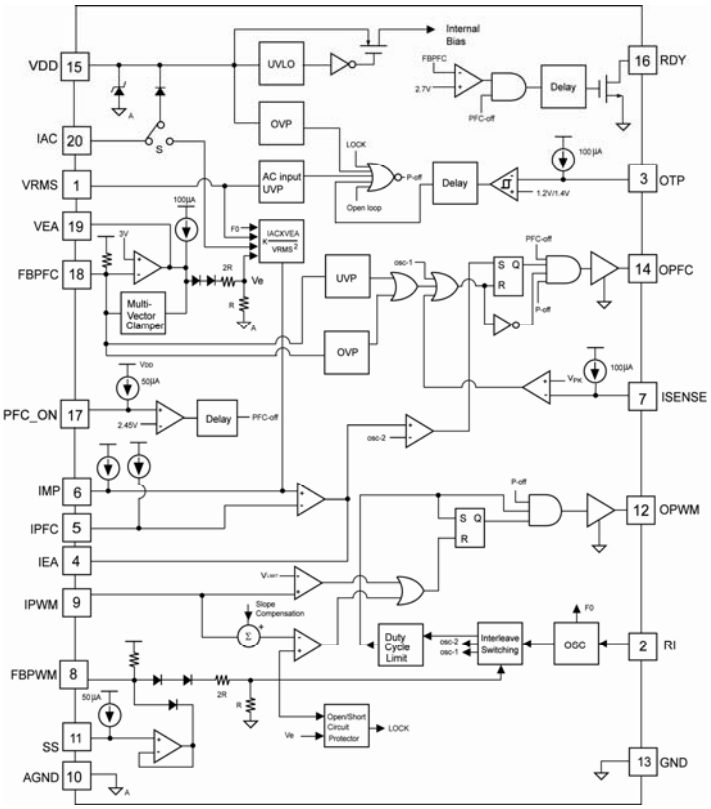
FEATURES OVERVIEW

- Interleaved PFC/PWM switching
- Green mode PWM operation
- Low start-up and operating current
- Innovative Switching-Charge® multiplier/divider
- Multi-vector control for improved PFC output transient response
- Average-current-mode control for PFC
- PFC over-voltage and under-voltage protections
- PFC remote on/off control
- PFC and PWM feedback open-loop protection
- Cycle-by-cycle current limiting for PFC/PWM
- Slope compensation for PWM
- Constant power limit for PWM
- Power-on sequence control
- Brownout protection
- Over-temperature protection

PIN CONFIGURATION



BLOCK DIAGRAM



DESCRIPTION

The highly integrated SG6905 has been especially designed for power supplies consisting of boost PFC and flyback PWM. It requires very few external components to achieve versatile protections. It is available in a 20-pin SOP package.

The patented interleave-switching feature synchronizes the PFC and PWM stages and reduces switching noise.

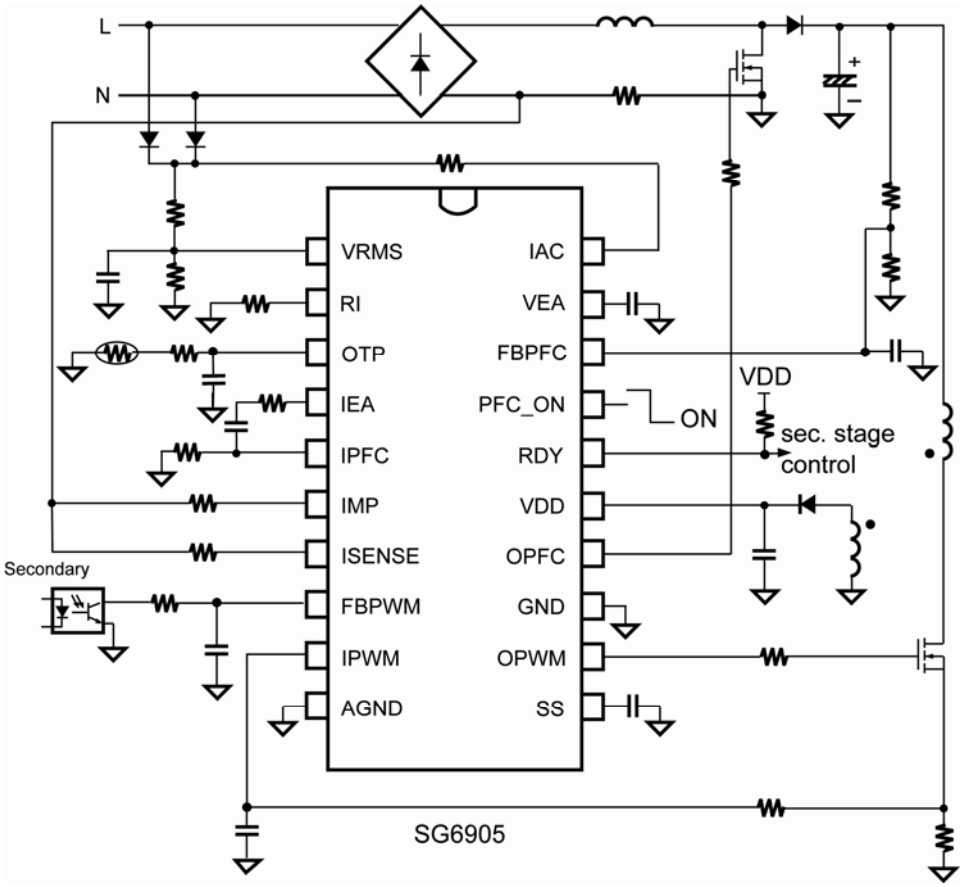
In the PFC stage, the proprietary multi-vector control scheme provides a fast transient response in a low-bandwidth PFC loop, in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, the SG6905 will shut the PFC off to prevent extra-high voltage on output.

In the flyback PWM, the synchronized slope compensation ensures the stability of the current loop during the continuous-conduction-mode operation. Built-in line-voltage compensation maintains a constant output power limit. Hiccup operation during output overloading is also guaranteed.

During startup, the RDY pin will be pulled low until the PFC output voltage reaches the setting level. This signal can be used to control the second power stage for proper power-on sequencing.

In addition, SG6905 provides complete protection functions, such as brownout protection and R_I pin open/short.

TYPICAL APPLICATION



PFC SECTION

SG6905 Power-On Sequence

SG6905 becomes active once the line voltage surpasses the brownout threshold. The PWM stage first switches; following an 11mS delay after FBPWM during which the voltage increases beyond the threshold voltage V_{TH}, the PFC stage is subsequently enabled.

PFC inductor

The switching frequency fs, the output power P_{out}, the efficiency η, maximum ripple current ΔI, and the minimum input voltage $V_{in.min}$ should be defined before determining the inductance the of PFC inductor. The following equations are utilized to determine the inductance of the PFC inductor. Normally, the maximum ripple current is set at 20~30% of maximum input current.

$$\Delta I = \frac{\sqrt{2} \times (P_{out} / \eta) \times 0.3}{V_{in.\min}} \quad \text{---------- (1)}$$

$$D = 1 - \frac{V_{in.\min} \times \sqrt{2}}{V_O} \quad \text{---------- (2)}$$

$$V = L\frac{di}{dt} \quad \text{---------- (3)}$$

$$L = \frac{V_{in.\min} \times \sqrt{2} \times D_{\max} / f_s}{\Delta I} \quad \text{---------- (4)}$$

For a 300W power factor correction circuit, η=0.75, $V_{in.min}$=90V_{AC}, f_s=65KHz, V_o=390V

ΔI=1.89A, D=0.674, and L=700 μH

PFC capacitor

One advantage of using interleaving switching in the PFC and PWM stages is that it reduces the switching noise. The ESR requirement for boost capacitor is also reduced.

The boost capacitor value is chosen to remain at the hold-up time of output voltage in the event that the line voltage is removed.

$$C_o > \frac{2 \times (P_{out} / \eta_{PWM}) \times T_{hold-up}}{(V_{o(normal)} - V_{ripple})^2 - V_{o.\min}{}^2} \quad \text{----- (5)}$$

$V_{O.min}$ represents the minimum output voltage in accordance with the requirement of the specification.

For a 300W power supply, the capacitor is determined as follows

$$C_O > \frac{2 \times (300W / 0.85) \times 28mS}{(390 - 20)^2 - 90^2} = 153uF$$

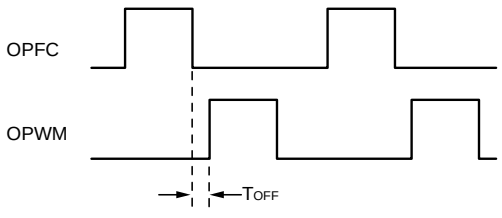


Fig. 1 Interleaving Switching

Because the capacitor includes a ±20% variation, the 180uF capacitor has been chosen.

Boost rectifier and switch

A fast reverse-recovery time of the boost diode is required to reduce the power losses and the EMI. In addition, a 500V voltage rating has been chosen in order to withstand 390V boosts potential. The average current and peak current flow through the boost diode and switch, respectively, are determined by:

$$I_{avg} = \frac{2 \times \sqrt{2} \times P_{out} / \eta}{\pi \times V_{RMS(Brownout)}} \quad \text{---------- (6)}$$

$$I_{avg} = \frac{2 \times \sqrt{2} \times 300 / 0.7}{\pi \times 75} = 5.15A$$

$$I_{peak} = \sqrt{2} \times \frac{P_{out} / \eta}{V_{RMS(Brownout)}} \quad \text{---------- (7)}$$

$$I_{peak} = \sqrt{2} \times \frac{300 / 0.7}{75} = 8.08A$$

Oscillator and Green Mode Operation

The resistor R_I connected from the R_I pin to GND programs the switching frequency of SG6905.

$$f_S = \frac{1560}{R_I(K\Omega)}(KHz) \quad \text{---------- (8)}$$

For example, a 24kΩ resistor R_I results in a 65 kHz switching frequency. The recommended range for the switching frequency of SG6905 is 33~100kHz.

SG6905 provides an off-time modulation to reduce the switching frequency in light-load and no-load conditions. The feedback voltage of the FBPWM pin can be used as a reference. When the feedback voltage falls below approximately 2.0V, the switching frequency will decrease accordingly. Most of the losses in the switching mode power supply are proportional to the switching frequency. Therefore, the off-time modulation of SG6905 will reduce the power consumption of the power supply in light-load and no-load conditions. For a typical case in which R_I = 24KΩ, the switching frequency is 65kHz at the nominal load, which decreases to 21kHz at the light load. The switching signal will be disabled if the switching frequency falls below 21kHz, thereby avoiding acoustic noises. The function to reduce the PWM stage switching frequency is enabled when the PFC stage does not work. After the PFC stage resumes working, the function to reduce the PWM stage switching frequency is disabled.

Due to stability issues, a capacitor connecting the R_I pin to GND is not suggested.

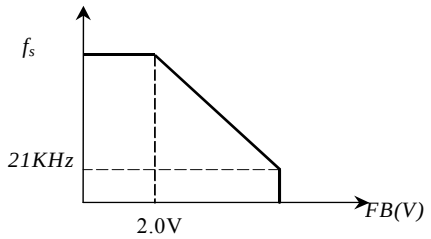


Fig. 2 Switch frequency versus FB voltage

I_{AC} signal

Figure 3 shows that the I_{AC} pin is connected to the input voltage via a resistor. A current I_{AC} is used for the PFC multiplier.

$$I_{AC(peak)} \approx \frac{V_{in(peak)}}{R_{AC}} \quad \text{---------- (9)}$$

For wide range input,

$$V_{in(peak)} = 264V \times \sqrt{2} = 374V$$

The linear range of I_{AC} is 0~360uA. A 1.2M resistor is suggested for a wide input range (90~264VAC).

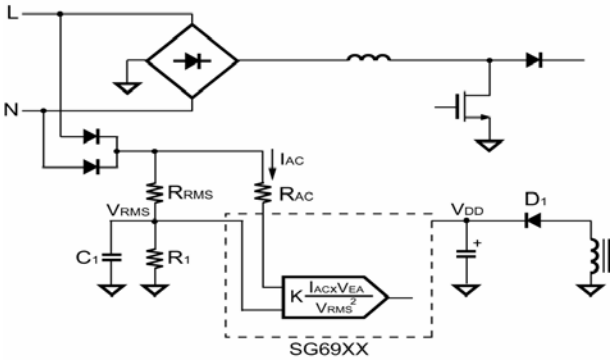


Fig. 3 The I_{AC} signal

Line Voltage Detection (V_{RMS})

Figure 3 also indicates the resistive divider from a low-pass filter connected to the V_{RMS} pin for line-voltage detection. The V_{RMS} input is used for the PFC multiplier and brownout protection.

For a sine wave input voltage, the voltage on the V_{RMS} pin is directly proportional to the input voltage. In order to achieve brownout protection, SG6905's PFC stage is disabled after a 195mS time delay once the V_{RMS} voltage drops below 0.8V. The PWM stage will be protected through the open loop detection on the FBPWM pin when the PFC stage's output voltage is too low. After that, SG6905 will turn off. When the V_{RMS} voltage increases above 0.99V, SG6905 restarts in accordance with power on sequence of the PFC and PWM stages.

For example, brownout protection is set at 75VAC. The R_{RMS} and R_1 can be determined as follows:

$$V_{in(Mean)} = V_{in} \times \sqrt{2} \times \frac{2}{\pi} \quad \text{---------- (10)}$$

$$V_{RMS} = \frac{R_1}{R_1 + R_{RMS}} \times V_{in} \times \sqrt{2} \times \frac{2}{\pi} \quad \text{----------(11)}$$

The threshold of V_{RMS}=0.8V; assuming that R_{RMS}=4.8MΩ and V_{in}=75V_{AC}, the value of R_1 will be 56.8KΩ.

PFC Operation

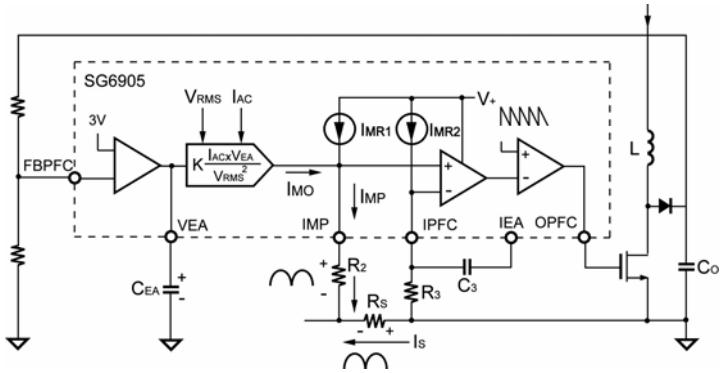


Fig. 4 Current feedback circuit

The current output from the Switching Charge® multiplier/divider can be expressed as:

$$I_{MO} = K \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^{\ 2}} (uA) \quad \text{---------- (12)}$$

Referring to Figure 4, the current output from the IMP pin, I_{MP}, is the summation of I_{MO} and I_{MR1}. The resistor R_2 is equipped similarly as R_3. The constant current source I_{MR1} is identical to I_{MR2}. Both are used to bias (pull up) the operating point of the I_{MP} and IPFC pins since the voltage across R_S goes negative with respect to the ground.

Through the differential amplification of the signal across R_S, a better noise immunity is achieved. The output of IEA compared with an internal sawtooth generates a switching signal for PFC. Through the feedback loop of the average current mode control, the input current I_S is proportional to I_{MO},

$$I_{MO} \times R_2 = I_S \times R_S \quad \text{---------- (13)}$$

According to equation 13, the minimum value of R_2 and maximum value of R_S can be determined. The I_{MO} should be estimated under its specified maximum value.

Other concerns in determining the value of the sense resistor R_S are the lower resistance, R_S will cause a lower power consumption for higher resistance, and R_S has a higher resolution for achieving a lower THD (total harmonic distortion) of the input current. Using a current transformer (CT) is recommended instead of R_S to improve the efficiency of high power converters.

For a 300W power supply, the power consumption of R_S=0.1Ω is :

$$P_{RS} = (\frac{300W / 0.75}{90})^2 \times 0.1 = 1.98W \quad \text{---------- (14)}$$

R_2 and R_3 can be determined as follows: (The brownout protection threshold is 75V)

$$I_{MAX} = \frac{300W / 0.7}{75V} * \sqrt{2} = 8.08A \quad \text{----------(15)}$$

$$V_{IPFC} = I_{MR2} * R3 = 50uA * 3.9Kohm = 0.195V \quad \text{----------(16)}$$

$$I_{MO} + I_{MR1} = \frac{0.195 - (-8.08A * 0.1ohm)}{3.9Kohm} = 257uA \quad \text{----------(17)}$$

$$I_{MO} = 257 - 50 = 207uA$$

The results indicate that R_S, R_2, and R_3 values fit when providing 300W output.

Cycle-by-cycle Current Limiting

SG6905 provides cycle-by-cycle current limiting for both PFC and PWM stages. Figure 5 shows the peak current limit for the PFC stage. The switching signal of the PFC stage will be turned off immediately once the voltage on the I_{SENSE} pin goes below the threshold voltage V+.

The voltage of V_{RMS} determines the threshold voltage V+. The correlation of the threshold voltage V+ and V_{RMS} is shown in Figure 5. The amplitude of the constant current I_P shown in Figure 5 is determined by a reference current I_T, in accordance with the following equation:

$$I_P = 2 \times I_T = 2 \times \frac{1.2V}{R_I} \quad \text{---------- (18)}$$

Therefore the peak current of I_S can be expressed as:

$$I_{S\_PEAK} = \frac{(I_P \times R_P) - 0.2V}{R_S} \quad \text{---------- (19)}$$

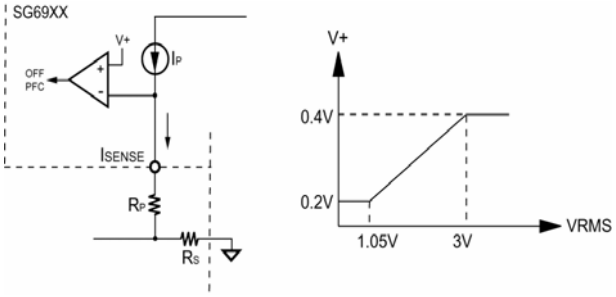


Fig. 5 Current limit

Multi-vector Error Amplifier

To achieve a good power factor, the voltage for V_{RMS} and V_{EA} should be kept as a DC-value according to equation 12. In other words, a low-pass RC filtering for V_{RMS} and a narrow bandwidth (lower than the line frequency) of the PFC voltage loop are suggested to achieve better input current shaping. The trans-conductance error amplifier has the output impedance R_O (>90kΩ). A capacitor C_{EA} (1~10uF) is suggested for connecting from the output of the error amplifier to the ground (Fig. 6). A dominant pole f_1 of the PFC voltage loop is shown as:

$$f_1 = \frac{1}{2\pi \times R_O \times C_{EA}} \quad \text{---------- (20)}$$

The average total input power can be expressed as:

$$P_{in} = V_{in(RMS)} \times I_{in(RMS)}$$

$$\propto V_{RMS} \times I_{MO}$$

$$\propto V_{RMS} \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^{\ 2}}$$

$$\propto V_{RMS} \times \frac{\frac{Vin}{R_{AC}} \times V_{EA}}{V_{RMS}^{\ 2}} \propto V_{EA} \quad \text{---------- (21)}$$

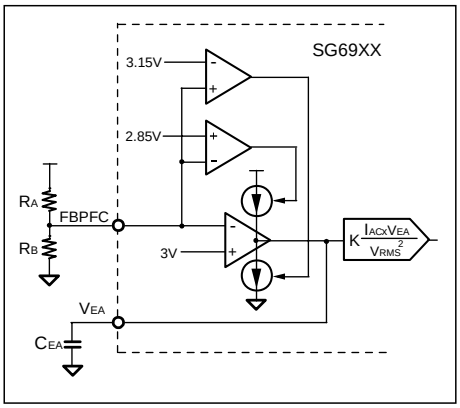


Fig. 6 Multi-vector Error Amp

Equation 21 demonstrates that the output of the voltage error amplifier, V_{EA}, controls the total input power and the power delivered to the load.

Although the PFC stage includes a low bandwidth loop to reach a better power factor, the innovated multi-vector error amplifier provides a fast transient response to clamp the overshoot and undershoot of the PFC output voltage.

Figure 6 shows the block diagram of the multi-vector error amplifier. When the variation of the feedback voltage (FBPFC) exceeds ±5% of the reference voltage (3V), the trans-conductance error amplifier will program its output current to speed up the loop response. If R_A is an open circuit, SG6905 will immediately turn off to prevent over-voltage on the output capacitor.

The resistor divider ratio R_A/R_B is determined by:

$$\frac{R_A}{R_B} = \frac{Vo}{3} - 1 \qquad \text{----------(22)}$$

$$\frac{R_A}{R_B} = \frac{390}{3} - 1 = 129$$

Assuming that R_A is 3Mohm and R_B=23.2Kohm, the output voltage is clamped at:

$$V_o(\max) = 3.15 * (\frac{R_A}{R_B} + 1) = 410V$$

In addition, another circuit provides a further over-voltage protection to inhibit the PFC from switching once the feedback voltage exceeds 3.25V:

$$V_{o_{(OVP)}} = 3.25 * (\frac{R_A}{R_B} + 1) = 423V$$

PFC On/Off

PFC_ON controls the PFC stage whether it works normally or not. The PFC stage is disabled when the voltage of PFC_ON surpasses 2.45V. The PFC stage remains active while the voltage of PFC_ON is low. At this point, OPFC can work normally, and the RDY pin will pull high.

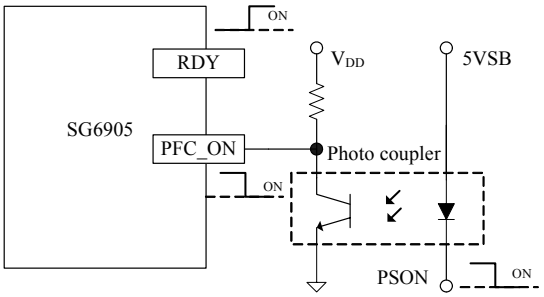


Fig. 7 PFC_ON pin application

RDY pin application

The state of RDY is determined by the PFC_ON pin and the FBPFC pin. The RDY pin rises to high when PFC_ON pulls low and the voltage of the FBPFC pin is higher than 2.7V. SG6905 can enable other PWM IC to work or not according to the RDY signal.

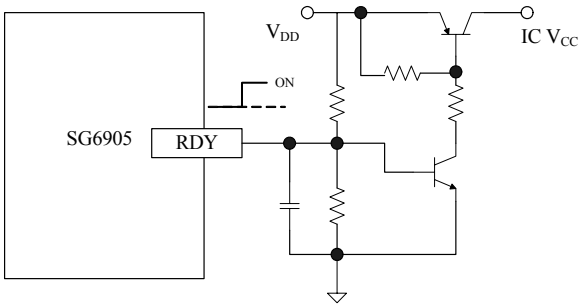


Fig. 8 RDY pin application

PWM SECTION

Soft start of the PWM stage

The soft-start pin has been developed to control the rising time of the output voltage and to prevent the overshoot during power on. The soft-start capacitor value for the soft-start period t_{SS} is given by:

$$C_{SS} = t_{SS} \times \frac{I_{SS}}{V_{OZ}} \quad \text{---------- (23)}$$

Where V_{OZ} represents the zero-duty threshold of FBPWM voltage.

Leading Edge Blanking

A voltage signal develops on the current sense resistor R_S to represent the switching current of MOSFET. Each time the MOSFET is turned on, a spike is produced, caused by the diode reverse recovery time and the parasitic capacitances of the MOSFET, and inevitably appears on the sensed signal. SG6905 has a built-in leading edge blanking time of about 120nsec to avoid premature termination of MOSFET by the spike. Therefore, only a small-value RC filter (e.g., 100ohm + 47pF) is required between the IPWM pin and R_S to prevent negative spike into the IPWM pin. A non-inductive resistor for R_S is recommended.

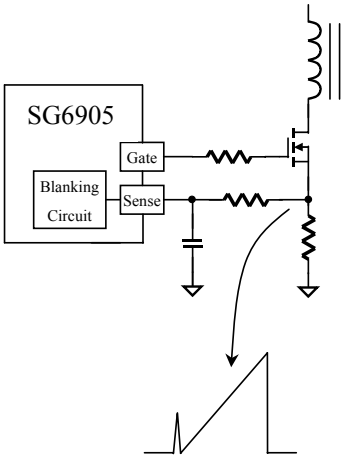


Fig. 9 Turn on

Flyback PWM and Slope Compensation

As shown in Figure 10, peak-current-mode control is utilized for Flyback PWM. SG6905 inserts a synchronized ramp at the beginning of each switching cycle. This built-in slope compensation ensures the stable operation for continuous current-mode operation.

When the IPWM voltage, across the sense resistor, reaches the threshold voltage (0.9V), the OPWM will be turned off after a small propagation delay, t_{PD-PWM}.

To improve stability or prevent sub-harmonic oscillation, a synchronized positive-going ramp is inserted at every switching cycle.

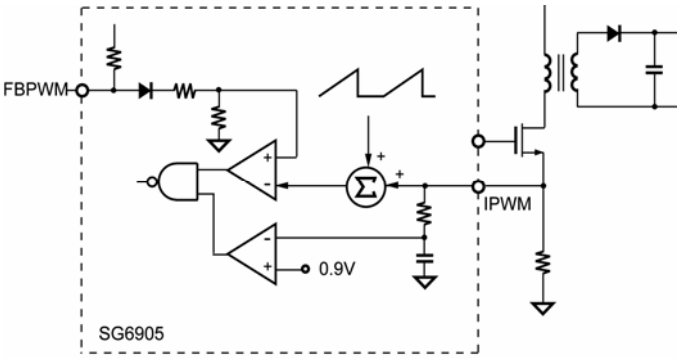


Fig. 10 Peak current control loop

Output driver of OPFC & OPWM

SG6905's OPFC and OPWM create a fast totem-pole gate driver able to directly drive external MOSFET. An internal zener diode clamps the driver voltage under 18V to protect MOSFET from over-voltage.

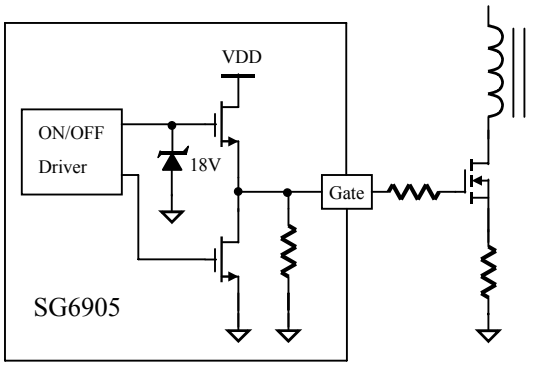


Fig.11 Gate drive

OCP & SCP

SG6905's OCP and SCP have been developed based on the detection of the feedback signal on the FBPWM pin. As shown in Figure 12, when over current or short circuit occurs, FBPWM will be pulled high through the feedback loop. If the FB voltage surpasses the 4.5V threshold for longer than the 56ms debounce time, SG6905 will be turned off. Once the V_{DD} falls below the turn-off threshold voltage, such as 10V, SG6905 will be UVLO (under voltage lockout) shut down. Using the start-up resistor, V_{DD} will be charged (up to the turn-on threshold voltage of 16V) until SG6905 is enabled again. If the over-loading condition still exists, the protection will take place repeatedly. This will prevent the power supply from being overheated during over-loading conditions. The 600ms time-out signal prevents SG6905 from being latched off when the input voltage is fast on/off.

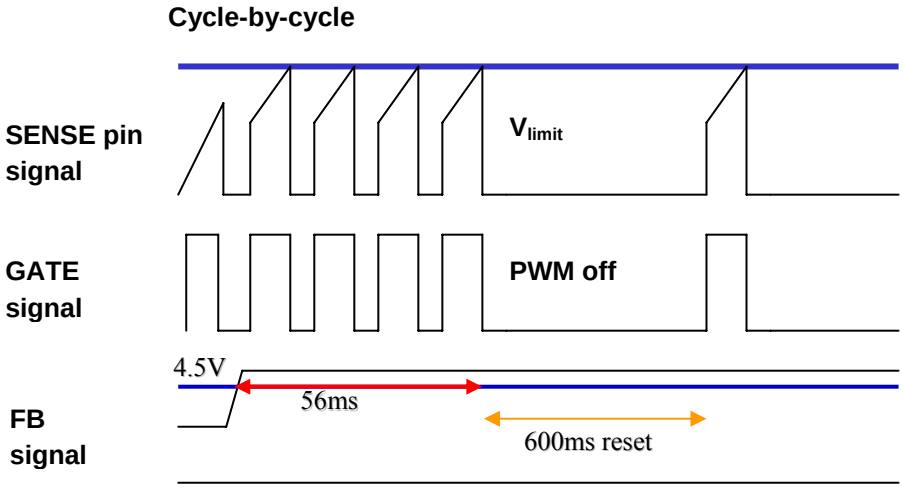


Fig. 12 OCP detection waveform

OTP

SG6905 provides an OTP pin for over-temperature protection. A constant current is outputted from this pin. When R_I equals 24kΩ, then the magnitude of the constant current will be 100uA. An external NTC thermistor must be connected from this pin to the ground, as shown in Figure 13. When the OTP voltage drops below 1.2V, SG6905 will be disabled until the OTP voltage exceeds 1.4V. Preventing OTP error caused by noise disturbance can be addressed by adding a capacitor.

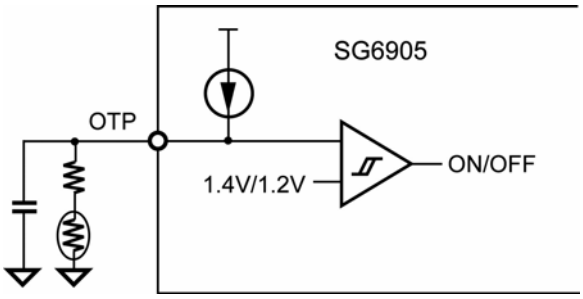


Fig. 13 OTP application circuit

Flyback transformer design

The turn ratio $n = N_P/N_S$, is an important parameter for a flyback power converter. It affects the maximum duty of the switching signal when the input voltage is at a minimum value. Moreover, it influences the voltage stresses of the MOSFET and the secondary rectifier.

In equations 24 and 25, if *n* increases, the voltage stress of the MOSFET will be increased. However, the voltage stress of the secondary rectifier will be decreased accordingly.

$$V_{DS.\max} = V_{in.\max} + n \times (V_o + V_f) \quad \text{---------- (24)}$$

$$V_{AK.\max} = \frac{V_{in.\max}}{n} + V_o \quad \text{---------- (25)}$$

Where V_f is the forward voltage of output diode $V_{in.max}$=390V.

In the maximum duty cycle and minimum input voltage at full load, the transformer inductance can be calculated as:

$$D_{\max} = \frac{n \times (V_o + V_f)}{V_{in.\min} + n \times (V_o + V_f)} \quad \text{---------- (26)}$$

$$L_p = \frac{\eta \times (V_{in.\min} \times D_{\max})^2}{2 \times P_{out} \times f_s \times Br} \quad \text{---------- (27)}$$

Where, Br is how much percentage of the output power will flow into CCM in the low line input voltage. Normally, the Br is set at 30~50% when $V_{in.min}$=90V.

Figure 13 shows the primary current waveform. Once the inductor L_p is determined, the primary peak current I_{pk} and average current I_{av} at the full load and low line input voltage can be expressed as:

$$I_{av} = \frac{P_o}{\eta \times V_{in.\min} \times D_{\max}} \quad \text{---------- (28)}$$

$$\Delta I_p = \frac{V_{in.\min}}{L_p} \times D_{\max} \times T_s \quad \text{---------- (29)}$$

$$I_{pk} = \frac{\Delta I_p}{2} + I_{av} \quad \text{---------- (30)}$$

$$I_{sq} = I_{pk} - \Delta I_p \quad \text{---------- (31)}$$

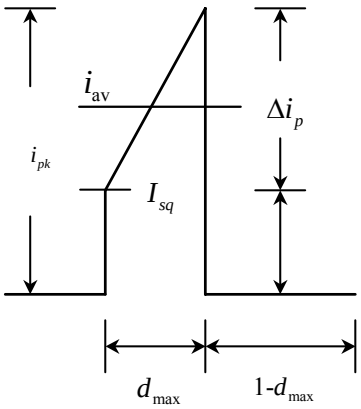


Fig. 14 Primary Current Waveform

From Faraday's law, the turns of primary side can be expressed as:

$$N_p = \frac{L_p \times I_{pk}}{B_{\max} \times A_e} \cdot 10^8 \quad \text{---------- (32)}$$

The turns of auxiliary winding can be expressed as:

$$N_{aux} = \frac{N_p \times (V_{DD} + V_{fa}) \times (1 - D_{\max})}{V_{in.\min} \times D_{\max}} \quad \text{---------- (33)}$$

where V_{DD} is set to around 12V and V_{fa} is the forward voltage of the V_{DD} rectifier diode.

Transformer winding structure

The auxiliary winding of the transformer has been developed to provide a power source (V_{DD} voltage) to the control circuit. In order to produce a regulated V_{DD} voltage, the reflected voltage of the auxiliary winding is designed to correlate to the output voltage of the secondary winding. However, a switching voltage spike caused by the leakage inductance of the primary winding can be coupled to the auxiliary winding to increase the V_{DD} voltage in response to the increase of the load.

When the V_{DD} voltage increases beyond the voltage of the over-voltage protection 24.5V, the control circuit will turn off the PWM and PFC stages to protect the power supply. Therefore, the transformer windings should prevent the auxiliary winding from primary winding interference.

Figure 15 shows a transformer winding structure, including the primary winding (N_{p1}), copper layer (shield), secondary winding (N_s), auxiliary winding (AUX), copper layer (shield), and primary winding (N_{p2}). Because the auxiliary winding is placed between the secondary and shield windings, it can alleviate the variation of V_{DD} voltage and prevent the V_{DD} voltage from reaching the over-voltage threshold 24.5V during normal operation.

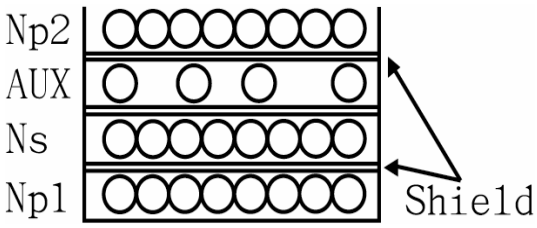


Fig. 15 Winding structure

Lab Note

Before reworking or soldering/desoldering the power supply, discharge the primary capacitors through the external bleeding resistor. Otherwise the PWM IC may be destroyed by external high voltage during soldering/desoldering.

This device is sensitive to ESD discharge. To improve production yield, the production line should be ESD protected according to ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1.

Printed Circuit Board Layout

Note that SG6905 has two ground pins. Good high-frequency or RF layout practices should be followed. Avoid long PCB traces and component leads. Locate decoupling capacitors near SG6905. A resistor (5~20Ω) is recommended for connecting the series from the OPFC and OPWM to the gate of the MOSFET.

Isolating the interference between the PFC and PWM stages is also important. Figure 16 shows an example of the PCB layout. The *ground trace* connecting the AGND pin of SG6905 to the decoupling capacitor should be low impedance and as short as possible. The *ground trace 1* provides a signal ground; it should be connected directly to the decoupling capacitor V_{DD} and/or to SG6905's AGND pin. The *ground trace* 2 shows that the AGND pins should connect to the PFC output capacitor C_O independently. The *ground trace 3* is independently tied from the GND to the PFC output capacitor C_O. The ground in the output capacitor C_O is the major ground reference for power switching. In order to provide a good ground reference and reduce the switching noise of both the PFC and PWM stages, the *ground traces 6 and 7* should be located near one another and be of minimal impedance.

The IPFC pin is connected directly to R_S through R_3 to improve noise immunity (beware that it may be incorrectly connected to the *ground trace 2*). The I_{MP} and I_{SENSE} pins should also be connected directly via the resistors R_2 and R_P to another terminal of R_S since the *ground traces 4 and 5* are PFC and PWM stages. The current loop should be as short as possible.

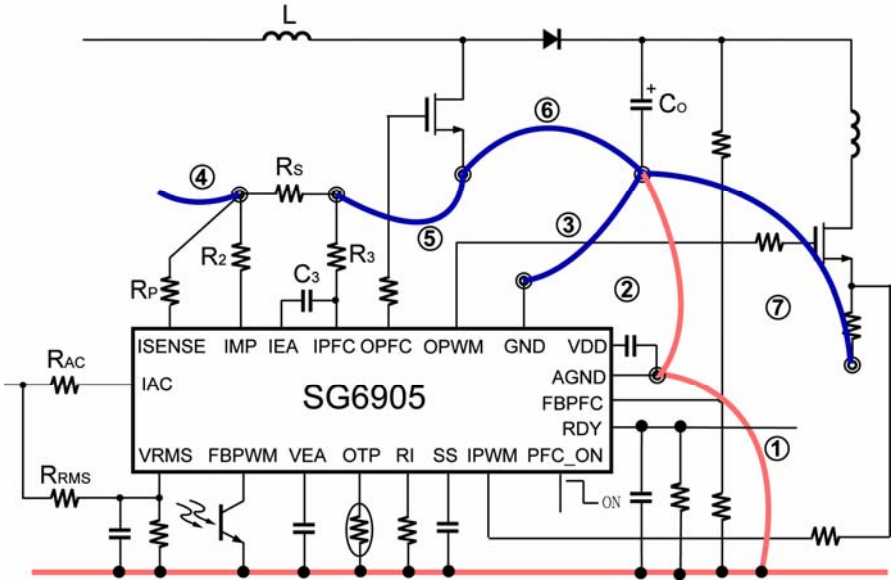


Fig. 16 PCB layout

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