PJ9910C	P.1
WIDE INPUT RANGE POWER LED DRIVER	

FEATURES

- >90% Efficiency
- 8V to 450V input range
- Constant-current LED driver
- Applications from a few mA to more than 1A output
- LED string from one to hundreds of diodes
- PWM Low-Frequency Dimming via Enable pin
- Input Voltage Surge ratings up to 450V

APPLICATIONS

- DC/DC LED driver
- Automotive
- Lighting

TYPICAL APPLICATION CIRCUIT

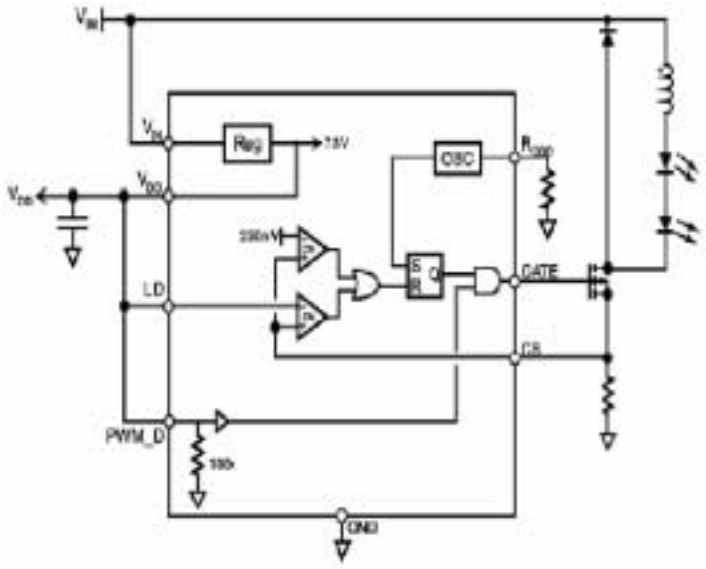
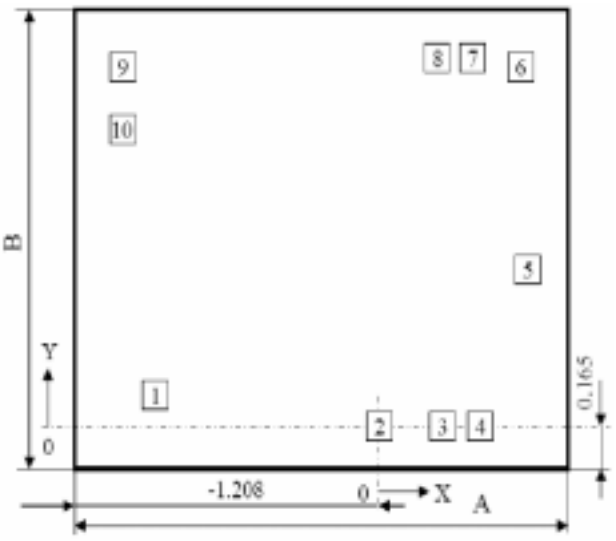


Figure 1. 8~450V Powered Driver for Two White Power LEDs

DESCRIPTION

The PJ9910C is a PWM high-efficiency LED driver control IC. It allows efficient operation of High Brightness (HB) LEDs from voltage sources ranging from 8Vdc up to 450Vdc. The PJ9910C controls an external MOSFET at fixed switching frequency up to 300 kHz. The frequency can be programmed using a single resistor. The LED string is driven at constant current rather than constant voltage, thus providing constant light output and enhanced reliability. The output current can be programmed between a few milliamperes and up to more than 1A.

PAD DIAGRAM

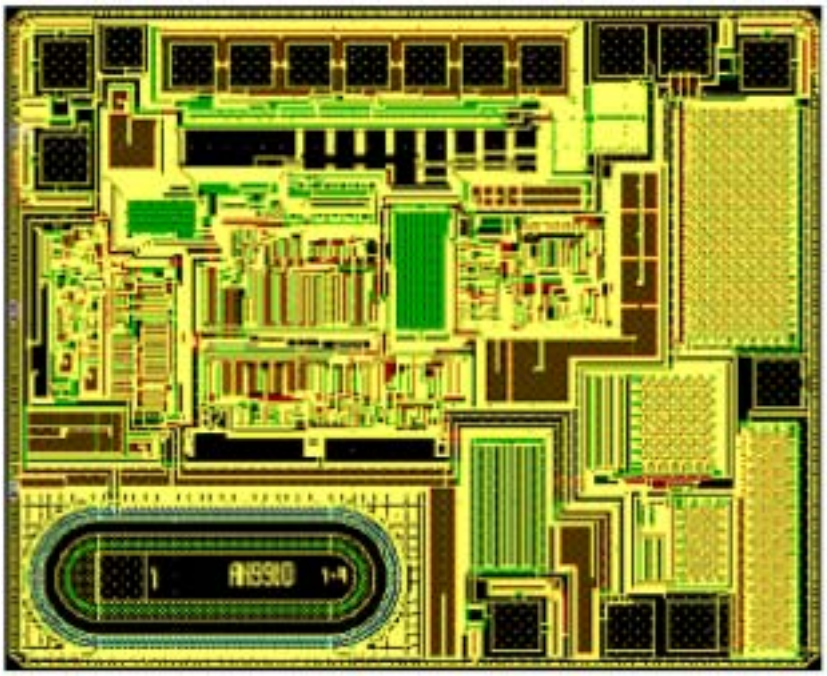


1. **Chip size: X=1.88mm, Y=1.54mm (without scribe line width).**
2. **Scribe line width: X=80µm, Y=80µm**
3. **Pad size: 100µm x 100µm**
4. **Substrate to GND**
5. **Wafer thickness: 460µm**

PAD LOCATION

Pad	Pad Name	X (μm)	Y (μm)
1	V_{IN}	-887.5	110
2	CS	0	0
3	GND	255.5	0
4	GND	395.5	0
5	GATE	587.0	544.5
6	PWM_D	556.5	1259.5
7	V_{DD}	375.5	1290
8	V_{DD}	235.5	1290
9	LD	-1012.5	1260.5
10	R_{OSC}	-1012.5	1044.5

DIE PHOTO



ELECTRICAL CHARACTERISTICS (T_A=25℃, unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit	Condition
V_{INDC}	Input DC supply voltage range	8.0		450	V	DC input voltage
I_{INsd}	Shut-Down mode supply current		0.5	1	mA	Pin PWM_D to GND, V_{IN}=8V
V_{DD}	Internally regulated voltage	7.0	7.5	8.0	V	V_{IN}=8-450V, $I_{DD(ext)}$=0, pin Gate open
V_{DDmax}	Maximal pin V_{DD} voltage			13.5	V	When an external voltage applied to pin V_{DD}
$I_{DD(ext)}$	V_{DD} current available for external circuitry			1.0	mA	V_{IN}=8-100V
UVLO	V_{DD} undervoltage lockout threshold	6.45	6.7	6.95	V	V_{IN} rising
ΔUVLO	V_{DD} undervoltage lockout hysteresis		500		mV	V_{IN} falling
$V_{EN(lo)}$	Pin PWM_D input low voltage			1.0	V	V_{IN}=8-450V
$V_{EN(hi)}$	Pin PWM_D input high voltage	2.4			V	V_{IN}=8-450V
RLN	Pin PWM_D pull-down resistance	50	100	150	kΩ	V_{EN}=5V
$V_{CS(hi)}$	Current sense pull-in threshold voltage	225	250	275	mV	@ TA=-40 ℃ to +85℃
$V_{GATE(hi)}$	GATE high output voltage	V_{DD}-0.3		V_{DD}	V	I_{OUT}=-10mA
$V_{GATE(lo)}$	GATE low output voltage	0		0.3	V	I_{OUT}=10mA
fosc	Oscillator frequency	20 80	25 100	30 120	kHz kHz	R_{OSC}=1.00MΩ R_{OSC}=223kΩ
D_{maxHT}	Maximum Oscillator PWM duty cycle			100	%	F_{PWMhf}=25kHz, at GATE, CS to GND
V_{LD}	Linear Dimming pin voltage range	0		250	mV	@ TA=<85 ℃ , V_{IN}=12V

T_{BLANK}	Current sense blanking interval	150	215	280	ns	V_{CS}=0.55V_{LD}, V_{LD}=V_{DD}
t_{DELAY}	Delay from CS trip to GATE lo			300	ns	V_{IN}=12V, V_{LD}=0.15V, V_{CS}=0 to 0.22V after T_{BLANK}
t_{RISE}	GATE output rise time		30	50	ns	C_{GATE}=500pF, 10% to 90% V_{GATE}
t_{FALL}	GATE output fall time		30	50	ns	C_{GATE}=500pF, 90% to 10% V_{GATE}

Note: Also limited by package power dissipation limit, whichever is lower.