

## N-Channel 30-V(D-S) MOSFET

### GENERAL DESCRIPTION

The ME4822 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

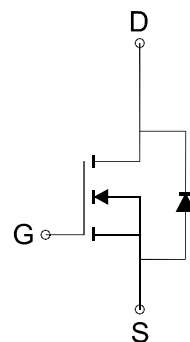
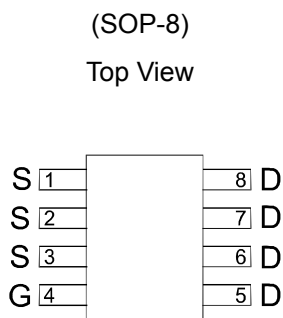
### FEATURES

- 30V/12A,  $R_{DS(ON)}=11m\Omega@V_{GS}=10V$
- 30V/9.9A,  $R_{DS(ON)}=16m\Omega@V_{GS}=4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

### APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

### PIN CONFIGURATION



N-Channel MOSFET

### Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ Unless Otherwise Noted)

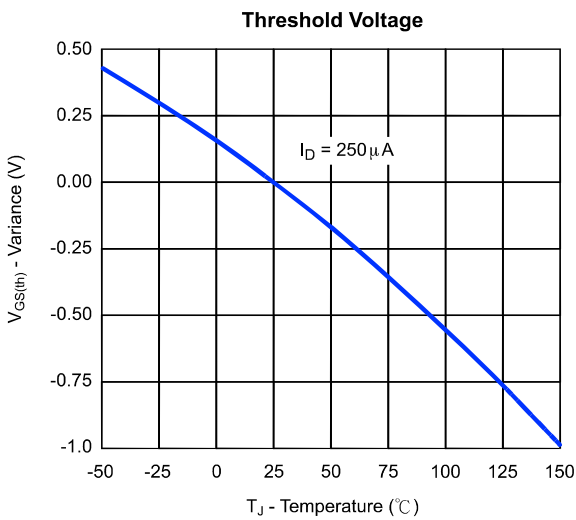
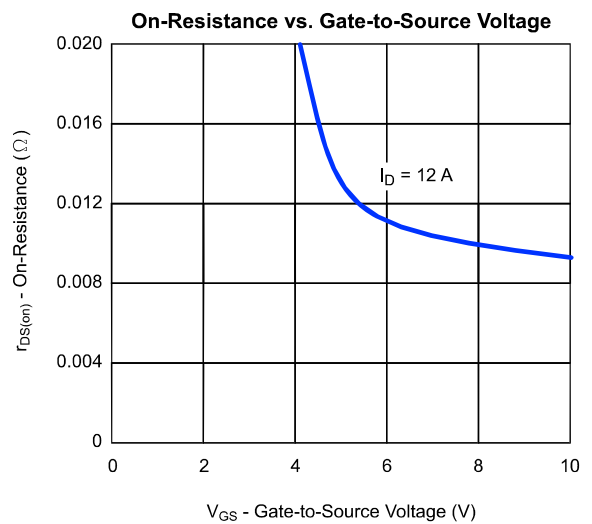
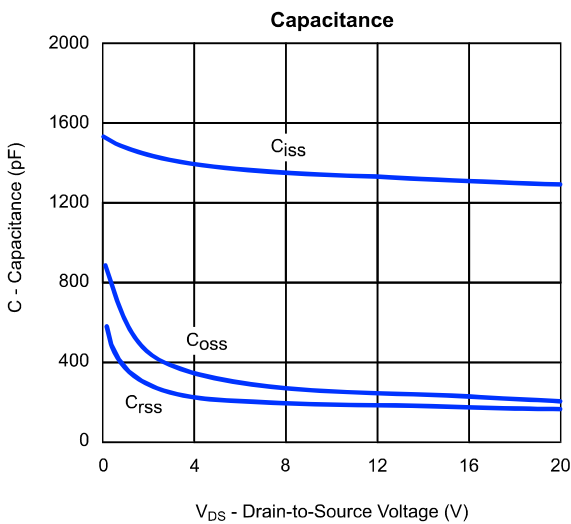
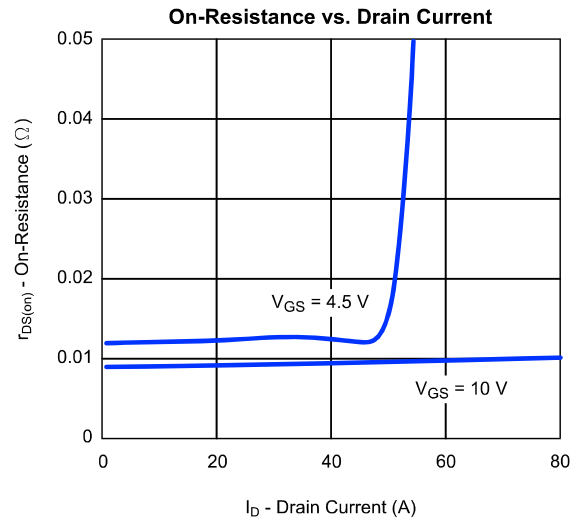
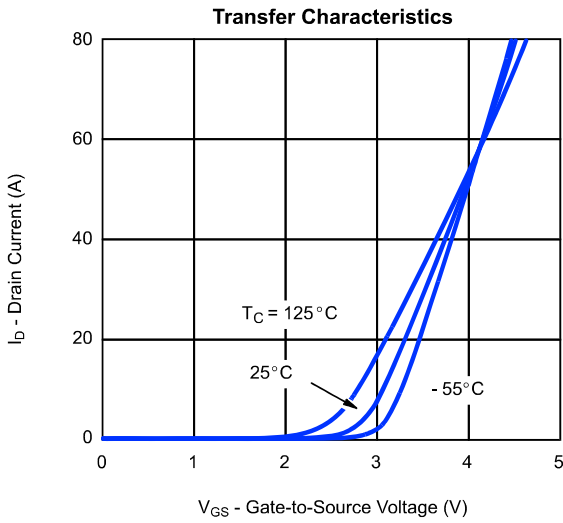
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DSS}$	30	V
Gate-Source Voltage	$V_{GSS}$	$\pm 20$	V
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ )	$I_D$	$T_A=25^\circ\text{C}$	12
		$T_A=70^\circ\text{C}$	9.7
Pulsed Drain Current	$I_{DM}$	60	A
Continuous Source Current (Diode Conduction)	$I_S$	2.3	A
Maximum Power Dissipation	$P_D$	$T_A=25^\circ\text{C}$	2.5
		$T_A=70^\circ\text{C}$	1.6
Operating Junction Temperature	$T_J$	-55 to 150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	$T \leq 10 \text{ sec}$	50
		Steady State	80

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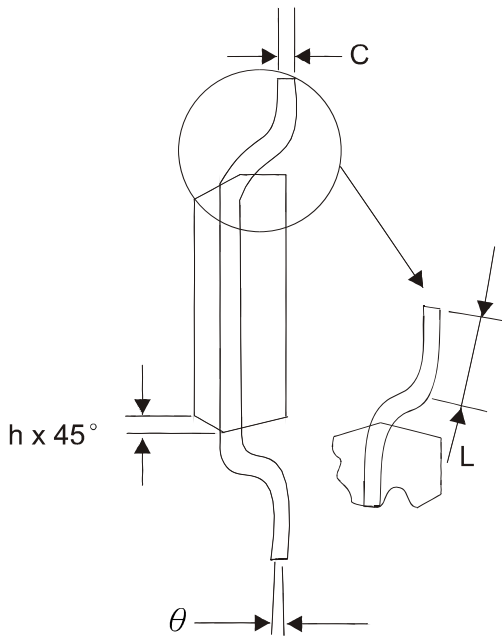
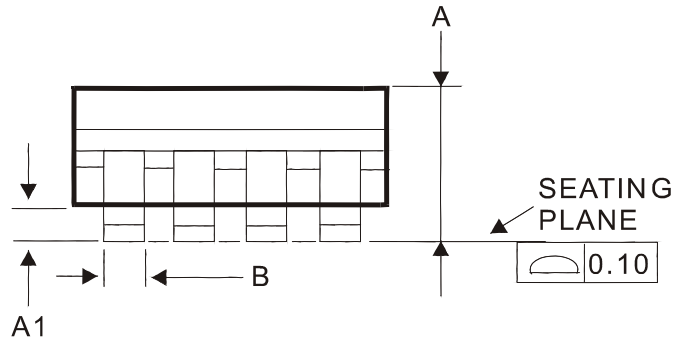
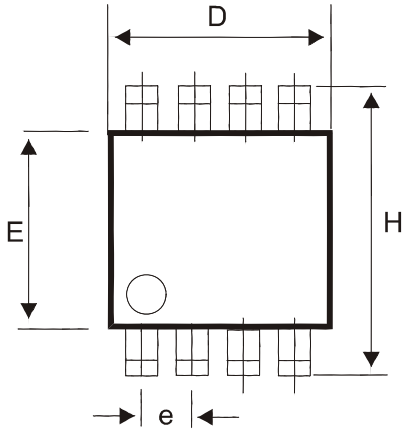
Electrical Characteristics (TA=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250 μA	30			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 μA	1.0		3.0	V
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V			1	μA
		V <sub>DS</sub> =24V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			5	
I <sub>D(ON)</sub>	On-State Drain Current	V <sub>DS</sub> ≥5V, V <sub>GS</sub> =10V	30			A
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =12A		9	11	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =9.9A		12	16	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =15V, I <sub>D</sub> =12A		8		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =2.3A, V <sub>GS</sub> =0V		0.7	1.1	V
<b>DYNAMIC</b>						
R <sub>g</sub>	Gate resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz		1.5		Ω
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =15V, V <sub>GS</sub> =5V, I <sub>D</sub> =12A		15	30	nC
Q <sub>gs</sub>	Gate-Source Charge			10		
Q <sub>gd</sub>	Gate-Drain Charge			8		
t <sub>d(on)</sub>	Turn-On Time	V <sub>DD</sub> =15V, R <sub>L</sub> =15Ω I <sub>D</sub> =1A, V <sub>GEN</sub> =10V		17	37	ns
t <sub>r</sub>				14	34	
t <sub>d(off)</sub>	Turn-Off Time	R <sub>G</sub> =6Ω		60	100	
t <sub>f</sub>				10	20	

### Typical Characteristics (T<sub>J</sub> = 25°C Noted)



**SOP-8 Package Outline**



DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
$\theta$	0°	7°