Green-Mode PWM Controller with High-Voltage Start-Up Circuit

REV: 04a

General Description

The LD7575 is a current-mode PWM controller with excellent power-saving operation. It features a high-voltage current source to directly supply the startup current from bulk capacitor and further to provide a lossless startup circuit. The integrated functions such as the leading-edge blanking of the current sensing, internal slope compensation, and the small package provide the users a high efficiency, minimum external component counts, and low cost solution for AC/DC power applications.

Furthermore, the embedded over voltage protection, over load protection and the special green-mode control provide the solution for users to design a high performance power circuit easily. The LD7575 is offered in both SOP-8 and DIP-8 package.

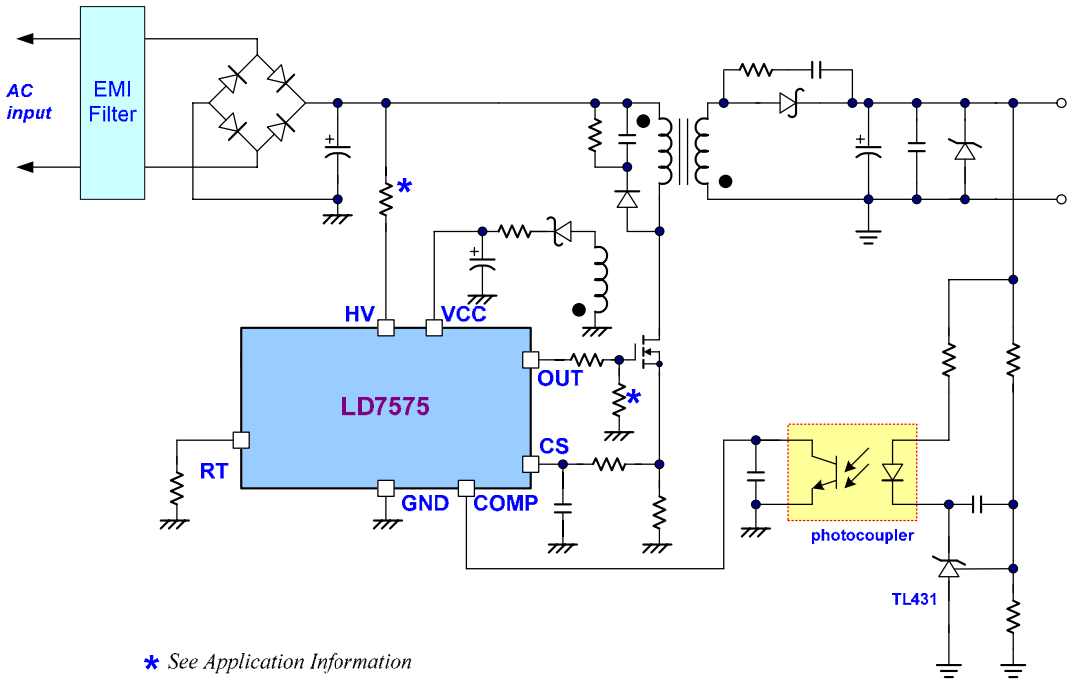
Features

- High-Voltage (500V) Startup Circuit
- Current Mode Control
- Non-Audible-Noise Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Programmable Switching Frequency
- Internal Slope Compensation
- OVP (Over Voltage Protection) on Vcc
- OLP (Over Load Protection)
- 500mA Driving Capability

Applications

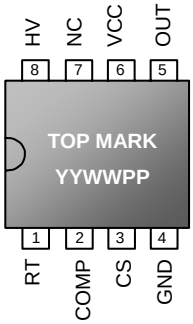
- Switching AC/DC Adapter and Battery Charger
- Open Frame Switching Power Supply
- LCD Monitor/TV Power

Typical Application



Pin Configuration

SOP-8 & DIP-8 (TOP VIEW)



YY: Year code
WW: Week code
PP: Production code

Ordering Information

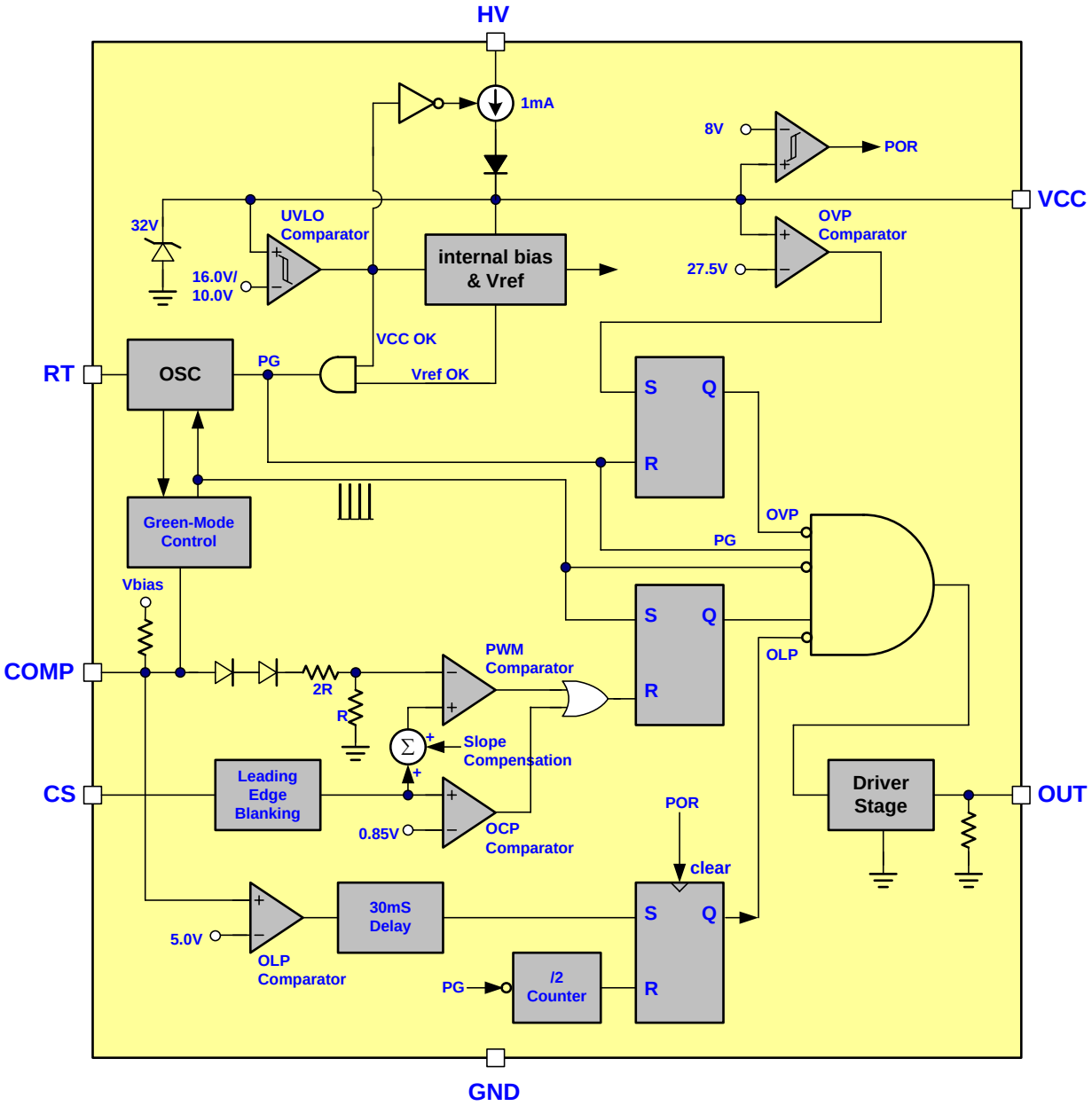
Part number	Package	Top Mark	Shipping
LD7575 PS	SOP-8	LD7575PS	2500 /tape & reel
LD7575 PN	DIP-8	LD7575PN	3600 /tube /Carton

The LD7575 is ROHS compliant.

Pin Descriptions

PIN	NAME	FUNCTION
1	RT	This pin is to program the switching frequency. By connecting a resistor to ground to set the switching frequency.
2	COMP	Voltage feedback pin (same as the COMP pin in UC384X), By connecting a photo-coupler to close the control loop and achieve the regulation.
3	CS	Current sense pin, connect to sense the MOSFET current
4	GND	Ground
5	OUT	Gate drive output to drive the external MOSFET
6	VCC	Supply voltage pin
7	NC	Unconnected Pin
8	HV	Connect this pin to positive terminal of bulk capacitor to provide the startup current for the controller. When Vcc voltage trips the UVLO(on), this HV loop will be off to save the power loss on the startup circuit.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	30V
High-Voltage Pin, HV	-0.3V~500V
COMP, RT, CS	-0.3 ~7V
Junction Temperature	150°C
Operating Ambient Temperature	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8)	160°C/W
Package Thermal Resistance (DIP-8)	100°C/W
Power Dissipation (SOP-8, at Ambient Temperature = 85°C)	400mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	650mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (except HV Pin)	3KV
ESD Voltage Protection, Machine Model	200V
Gate Output Current	500mA

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Supply Voltage Vcc	11	25	V
Vcc Capacitor	10	47	μF
Switching Frequency	50	130	KHz

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High-Voltage Supply (HV Pin)					
High-Voltage Current Source	Vcc< UVLO(on), HV=500V	0.5	1.0	1.5	mA
Off-State Leakage Current	Vcc> UVLO(off), HV=500V			35	μA
Supply Voltage (Vcc Pin)					
Startup Current				100	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V		2.0	3.0	mA
	V_{COMP}=3V		2.5	4.0	mA
	Protection tripped (OLP, OVP)		0.5		mA
UVLO (off)		9.0	10.0	11.0	V
UVLO (on)		15.0	16.0	17.0	V
OVP Level		25.0	27.5	30.0	V
Voltage Feedback (Comp Pin)					
Short Circuit Current	V_{COMP}=0V		1.5	2.2	mA
Open Loop Voltage	COMP pin open		6.0		V
Green Mode Threshold VCOMP			2.35		V
Current Sensing (CS Pin)					
Maximum Input Voltage		0.80	0.85	0.90	V
Leading Edge Blanking Time			350		nS
Input impedance		1			MΩ
Delay to Output			100		nS
Oscillator (RT pin)					
Frequency	RT=100KΩ	60.0	65.0	70.0	KHz
Green Mode Frequency	Fs=65.0KHz		20		KHz
Temp. Stability	(-40°C ~105°C)			3	%
Voltage Stability	(VCC=11V-25V)			1	%
Gate Drive Output (OUT Pin)					
Output Low Level	VCC=15V, Io=20mA			1	V
Output High Level	VCC=15V, Io=20mA	9			V
Rising Time	Load Capacitance=1000pF		50	160	nS
Falling Time	Load Capacitance=1000pF		30	60	nS
OLP (Over Load Protection)					
OLP Trip Level			5.0		V
OLP Delay Time (note)	Fs=65KHz		30		mS

Note: The OLP delay time is proportional to the period of switching cycle. So that, the lower RT value will set the higher switching frequency and the shorter OLP delay time.

Typical Performance Characteristics

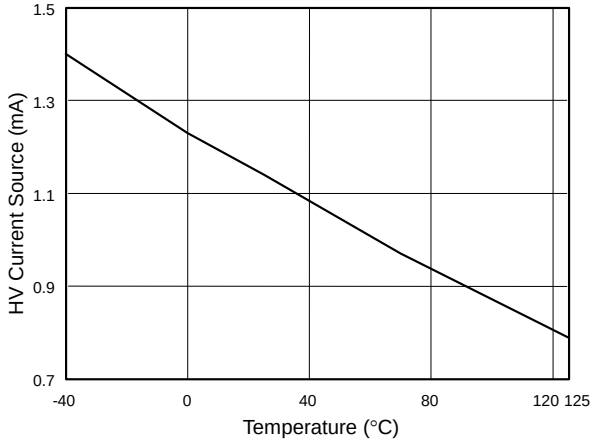


Fig. 1 HV Current Source vs. Temperature (HV=500V, Vcc=0V)

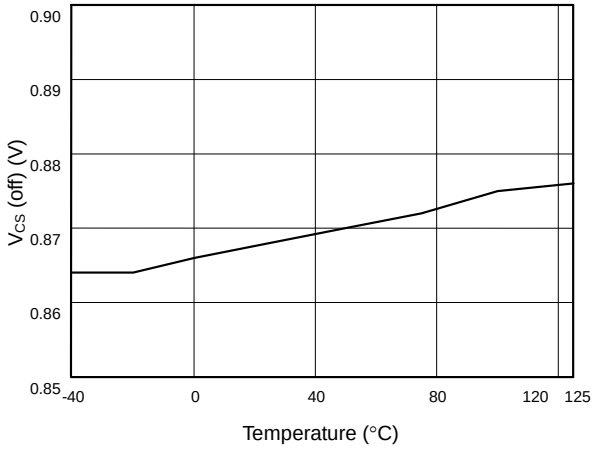


Fig. 2 V_{CS} (off) vs. Temperature

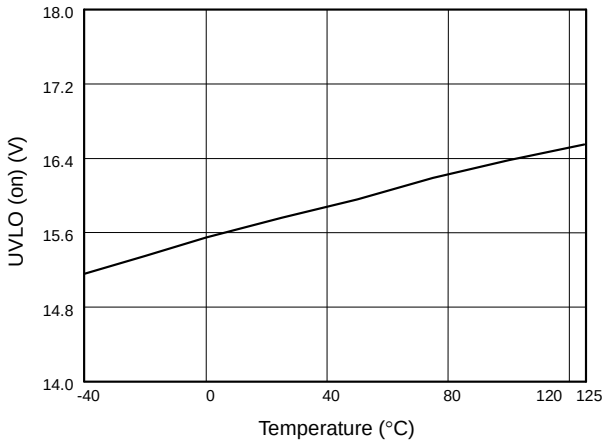


Fig. 3 UVLO (on) vs. Temperature

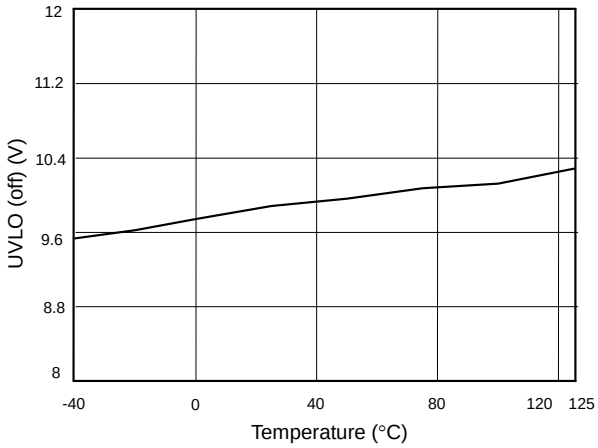


Fig. 4 UVLO (off) vs. Temperature

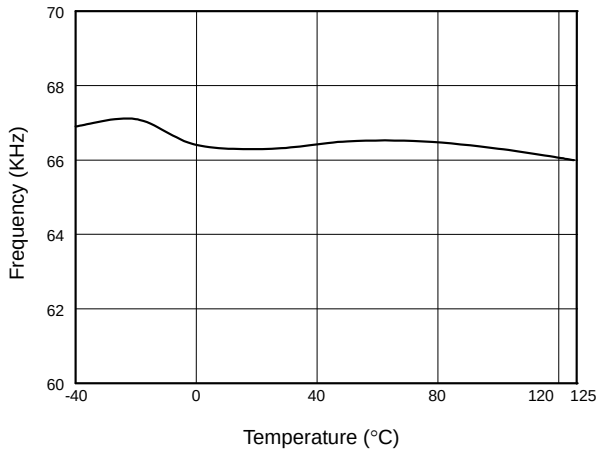


Fig. 5 Frequency vs. Temperature

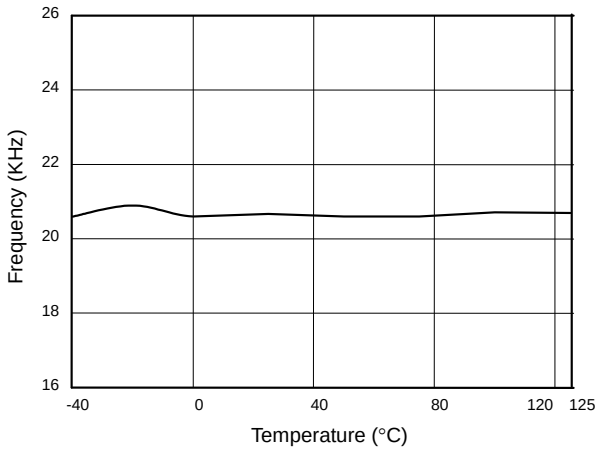


Fig. 6 Green Mode Frequency vs. Temperature

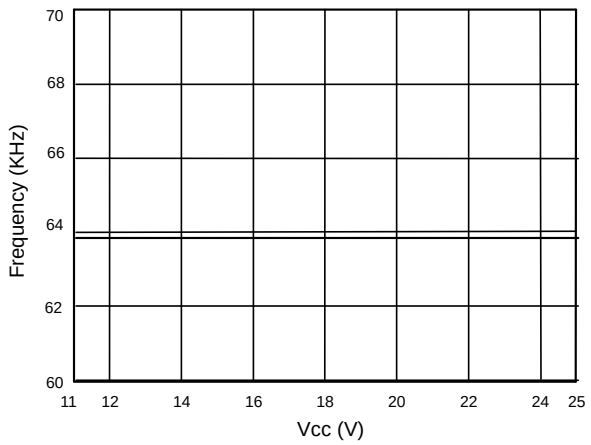


Fig. 7 Frequency vs. Vcc

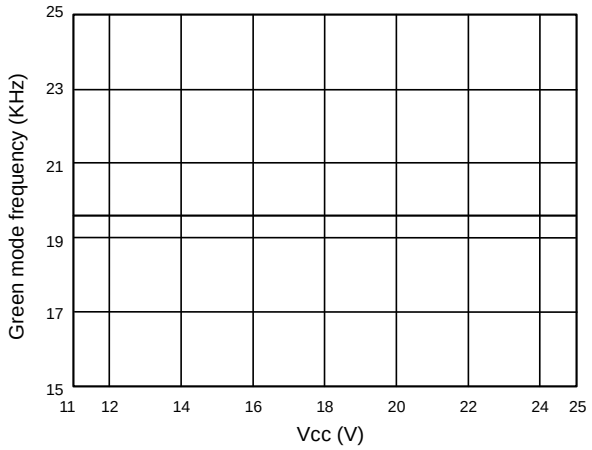


Fig. 8 Green mode frequency vs. Vcc

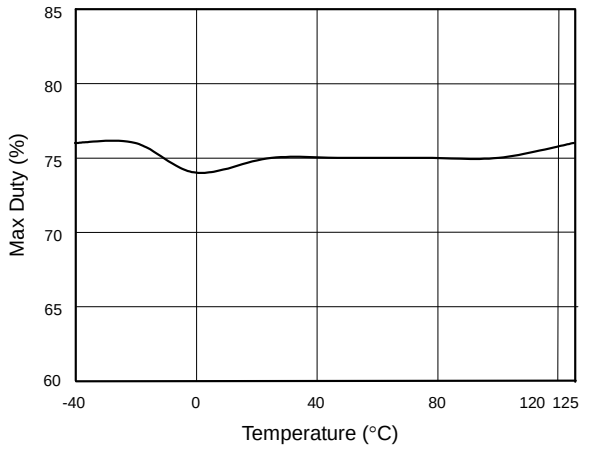


Fig. 9 Max Duty vs. Temperature

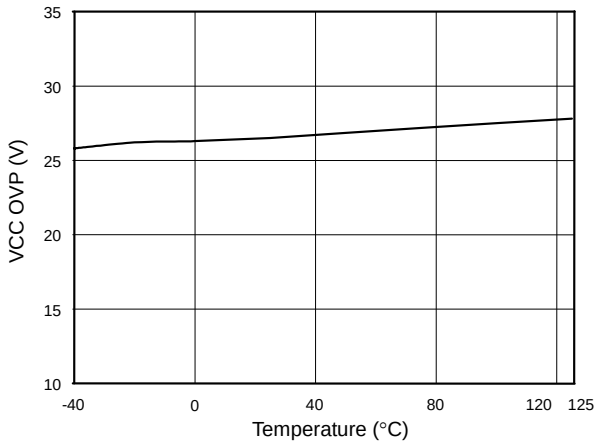


Fig. 10 VCC OVP vs. Temperature

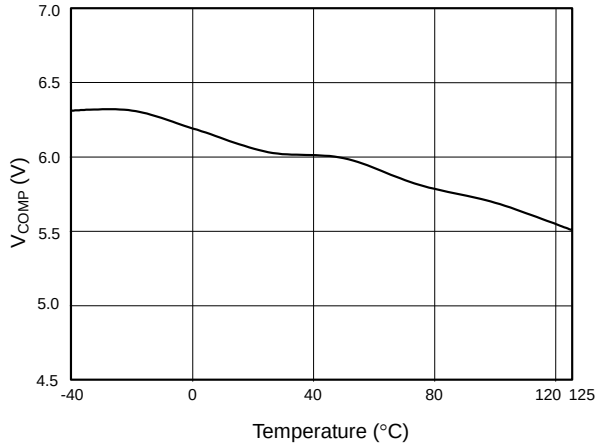


Fig. 11 V_{COMP} open loop voltage vs. Temperature

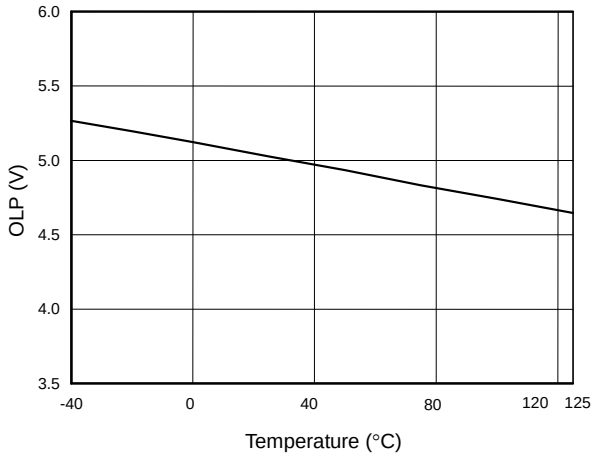


Fig. 12 OLP-Trip Level vs. Temperature

Application Information

Operation Overview

As long as the green power requirement becomes a trend and the power saving is getting more and more important for the switching power supplies and switching adaptors, the traditional PWM controllers are not able to support such new requirements. Furthermore, the cost and size limitation force the PWM controllers need to be powerful to integrate more functions to reduce the external part counts. The LD7575 is targeted on such application to provide an easy and cost effective solution; its detail features are described as below:

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

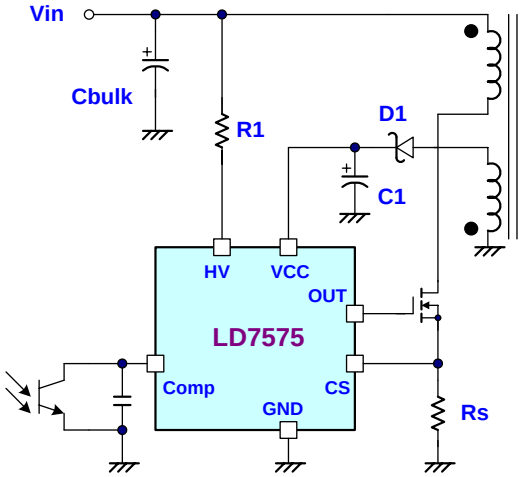


Fig. 13

Traditional circuit powers up the PWM controller through a startup resistor to provide the startup current. However, the startup resistor consumes significant power which is more and more critical whenever the power saving requirement is coming tight. Theoretically, this startup resistor can be very high resistance value. However, higher resistor value will cause longer startup time.

To achieve an optimized topology, as shown in figure 13, LD7575 implements a high-voltage startup circuit for such requirement. During the startup, a high-voltage current source sinks current from the bulk capacitor to provide the startup current as well as charge the Vcc capacitor C1. During the startup transient, the Vcc is lower than the UVLO threshold thus the current source is on to supply a current with 1mA. Meanwhile, the Vcc supply current is as low as 100μA thus most of the HV current is utilized to charge the Vcc capacitor. By using such configuration, the turn-on delay time will be almost same no matter under low-line or high-line conditions.

Whenever the Vcc voltage is higher than UVLO(on) to power on the LD7575 and further to deliver the gate drive signal, the high-voltage current source is off and the supply current is provided from the auxiliary winding of the transformer. Therefore, the power losses on the startup circuit can be eliminated and the power saving can be easily achieved.

An UVLO comparator is included to detect the voltage on the Vcc pin to ensure the supply voltage enough to power on the LD7575 PWM controller and in addition to drive the power MOSFET. As shown in Fig. 14, a hysteresis is provided to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16V and 10.0V, respectively.

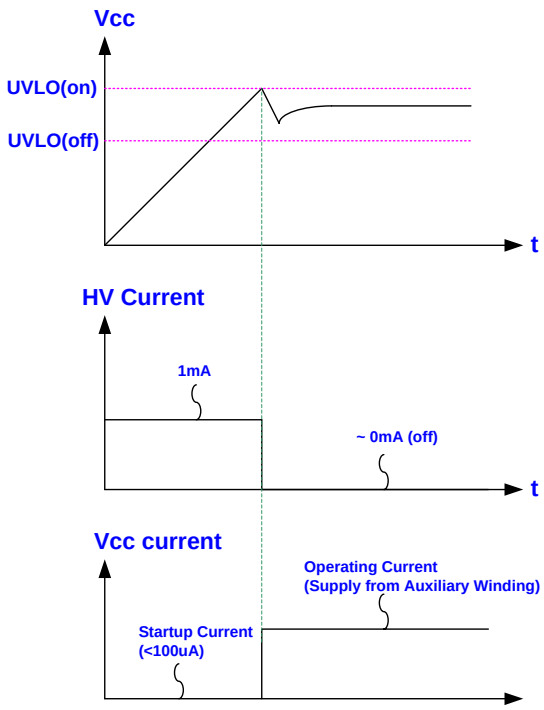


Fig. 14

Current Sensing, Leading-edge Blanking and the Negative Spike on CS Pin

The typical current mode PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. The LD7575 detects the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set as 0.85V. Thus the MOSFET peak current can be calculated as:

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

A 350nS leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger caused by the current spike. In the low power application, if the total pulse width of the turn-on spikes is less than 350nS and the negative spike on the CS pin is not exceed -0.3V, the R-C filter (as shown in figure15) can be eliminated.

However, the total pulse width of the turn-on spike is related to the output power, circuit design and PCB layout. It is strongly recommended to add the small R-C filter (as shown in figure 16) for higher power application to avoid the CS pin damaged by the negative turn-on spike.

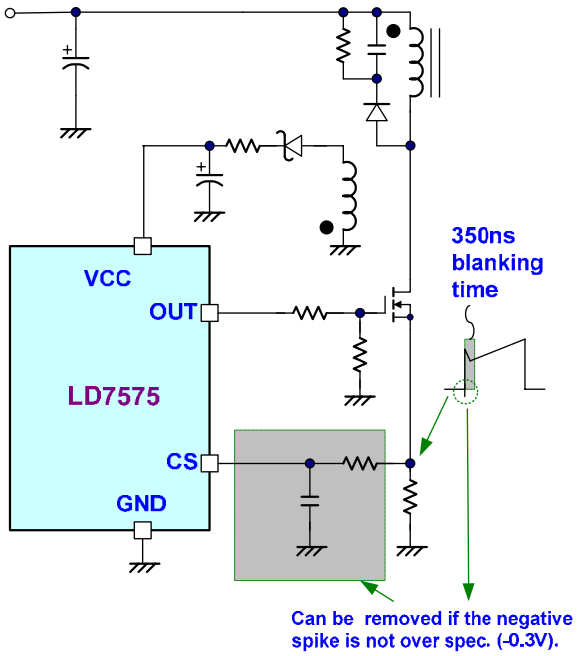


Fig. 15

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 500mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD7575 is limited to 75% to avoid the transformer saturation.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 in the secondary side through the photo-coupler to the COMP pin of LD7575. The input stage of LD7575, like the UC384X, is with 2 diodes voltage offset then feeding into the voltage divider with 1/3 ratio, that is,

$$V_{+(PWM_{COMPARATOR})} = \frac{1}{3} \times (V_{COMP} - 2V_F)$$

A pull-high resistor is embedded internally thus can be eliminated on the external circuit.

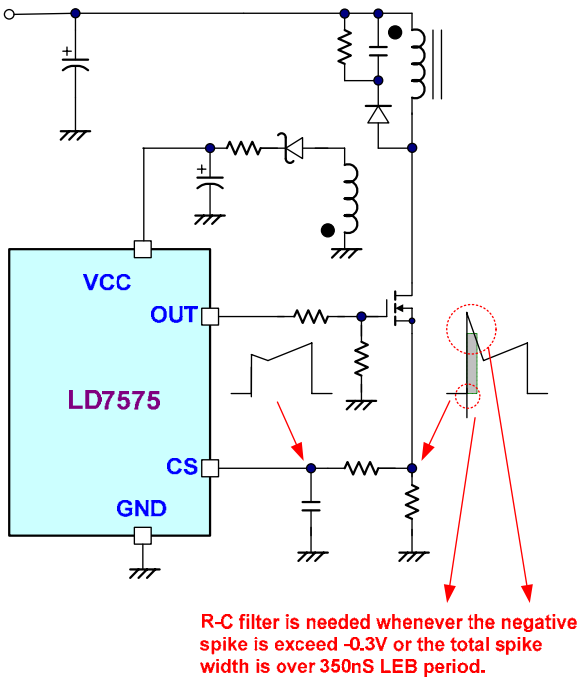


Fig. 16

Oscillator and Switching Frequency

Connecting a resistor from RT pin to GND according to the equation can program the normal switching frequency:

$$f_{SW} = \frac{65.0}{RT_{(K\Omega)}} \times 100(KHz)$$

The suggested operating frequency range of LD7575 is within 50KHz to 130KHz.

Internal Slope Compensation

A fundamental issue of current mode control is the stability problem when its duty-cycle is operated more than 50%. To stabilize the control loop, the slope compensation is needed in the traditional UC384X design by injecting the ramp signal from the RT/CT pin through a coupling capacitor. In LD7575, the internal slope compensation circuit has been implemented to simplify the external circuit design.

On/Off Control

The LD7575 can be controlled to turn off by pulling COMP pin to lower than 1.2V. The gate output pin of LD7575 will be disabled immediately under such condition. The off mode can be released when the pull-low signal is removed.

Dual-Oscillator Green-Mode Operation

There are many difference topologies has been implemented in different chips for the green-mode or power saving requirements such as “burst-mode control”, “skipping-cycle Mode”, “variable off-time control “…etc. The basic operation theory of all these approaches intended to reduce the switching cycles under light-load or no-load condition either by skipping some switching pulses or reduce the switching frequency.

Over Load Protection (OLP)

To protect the circuit from the damage during over load condition or short condition, a smart OLP function is implemented in the LD7575. Figure 17 shows the waveforms of the OLP operation. Under such fault condition, the feedback system will force the voltage loop toward the saturation and thus pull the voltage on COMP pin (VCOMP) to high. Whenever the VCOMP trips the OLP threshold 5.0V and keeps longer than 30mS (when switching frequency is 65KHz), the protection is activated and then turns off the gate output to stop the switching of power circuit. The 30mS delay time is to prevent the false trigger from the power-on and turn-off transient.

A divide-2 counter is implemented to reduce the average power under OLP behavior. Whenever OLP is activated, the output is latched off and the divide-2 counter starts to count the number of UVLO(off). The latch is released if the 2nd UVLO(off) point is counted then the output is recovery to switching again.

By using such protection mechanism, the average input power can be reduced to very low level so that the component temperature and stress can be controlled within the safe operating area.

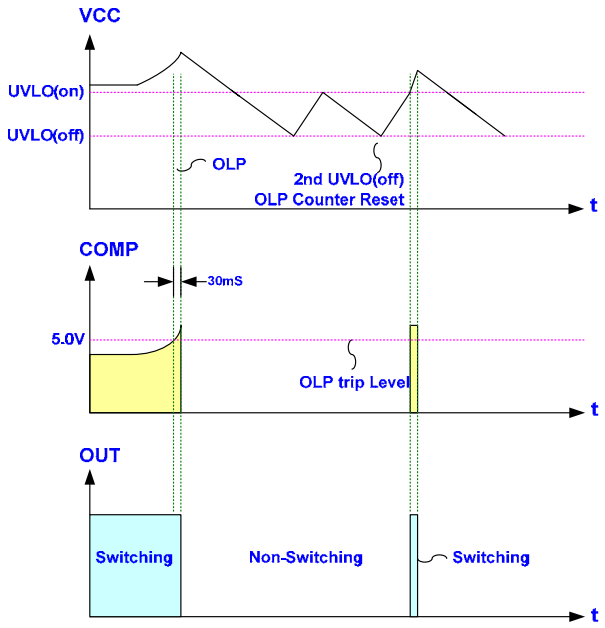


Fig. 17

OVP (Over Voltage Protection) on Vcc

The Vgs ratings of the nowadays power MOSFETs are most with maximum 30V. To prevent the Vgs from the fault condition, LD7575 is implemented an OVP function on Vcc. Whenever the Vcc voltage is higher than the OVP threshold voltage, the output gate drive circuit will be shutdown simultaneous thus to stop the switching of the power MOSFET until the next UVLO(on).

The Vcc OVP function in LD7575 is an auto-recovery type protection. If the OVP condition, usually caused by the

feedback loop opened, is not released, the Vcc will tripped the OVP level again and re-shutdown the output. The Vcc is working as a hiccup mode. Figure 18 shows its operation.

On the other hand, if the OVP condition is removed, the Vcc level will get back to normal level and the output is automatically returned to the normal operation.

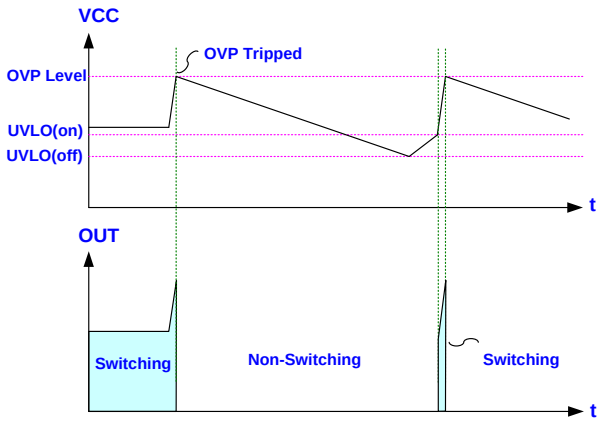


Fig. 18

Fault Protection

A lot of protection features have been implemented in the LD7575 to prevent the power supply or adapter from being damaged caused by single fault condition on the open or short condition on the pin of LD7575. Under the conditions listed below, the gate output will be off immediately to protect the power circuit ---

- RT pin short to ground
- RT pin floating
- CS pin floating

Pull-Low Resistor on the Gate Pin of MOSFET

In LD7575, an anti-floating resistor is implemented on the OUT pin to prevent the output from any uncertain state which may causes the MOSFET working abnormally or false triggered-on. However, such design won't cover the condition of disconnection of gate resistor Rg thus it is still strongly recommended to have a resistor connected on the MOSFET gate terminal (as shown in figure 19) to provide extra protection for fault condition.

This external pull-low resistor is to prevent the MOSFET from damage during power-on under the gate resistor is disconnected. In such single-fault condition, as show in figure 21, the resistor R8 can provide a discharge path to avoid the MOSFET from being false-triggered by the current through the gate-to-drain capacitor Cgd. Therefore, the MOSFET is always pull-low and kept in the off-state whenever the gate resistor is disconnected or opened in any case.

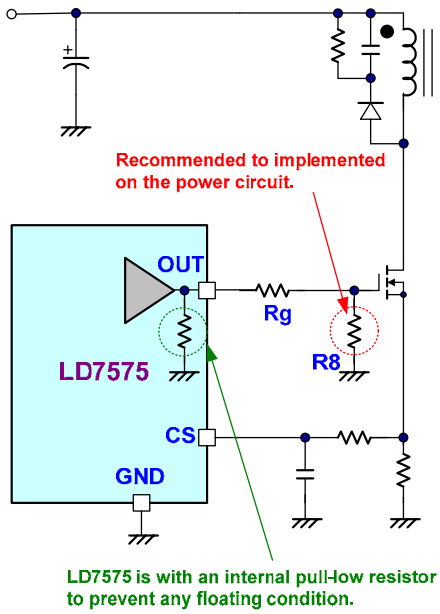


Fig. 19

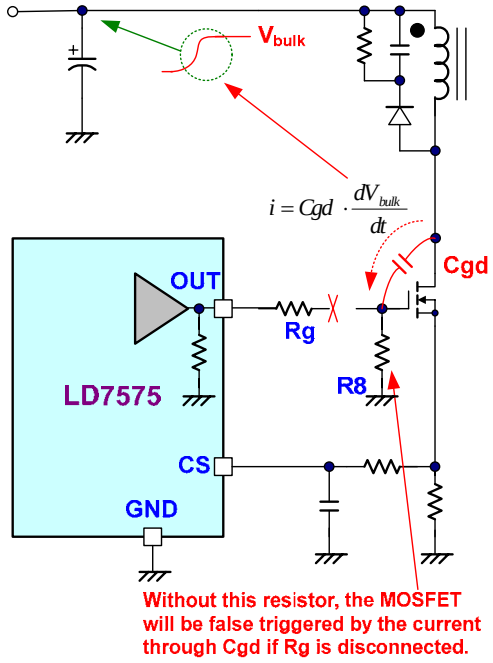


Fig. 20

Protection Resistor on the Hi-V Path

In some other Hi-V process and design, there may cause a parasitic SCR between HV pin, Vcc and GND. As shown in figure 22, a small negative spike on the HV pin may trigger this parasitic SCR and causes the latchup between Vcc and GND. And such latchup is easy to damage the chip because of the equivalent short-circuit which is induced by such latchup behavior.

Thanks to the Leadtrend's proprietary Hi-V technology, there is no such parasitic SCR in LD7575. Figure 23 shows the equivalent circuit of LD7575's Hi-V structure. So that LD7575 is with higher capability to sustain negative voltage than similar products. However, a 10KΩ resistor is recommended to implement on the Hi-V path to be played the role as a current limit resistor whenever a negative voltage is applied in any case.

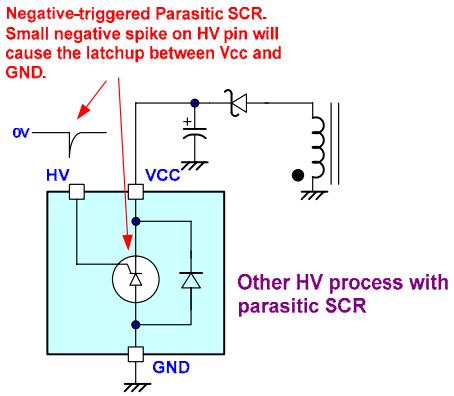


Fig. 21

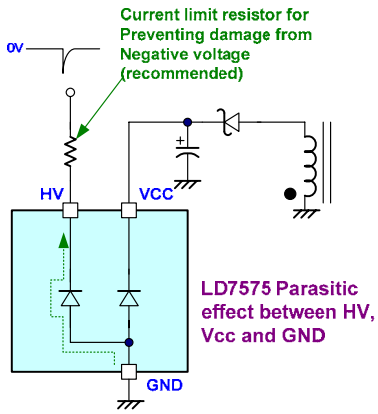
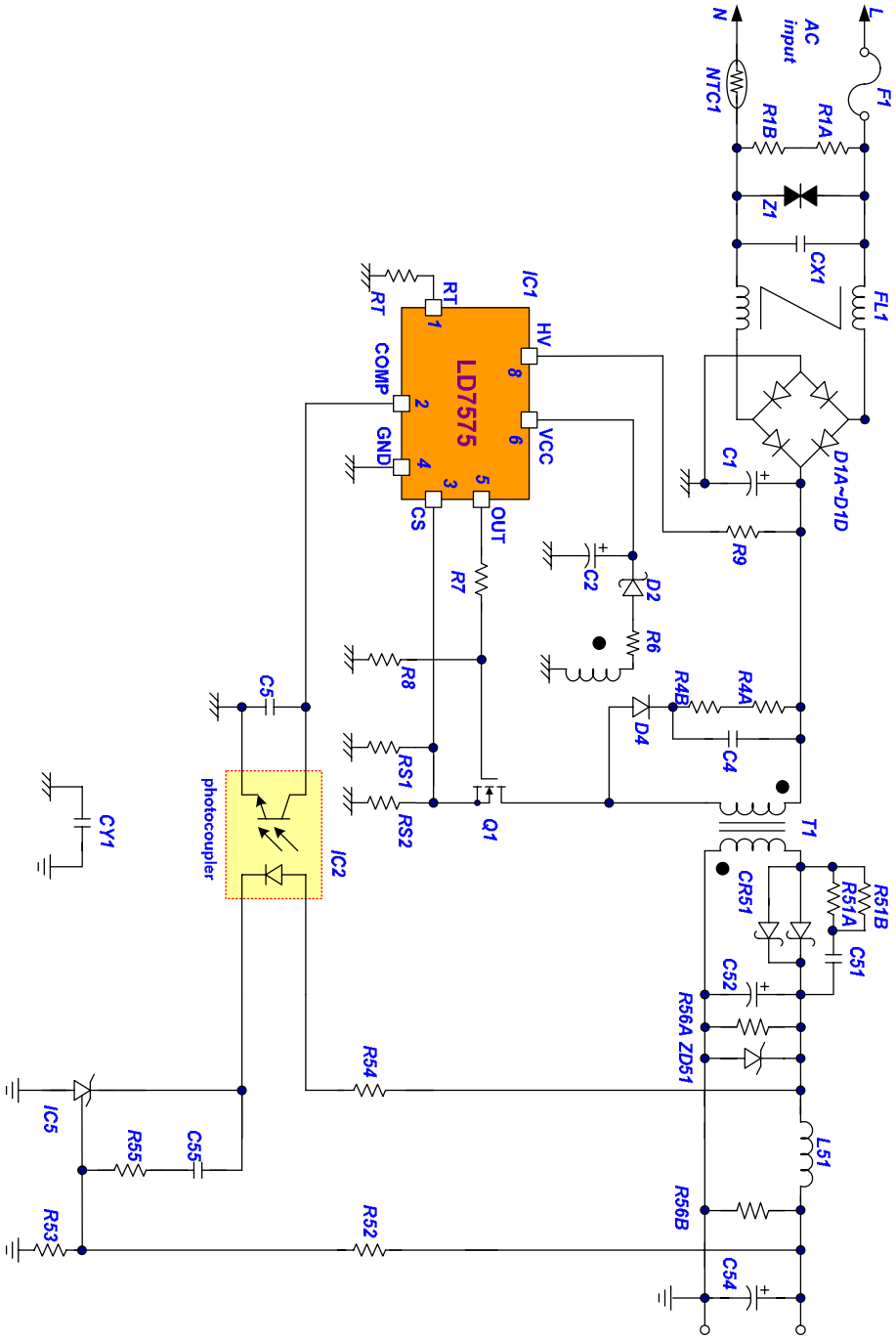


Fig. 22

Reference Application Circuit --- 10W (5V/2A) Adapter

Pin < 0.15W when Pout = 0W & Vin = 264Vac

Schematic



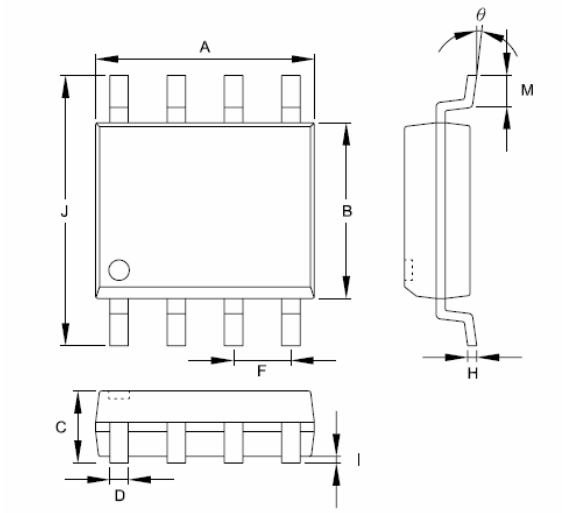
BOM

P/N	Component Value	Original
R1A	N/A	
R1B	N/A	
R4A	39KΩ, 1206	
R4B	39KΩ, 1206	
R6	2.2Ω, 1206	
R7	10Ω, 1206	
R8	10KΩ, 1206	
R9	10KΩ, 1206	
RS1	2.7Ω, 1206, 1%	
RS2	2.7Ω, 1206, 1%	
RT	100KΩ, 0805, 1%	
R51A	100Ω, 1206	
R51B	100Ω, 1206	
R52	2.49KΩ, 0805, 1%	
R53	2.49KΩ, 0805, 1%	
R54	100Ω, 0805	
R55	1KΩ, 0805	
R56A	2.7KΩ, 1206	
R56B	N/A	
NTC1	5Ω, 3A	08SP005
FL1	20mH	UU9.8
T1	EI-22	
L51	2.7μH	

P/N	Component Value	Note
C1	22μF, 400V	L-tec
C2	22μF, 50V	L-tec
C4	1000pF, 1000V, 1206	Holystone
C5	0.01μF, 16V, 0805	
C51	1000pF, 50V, 0805	
C52	1000μF, 10V	L-tec
C54	470μF, 10V	L-tec
C55	0.022μF, 16V, 0805	
CX1	0.1μF	X-cap
CY1	2200pF	Y-cap
D1A	1N4007	
D1B	1N4007	
D1C	1N4007	
D1D	1N4007	
D2	PS102R	
D4	1N4007	
Q1	2N60B	600V, 2A
CR51	SB540	
ZD51	6V2C	
IC1	LD7575PS	SOP-8
IC2	EL817B	
IC51	TL431	1%
F1	250V, 1A	
Z1	N/A	

Package Information

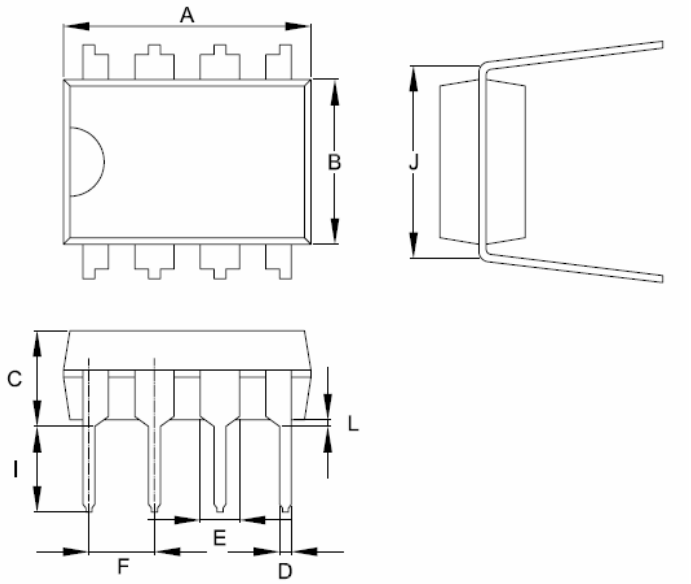
SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.229	0.007	0.009
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

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Revision History

Rev.	Date	Change Notice
00	07/21/'05	Original Specification.
01	07/28/'05	1. Page 2, Remove the unexpected code "skype.lnk" before the "ordering information". 2. Page 4, Recommended operating condition, change the "min. supply voltage Vcc" from 10V to 11V since the UVLO range is from 9V to 11V. 3. Page 9, Add the gate resistor on figure 15 and figure 16 to avoid misunderstanding. 4. Page 11, Add the description "Figure 17 shows its operation." In the section of "OVP on Vcc". 5. Page 13, Add "Vin=264Vac" on the title.
02	10/24/'05	1. Add DIP-8 Package a. Page 1 --- modify the general description "The LD7575 is offered in both SOP-8 and DIP-8 package.". b. Page 2 --- Add DIP-8 data on the "pin configuration" and "ordering information". c. Page 4 --- Add DIP-8 data on the "absolute maximum rating". d. Page 15 --- Add DIP-8 package drawing 2. Add information of HV current limit resistor and gate-to-GND resistor a. Page 1, 8 (figure13), 9 (figure15,16), 12, 13 --- Update the drawing, BOM and schematics for such resistors. b. Page 11, 12 --- Add the sections "Pull-Low Resistor on the Gate Pin of MOSFET", "Protection Resistor on the Hi-V Path" and figure 19~22. c. Page 4 --- Add negative voltage limitation of HV pin on the "absolute maximum rating". 3. Correction on the block diagram a. Page 3 --- Add flip-flop on the OVP loop to be matched with the OVP operation and add the anti-floating resistor on the output. 4. Correction on the description of Over Load Protection (OLP) a. Page 10 --- Original description "Whenever….30mS (when switching frequency is 100KHz)". Where the "100KHz" should be corrected to "65KHz".

Continued…

03	11/28/'05	1. Page3, Correction on the block diagram by modifying the AND gate (following the PWM comparator) to OR gate. 2. Page 5, Correction on the parameters on "Gate Drive Output" because LD7575 can support to 500mA driving capability but the parameters in the previous datasheet are for 300mA driving current. The output high level will be updated from min. 8V to min. 9V. The rising time will be updated from max. 200nS to max. 160nS. The falling time will be updated from max. 100nS to max. 60nS. All these parameters are for correction and no design change on the related circuits.
04	1/22/'07	Revision: Block Diagram
04a	6/5/2007	HV=500V (supplement to HV current source/ off state leakage current)