Data Sheet

BIT3206

Low Cost PWM Controller

Version: A1

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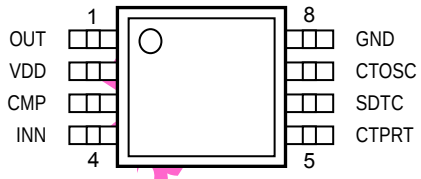
Features:

- **Fixed Frequency, Voltage Mode PWM Controller**
- **Up to 750KHz Programmable Operating Frequency**
- **Internal UVLO (Under Voltage Lock Out)**
- **Latched Off Protection with Programmable Timer**
- **Programmable Soft Start**
- **Programmable Maximum Duty Time Control**
- **CMOS Totem Pole Output**
- **3-State, Low Active Output**
- **SOP-8 Package**

Pin Layout:



General Description:

The BIT3206 is a high frequency PWM controller which integrates the required functions for DC/DC conversion in a single 8- pin chip. CMOS process greatly reduces the operating current (1mA typical) when comparing to similar products.

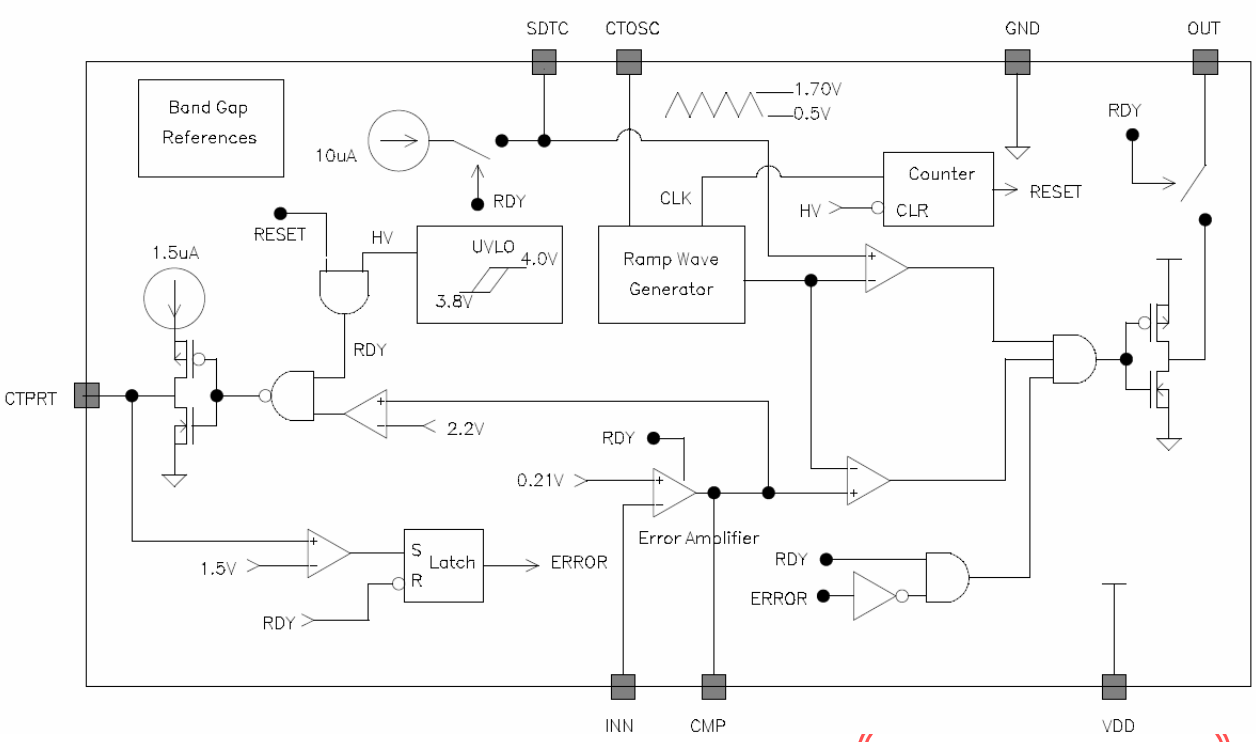
Recommended Operating Condition:

Supply Voltage……4.0~ 5.5 V
Operating Frequency……80K ~ 750KHz
Operating Ambient Temperature……..0 ~ 70 ℃

Absolute Ratings: (if Ta=25℃)

VDD……-0.3 ~ +6.5 V
GND……±0.3 V
Input Voltage……-0.3 ~ VDD+0.3 V
Operating Ambit Temperature…….0 ~ +70 ℃
Operating Junction Temperature….+150 ℃
Storage Temperature……-55~+150 ℃

Functional Block Diagram:



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Function Description:

UVLO: The Under-Voltage-Lock-Out circuit turns the output driver off when supplying voltage drops to a specified low level. When IC supplies voltage less than 3.8V, BIT3206 goes to the reset mode with the status in Table 1:

Table 1. Low Voltage Reset Status

Pin Name	Status
OUT(1)	Disable to "Floating"
CMP(3)	GND
CTPRT(5)	GND
SDTC(6)	GND
CTOSC(7)	GND

The Power On Initialization: When IC supply voltage rises to > 4.0V, the CTOSC is active to enable an internal digital counter. After 31 clock cycles of the CTOSC frequency, a 10uA begin to charges the SDTC pin. The OUT pin becomes a "low active" output. The controller is in the reset mode as table 1 before the 31 clock cycles are over.

Programmable Ramp Wave Generator: This circuit generates a typical 100KHz ramp wave. (as C_{CTOSC} =820 pF) The relation between frequency and capacitor C_{CTOSC} is as Fig. 3

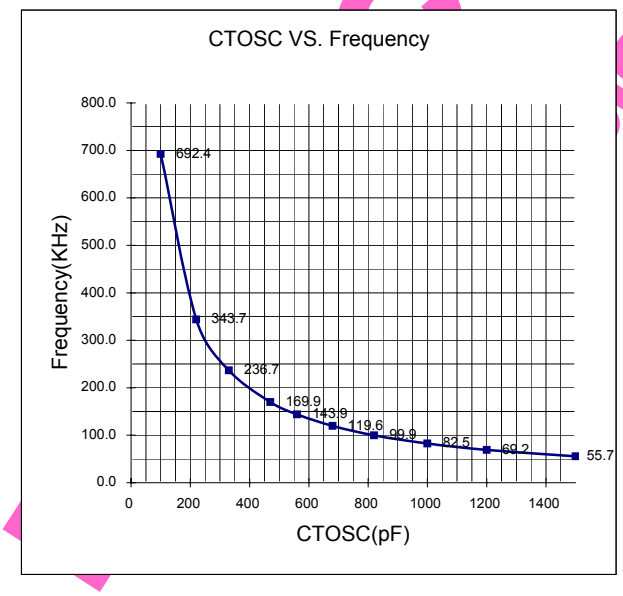

Fig. 3

The PWM Controller: The pulse width modulation control circuit includes a ramp wave generator, an error amplifier and a comparator. These devices provide the required active components for the PWM feedback control application.

The Programmable Soft Start and Duty Control: A current mirror provides current with value 10uA to charge the SDTC pin. The slope of Soft Start $\Delta V/\Delta T$ can be determined by

$$\frac{\Delta V}{\Delta T} = \frac{10uA}{C_{SDTC}} \quad .....(1)$$

The increasing voltage of SDTC pin increases the duty cycle of the PWM controller.

Soft-Start can be implemented by error amplifier too (C_{SDTC}<<). In this case, SDTC pin can only control the duty cycle.

To connect a resistor between SDTC and GND to fix the voltage of SDTC pin may limit the maximum duty cycle of the PWM controller. The maximum voltage of CTOSC is varied with the operation frequency (Fig.4). Please use a larger resistor to define the maximum duty cycle when operation frequency is higher. Maximum duty cycle may be determined by (2):

$$Duty(Max) = \frac{V_{MAX.(SDTC)} - V_{MIN.(CTOSC)}}{V_{MAX.(CTOSC)} - V_{MIN.(CTOSC)}} \quad ...(2)$$

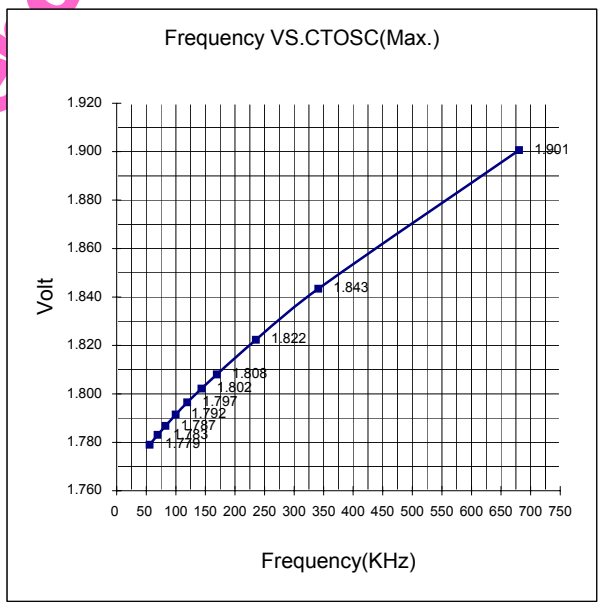

Fig. 4

The Latched Off Protection: A larger than 2.2V CMP voltage triggers a 1uA current source to charge the CTPRT pin. The OUT will be latched off (to floating state) when CTPRT > 1.5V. If the CMP pin < 2.2V, the CTPRT is discharged to GND with an internal switch. The latched off status can be reset by reducing the supply voltage to lower than 3.8V. The output pin OUT is in a "floating state" while the system is latched off.

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Pin Description:

Pin No.	Names	Description
1	OUT	3-state CMOS output. “Low active”
2	VDD	Supply voltage input.
3	CMP	The output of the error amplifier. This pin is forced to GND during initial state.
4	INN	PWM controller input, the inverting input of error amplifier.
5	CTPRT	Timer for latched off protection.
6	SDTC	Soft Start and Duty Time Control.
7	CTOSC	Operation frequency control.
8	GND	Ground

DC/AC Characteristics:

Parameter	Test Conditions	Min.	Typ.(Limits)	Max.	Unit
Reference Voltage					
Output voltage	Measure INN short CMP Ta=25°C VDD=4.0 ~ 5.5 V	0.2037	0.21	0.2163	V
Line regulation			2	20	mV
Under Voltage Look Out					
Upper threshold voltage	Ta=25℃	3.8	4	4.2	V
Hysteresis		0.1	0.2	0.3	V
Ramp Wave Generator					
Frequency	C_{CTOSC}=820pF	-	100		KHz
Operating Frequency	note 1	-		750	KHz
Output peak			1.77	1.92	V
Output valley			0.46		V
Error Amplifier					
Input voltage	note 1	-		2.25	V
Open loop gain		60	80		dB
Unit gain band width		1	1.5		MHz
Soft Start and Duty Time Control					
SDTC Output current	VDD=5V, Ta=25℃	9	10	11	uA
Latched Off Protection					
CTPRT Output Current	VDD=5V, Ta=25℃	0.9	1	1.1	uA
CTPRT Time-Up threshold voltage		1.45	1.5	1.55	V
CMP threshold voltage		2.1	2.2	2.3	V
Output					
CMOS output impedance	note 1		50		Ω
Rising Time	1000pF load, note 1		110		ns
Falling Time			100		ns

Ta : ambient temperature.

Note 1: It is guaranteed by design, and not 100% tested.

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Soldering Information:

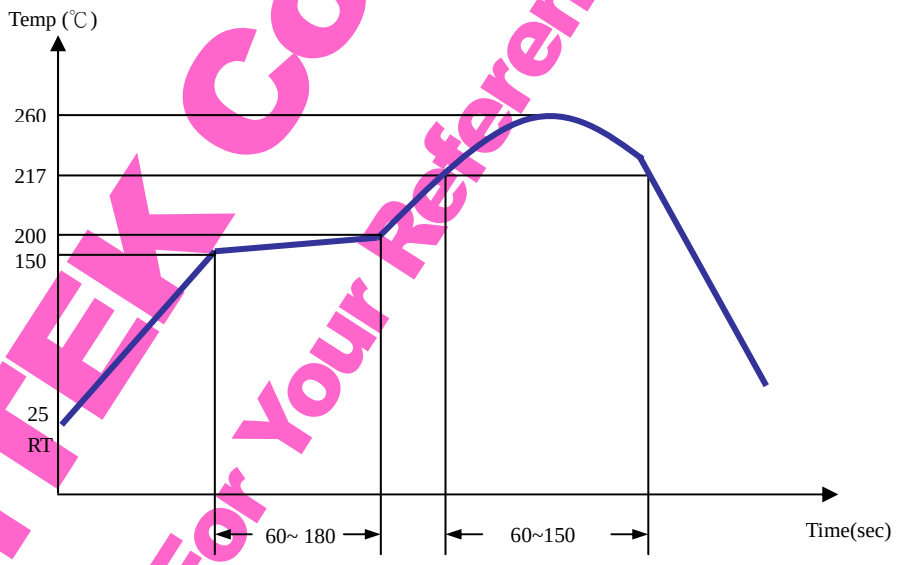
Reflow Soldering:

The choice of heating method may be influenced by plastic QFP package). If infrared or vapor phase heating is used and the package is not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stenciling or pressure-syringe dispensing before package placement. Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferable be kept below 245 °C for thick/large packages (packages with a thickness ≧ 2.5 mm or with a volume ≧ 350 mm^3 so called thick/large packages). The top-surface temperature of the packages should preferable be kept below 260 °C for thin/small packages (packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called thin/small packages).

Stage	Condition	Duration
1'st Ram Up Rate	max3.0+/-2℃/sec	-
Preheat	150℃~200℃	60~180 sec
2'nd Ram Up	max3.0+/-2℃/sec	-
Solder Joint	217℃ above	60~150 sec
Peak Temp	260 +0/-5℃	20~40 sec
Ram Down rate	6℃/sec max	-



Wave Soldering:

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

Manual Soldering:

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Order Information:

BIT3206-SO

SO: SOP

Part number

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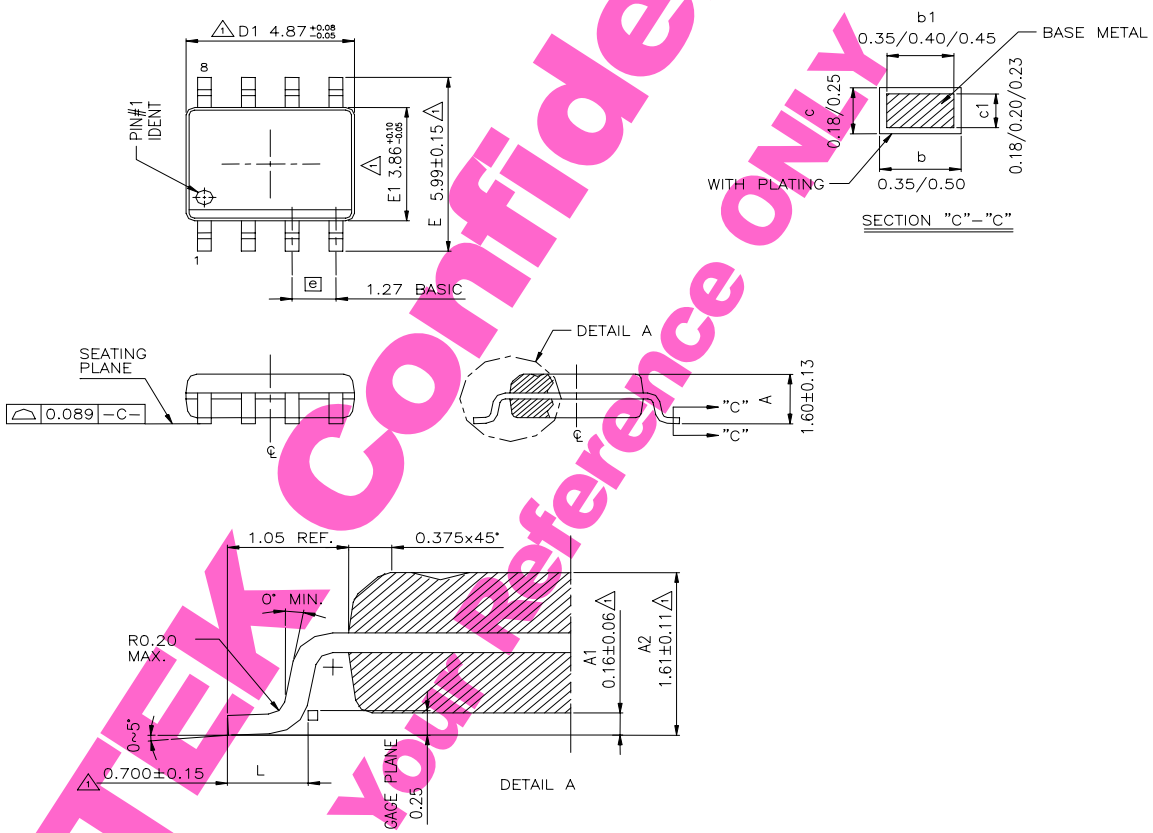
Package Information :

Unit: mm

SOP type :



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