AN-6052 — Instructions for the Multi-Phase VR11 MathCad® Design Tool

Summary

This purpose of this application note is to assist design and optimization of the applicable devices to the meet critical dynamic performance requirements of multi-phase in VR implementations. This application note should be used in conjunction with the associated Mathcad® Design Tool, Revision 10/20/05. Please check with Fairchild Semiconductor for latest design tool and availability.

Applications

- Desktop PC / server processor power supplies for existing and next-generation Intel processors
- VRM modules

Note: Highlighted fields are required.

Related Devices

FAN5019, FAN5031, FAN5032, FAN5032B, FAN5033, FAN50FC3

Input Parameters

Vin := 12 — Input voltage (V)

Vo := 1.20 — Output voltage (V)

Iomax := 125 — Max. output current (A)

η := 83% — Estimated converter efficiency at maximum load

$D := \frac{Vo}{Vin \cdot \eta}$ D = 0.120 — Duty cycle

$fs := 300 \cdot 10^{3}$ — Per-phase switching frequency (Hz)

$Ts := \frac{1}{fs}$ $Ts = 3.333 \times 10^{-6}$ — Per-phase switching period

Np := 5 — Number of phases

$Ro := \frac{Vo}{Iomax}$ $Ro = 9.600 \times 10^{-3}$

$Irms := Iomax \cdot \sqrt{\frac{D}{Np} - D^{2}}$ Irms = 12.235

Choose input capacitors based on this input RMS current.

Select inductor peak-to-peak ripple current from 25% to 55%.

iripple := 33.5% — Per-phase inductor peak-to-peak ripple current percentage

$Iripple := \frac{Iomax}{Np} \cdot iripple$ Iripple = 8.375 — Per-phase inductor peak-to-peak ripple current (A)

$L := \frac{(1 - D)}{fs} \cdot \frac{Vo \cdot Np}{Iomax \cdot iripple}$ $L = 4.201 \times 10^{-7}$

$L := 0.44 \cdot 10^{-6}$ — Per-phase inductance (at 0A load)

kL := 0.91 — Inductor roll-off factor at maximum load

$L := \frac{L \cdot kL}{Np}$ $L = 8.008 \times 10^{-8}$ Equivalent Np phase inductance

$RL := 0.83 \cdot 10^{-3}$ Per-phase inductor series resistance (ohm)

$RL := \frac{RL}{Np}$ Np phase equivalent inductor series resistance (ohm)

$C := 560 \cdot 10^{-6}$ Enter single output bulk capacitance (F)

$Ncbulk := 10$ Number of output bulk capacitors

$C := C \cdot Ncbulk$ $C = 5.600 \times 10^{-3}$ Np phase (total) output bulk capacitance (F)

$Rc := 5 \cdot 10^{-3}$ Single output bulk capacitor ESR (ohm)

$Rc := \frac{Rc}{Ncbulk}$ $Rc = 5.000 \times 10^{-4}$ Np phase equivalent output bulk capacitor ESR (ohm)

$C2 := 22 \cdot 10^{-6}$ Enter single output ceramic capacitance (F)

$Ncceramic := 18$ Number of output ceramic capacitors

$C2 := \frac{C2}{Ncceramic}$ $C2 = 1.222 \times 10^{-6}$ Np phase (total) output ceramic capacitance (F)

$Rc2 := 2 \cdot 10^{-3}$ Single output ceramic capacitor ESR (ohm)

$Rc2 := \frac{Rc2}{Ncceramic}$ $Rc2 = 1.111 \times 10^{-4}$ Np phase equivalent output ceramic capacitor ESR (ohm)

$Ronbot := 2.5 \cdot 10^{-3}$ R_{dson} of equivalent bottom MOSFET (ohm) - (R_{dson} / # of bot FETs per phase)

$Ric := \frac{Ronbot}{Np}$ $Ric = 5.000 \times 10^{-4}$ Equivalent Np phase i balance sense resistance (ohm)

$Gsw := 5$ Switch amplifier gain

$Ri := \frac{Ronbot}{Np} \cdot Gsw$ $Ri = 2.500 \times 10^{-3}$ Equivalent Np phase current sense gain (ohm)

$Sn := \frac{(Vin - Vo)}{L} \cdot Ri$ $Sn = 3.372 \times 10^{5}$ Sensed Np phase equivalent inductor rising slope (V/s)

$Rramp := 274 \cdot 10^{3}$ Input ramp resistance (ohm) - See the Appendix for Rramp design

$Se(Iomax) := \frac{Vin - Vo}{Rramp + 2 \cdot 10^{3}} \cdot \frac{0.2}{5 \cdot 10^{-12}} - Sn$ External ramp (V/s)

$Mc(Iomax) := 1 + \frac{Se(Iomax)}{Sn}$ $Mc(Iomax) = 4.642$ External ramp parameter

$Fm(Iomax) := \frac{1}{(Sn + Se(Iomax)) \cdot Ts}$ $Fm(Iomax) = 0.192$ Modulator Gain

$n := 600$ $i := 0..n$

$min := 1000$ Input Bode Plot start frequency (Hz)

$max := 10^{6}$ Input Bode Plot end frequency (Hz)

$$r := \ln\left(\frac{max}{min}\right) \qquad s_i := min \cdot e^{i \cdot \frac{r}{n}} \qquad j := \sqrt{-1}$$

Open-Loop Transfer Function Definition

$sz1 := \frac{1}{Rc \cdot C}$	$fz1 := \frac{sz1}{2 \cdot \pi}$	$fz1 = 5.684 \times 10^4$	Output bulk capacitor ESR zero (Hz)
$sz2 := \frac{1}{Rc2 \cdot C2}$	$fz2 := \frac{sz2}{2 \cdot \pi}$	$fz2 = 1.172 \times 10^9$	Output ceramic capacitor ESR zero (Hz)
$wo := \frac{1}{\sqrt{L \cdot C}}$	$fo := \frac{wo}{2 \cdot \pi}$	$fo = 7.516 \times 10^3$	Open-loop power stage double poles (Hz)
$Q(Ro) := \frac{1}{wo} \cdot \frac{1}{\left(\frac{L}{Ro}\right) + C \cdot Rc}$		$Q(Ro) = 1.901$	Open-loop power stage damping factor

Open-Loop Control-to-Output Transfer Function F2(s)

$$A(Ro) := Rc \cdot Rc2 \cdot C \cdot C2 + \frac{L}{Ro} \cdot (Rc \cdot C + Rc2 \cdot C2) + L \cdot (C + C2)$$

$$B(Ro) := \frac{L}{Ro} \cdot Rc \cdot Rc2 \cdot C \cdot C2 + L \cdot C \cdot C2 \cdot (Rc + Rc2)$$

$$F2(s, Ro) := Vin \cdot \frac{(1 + s \cdot Rc \cdot C) \cdot (1 + s \cdot Rc2 \cdot C2)}{1 + s \cdot \left(Rc \cdot C + Rc2 \cdot C2 + \frac{L}{Ro}\right) + s^2 \cdot A(Ro) + s^3 \cdot B(Ro)}$$

$$magF2(i, Ro) := 20 \cdot \left(\log\left(\left|F2\left(s_i \cdot j \cdot 2 \cdot \pi, Ro\right)\right|\right)\right)$$

$$phaseF2(i, Ro) := angle\left(Re\left(F2\left(s_i \cdot j \cdot 2 \cdot \pi, Ro\right)\right), Im\left(F2\left(s_i \cdot j \cdot 2 \cdot \pi, Ro\right)\right)\right) \cdot \frac{180}{\pi} - 360$$

$$coef := \begin{pmatrix} 1 \\ Rc \cdot C + Rc2 \cdot C2 + \frac{L}{Ro} \\ A(Ro) \\ B(Ro) \end{pmatrix} \qquad polyroots(coef) = \begin{pmatrix} -1.396 \times 10^9 \\ -1.180 \times 10^4 - 4.449i \times 10^4 \\ -1.180 \times 10^4 + 4.449i \times 10^4 \end{pmatrix}$$

Open-Loop Output Impedance Zp(s)

$$Zp(s, Ro) := \frac{RL \cdot (1 + s \cdot Rc \cdot C) \cdot (1 + s \cdot Rc2 \cdot C2) \cdot \left(1 + s \cdot \frac{L}{RL}\right)}{1 + s \cdot \left(Rc \cdot C + Rc2 \cdot C2 + \frac{L}{Ro}\right) + s^2 \cdot A(Ro) + s^3 \cdot B(Ro)}$$

$$magZp(i, Ro) := 20 \cdot \left(\log\left(\left|Zp\left(s_i \cdot j \cdot 2 \cdot \pi, Ro\right)\right|\right)\right)$$

$$phaseZp(i, Ro) := angle\left(Re\left(Zp\left(s_i \cdot j \cdot 2 \cdot \pi, Ro\right)\right), Im\left(Zp\left(s_i \cdot j \cdot 2 \cdot \pi, Ro\right)\right)\right) \cdot \frac{180}{\pi}$$

Sampling Gain He(s)

$$Wn := \frac{\pi}{Ts} \qquad Qz := \frac{-2}{\pi}$$

$$He(s) := 1 + \frac{s}{Wn \cdot Qz} + \frac{s^2}{Wn^2}$$

$$Fi(s) := Ri \cdot He(s)$$

Current sense gain

$$magFi(i) := 20 \cdot \left(\log\left(\left| Fi\left(s_i \cdot j \cdot 2 \cdot \pi \right) \right| \right) \right)$$

$$phaseFi(i) := angle\left(Re\left(Fi\left(s_i \cdot j \cdot 2 \cdot \pi \right) \right), Im\left(Fi\left(s_i \cdot j \cdot 2 \cdot \pi \right) \right) \right) \cdot \frac{180}{\pi}$$

Open-Loop Transfer Function: F5(s) = iL/io

$$F5(s, Ro) := \frac{1}{\left(\frac{1}{Rc + \frac{1}{s \cdot C}} + \frac{1}{Rc2 + \frac{1}{s \cdot C2}} + \frac{1}{Ro} + \frac{1}{s \cdot L + RL} \right)} \cdot \frac{1}{s \cdot L + RL}$$

$$magF5(i, Ro) := 20 \cdot \left(\log\left(\left| F5\left(s_i \cdot j \cdot 2 \cdot \pi, Ro \right) \right| \right) \right)$$

$$phaseF5(i, Ro) := angle\left(Re\left(F5\left(s_i \cdot j \cdot 2 \cdot \pi, Ro \right) \right), Im\left(F5\left(s_i \cdot j \cdot 2 \cdot \pi, Ro \right) \right) \right) \cdot \frac{180}{\pi} - 360$$

Open-Loop Control-to-Inductor Current Transfer Function: F4(s) = iL/d

$$F4(s, Ro) := Vin \cdot \frac{1}{s \cdot L + RL + \frac{1}{\frac{s \cdot C}{1 + s \cdot Rc \cdot C} + \frac{s \cdot C2}{1 + s \cdot Rc2 \cdot C2} + \frac{1}{Ro}}}$$

$$magF4(i, Ro) := 20 \cdot \left(\log\left(\left| F4\left(s_i \cdot j \cdot 2 \cdot \pi, Ro \right) \right| \right) \right)$$

$$phaseF4(i, Ro) := angle\left(Re\left(F4\left(s_i \cdot j \cdot 2 \cdot \pi, Ro \right) \right), Im\left(F4\left(s_i \cdot j \cdot 2 \cdot \pi, Ro \right) \right) \right) \cdot \frac{180}{\pi} - 0$$

Voltage Compensator Gain Fv(s)

For most of applications using electrolytic-type dominant output capacitors, a 2-pole-1-zero compensator, consisting of R2, R3, C2, and C3 (as shown below), is sufficient to meet the VR dynamic requirements. A placeholder for a 3-pole-2-zero compensator is always recommended in the PCB layout to have flexibility to fine tune the VR performance.

For ceramic types of output capacitor dominant applications, a 3-pole-2-zero compensator is usually mandatory.

In this design example, electrolytic-type dominant output capacitors are used.

The compensator design adopts an interactive approach. In such a condition, the control design can be optimized through interactive tuning the compensator parameters through a few iterations.

As a good starting point, select the compensator zero to be around 1.5 ~ 3.5X open-loop, power-stage, double poles and select the high-frequency pole to be around 0.8 ~ 2.5X per phase switching frequency. The compensator high-frequency pole is placed to filter out high-frequency switching noise. It's not recommended to place it too close to the control bandwidth. Use the DC gain of ωI to adjust the control bandwidth.

Note that the compensator zero and DC gain are critical parameters that need to be fine-tuned interactively through a few iterations of this program.

$fzc1 := 22 \cdot 10^{3}$ Place the compensator zero to cancel the power stage pole (1.5 ~ 3.5X open loop power stage double poles) (Hz)

$\omega zc1 := 2 \cdot \pi \cdot fzc1$

$fzc2 := 7.5 \cdot 10^{15}$ To cancel the power stage pole (Hz)

$\omega zc2 := 2 \cdot \pi \cdot fzc2$

$fpc1 := 700 \cdot 10^{3}$ To be placed around 0.8 ~ 2.5X the per-phase switching frequency (Hz)

$\omega pc1 := 2 \cdot \pi \cdot fpc1$

$fpc2 := 1 \cdot 10^{15}$ To cancel the lower power stage ESR zero (Hz)

$\omega pc2 := 2\pi \cdot fpc2$

$\omega I := 2.068 \, 10^{6}$ Cross over frequency adjustment

$$Fv(s) := \frac{\omega I \cdot \left(1 + \frac{s}{\omega zc1}\right) \cdot \left(1 + \frac{s}{\omega zc2}\right)}{s \cdot \left(1 + \frac{s}{\omega pc1}\right)\left(1 + \frac{s}{\omega pc2}\right)}$$

Input the 1% feedback resistor (R_{fb}) first. Instructions of how to calculate R_{fb} can be found in the Appendix.

$R2 := 1.24 \, 10^{3}$ Input R2 (R_{fb} - 1% resistor) here (ohm).
See the Appendix section for how to calculate R_{fb}.

Given

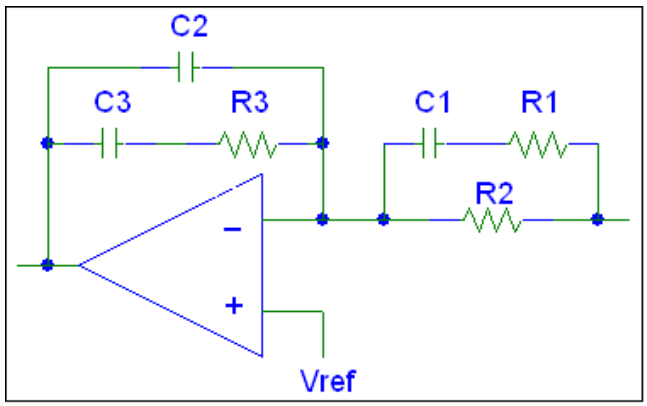
$$\frac{1}{R3 \cdot C3} = \omega zc1$$

$$\frac{1}{(R1 + R2) \cdot C1} = \omega zc2$$

$$\frac{1}{R3 \cdot C2 \cdot C3}(C2 + C3) = \omega pc1$$

$$\frac{1}{R1 \cdot C1} = \omega pc2$$

$$\frac{1}{R2 \cdot (C2 + C3)} = \omega I$$



$$Find(C1, C2, C3, R1, R3) \rightarrow \begin{pmatrix} -1.1123732581691609489 \cdot 10^{-19} \\ 1.2256103539562702226 \cdot 10^{-11} \\ 3.7771082726470509587 \cdot 10^{-10} \\ -1430.7692307692307692 \\ 19153.053269548560820 \end{pmatrix}$$

Calculated C1 (F)
Calculated C2 (F)
Calculated C3 (F)
Calculated R1 (ohm)
Calculated R3 (ohm)

Select the closed 1% resistors and NPO- or X7R-type capacitors as the compensator elements. If the calculated value is either less than 1pF or negative, these components are not necessary. It is a good practice to have at least 10pF capacitance for C2.

Select:

$C2 := 12 \cdot 10^{-12}$ Input capacitance closing to the above calculated compensator value (F)

$C3 := 0.39 \cdot 10^{-9}$ Input capacitance closing to the above calculated compensator value (F)

$R3 := 18.2 \cdot 10^{3}$ Input resistance closing to the above calculated compensator value (ohm)

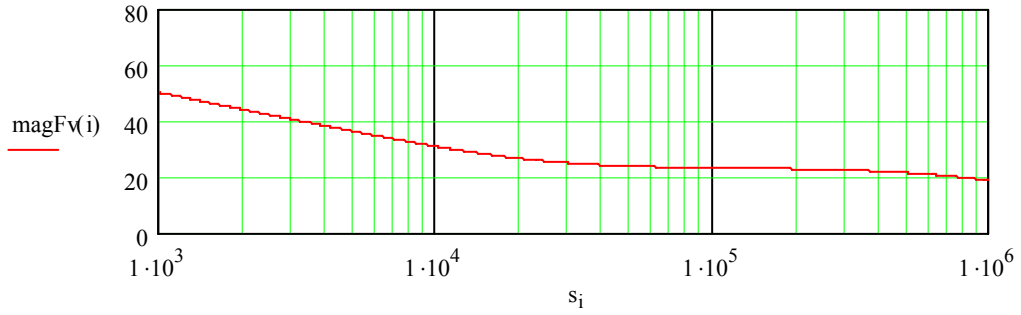
$C1 := 4.7 \cdot 10^{-18}$ Input capacitance closing to the above calculated compensator value (F)

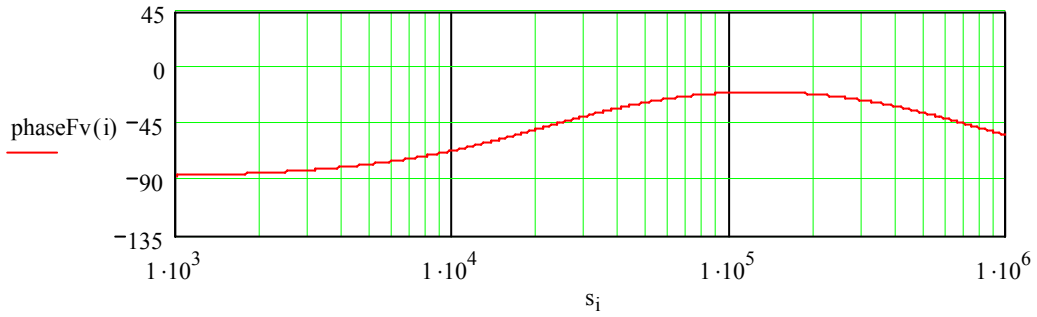
$R1 := 0.000001 \cdot 10^{3}$ Input resistance closing to the above calculated compensator value (ohm)

$$Fv(s) := \frac{(1 + s \cdot R3 \cdot C3) \cdot [1 + s \cdot (R1 + R2) \cdot C1]}{\left[\frac{1}{25000} + s \cdot R2 \cdot (C2 + C3)\right] \cdot \left(1 + s \cdot R3 \cdot \frac{C2 \cdot C3}{C2 + C3}\right) \cdot (1 + s \cdot R1 \cdot C1)}$$

$$magFv(i) := 20 \cdot \log\left(\left|Fv\left(s_i \cdot j \cdot 2 \cdot \pi\right)\right|\right)$$

$$phaseFv(i) := \frac{180}{\pi} \cdot angle\left(Re\left(Fv\left(s_i \cdot j \cdot 2 \cdot \pi\right)\right), Im\left(Fv\left(s_i \cdot j \cdot 2 \cdot \pi\right)\right)\right) - 360$$





Current Loop Gain Ti & Voltage Loop Gain Tv

$$Ti(s, Ro) := Fm(Iomax) \cdot Fi(s) \cdot F4(s, Ro)$$

$$Tv(s, Ro) := Fm(Iomax) \cdot Fv(s) \cdot F2(s, Ro)$$

$$magTi(i, Ro) := 20 \cdot \left(\log\left(\left|Ti\left(s_i \cdot j \cdot 2 \cdot \pi, Ro\right)\right|\right)\right)$$

$$phaseTi(i, Ro) := angle\left(Re\left(Ti\left(s_i \cdot j \cdot 2 \cdot \pi, Ro\right)\right), Im\left(Ti\left(s_i \cdot j \cdot 2 \cdot \pi, Ro\right)\right)\right) \cdot \frac{180}{\pi}$$

$$magTv(i, Ro) := 20 \cdot \left(\log\left(\left|Tv\left(s_i \cdot j \cdot 2 \cdot \pi, Ro\right)\right|\right)\right)$$

$$phaseTv(i, Ro) := angle\left(Re\left(Tv\left(s_i \cdot j \cdot 2 \cdot \pi, Ro\right)\right), Im\left(Tv\left(s_i \cdot j \cdot 2 \cdot \pi, Ro\right)\right)\right) \cdot \frac{180}{\pi} - 360$$

Overall Loop Gain T1

$$T1(s,Ro) := Tv(s,Ro) + Ti(s,Ro)$$

$$magT1(i,Ro) := 20\cdot\left(\log\left(\left|T1\left(s_i\cdot j\cdot 2\cdot\pi, Ro\right)\right|\right)\right)$$

$$phaseT1(i,Ro) := angle\left(Re\left(T1\left(s_i\cdot j\cdot 2\cdot\pi, Ro\right)\right), Im\left(T1\left(s_i\cdot j\cdot 2\cdot\pi, Ro\right)\right)\right)\cdot\frac{180}{\pi} - 180$$

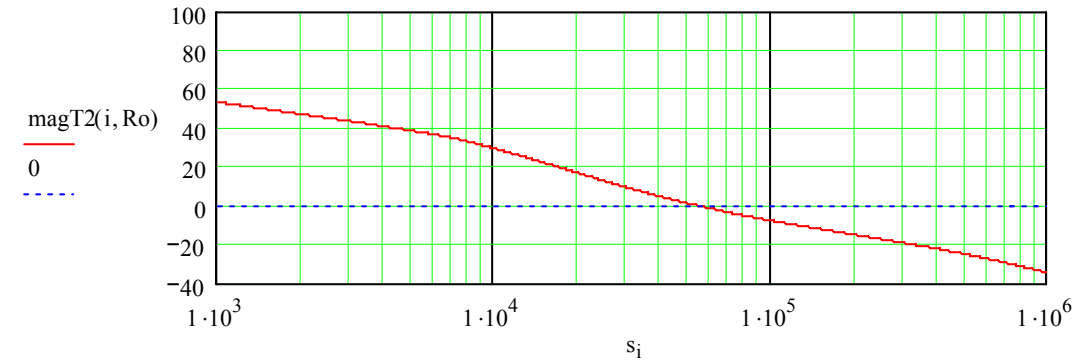
Outer Loop Gain T2

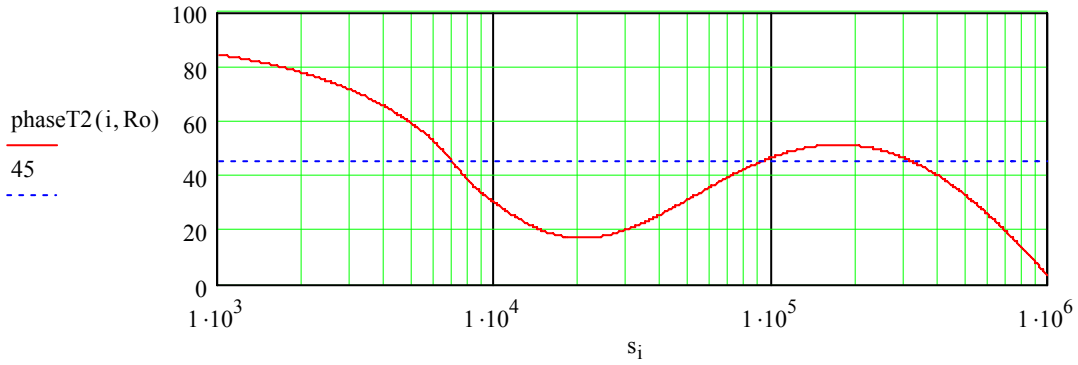
$$T2(s,Ro) := \frac{Tv(s,Ro)}{1 + Ti(s,Ro)}$$

$$magT2(i,Ro) := 20\cdot\left(\log\left(\left|T2\left(s_i\cdot j\cdot 2\cdot\pi, Ro\right)\right|\right)\right)$$

$$phaseT2(i,Ro) := angle\left(Re\left(T2\left(s_i\cdot j\cdot 2\cdot\pi, Ro\right)\right), Im\left(T2\left(s_i\cdot j\cdot 2\cdot\pi, Ro\right)\right)\right)\cdot\frac{180}{\pi} - 180$$

$$phaseT2(i,Ro) := \begin{cases} phaseT2(i,Ro) & \text{if } phaseT2(i,Ro) < 180 \\ phaseT2(i,Ro) - 360 & \text{otherwise} \end{cases}$$





$$magT2(0,Ro) = 53.267$$

Guess: $m := 300$

Given

$$20\cdot\left(\log\left(\left|T2\left(\min\cdot e^{m\cdot\frac{r}{n}}\cdot j\cdot 2\cdot\pi, Ro\right)\right|\right)\right) = 0$$

$m := \text{round}(\text{Find}(m))$

$m = 347.000$

$s_m = 5.433\times 10^4$

$fcrossT2 := s_m$

$fcrossT2 = 5.433\times 10^4$

T2 Crossover Frequency:

$$PmarginT2 := 0 + phaseT2(m,Ro)$$

T2 Phase Margin:

$PmarginT2 = 33.246$

Droop Loop Gain T_{drp}

$Ridrp := RL$ Droop current sense resistance = Inductor DCR / Number of Phase

Input the following droop amplifier component values for Rcs, Rph, and Ccs. Please see the Appendix for instructions of how to calculate component values.

$Rcs := 97.3 \cdot 10^{3}$ Input droop amplifier component value here (ohm)

$Rph := 82.5 \cdot 10^{3}$ Input droop amplifier component value here (ohm)

$$Rph := \frac{Rph}{Np}$$

$Ccs := 3.3 \cdot 10^{-9} + 1.5 \cdot 10^{-9}$ Droop amplifier component value (F)

$$Fdrp(s) := \frac{\left(1 + s \cdot \frac{L}{RL}\right)}{1 + s \cdot Rcs \cdot Ccs} \cdot \frac{Rcs}{Rph}$$

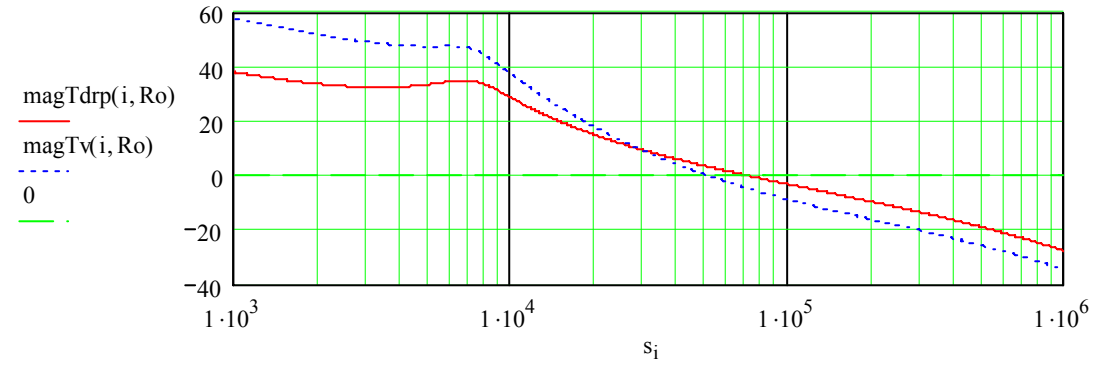
To simplify the analysis, assume that the droop amplifier time constant Rcs*Ccs exactly matches the inductor time constant L/RL, allowing the above equation to be reduced to a simple gain.

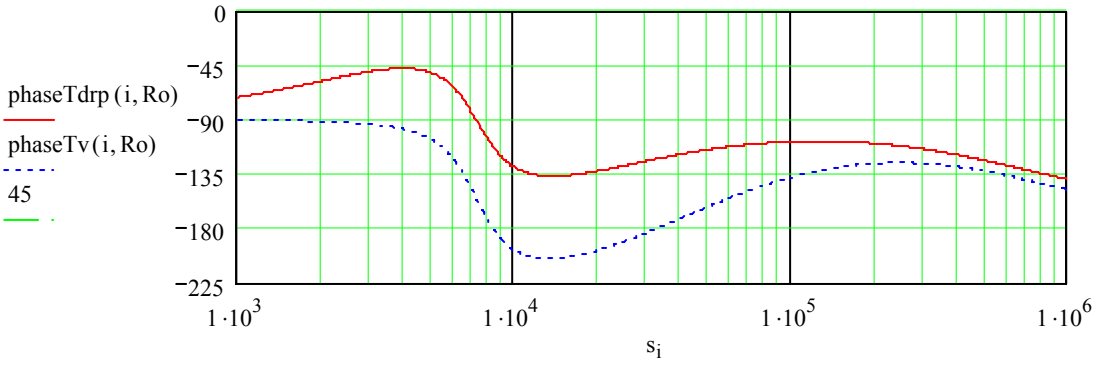
$$Fdrp(s) := \frac{Rcs}{Rph}$$

$$Tdrp(s, Ro) := F4(s, Ro) \cdot Ridrp \cdot Fdrp(s) \cdot (1 + Fv(s)) \cdot Fm(Mc)$$

$$magTdrp(i, Ro) := 20 \cdot \left(\log\left(\left|Tdrp\left(s_i \cdot j \cdot 2 \cdot \pi, Ro\right)\right|\right)\right)$$

$$phaseTdrp(i, Ro) := angle\left(Re\left(Tdrp\left(s_i \cdot j \cdot 2 \cdot \pi, Ro\right)\right), Im\left(Tdrp\left(s_i \cdot j \cdot 2 \cdot \pi, Ro\right)\right)\right) \cdot \frac{180}{\pi} - 360$$





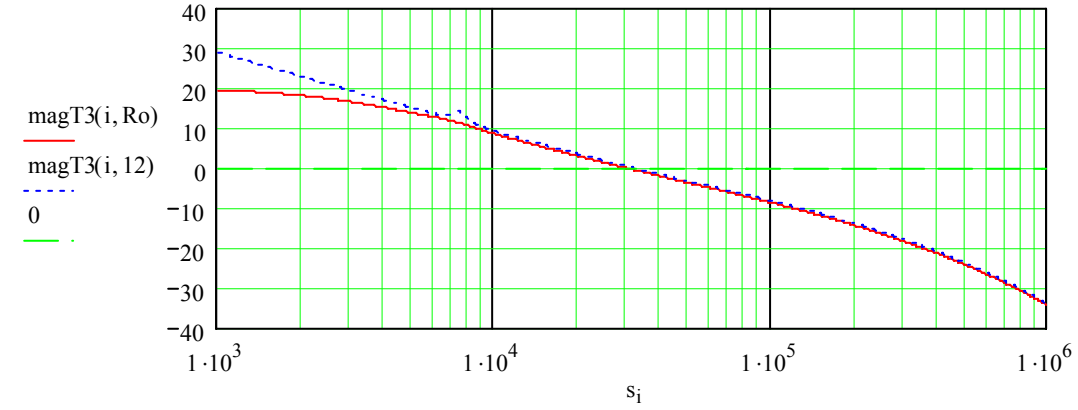
Outer Loop Gain T3 (T2 with Droop Loop Closed)

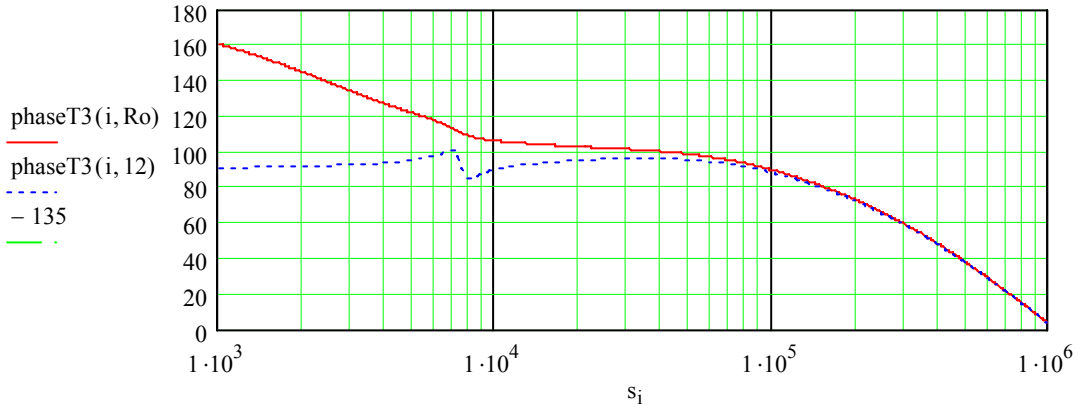
$$T3(s,Ro) := \frac{Tv(s,Ro)}{1 + Ti(s,Ro) + Tdrp(s,Ro)} \cdot 1.0$$

$$magT3(i,Ro) := 20 \cdot \left(\log\left(\left| T3\left(s_i \cdot j \cdot 2 \cdot \pi, Ro \right) \right| \right) \right)$$

$$phaseT3(i,Ro) := angle\left(Re\left(T3\left(s_i \cdot j \cdot 2 \cdot \pi, Ro \right) \right), Im\left(T3\left(s_i \cdot j \cdot 2 \cdot \pi, Ro \right) \right) \right) \cdot \frac{180}{\pi} - 180$$

The solid and dotted lines in the following picture represent closed outer loop gain at the maximum load and light load (= V_{IN} / 12 (A)) respectively.





$magT3(0,Ro) = 19.427$

Guess: $m := 350$

Given

$$20 \cdot \left(\log\left(\left| T3\left(\min \cdot e^{m \cdot \frac{r}{n}} \cdot j \cdot 2 \cdot \pi, Ro \right) \right| \right) \right) = 0$$

$m := \text{round}(\text{Find}(m))$

$m = 295.000$

$s_m = 2.985 \times 10^4$

$fcrossT3 := s_m$

T3 Crossover Frequency: @ the max load

(Hz)

$fcrossT3 = 2.985 \times 10^4$

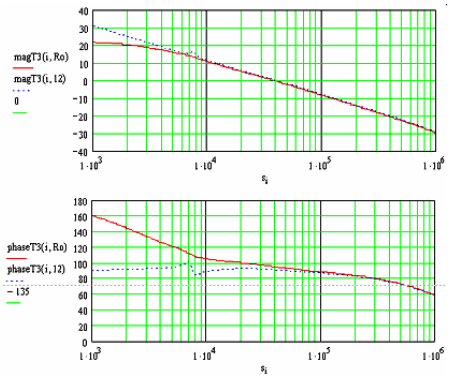
$PmarginT3 := 0 + phaseT3(m,Ro)$

T3 Phase Margin @ the max load:

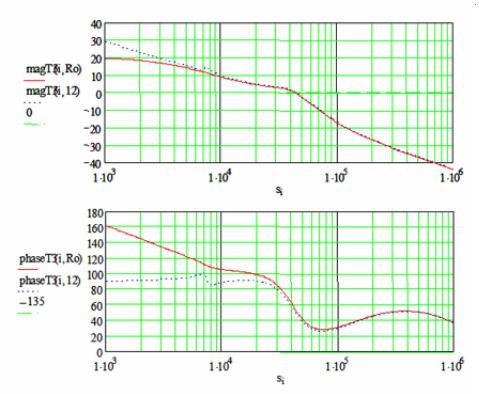
(deg)

$PmarginT3 = 101.354$

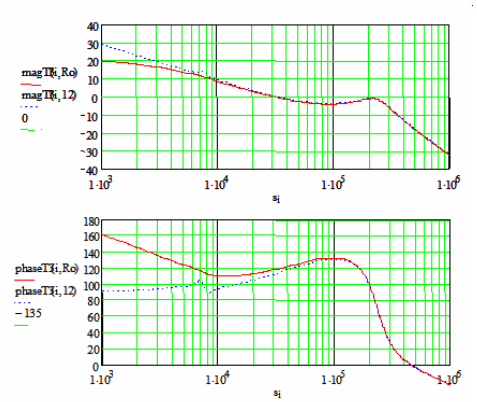
If the compensator zero is properly placed, the closed outer loop gain, T3, looks like the following plot with -1 (-20dB/decade) slope. In this case, proceed and check the closed-loop output impedance plot in the following section to ensure good dynamic performance. Generally, there's no need for the closed outer loop bandwidth to be higher than the bulk capacitor ESR zero frequency.



If the compensator zero is placed too high, the following T3 behavior appears (left picture). The zero has to be moved to lower frequency. If the compensator zero is placed too low, the outer loop gain plot looks like the right picture and the zero has to be moved to higher frequency. Tune the zero placement until the closed outer loop gain has -1 (-20dB/decade) slope. Improper placement of the compensator zero can also affect the closed output impedance.



Zero Too High



Zero Too Low

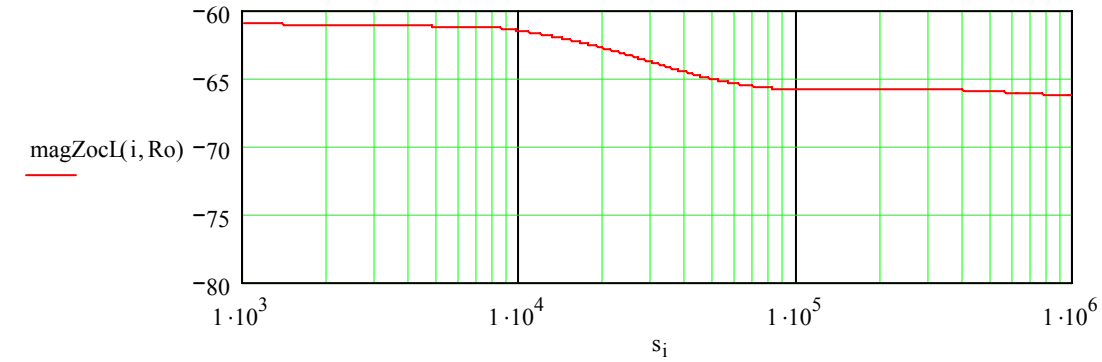
Closed-Loop Output Impedance with Droop ZocL

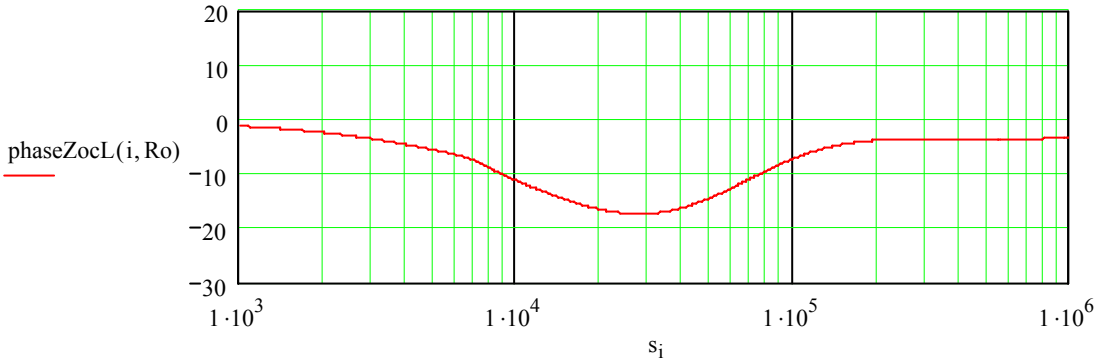
$$ZocL(s,Ro) := \frac{Zp(s,Ro)\cdot(1 + Ti(s,Ro) + Tdrp(s,Ro)) + \frac{F2(s,Ro)\cdot F5(s,Ro)\cdot(Ti(s,Ro) + Tdrp(s,Ro))}{F4(s,Ro)}}{1 + Ti(s,Ro) + Tv(s,Ro) + Tdrp(s,Ro)}$$

$$magZocL(i,Ro) := 20\cdot\left(\log\left(\left|ZocL\left(s_i\cdot j\cdot 2\cdot\pi, Ro\right)\right|\right)\right)$$

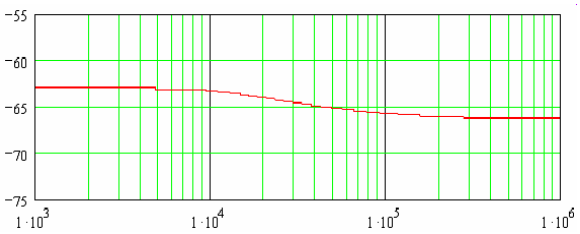
$$phaseZocL(i,Ro) := angle\left(Re\left(ZocL\left(s_i\cdot j\cdot 2\cdot\pi, Ro\right)\right), Im\left(ZocL\left(s_i\cdot j\cdot 2\cdot\pi, Ro\right)\right)\right)\cdot\frac{180}{\pi} - 0$$

$$phaseZocL(i,Ro) := \begin{cases} phaseZocL(i,Ro) & \text{if } phaseZocL(i,Ro) < 180 \\ phaseZocL(i,Ro) - 360 & \text{otherwise} \end{cases}$$

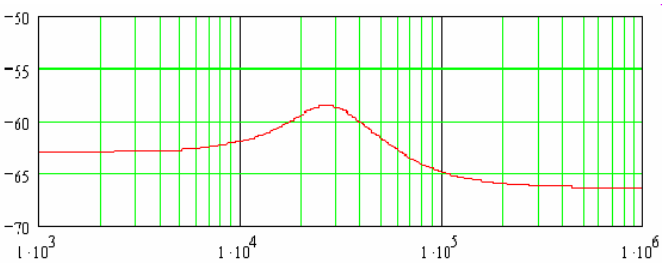


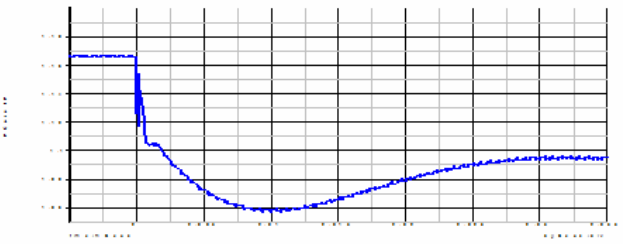


The ideal magnitude of the closed-loop output impedance plot should be close to the following plot; constant impedance at low frequency and monotonic close to or above the closed-loop control bandwidth.



If the magnitude of the closed-loop output impedance has an upward bump as shown in the following left picture, the closed-loop control bandwidth is too low. As a result, during load transient response, the output voltage has delayed response, as shown in the below right picture. In such a case, go back to the voltage compensator section and increase the compensator DC gain to extend the control bandwidth until the monotonic-like output impedance plot is achieved.

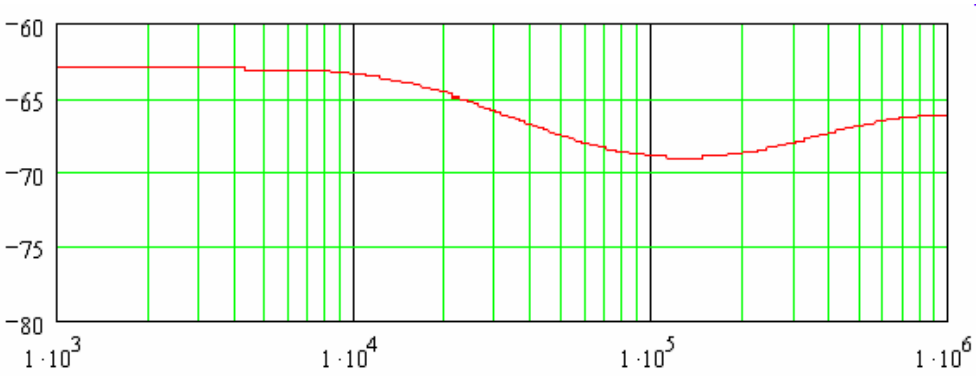




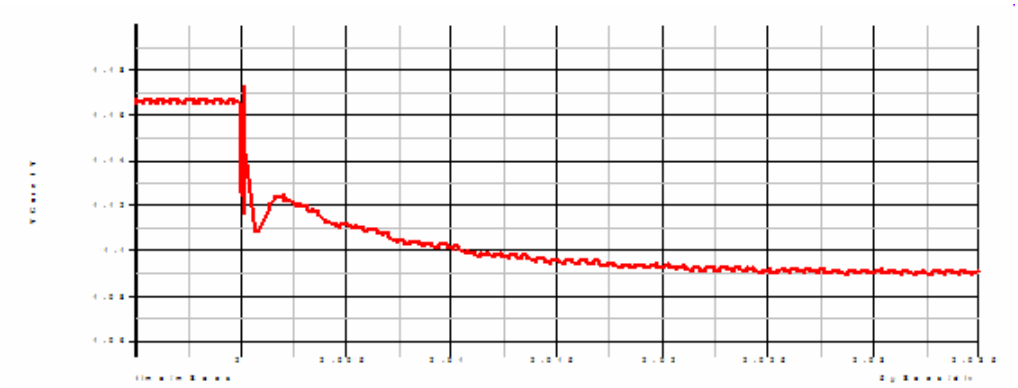
If the magnitude of the closed-loop output impedance has a downward bump, as shown in the below left picture, the closed-loop control bandwidth is too high. During load transient response, the output voltage ends up with ringing back (which may violate the VR specifications), as shown in the below right picture. In this case, go back to the voltage compensator and decrease the compensator DC gain until the monotonic-like output impedance plot is achieved.

Exercise the compensator zero placement and its DC gain in an interactive manner and run iterations until achieving satisfactory -1 (-20dB/decade) closed-loop outer-loop gain and monotonic-like closed-loop output impedance.

Change the input voltage to low and high lines and check the stability in these corner conditions. Minor adjustment / compromise may be necessary if there are problems at the high and low lines.



Bandwidth Too High



Ringing

Once the paper design is complete, start a bench test. Before measuring the loop gain on bench, the following procedures and test items should be satisfied. Any of the following factors can shift or distort the outer-loop gain Bode plot. Please see the Appendix for the droop amplifier and its component designation.

1. Tune phase-current balance until the load current is roughly equally distributed among phases.
2. Tune the thermistor temperature compensation by trimming Rcs2 (in general) to ensure that the output voltage doesn't change at TDC and given airflow, if any, from the system.
3. Tune the load line slope to meet the VR specifications by trimming R_{ph} resistance.
4. Tune droop amplifier component C_{CS} to match the inductor and its DCR time constant.

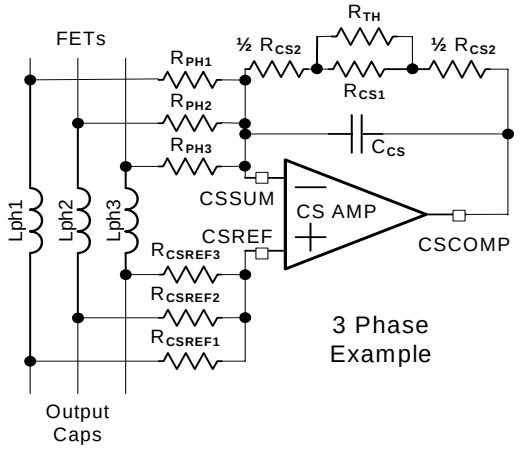
With regard to Step 4, since the inductor time constant L/RL is long, tune the droop amplifier R_{CS}*C_{CS} time constant through an electronic load instead of V_{TT}-type loads. Set the electronic load to constant current and dynamic mode with slew rate at 1A/µs or above. Set the load step from light load to half of full load. Zoom in and monitor the output voltage response to the electronic load step changing. If the output has an overshoot to the load step change, increase the C_{CS} slightly. Similarly, if the output shows over-damped response, decrease the C_{CS} slightly. Since it's hard to justify the output response at over-damped conditions, to simplify the tuning, start with a small C_{CS} (under damped) and slightly increase it until critical damped response is observed. Since there are only limited standard capacitor values available, select a higher capacitor rather than a lower one if there has to be compromise. As long as the output has a critical damped response to a load step change, the C_{CS} is the correct value to use to match the L/RL time constant.

Appendix A

Inductor DCR Temperature Compensation

In FAN50xx VR design, the inductor winding is used as the current-sense element to program the load line. Since the copper resistance of the inductor winding (DCR) has a positive temperature coefficient of 0.39%/°C, it's necessary to compensate the DCR variation due to temperature change by using a thermistor to improve current sense and load line accuracy.

Due to the nonlinear nature of a NTC thermistor, resistors Rcs1 and Rcs2 are required to linearize the NTC thermistor resistance and produce the desired compensation strength.



Select a NTC to be used based on type and value. Start with a thermistor with a value close to R_{CS}. The NTC should have an initial tolerance of greater than 5%.

$TC := 0.39\%$

Copper temperature coefficient

$Rcs := 100 \cdot 10^{3}$

Input desired Rcs resistance (ohm)

Based on the type of NTC selected, find its relative resistance value at two temperatures. The two temperatures recommended are 50°C and 90°C. Call these resistance values A (Rth(50°C)/Rth(25°C)) and B (Rth(90°C)/Rth(25°C)). Note that the NTC's relative value is always 1 at 25°C.

$T1 := 50$

$T2 := 90$

$Rth := 100 \cdot 10^{3}$

Input an initial thermistor value at 25°C (ohm)
(Panasonic, ERT-J1V V104J)

$A := 0.2954$

A = Rth50/25

$B := 0.05684$

B = Rth90/25

Find the relative value of R_{CS} required for each of these temperatures.

$$r1 := \frac{1}{1 + TC \cdot (T1 - 25)}$$

r1 = 0.911

$r2 := \frac{1}{1 + TC \cdot (T2 - 25)}$ $r2 = 0.798$

$rcs2 := \frac{(A - B) \cdot r1 \cdot r2 - A \cdot (1 - B) \cdot r2 + B \cdot (1 - A) \cdot r1}{A \cdot (1 - B) \cdot r1 - B \cdot (1 - A) \cdot r2 - (A - B)}$ Compute the relative value for Rcs2

$rcs2 = 0.743$

$rcs1 := \frac{1 - A}{\frac{1}{1 - rcs2} - \frac{A}{r1 - rcs2}}$ $rcs1 = 0.330$ Compute the relative value for Rcs1

$rth := \frac{1}{\frac{1}{1 - rcs2} - \frac{1}{rcs1}}$ $rth = 1.165$ Compute the relative value for Rth

$Rthc := rth \cdot Rcs$ $Rthc = 1.165 \times 10^{5}$

$Rth := 100 \cdot 10^{3}$ Select an available thermistor at 25°C (ohm)

$k := \frac{Rth}{Rthc}$ $k = 0.859$

$Rcs1 := Rcs \cdot k \cdot rcs1$ $Rcs1 = 2.837 \times 10^{4}$

$Rcs2 := Rcs \cdot [(1 - k) + (k \cdot rcs2)]$ $Rcs2 = 7.790 \times 10^{4}$

Select:

$Rcs1 := 28.7 \cdot 10^{3}$ Select the closest 1% resistor for Rcs1 (ohm)

$Rcs2 := 75 \times 10^{3}$ Select the closest 1% resistor for Rcs2 (ohm)

Output Voltage Set-Point

Intel's specifications require that, at no load, the output voltage of the VR be offset to a lower value than the nominal voltage corresponding to the VID code. The offset is set by a constant current source flowing out of the FB pin (Ifb) and flowing through feedback resistor Rfb.

$Ifb := 15 \cdot 10^{-6}$

$Vtob := 19 \cdot 10^{-3}$ Input desired amount of offset (V)

$Rfb := \frac{Vtob}{Ifb}$ $Rfb = 1.267 \times 10^{3}$ Calculated feedback resistance (ohm)

$Rfb := 1.24 \cdot 10^{3}$ Select the closest 1% resistor for Rfb (ohm)

Droop Amplifier Component Selection

$Rth = 1.000 \times 10^{5}$ Thermistor resistance at 25°C (ohm)

$Rcs1 := 28.7 \cdot 10^{3}$ Droop amplifier component (ohm)

$Rcs2 := 75 \times 10^{3}$ Droop amplifier component (ohm)

$Rcs := \frac{Rth \cdot Rcs1}{Rth + Rcs1} + Rcs2$ $Rcs = 9.730 \times 10^{4}$

$$Ccs := \frac{L}{(RL \cdot 1.0) \cdot Rcs} \qquad Ccs = 4.958 \times 10^{-9}$$

$Ccs := 1.5 \cdot 10^{-9} + 3.3 \cdot 10^{-9}$

Select available NPO / X7R capacitors (F)
Bench tuning determines the final capacitance to match inductor time constant

$RLL := 1 \cdot 10^{-3}$

Load line slope (ohm)

$$Rph := RL \cdot 1.0 \cdot \frac{Rcs \cdot Np}{RLL}$$

Individual phase node resistor (ohm)

$Rph := 82.5 \cdot 10^{3}$ $\qquad Rph = 8.076 \times 10^{4}$

Select 1% resistor (ohm)

Ramp Resistor Selection

$Vdac := 1.25$

Input DAC voltage somewhere in the middle of minimum and maximum set-points (V)

$$D := \frac{Vdac}{12}$$

Vramp peak-to-valley voltage can be selected from a few hundred mV to a couple of volts. Vramp selection can be layout dependent. Select a small Vramp for a good PCB layout to enforce good phase current balance. If the PCB noise level is high, pick a relatively high Vramp for better signal-to-noise ratio, while compromising phase current balance performance slightly.

$Vramp := 0.55$

Input desired ramp peak-to-valley voltage at Vdac (V)

$$Rramp := \frac{0.2 \cdot Vdac \cdot (1 - D)}{fs \cdot Vramp \cdot 5 \cdot 10^{-12}}$$

$Rramp = 2.715 \times 10^{5}$

Calculated ramp resistance (ohm)

$Rramp := 274 \cdot 10^{3}$

Select 1% ramp resistor (ohm)

Once selecting a ramp resistor, verify Vramp at all operating conditions to make sure ramp peak-to-valley plus sensed phase current doesn't saturate the voltage error amplifier. Verify that it's not too low at the worst-case operation conditions as well.

$Vdac := 1.25$

Input DAC voltage around in the middle of min and max set-point (V)

$$D := \frac{Vdac}{Vin}$$

$$\frac{0.2 \cdot Vdac \cdot (1 - D)}{Rramp \cdot fs \cdot 5 \cdot 10^{-12}} = 0.545$$

Vramp peak-to-valley voltage (V)

$Vdac := 1.6$

Input the max DAC set-point (V)

$$D := \frac{Vdac}{Vin}$$

$$\frac{0.2 \cdot Vdac \cdot (1 - D)}{Rramp \cdot fs \cdot 5 \cdot 10^{-12}} = 0.675$$

Vramp peak-to-valley voltage at the max DAC set-point (V)

$VinH := 14$

Enter the max input voltage (V)

$D := \frac{Vdac}{VinH}$

$\frac{0.2 \cdot Vdac \cdot (1 - D)}{Rramp \cdot fs \cdot 5 \cdot 10^{-12}} = 0.690$ Vramp peak-to-valley voltage at the maximum DAC set-point (V)

$Vdac := 0.5$ Input the minimum DAC set-point (V)

$D := \frac{Vdac}{Vin}$

$\frac{0.2 \cdot Vdac \cdot (1 - D)}{Rramp \cdot fs \cdot 5 \cdot 10^{-12}} = 0.233$ Vramp peak-to-valley voltage at the minimum DAC set-point (V)

$VinL := 10$ Enter the minimum input voltage (V)

$D := \frac{Vdac}{VinL}$

$\frac{0.2 \cdot Vdac \cdot (1 - D)}{Rramp \cdot fs \cdot 5 \cdot 10^{-12}} = 0.231$ Vramp peak-to-valley voltage at the minimum DAC set-point (V)

Set the Clock Frequency (RT Selection)

$RT := \frac{1}{Np \cdot fs \cdot 3.9 \cdot 10^{-12}} - 13 \cdot 10^{3}$ $RT = 1.579 \times 10^{5}$

$RT := 147 \cdot 10^{3}$ Select 1% resistor (ohm)

Current Limit (RiLimit Selection)

$kocp := 130\%$ Define the OCP threshold

$Iocp := Iomax \cdot kocp$ $Iocp = 162.500$

$ViLimit := 1.7$

$RiLimit := ViLimit \cdot 2.5 \cdot 10^{3} \cdot \frac{Rph}{Np \cdot Rcs \cdot (RL \cdot 1.1) \cdot Iocp}$ $RiLimit = 9.716 \times 10^{4}$

$RiLimit := 100 \cdot 10^{3}$ Select:1% OCP resistor (ohm)

Verify the design over worst cases to ensure no false trip condition exists over parameter distribution. Make sure there is enough head room for dynamic response.

$ViLimit := 1.7$

$Iocp := ViLimit \cdot 2.5 \cdot 10^{3} \cdot \frac{Rph}{Np \cdot Rcs \cdot (RL \cdot 1.1) \cdot RiLimit}$ $Iocp = 157.877$ $\frac{Iocp}{Iomax} = 1.263$

$ViLimit := 1.6$ Min ViLimit (V) (refer to datasheet)

$Iocp := ViLimit \cdot 2.5 \cdot 10^{3} \cdot \frac{Rph}{Np \cdot Rcs \cdot (RL \cdot 1.1) \cdot RiLimit}$ $Iocp = 148.590$ $\frac{Iocp}{Iomax} = 1.189$

$ViLimit := 1.8$ Max ViLimit (V) (refer to datasheet)

$Iocp := ViLimit \cdot 2.5 \cdot 10^{3} \cdot \frac{Rph}{Np \cdot Rcs \cdot (RL \cdot 1.1) \cdot RiLimit}$ $Iocp = 167.164$ $\frac{Iocp}{Iomax} = 1.337$

Appendix B

Layout and Component Placement

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

General Recommendations

For good results, a PCB with at least four layers is recommended. This should allow the needed versatility for control circuitry interconnections with optimal placement, power planes for ground, input and output power, and wide interconnection traces in the remainder of the power delivery current paths. Keep in mind that each square unit of 1-ounce copper trace has a resistance of ~0.53mΩ at room temperature.

Whenever high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.

If critical signal lines (including output voltage sense lines) must cross through power circuitry; it is best if a signal ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making signal ground a bit noisier.

An analog ground plane should be used around and under the part as a reference for the components associated with the controller. This plane should be tied to the nearest output decoupling capacitor ground and should not be tied to any other power circuitry to prevent power currents from flowing in it.

The components should be located close to the controller with short traces. The most important traces to keep short and away from other traces are the FB and CSSUM pins. The output capacitors should be connected as close as possible to the load (or connector); for example, a microprocessor core that receives the power. If the load is distributed, the capacitors should also be distributed and generally be in proportion to where the load tends to be more dynamic.

Avoid crossing any signal lines over the switching power path loop, described in the following section.

Power Circuitry Recommendations

The switching power path is the loop formed by the current path through the input capacitors and the power MOSFETs, including all interconnecting PCB traces and planes. Using short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high-energy ringing, and it accommodates the high current demand with minimal voltage loss.

The switching power path should be routed on the PCB to encompass the shortest possible length to minimize radiated switching noise energy (i.e., EMI) and conduction losses in the board. Failure to take proper precautions result in EMI problems for the entire PC system as well as noise-related operational problems in the power converter control circuitry.

Whenever a power dissipating component, such as a power MOSFET, is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons are improved current rating through the vias and improved thermal performance from vias extended to the opposite side of the PCB, where a plane can more readily transfer the heat to the air. Make a mirror image of any pad being used to heatsink the MOSFETs on the opposite side of the PCB to achieve the best thermal dissipation to the air around the board. To further improve thermal performance, use the largest possible pad area.

The output power path should also be routed to encompass a short distance. The output power path is formed by the current path through the inductor, the output capacitors, and the load.

For best EMI containment, a solid power ground plane should be used as one of the inner layers, extending fully under all the power components.

Signal Circuitry Recommendations

The output voltage is sensed and regulated between the FB and FBRTN pins, which connect to the signal ground at the load. To avoid differential mode noise pickup in the sensed signal, the loop area should be small. The FB and FBRTN traces should be routed adjacent to each other on top of the power ground plane back to the controller.

The feedback traces from the switch nodes should be connected as close as possible to the inductor. The CSREF signal should be connected to the output voltage at the nearest inductor to the controller.

References

FAN5029 datasheet, available at http://www.fairchildsemi.com/pf/FA/FAN5029.html

FAN5031 datasheet, available at http://www.fairchildsemi.com/pf/FA/FAN5031.html

FAN5032 datasheet, available at http://www.fairchildsemi.com/pf/FA/FAN5032.html

FAN5032B datasheet, available at http://www.fairchildsemi.com/pf/FA/FAN5032b.html

FAN5033 datasheet, available at http://www.fairchildsemi.com/pf/FA/FAN5033.html

FAN50FC3 datasheet, available at http://www.fairchildsemi.com/pf/FA/FAN50FC3.html