CS8826(AF/AN/AM/BP)

16-Bit Constant current LED driver with 3.0V to 5.5V supply voltage

■ Description

The CS8826 is a 16-Bit constant current LED driver IC which is designed for LED displays. The output current can be adjusted by using an external resistor. All outputs will have the same current drive level which is crucial in LED display application. This driver has built-in 16-bit constant current outputs, a 16-bit shift register, and a 16-bit latch circuit. These drivers have been designed by using CMOS process.

■ Feature

- Output current capability: 60mA each output
- Constant current range: 5mA to 60mA
- For common anode LED application
- Power supply voltage range VDD=3.0V to 5.5V
- Maximum output drain voltage 7.0V
- Serial data transfer rate: 25Mhz(Cascade Connection)
- Operating temperature range: -40 to 85 degree C
- Current accuracy:

  Between Bits : < +-3 %

  Between ICs: < +-6%

■ Product Family

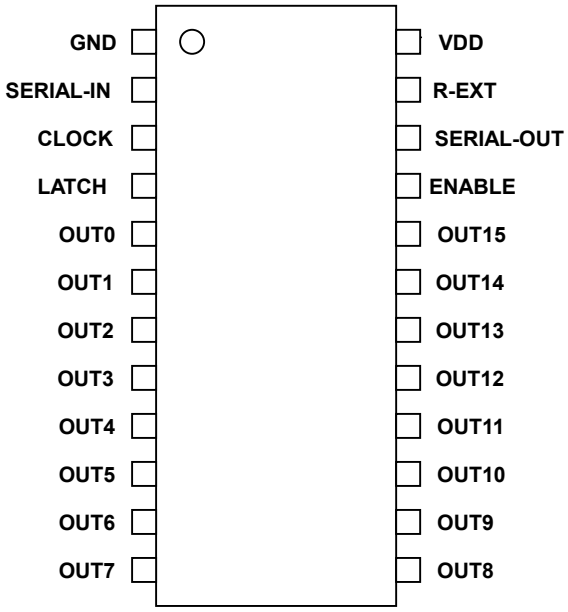
CS8826AF ------- 24SSOP(236mil, 1.0mm lead-pitch)

CS8826AN ------- 24SSOP(150mil, 0.64mm lead-pitch)

CS8826AM ------- 24SOP(300mil, 1.27mm lead-pitch)

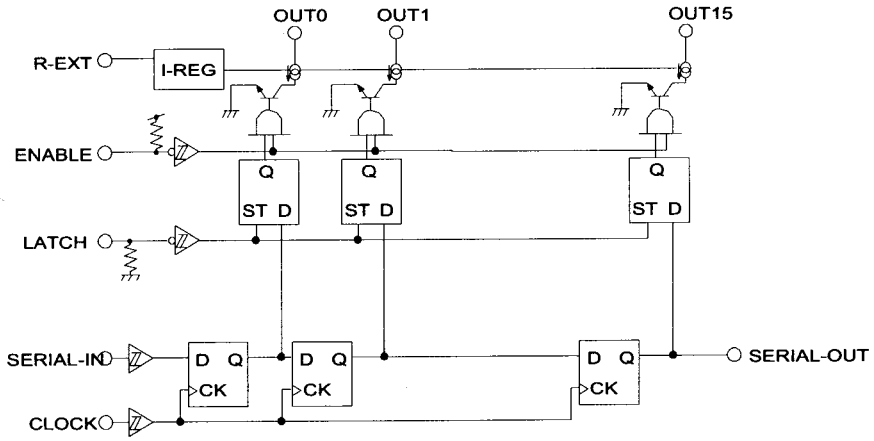
CS8826BP ------- 24PDIP(300mil, 2.54mm lead-pitch)

■ Pin Assignment



(AF/AN/AM/BP)

■ Block Diagram



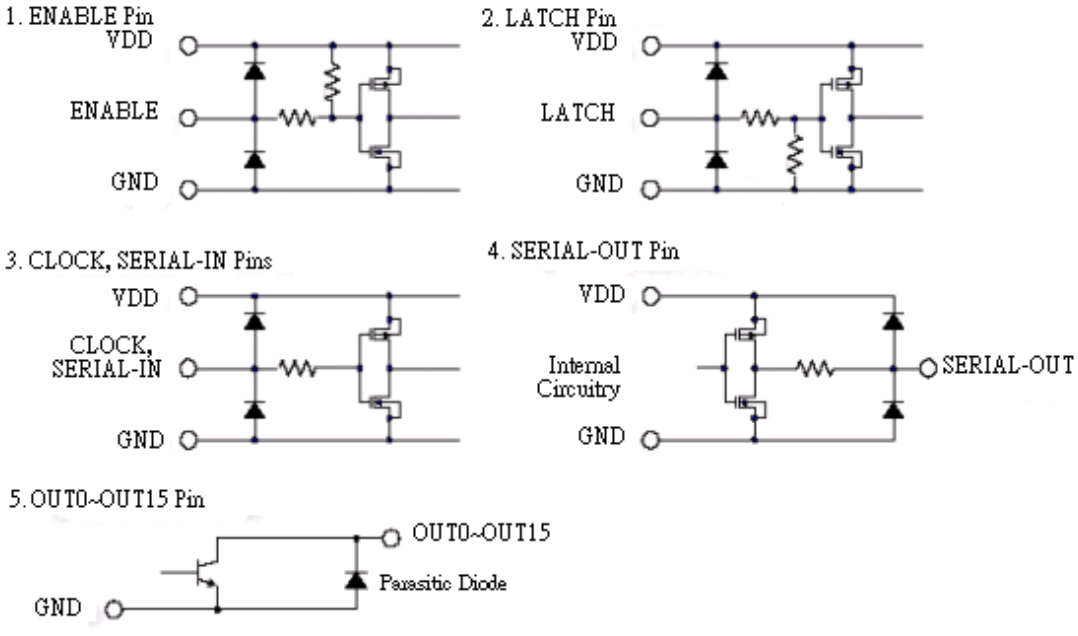
■ Truth Table

CLOCK	LATCH	ENABLE	SERIAL-IN	OUT0---OUT7---OUT15	SERIAL-OUT
Positive edge	H	L	Dn	/Dn---/Dn-7---/Dn-15	Dn-15
Positive edge	L	L	Dn+1	No Change	Dn-14
Positive edge	H	L	Dn+2	/Dn+2---/Dn-5---/Dn-13	Dn-13
Negative edge	X	L	Dn+3	/Dn+2---/Dn-5---/Dn-13	Dn-13
Negative edge	X	H	Dn+3	Off	Dn-13

■ Pin Description

Pin No.	Pin Name	Function
1	GND	GND Pin
2	SERIAL-IN	Serial input data pin
3	CLOCK	Clock input terminal for shift register, rising edge trigger
4	LATCH	Data latch input pin. When LATCH=High-level, data is passed to OUT0~OUT15, when LATCH=Low-level, data is latched.
5~20	OUT0~OUT15	16 constant current output pin to drive common anode LEDs
21	ENABLE	Data output enable pin, when ENABLE=High-level, all OUT0~OUT15 are turned off, and when ENABLE=Low-level, all OUT0~OUT15 are enabled.
22	SERIAL-OUT	Serial data output pin for cascade operation
23	R-EXT	The external resistor connection pin to adjust the output current
24	VDD	3.0V~5.5V supply voltage pin

■ Equivalent circuits of I/O pins



■ Absolute Maximum Ratings

Characteristics	Symbol	Rating	Unit
Supply Voltage	VDD	+7.0	V
Input Voltage	Vin	-0.4 to VDD+0.4	V
Output Current	Iout	+60	mA
Output Voltage	Vout	-0.5 to 7.0	V
GND Pin current	IGND	880	mA
Clock Frequency	fCLK	25	Mhz
Power Dissipation	Pd	AF: 1.45 AN: 1.39 AM: 2.51 BP: 2.32	W
Thermal Resistance	Rth(j-a)	AF: 96 AN: 112 AM: 49.81 BP: 53.82	℃/W
Operating Temperature	Top	-40 to 85	℃
Storage Temperature	Tstg	-55 to 150	℃

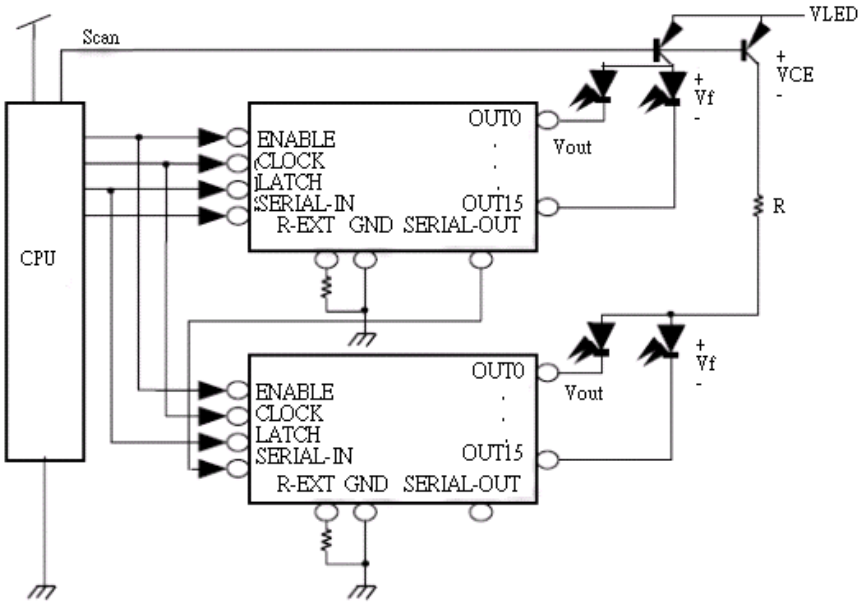
■ Typical Application

LED supply voltage is set-up by following equation:

VLED = VCE + Vf+ Vo

To prevent too much power dissipated by driver due to the higher VLED,
an additional R can be introduced to reduce the Vo when output is consuming current.

R = (VLED – VCE – Vf – Vo min)/ (Io max * Bit max)



■ Order information

Part No.	Package Type	Lead Pitch
CS8826AF	24SSOP(236mil)	1.0 mm
CS8826AN	24SSOP(150mil)	0.64 mm
CS8826AM	24SOP(300mil)	1.27mm
CS8826BP	24PDIP(300mil)	2.54mm

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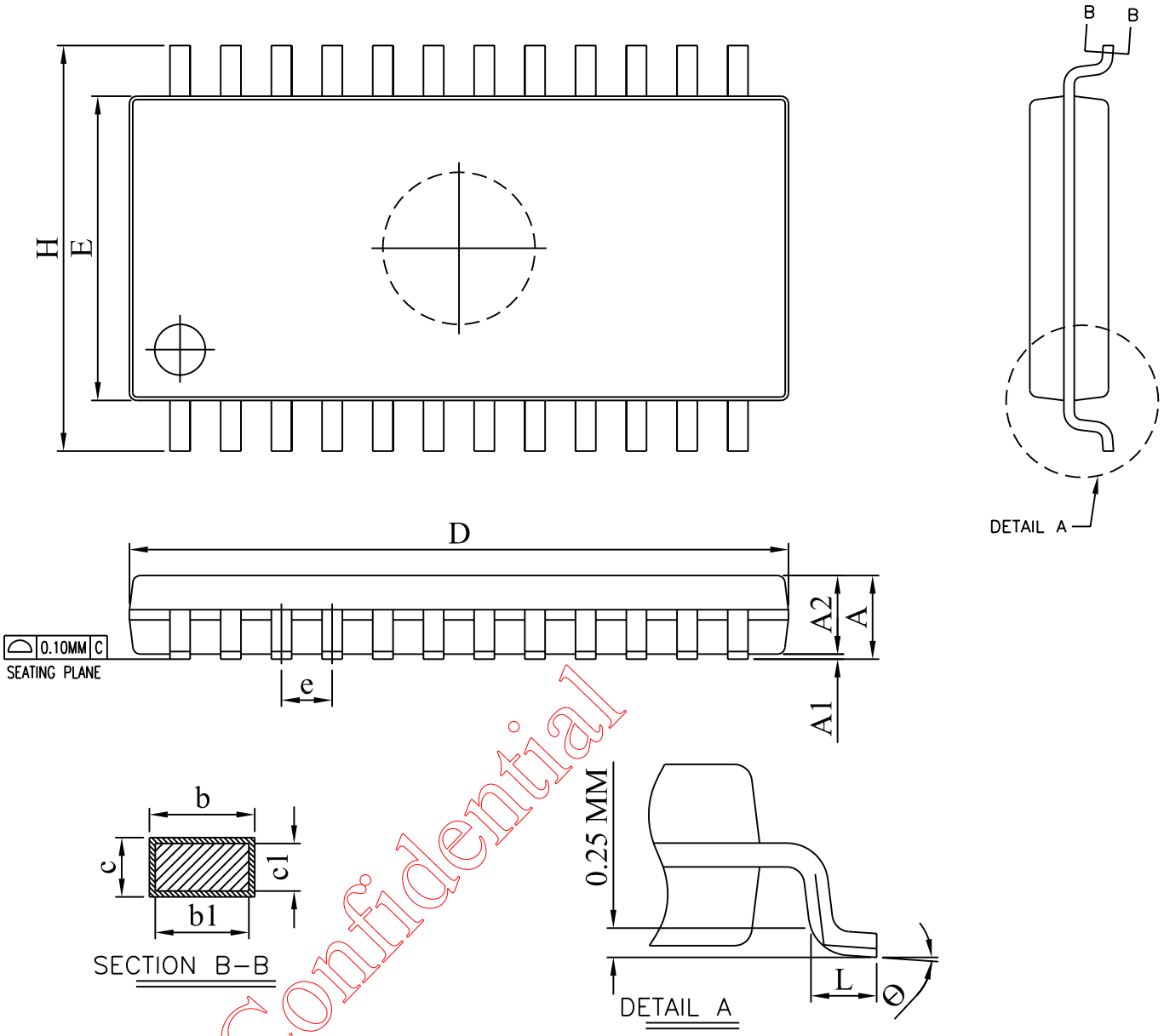
Title: Package outline for 24 SSOP-236 mil



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL / UNIT		A	A1	A2	b	b1	c	c1	D	e	E	H	L	θ°
mm	Min.	-	0.05	1.30	0.30	0.30	0.10	0.10	12.80	1.00 BSC	5.80	7.70	0.25	0
	Nom.	-	0.10	1.50	0.40	0.40	0.15	0.15	13.00		6.00	8.00	0.45	-
	Max.	1.90	0.15	1.70	0.52	0.50	0.27	0.25	13.20		6.20	8.30	0.65	10

DWG. NO.	ORIGINATOR	ISSUE DATE	REV.
PC600-0034	Yuki_Yeh	03-Jan.-'08	1

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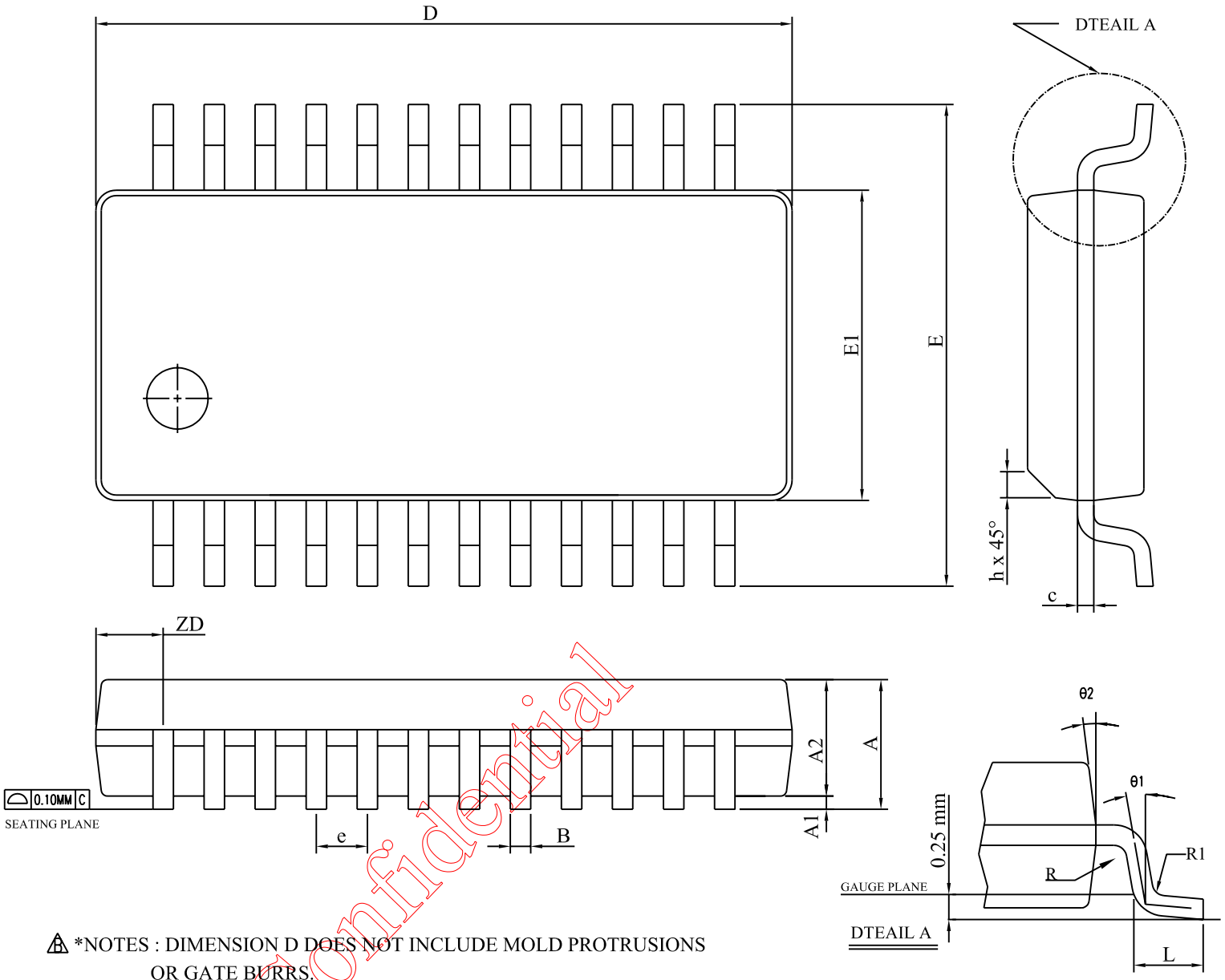
Title: Package outline for 24 SSOP-150 mil

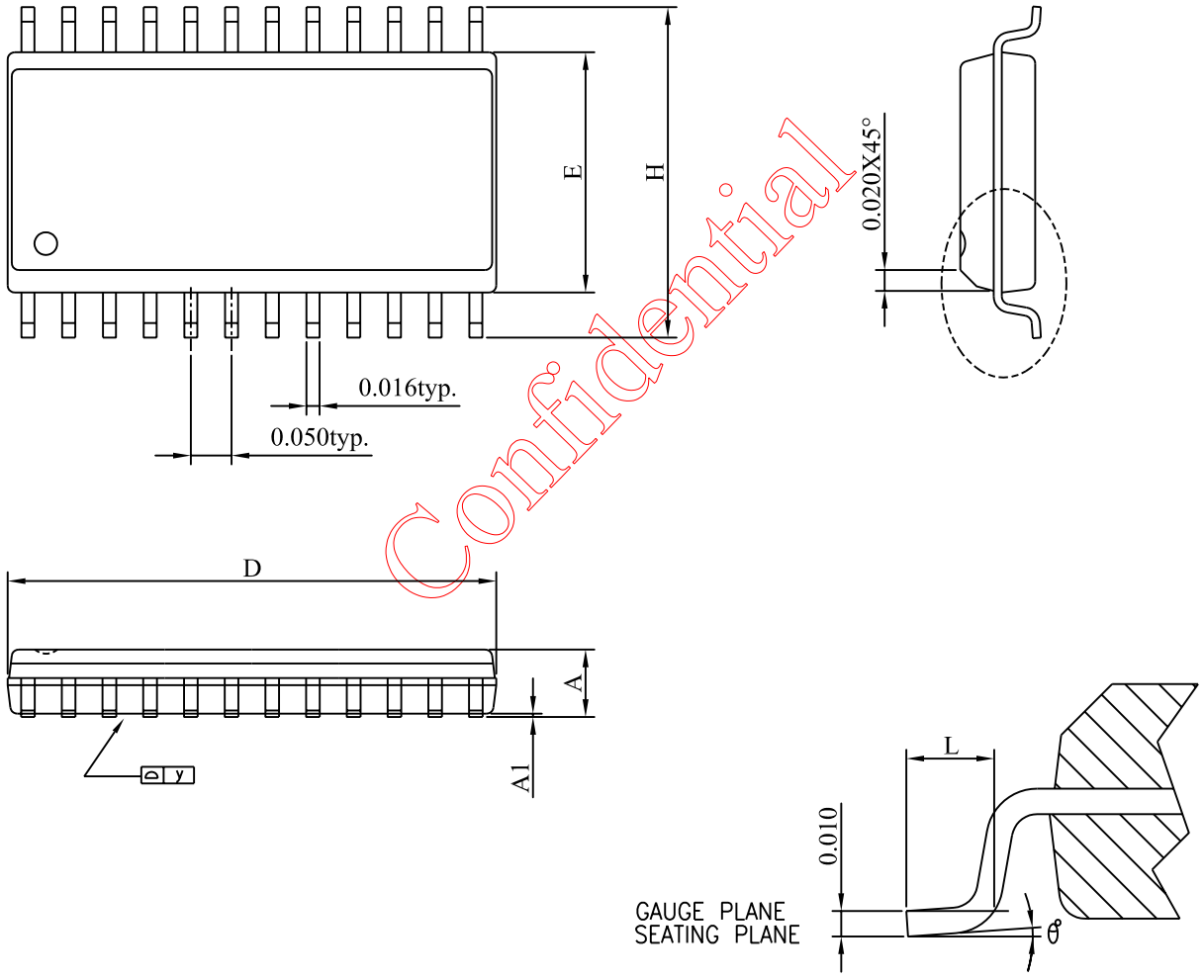


⚠ *NOTES : DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS.
MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 INCH PER SIDE.
Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL / UNIT		A	A1	A2	B	c	e	D	E	E1	L	h	ZD	R1	R	θ	θ1	θ2
mm	Min.	1.35	0.10	-	0.20	0.18	0.635 BSC	8.56	5.79	3.81	0.41	0.25	0.838 REF	0.20	0.20	0°	0°	5°
	Nom.	1.63	0.15	-	-	-		8.66	5.99	3.91	0.635	-		-	-	-	-	10°
	Max.	1.75	0.25	1.50	0.30	0.25		8.74	6.20	3.99	1.27	0.50		0.33	-	8°	-	15°

DWG. NO.	ORIGINATOR	ISSUE DATE	REV.
PC600-0035	Yuki_Yeh	03-Jan.-'08	1

Title: Package outline for 24L SOP-300mil

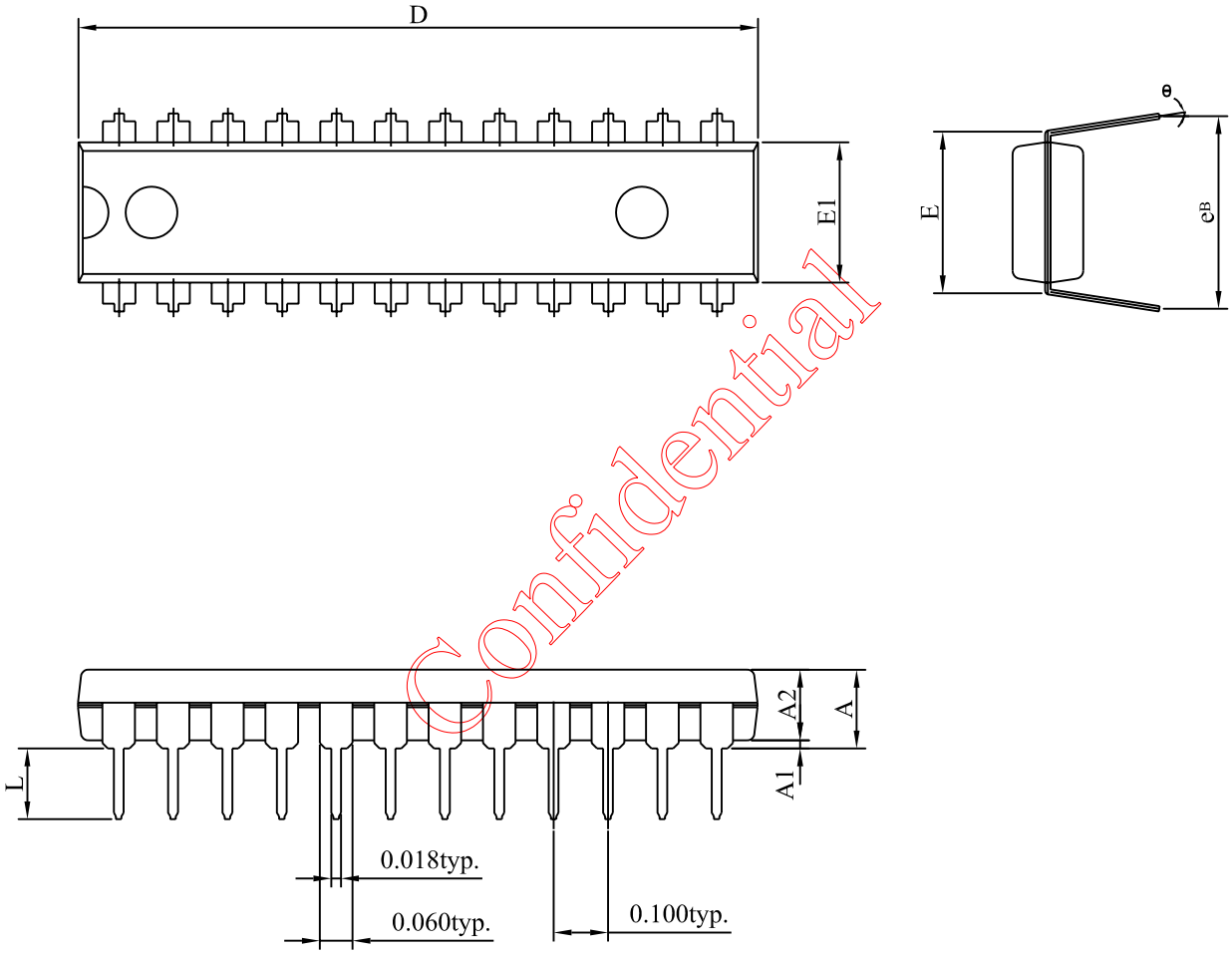


Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL / UNIT		A	A1	D	E	H	L	θ°
inch	Min.	–	0.004	0.599	0.291	0.394	0.016	0
	Nom.	–	–	0.600	0.295	0.406	0.035	4
	Max.	0.104	–	0.624	0.299	0.419	0.050	8

DWG. NO.	ORIGINATOR	ISSUE DATE	REV.
PC600-0023	Yuki_Yeh	03-Jan.-'08	1

Title: Package outline for 24L PDIP-300mil



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL / UNIT		A	A1	A2	D	E	E1	L	eB	θ°
inch	Min.	–	0.015	0.125	1.230	0.300 BSC	0.253	0.115	0.335	0
	Nom.	–	–	0.130	1.250		0.258	0.130	0.355	7
	Max.	0.210	–	0.135	1.280		0.263	0.150	0.375	15

DWG. NO.	ORIGINATOR	ISSUE DATE	REV.
PC600-0026	Yuki_Yeh	03-Jan.-'08	1