Design Consideration of the Active-Clamp Forward Converter with Current Mode Control during Large-Signal Transient †

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Abstract - The design issues of the active-clamp forward converter circuit with peak current mode control in small signal stability and large-signal transients are discussed. A design procedure is provided to solve circuit issues under these conditions. It is the first time that with the aid of simulation, we are able to optimize the circuit design of the active-clamp forward converter for large-signal transient behaviors.

I. INTRODUCTION

The forward converter with the active-clamp reset offers many advantages over the forward converter with other transformer reset methods [1]. However, during the large-signal transients, the maximum magnetizing current of the transformer and the peak voltage of the primary switch are strongly affected by the active-clamp circuit dynamics. Although some design issues have been discussed [2-6], the design of active-clamp forward converter is still based on steady state performance. The voltage and current stresses of the circuit are very hard to predict during the large-signal transient and under abnormal conditions due to the non-linearity of the circuit, and the conflict effect of the different parameters makes it even harder to generate a design procedure [6-7].

In this paper, the design issues of the active-clamp forward converter circuit with peak current mode control in small signal stability and large-signal transients are discussed. A design procedure is proposed by using design curves that are generated by running a large amount of simulations. The design procedure will cover all the problems related to large-signal transient as well as small-signal stability. It shows that the dynamic performance and the robust of the circuit can be improved by using this approach. It is the first time that with the aid of simulation, we are able to optimize the circuit design of the active-clamp forward converter for the large-signal transient behaviors.

II. DESIGN ISSUES OF THE ACTIVE-CLAMP CIRCUIT

The active-clamp forward converter circuit diagram is shown in Fig. 1. Fig. 2 shows the load transient waveforms of the active-clamp circuit, where v_o is the output voltage, v_{ds_main} is the voltage across the main switch, and i_m is the magnetizing current of the transformer. From Fig. 2 we can see that the maximum voltage of the main switch and the maximum magnetizing current of the transformer during transient are much larger than that at the steady state. These could cause circuit problems such as voltage stresses, transformer saturation, and the diode reverse recovery problem [2, 3, 6], which are marked as dotted circles in Fig. 2.

Besides the large-signal transient problems, circuit could have stability problem due to the interaction of the resonant network of the active-clamp-reset circuit [4]. Fig. 3 shows small-signal transfer function of the loop gain at Vin = 36 V. The phase margin of the loop gain at crossover frequency is negative due to the additional pole in the active-clamp-reset circuit near the resonant frequency. This paper is going to demonstrate how to design the circuit to solve these problems.

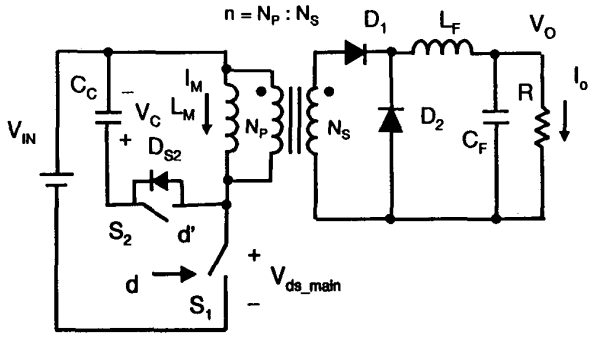

Fig. 1 Active-clamp forward converter circuit diagram.

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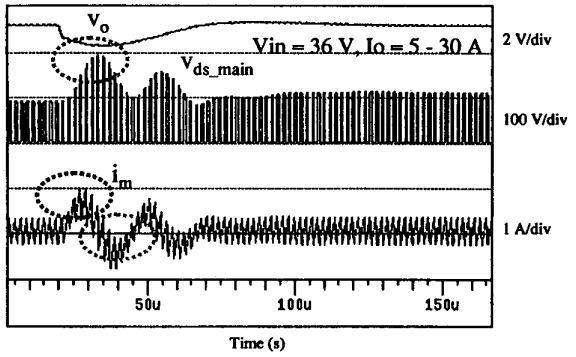


Fig. 2 Active-clamp circuit problems during large-signal transient.

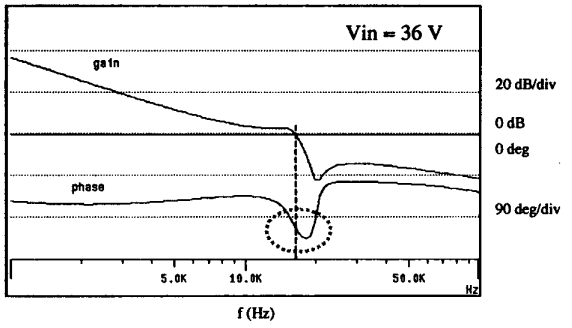


Fig. 3 Stability problem due to the resonant network of the active-clamp reset circuit.

III. CIRCUIT UNDER WORST CASE CONDITION

The fist step before we start the design is to find the worst case condition during large-signal transient, so we can design the circuit under worst case condition. A virtual prototype test procedure is used to detect the circuit worst case condition by simulating the circuit dynamic performance under different lines, loads, and the abnormal conditions [7].

An active-clamp forward converter circuit with peak current mode control is used as an example to demonstrate the design process. The circuit has input voltage 36 - 72 V and full load 30 A. The duty cycle limit of the controller chip is 0.75. The control bandwidth of the current circuit design is 14 kHz. From the simulation, it shows that the worst condition occurs when the circuit has a large load transient from no load to full load at low line.

In order to verify the accuracy of simulation, a circuit prototype was built to compare the circuit dynamic performance. Fig. 4 shows the large-signal response waveforms at Vin = 36 V, Io from no load to full load to no load transient. The load step slew rate is 1 A/us. Fig. 4(a) is the measured waveform from no load to full load transient. Fig. 4(b) is the simulated waveform from no load to full load transient. Fig. 4(c) is the measured waveform from full load to no load transient. Fig. 4(d) is the simulated waveform from full load to no load transient. Comparing the measurement and simulation, it shows that the simulation is accurate enough to provide the design information and predict the dynamic behavior of the system.

IV. DESIGN PROCEDURE OF THE ACTIVE-CLAMP CIRCUIT

Although it is possible to adjust the circuit parameters by trials and errors to fix the problems, the problem's solution is not straightforward. It may require a lot of time and effort but still not come out a robust design, since these parameters are not independent parameters and involve different circuit design issues.

This section will demonstrate how to generate design information and optimize the design parameters related to these design issues. The design parameters discussed here are the magnetizing inductance of the transformer L_m, the clamp capacitance C_c, the control bandwidth f_c, and the maximum duty cycle limit Dmax. The design process focuses on solving the potential problems in the circuit: voltage stress of the main switch, transformer core saturation, diode reverse recovery of the active-clamp switch, small-signal instability due to the active-clamp resonant network.

A. Normalization

The normalized peak voltage and peak current values will be used in the design curve. The normalized switch voltage is $\frac{V_s}{V_{in}(\min)}$ and the normalized magnetizing current is $\frac{i_m \cdot Z_o}{V_{in}(\min)}$. The x-axis of the design curve uses resonant frequency, f_o as a parameter, and Z_o is the character impedance.

$$f_o = \frac{1}{2 \cdot \pi \cdot \sqrt{L_m \cdot C_c}} \quad (1)$$

$$Z_o = \sqrt{\frac{L_m}{C_c}} \quad (2)$$

B. Design constraints

There are four design criteria: the voltage stress of the main switch, the transformer saturation, the reverse recovery problem of the body diode of the active clamp switch, and the small-signal stability problem.

- Design constraint 1: switch voltage stress

The design constraint for the switch voltage stress is:

V_s (peak) < V_s (rating) (3)

Where, V_s (peak) is the peak voltage during the transient, V_s (rating) is the device voltage rating of the main switch.

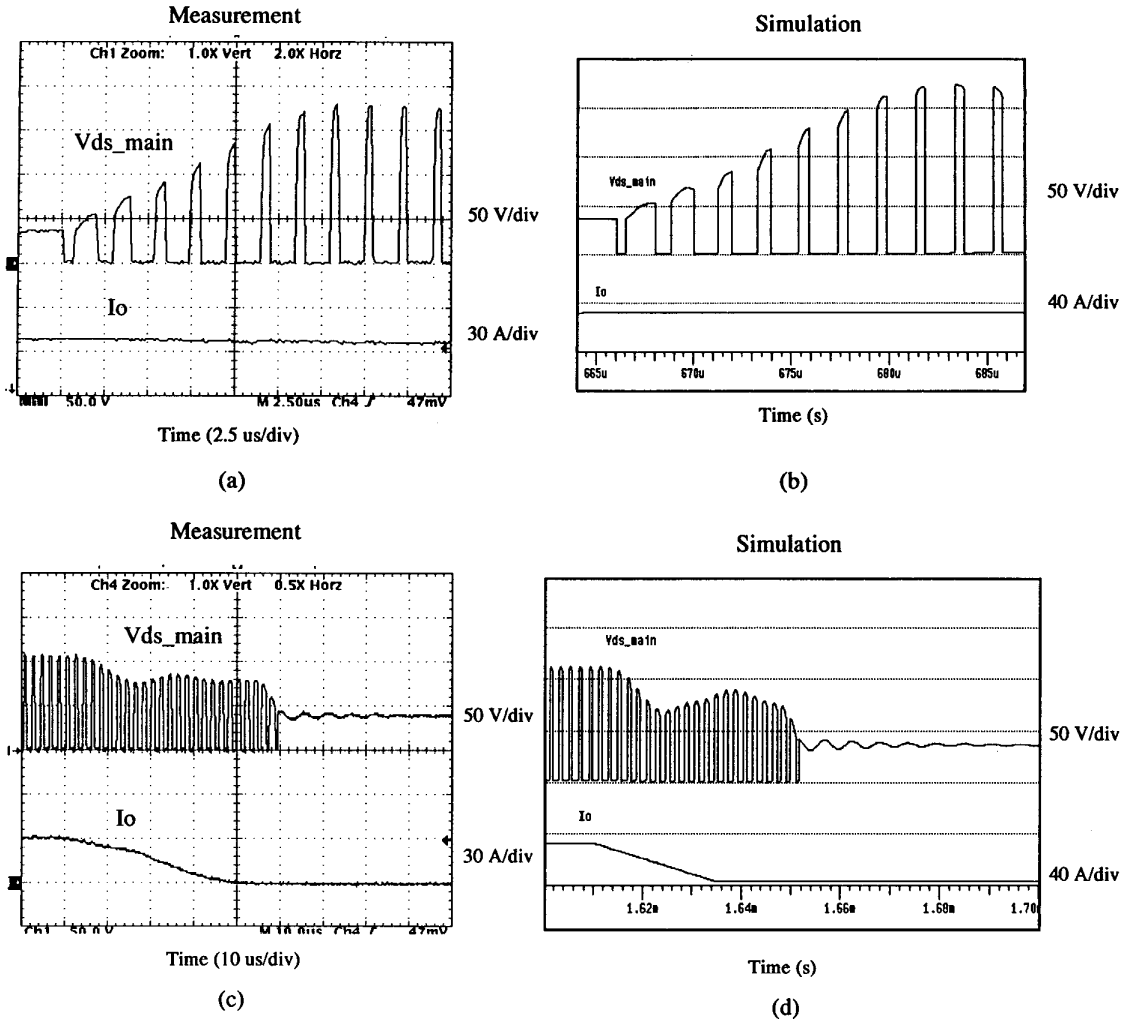


Fig. 4. Large-signal response waveforms at Vin = 36 V, Io from no load to full load to no load transient. Load step slew rate is 1 A/us. (a) measured waveform of no load to full load transient. (b) simulated waveform of no load to full load transient. (c) measured waveform of full load to no load transient. (d) simulated waveform of full load to no load transient.

- Design constraint 2: small signal stability

The resonant frequency of the active-clamp circuit should meet the following equation in order to have a stable system and not affect the phase margin.

$$f_o > \frac{2 \cdot f_c}{d'_{\lim}} \tag{4}$$

where d'_{lim} is the duty cycle limit value of the controller chip, f_c is the control bandwidth.

- Design constraint 3: transformer saturation

Fig.5 shows the relation between the flux and the magnetizing current, where, A_e is the effective cross sectional area of the core, Lm is the magnetizing current. From Fig.5, we can get:

$$i_m(sat) = \frac{B_{sat} \cdot A_e \cdot N_p}{L_m} \tag{5}$$

We can rewrite saturating magnetizing current into:

$$i_m(sat) = \frac{B_{sat} \cdot A_e \cdot N_p \cdot 2 \cdot \pi \cdot f_o}{Z_o} \tag{6}$$

The design constraint for transformer saturation is:

$$\frac{i_m(peak) \cdot Z_o}{V_{in}(\min)} < \frac{B_{sat} \cdot A_e \cdot N_p \cdot 2 \cdot \pi \cdot f_o}{V_{in}(\min)} \tag{7}$$

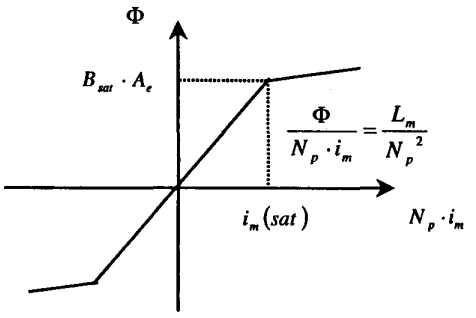


Fig.5. Relation of the saturation flux to the saturation magnetizing current.

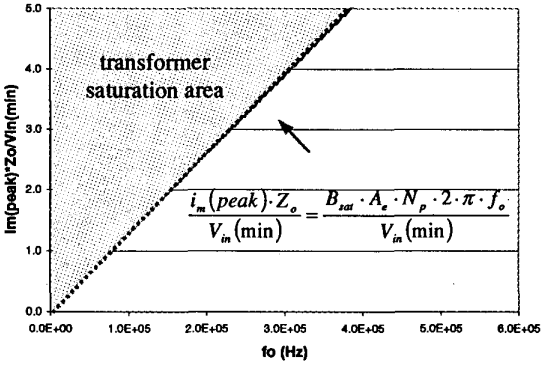


Fig. 6 The transformer saturation area.

The design constraint for the transformer saturation is shown as shaded area in Fig. 6. It is a straight line in the normalized design curve.

- Design constraint 4: diode reverse recovery problem

The magnetizing current to prevent the diode from reverse recovery problem is:

$$i_m(peak) < i_m(ripple) \tag{8}$$

where,

$$i_m(ripple) = \frac{V_{in} \cdot D \cdot T_s}{L_m} = \frac{n \cdot V_o \cdot T_s}{L_m} \tag{9}$$

The ripple current can be written as:

$$\frac{i_m(ripple) \cdot Z_o}{V_{in}(\min)} = \frac{n \cdot V_o \cdot 2 \cdot \pi \cdot f_o}{f_s \cdot V_{in}(\min)} \tag{10}$$

The diode reverse recovery problem area is shown as in Fig.7. It is a straight line in the normalized design curve.

According to four design constraints, we can draw the feasible operating regions for voltage and magnetizing current as shown in Fig.8.

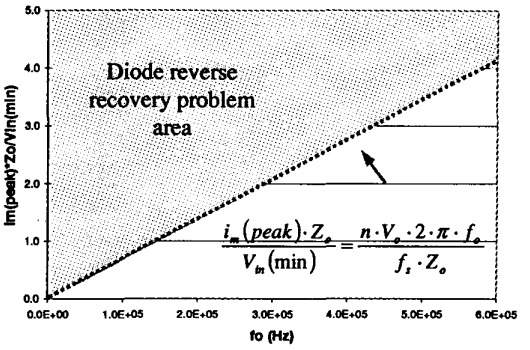
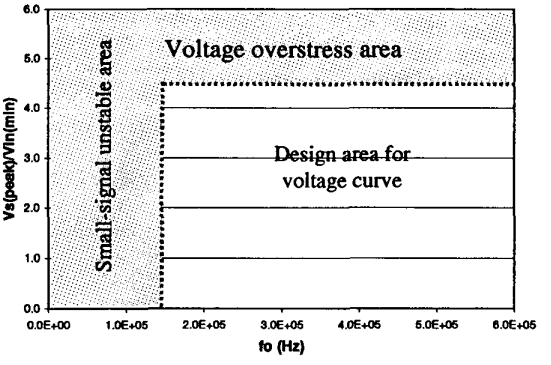
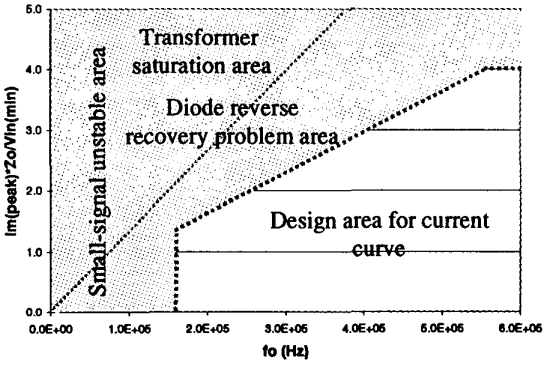


Fig.7. The diode reverse recovery problem area.



(a)



(b)

Fig.8 Feasible operating regions for voltage and magnetizing current. (a) design area for normalized switch voltage curve. (b) design area for normalized magnetizing current curve.

C. Generating design curves

The worst case happens at low line and load from low to high transient. In this example, Vin is 36 V, and Io changes from 0 A to 30 A. A set of design curves is generated by

varying L_m and C_c values with a fixed control bandwidth, 14 kHz, and maximum duty cycle limit, 0.75. Each single simulation generates one point in the voltage design curve and one point in the magnetizing current curve. The normalized design curve for peak voltage and magnetizing current are shown in Fig. 9 and Fig. 10, respectively. The shaded areas are the design prohibited area. The total simulation CPU time is only 9 minutes by using an adequate simulation and modeling approach [7].

D. The feasible Lm and Cc to meet the design constraints

After we generate the design curves with design constraints, the feasible L_m and C_c to meet all the design criteria can be easily determined.

Assuming the device rating of the main switch is 180 V, so the normalized boundary of the voltage stress is 5 when $V_{in}(min)$ = 36 V. When the control bandwidth, f_c = 14 kHz, and maximum duty cycle limit, d_{lim} = 0.75, the boundary of the resonant frequency for small-signal stability is 112 kHz. The feasible L_m and C_c can be determined by three steps.

1. Find the desired parameter ranges for f_o and L_m in peak-voltage design curves.

Fig. 9 is the peak-voltage design curves with f_c 14 kHz and d_{lim} 0.75. These is a big dot in Fig. 9, which corresponds to the original design, L_m = 80 uH and C_c = 0.01 uF. The maximum voltage is about 200 V, so the original design exceeds the 180 V voltage rating of the switch under worst case condition.

The dotted lines covered area is the desired design area to meet voltage stress limitation and small signal stable criterion in the normalized peak switch voltage vs. f_o curves. We can see that only the curve at L_m = 20 uH meets the constraints when f_o is at 112 kHz to 480 k Hz range.

2. Within the defined ranges for f_o and L_m in step 1, we can find the desired ranges for f_o and L_m that also meet the magnetizing current constraints.

Fig. 10 is the peak magnetizing-current design curves with f_c 14 kHz and d_{lim} 0.75. These is a big dot in Fig. 10, which corresponds to the original design, L_m = 80 uH and C_c = 0.01 uF. It shows that the original design has diode reverse recovery problem and is at the boundary of the transformer saturation.

From the design curves, we can see that there are no feasible parameters available within the desired areas from step1. It also means that there is no feasible L_m and C_c can meet all the design constraints in the previous circuit condition.

3. If we find the desired ranges for f_o and L_m from step 1 and 2, C_c can be calculated by

$$C_c = \frac{1}{(2 \cdot \pi \cdot f_o)^2 \cdot L_m} \qquad (11)$$

Within the desired parameter range, a smaller f_o, thus a smaller C_c is preferred to reduce the voltage and current stresses.

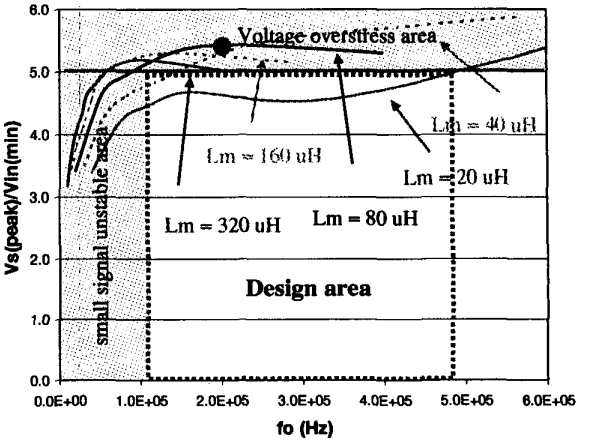


Fig. 9 Design curve of the normalized peak switch voltage vs. f_o.

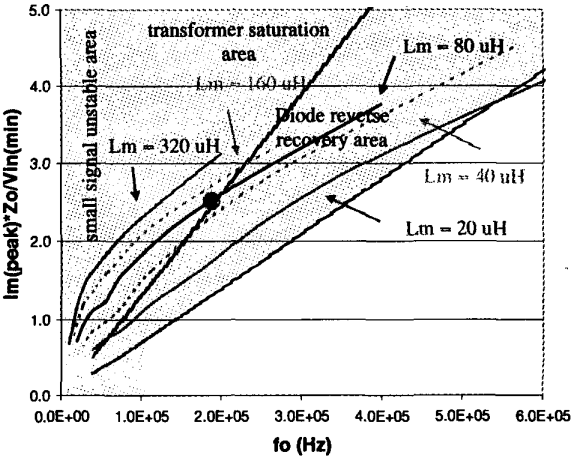


Fig. 10 Design curve of normalized peak magnetizing current vs. f_o.

V. DESIGN TRADE-OFF

Previous example shows that there is no adequate L_m and C_c to meet all the design criteria. There are several design trade-off to solve the problem.

A. Design trade-off 1: increasing device rating

From Fig. 9 and Fig. 10, we see that if we do not restrict the device voltage rating to 180 V, there is a small area in Fig. 10 which can meet all the design criteria with Lm = 20 uH. The disadvantages of this solution are the higher voltage rating device and the high ripple current of the magnetizing current due to a small L_m.

It is worthwhile to mention that a very small magnetizing inductance could have a high ripple of the magnetizing current which will increase the loss of the circuit and may affect the

main converter operation if the ripple of the magnetizing current is not negligible to the reflected load.

B. Design trade-off 2: getting rid of the constraint of the body diode reverse recovery

From Fig. 10, we see that the diode reverse recovery constraint is the hardest one to meet in the parameter design. The design is more flexible without this constraint. This can be done by connecting a Schottky diode in series with the auxiliary switch to block the conduction of the body diode, and then to connect a fast-recovery anti-parallel diode around the series connection of the Schottky and the auxiliary switch [56]. The disadvantage is the additional components to increase the cost of the circuit.

C. Design trade-off 3: decreasing control bandwidth

A smaller bandwidth in the design can reduce the peak voltage and current during load transients. The disadvantage is a slower recovery from transient in the output voltage of the main converter.

D. Design trade-off 4: reducing maximum duty cycle limit value

The voltage and current stresses can also be reduced by reducing the maximum duty cycle limit value. Similar to solution 3, the disadvantage is a slower recovery from transient in the output voltage of the main converter.

E. Circuit redesign by using trade-off 4

We will use design trade-off 4 as an example to show the circuit redesign result. The design procedure is the same as in the previous section.

Fig.11 and Fig.12 shows the normalized voltage design curve with reduced maximum duty cycle limit. The maximum duty cycle limit is reduced from 0.75 to 0.7. The design result is L_m = 40 uH, C_c is less than 0.011 uF. A smaller C_c has a larger voltage stress, but less current stress and more design margin without saturation and diode reverse recovery problem.

VI. VALIDATION OF THE DESIGN BY VIRTUAL PROTOTYPE TEST

Fig. 15 shows the comparisons between the original circuit problems and the circuit behavior after the final design modification. The circuit parameters are modified by reducing the maximum duty cycle limit from 0.75 to 0.7 and magnetizing inductance from 80 uH to 40 uH. The clamp capacitance is 0.01 uF.

Fig. 13 shows design verification of dc bias of magnetizing current of transformer. The dc bias of the magnetizing current does not shown any problems since the magnetizing current ripple is about 800 mA.

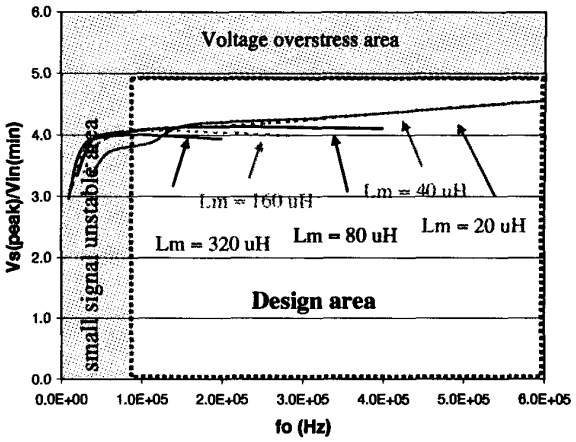


Fig.11 Normalized voltage design curve reduced maximum duty cycle limit. The Dlim is reduced from 0.75 to 0.7. The design area to meet voltage stress limitation and small signal stable criteria is shown in the dotted area.

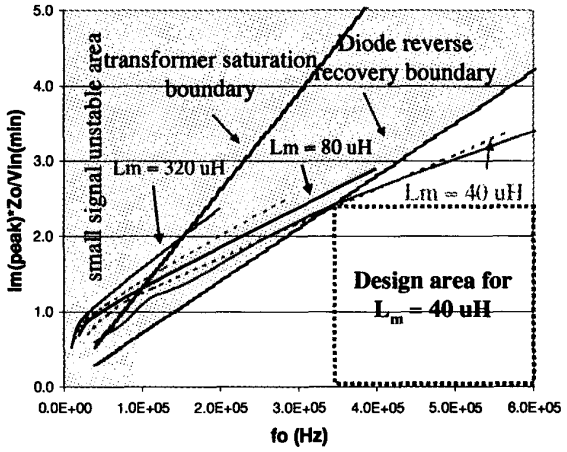


Fig.12 Normalized magnetizing current design curve with reduced maximum duty cycle limit. The Dlim is reduced from 0.75 to 0.7. The design area without transformer saturation and diode reverse recovery problem shows in the dotted line.

Fig. 14 shows the design verification of the small signal analysis under worst case condition. The resonant frequency of the active-clamp circuit has been pushed high enough and does not interfere with the crossover frequency of the loop gain.

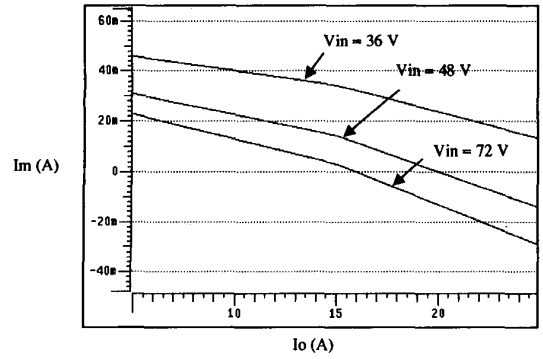


Fig. 13. Design verification of dc bias of magnetizing current of transformer at steady state.

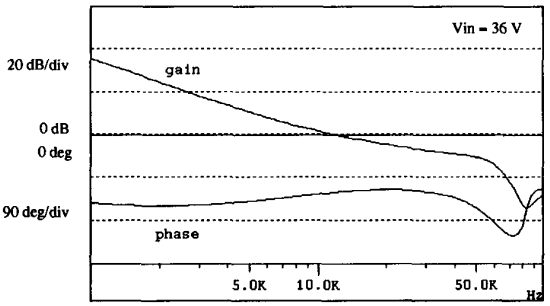
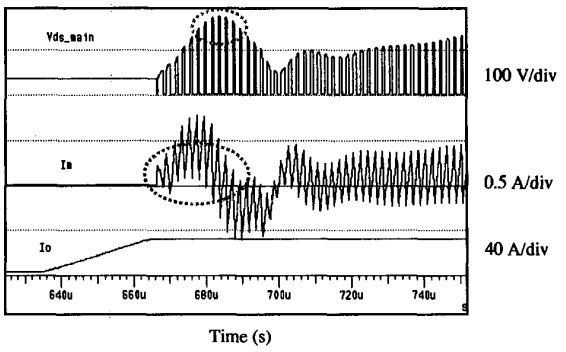


Fig. 14 Design verification of the small signal analysis.

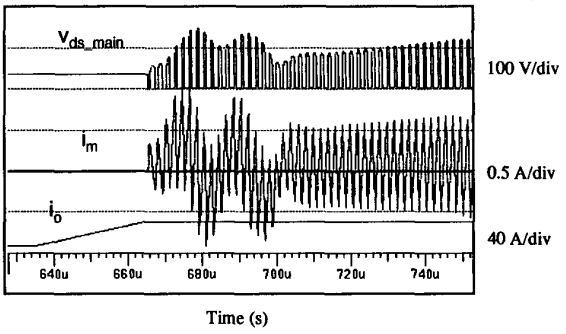
Fig. 15 shows the design verification of the large-signal transient analysis under worst case: Vin = 36 V, Io = 0 to 30 A. Fig. 15(a) shows the waveforms with original design. Fig. 15(b) shows the waveforms after design modification. The original circuit problems during large-signal transient are solved.

VII. CONCLUSIONS

The design issues of the active-clamp forward converter circuit with peak current mode control in small signal stability and large-signal transients are discussed. A design procedure is proposed to solve design issues. The circuit performances of the power supply system design are improved by redesign the active-clamp reset circuit. It is the first time that with the aid of the virtual prototype, we are able to optimize the circuit design of the active-clamp forward converter for large-signal transient behaviors.



(a)



(b)

Fig. 15 Design verification of the large-signal transient analysis with worst case: Vin = 36 V, Io = 0 to 30 A. (a) waveforms with original design. (b) waveforms after design modification.

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