A FAMILY OF CONVERTERS FOR POWER RECYCLING DURING UPS's BURN-IN TEST

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ABSTRACT

This paper introduces a family of power converters for power recycling during the burn-in test of synchronized UPS's.

The main feature of the new circuits is their ability to draw from the UPS and inject into the utility grid a low total harmonic distortion(THD) current with no need of active harmonic current elimination.

The new circuits operate at constant frequency and are regulated by conventional PWM, using dedicated PWM integrated circuits developed for power supplies.

Circuit operation, mathematical analysis, design example and experimental results are provided in this paper.

I. INTRODUCTION

Usually, in burn-in tests of UPS's, the manufacturers use resistors as load, which present large energy losses and contribute in increasing the cost of the final product.

Methods to feed this energy back into the utility have been proposed in the recent literature.

In [1,2], a technique that uses power converters is presented and the corresponding block-diagram is shown in Fig. 1. The PWM inverter is modulated to impose a sinusoidal output current, so that a low THD current is injected into the utility. This technique, therefore, requires an active control of the AC inverter current, which needs complex circuitry. Besides, a low frequency transformer, TR, is necessary to adapt the voltages to ensure the correct operation of the inverter and a bulky capacitor C_F must be used to filter the rectified voltage at the DC link.

In [3], the quadrature voltage injection is used to transfer power from the UPS to the utility. The injected voltage can be obtained by using two auto transformers or a controlled voltage inverter. Fig. 2 illustrates the block diagram for this proposal.

In [4], the proposal consists of using a regulating transformer between the UPS under test and the utility grid. This method uses passive and heavy equipments, not suitable for automation of the test procedures. Fig. 3 shows the equivalent circuit diagram for this case.

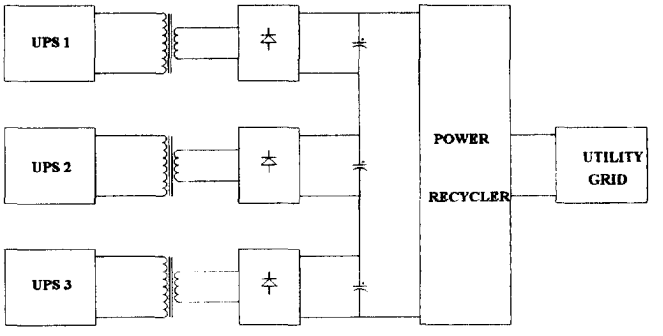

Fig. 1. Block diagram of proposal in [1,2].

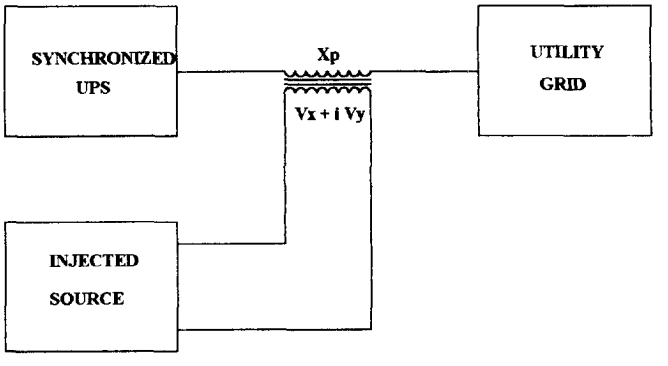

Fig. 2. Block diagram of proposal in [3].

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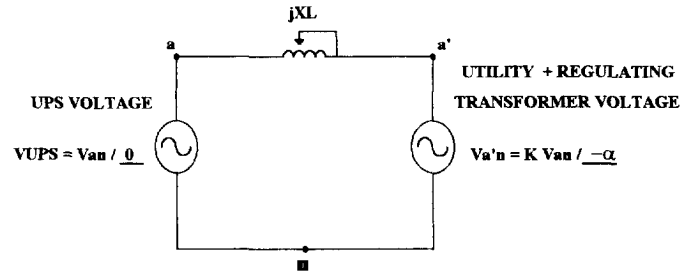


Fig. 3. Equivalent circuit diagram of proposal in [4].

A different technique, intended to be used in burn-in test of synchronized UPS's, is proposed in this paper, which is described and studied hereafter. The new technique does not require a low frequency transformer, electrolytic filter capacitor, or active power factor correction.

II. THE NEW POWER CONVERTER AND PRINCIPLE OF OPERATION

Fig. 4 shows the converter for the burn-in test of the UPS synchronized with the utility grid. The first stage of power processing is a full wave rectifier, resulting in a positive 120 Hz rectified output voltage. The second stage is a buck-boost DC/DC converter. This stage is responsible for imposing the desired sinusoidal load current drained from the UPS. The last stage is a current inverter that converts the rectified sinusoidal current from the preceding stage to a sinusoidal current synchronized with the utility grid. The current inverter operates at low frequency, changing the pair of active switches every 120 Hz. As the DC/DC converter introduces high frequency current harmonics, it is necessary to use LC filters at the input and output of the structure.

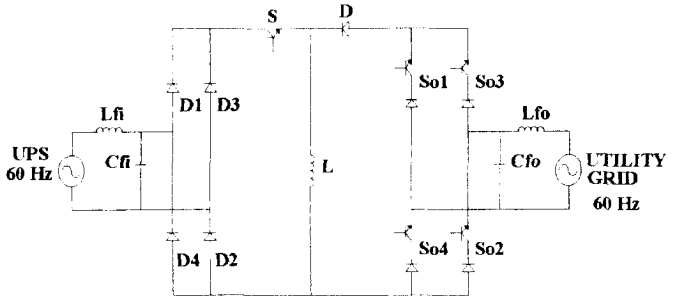


Fig.4. Proposed power recycler for UPS burn-in test.

In Fig. 4, a buck-boost converter is used in the second stage and it can operate in DCM (Discontinuous Current Mode) or CCM (Continuous Current Mode) as every DC/DC converter. In this paper, the DCM is analyzed because the switch current peak naturally follows the sinusoidal waveform of the UPS voltage. Then, no active control is necessary to obtain a sinusoidal waveform in the current drained from the UPS and the current injected into the utility grid. To analyze the operation stages of the converter, one can consider that the input and output voltages are constant during the switching period since the switching frequency is much higher than the grid one. In DCM, there are 3 stages of operation:

1st stage (t_0 - t_1): At instant t_0, the switch is turned on. The diode is off and the switch current increases linearly from zero, storing the energy in the inductor. At instant t_1, the switch is turned off and this stage is finished.

Defining the UPS voltage:

$$V_i(\theta) = V_{ip} \sin\theta \tag{1}$$

where: V_{ip} : UPS voltage peak

During this interval, the current in the switch and in the inductor are the same and are given in eq. 2.

$$I_L(t) = I_S(t) = \frac{V_{ip} \sin\theta}{L} t \tag{2}$$

$$I_D(t) = 0 \tag{3}$$

2nd stage (t_1 - t_2): At instant t_1, the switch is blocked, the diode conducts and the energy stored in the inductor is transferred to the output. The diode current decreases linearly. At instant t_2, this current reaches zero and the diode blocks, finishing this stage.

The utility voltage is given in eq. 4.

$$V_o(\theta) = V_{op} \sin\theta \tag{4}$$

where: V_{op} : utility voltage peak

The current in the diode and in the inductor are the same during this interval and are given in eq. 5.

$$I_L(t) = I_D(t) = I_P(\theta) - \frac{V_{op} \sin\theta}{L} t \tag{5}$$

where: $I_p(\theta)$: is the switch current peak in angle θ

$$I_S(t) = 0 \tag{6}$$

3rd stage (t_2 - t_3): In this stage, all the semiconductors are off and no energy is transferred.

$$I_S(t) = I_D(t) = I_L(t) = 0 \tag{7}$$

Fig. 5 shows the three stages of operation in DCM for a half period of the grid voltage, Fig 6 illustrates the most relevant waveforms in this interval (a low switching frequency was used for clarity), and in Fig. 7, one can find the main current waveforms in a switching period.

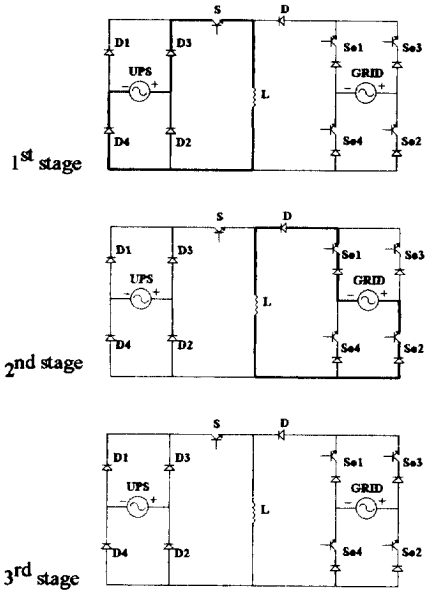


Fig. 5. The stages of operation for a half period of the grid voltage.

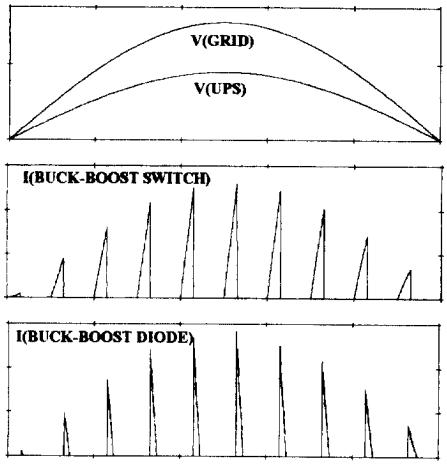


Fig. 6. Main waveforms in a half period of the grid voltage.

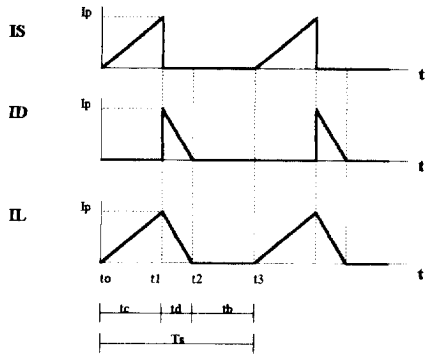


Fig. 7. Main waveforms in a switching period.

III. RELEVANT ANALYSIS RESULTS

The most relevant results are presented hereafter.

Defining:

T_s : switching period;

t_c : interval t_0 - t_1 where the switch is on;

t_d : interval t_1 - t_2 where the diode is on;

t_b : interval t_2 - t_3 where the switch and the diode are off;

D : duty cycle.

Using eq. 2 and 5, one can obtain:

$$t_d = \alpha t_c = \alpha D T_s \tag{8}$$

where: $$\alpha = \frac{V_{ip}}{V_{op}} \tag{9}$$

The condition for DCM operation is:

$$t_d + t_c \leq T_s \tag{10}$$

The limit for DCM operation imposes a maximum value for the duty cycle:

$$D_{max} \leq \frac{1}{1+\alpha} \tag{11}$$

The graph representing the maximum duty cycle for DCM is plotted in Fig. 7.

The average output current can be obtained by integrating the output current in the switching period and again in a half period of the utility:

$$\overline{I_{O_{med}}} = \frac{X_L}{V_{op}} I_{O_{med}} = 2\alpha^2 D^2 \tag{12}$$

Using eq. 12, the output characteristic can be expressed in terms of the normalized output power:

$$\overline{P_o} = \frac{X_L}{V_{op}^2} P_o = \frac{\pi \alpha^2 D^2}{2} \tag{13}$$

The normalized inductance can be obtained directly from the normalized output power:

$$\overline{X_L} = \frac{P_o}{V_{op}^2} X_L = \frac{\pi \alpha^2 D^2}{2} \tag{14}$$

Fig. 9 shows the graph of normalized output power or impedance. The semiconductors current stress can be easily calculated using the graphics of Fig. 10. The normalized currents are made in terms of X_L/V_{op}:

$$\overline{I_i} = \frac{X_L}{V_{op}} I_i \tag{15}$$

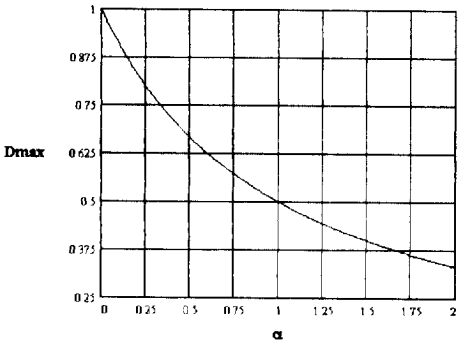


Fig. 8. Maximum duty cycle for DCM operation.

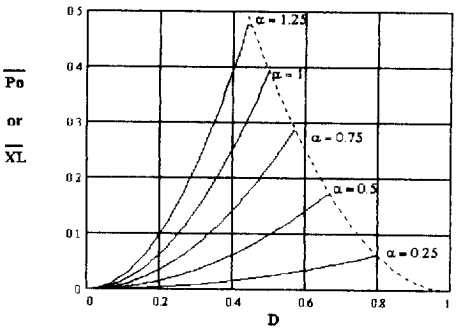


Fig. 9. Normalized output power or inductance.

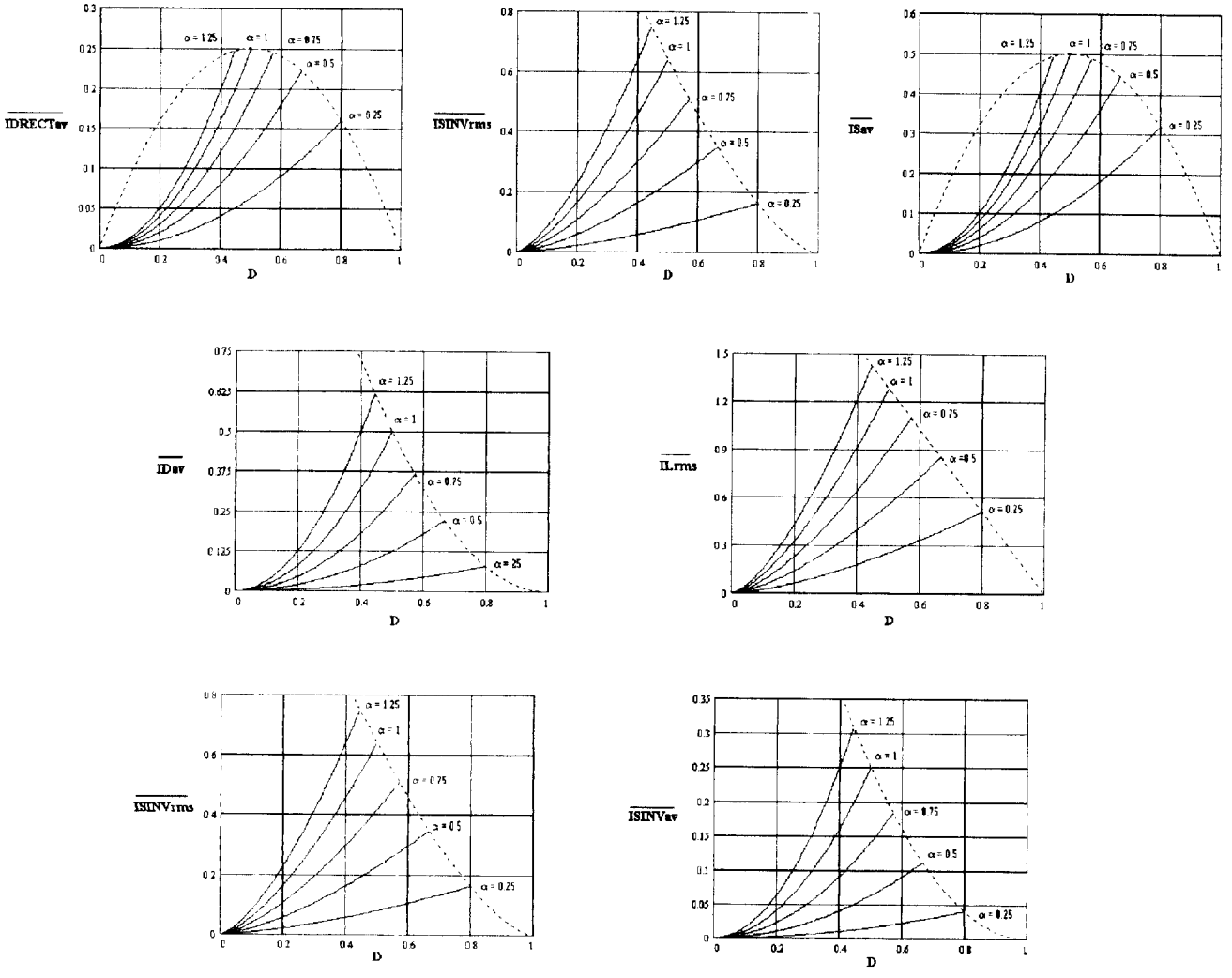


Fig. 10. Semiconductors current stress.

IV. DESIGN AND SIMULATION RESULTS

To corroborate the theoretical analysis, a power recycler of 350 W was designed and simulated. The characteristics of the converter are:

$V_i = 110\ V_{rms}$ (60 Hz)
$V_o = 110\ V_{rms}$ (60 Hz)
$P_o = 350$ W
$f_s = 20$ kHz

The value of α is:

$$\alpha_{nom} = 1$$

Using eq. 11 or Fig. 8, the critical condition is:

$$D_{max} \leq 0.5$$

To guarantee DCM operation, we choose:

$$D = 0.4$$

Then, the normalized inductance is obtained using eq. 14 or Fig. 9:

$$\overline{X_L} = 0.251 \quad \Rightarrow$$

$$X_L = \frac{V_{op}^2}{P_o}\overline{X_L} = \frac{(110\sqrt{2})^2}{350}0.251 = 17.35\,\Omega$$

Using the switching frequency, the inductor can be calculated:

$$L = 138\ \mu H$$

The input and output filters are $L_{fi} = L_{fo} = 1.35$ mH and $C_{fi} = C_{fo} = 2\ \mu$F.

A dead time near the zero crossing was introduced in the drive signal as shown in fig. 11. Then, the current of the buck-boost switch is zero during the dead time and the switches of the current source inverter commute under zero current. This fact hardly affects the theoretical analysis since near the zero crossing, the transferred power is low.

The simulation results are shown in Fig. 12. Notice that, in Fig. 12, the current injected into the utility grid is represented in 180° shifted from the utility voltage because the power flux is from the converter to the grid.

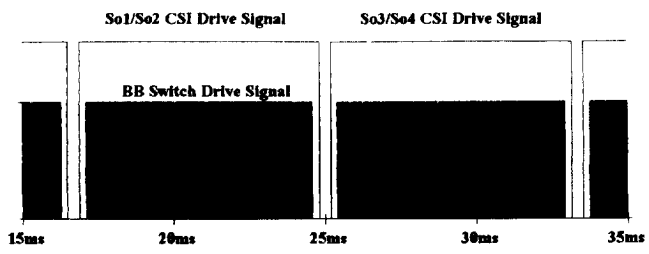


Fig. 11. Control signals.

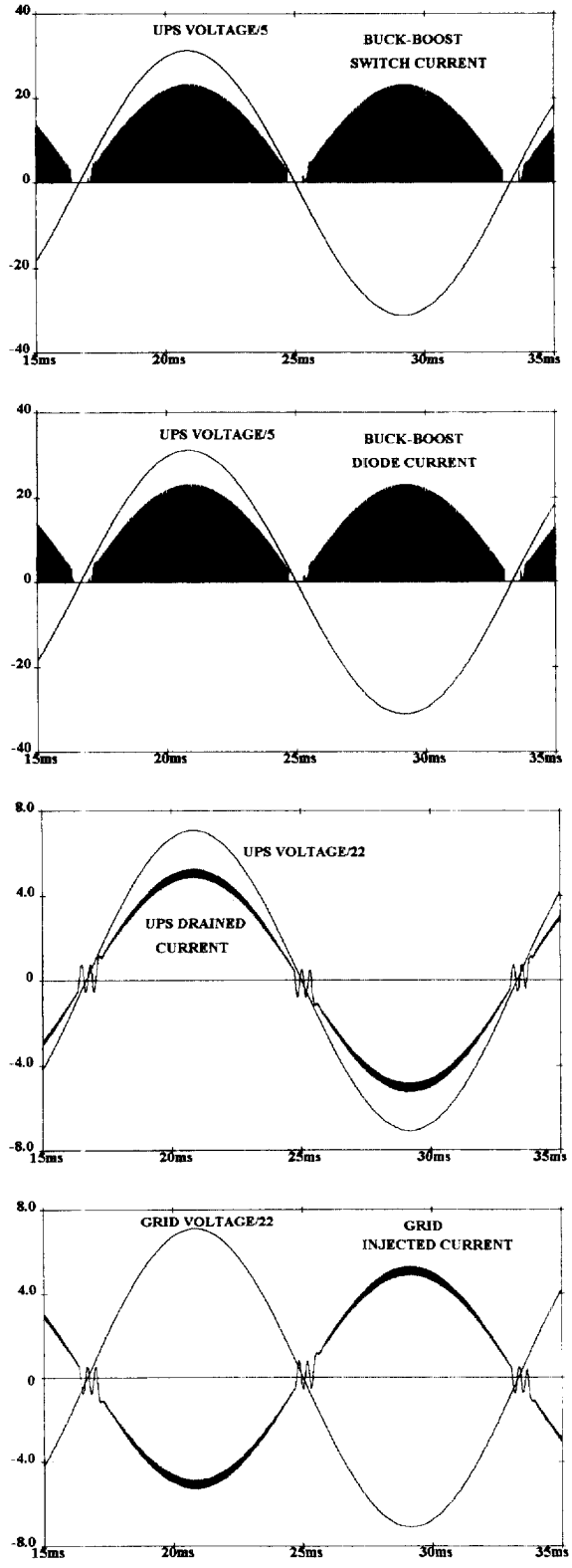


Fig. 12. Simulation results using a dead time.

V. EXPERIMENTAL RESULTS

A prototype of the 350W designed converter was implemented. The circuit is shown in Fig. 13. One can notice that the switches are oversized because the main objective was to prove the principle of operation of the converter. Fig 14 shows the obtained experimental results.

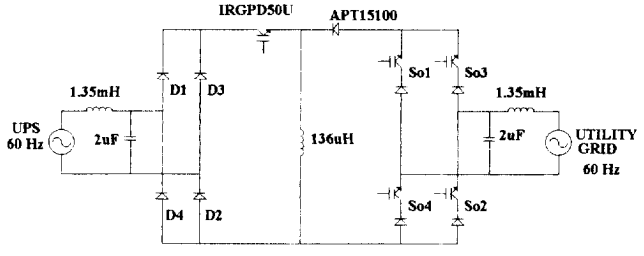
The prototype drained around 380 W from the UPS using a duty cycle equal to 0.4. This result corroborates the theoretical analysis of the converter. This small difference is due to the 115V voltage grid at the moment of acquisition. During the experimentation a transformer was used to replace the synchronized UPS. The utility voltage presented a THD of 3.3%. The current injected into the utility grid presented a THD of around 7% and a lag displacement angle of around 4°, resulting in an almost unitary power factor. The current drained from the UPS also presented a quasi unitary power factor with a small lead displacement angle of 1° and a THD of 5%. Notice that, in Fig. 14, the current injected into the utility grid is also represented 180° shifted from the utility voltage(as in Fig. 12).

VI. EXTENSION TO OTHER TOPOLOGIES

One can extend this technique to all basic DC/DC converters as shown in Fig. 15.

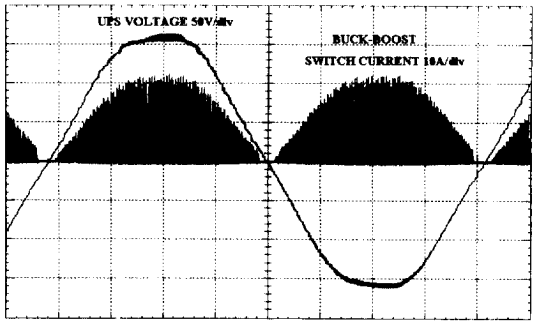
Using the basic converters, some isolated converters can be obtained.

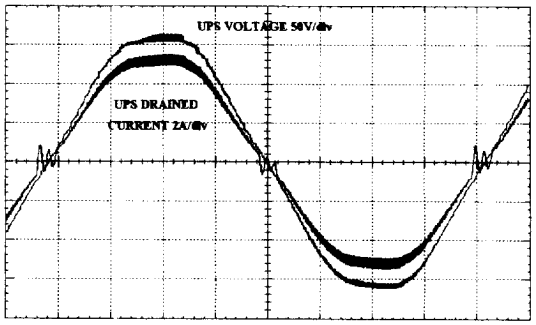
Operating in DCM, the DC/DC converter presents a lower switching loss but with greater current peak in the switches. To reduce this current peak, the interleaving technique can be used: two DC/DC converters operating in DCM and shifted 180°, each processing 50% of the total power. As a consequence, the volume of the filters can be reduced. Fig. 16 shows the circuit diagram for this case and the main waveforms.

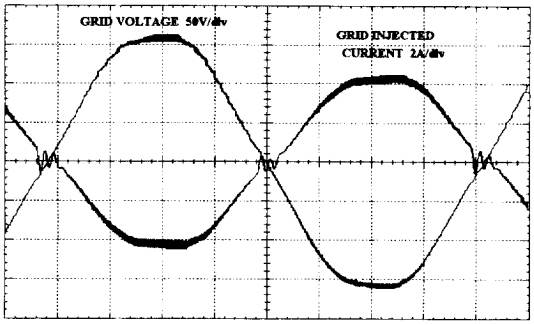


IGBT's of So1, So2, So3 and So4 : IRGPC50U
Diodes of So1, So2, So3 and So4 : MUR1530
D1, D2, D3 and D4 : Diodes bridge SKB7/08

Fig. 13. Implemented circuit.







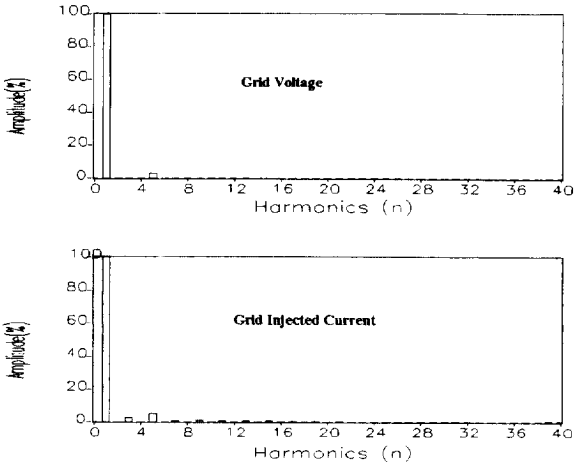


Fig. 14. Experimental results.

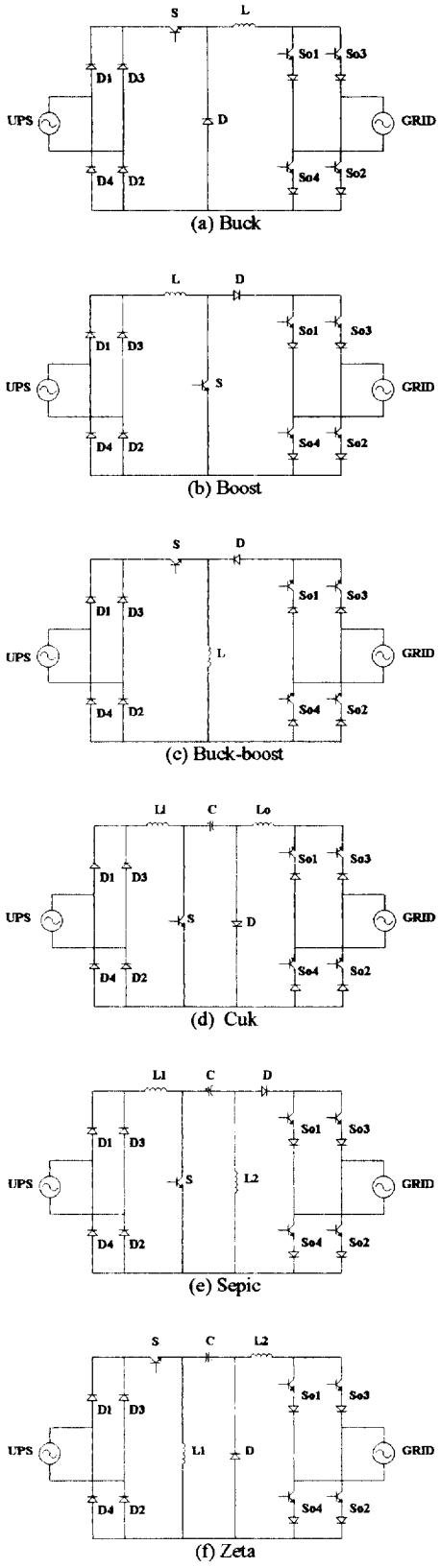


Fig. 15. The six basic topologies of the power recycler for synchronized UPS.

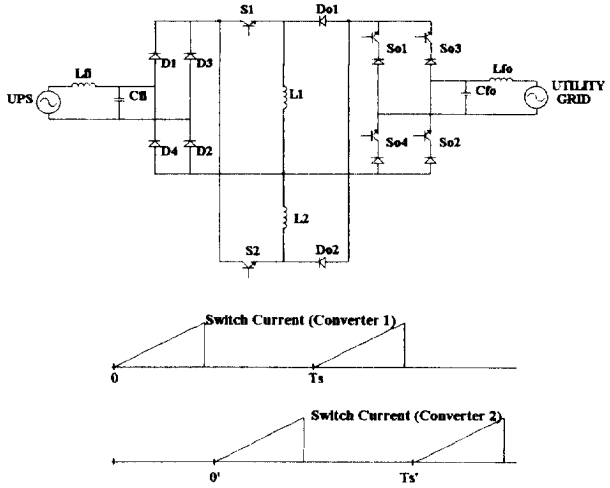


Fig. 16. Two converters operating 180^{o} shifted

VII. CONCLUSION

In this paper we introduce and describe the operation of a family of converters intended to be used in synchronized UPS burn-in test. This converter replaces the resistor load banks with the advantage that most of the electrical energy is sent back to the utility grid. The power recycling concept is totally agreeable to the world concern about ecology and the economical benefits due to energy savings are evident

The most important characteristic of the proposed converters is their ability to drain from the UPS and to inject into the utility low THD currents with high power factor with no need of active control.

Mathematical analysis, design procedure and a 350 W prototype experimental results are provided in the paper.

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