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High-Efficiency Energy Recycling System for AC Power Source Burn-In Test

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Abstract

This paper presents a feasible method for AC power source burn-in test. The proposed architecture consists of two power stages, the AC/DC converter and the DC/AC inverter, where the former imitates the load characteristic and the latter sends back the recycling energy to the utility. Both two stages are regulated by conventional pulse width modulation (PWM) and operated in current-mode control. It consumes a less amount of energy than conventional method and provides extra flexibility for the test load. In addition, it can also correct the utility current which is rich in high harmonic distortion. To implement the proposed idea, a simple control strategy and system design are presented in this paper. Case study for AC motor driver is demonstrated by means of prototype experiment to prove its performance and effectiveness.

1. Introduction

Traditionally, a new manufacture of AC power supplies, such as UPS, AC motor driver, ...etc., must have a burn-in test about 24 to 72 hours in order to verify the stiffness of this new equipment and to improve its defective index, reliability and stability. A load bank is generally used, and significant energy is wasted. In order to reduce production cost, the burn-in test energy must be save. Therefore, it should not be encouraged to use the conventional method in the future.

To improve this situation, a load consumption free method is needed. By replacing the load bank with a newly developed power electronic technology, the consumed energy can be fed back to the utility system. Recently, some methods for power supplies and UPS's burn-in have been proposed and demonstrated [1-2]. These offer many advantages over the conventional resistor bank including energy cost reduction, test space reduction, reduced air ventilation requirement, and lower peak power demand [1]. However, there are very little literature consider about the burn-in test of AC motor driver, furthermore, none has considered improving the utility harmonics induced by the burn-in test equipment.

In this paper, a general strategy about exam of AC power supplies including UPS and/or AC motor driver burn-in test is presented. As the AC motor driver is non-synchronized with the utility, the voltage-mode control strategy which usually presented in UPS burn-in test can not be used directly here. This involves the proposed consumption power feedback unit (CPFU) consists of two power stages, where the first stage used to imitates the load characteristic, such as the RL load characteristic to the AC motor driver, and the second stage sent back the recycling energy to the utility. The proposed method uses a current-mode control instead of the voltage-mode control in order to improve the induced utility harmonics. The test energy can be fed back to the utility with two different operating modes, called the power control mode and the power correction mode respectively. These two stages are independently operated to implement the desired functions. In this paper, the theoretical expectation is verified by the experimental results in a laboratory prototype system.

2. System Configuration

Fig. 1 shows the main circuit of the proposed CPFU system. It consists of a three-phase PWM converter and a mirrorlike inverter, which is connected, in parallel to utility source. These two stages have the same control algorithm except that an additional DC bus regulation loop which existing only in the latter. Thus, we focus only on the latter stage

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shown in the subblock for the system analysis and design. From the subblock shown in Fig. 1, we have

$$V_{Rn} = R_f i_R + L_f \frac{di_R}{dt} + d_1^* \frac{V_{dc}}{2} + v_{on}, \quad (1)$$

$$V_{Sn} = R_f i_S + L_f \frac{di_S}{dt} + d_2^* \frac{V_{dc}}{2} + v_{on}, \quad (2)$$

$$V_{Tn} = R_f i_T + L_f \frac{di_T}{dt} + d_3^* \frac{V_{dc}}{2} + v_{on}, \quad (3)$$

$$C_{dc} \frac{dV_{dc}}{dt} = i_R d_1^* + i_S d_2^* + i_T d_3^* - i_{load}, \quad (4)$$

where d_1^*, d_2^*, d_3^* are the switching function, and. are determined by the pulse width modulators. For a balance three-phase system without a neutral line, the sums of the phase currents and phase voltages are equal to zero, thus, the term v_{0n} can be obtained as follows:

$$v_{on} = -\frac{1}{6} V_{dc} \sum_{k=1}^{3} d_k^*$$

Therefore, these equations can be represented as the matrix-form differential equation as follows:

$$Z\dot{X} = AX + BU, \quad (5)$$

where

$$X = [i_R \quad i_S \quad i_T \quad V_{dc}], \quad (6)$$

$$U = [V_{Rn} \quad V_{Sn} \quad V_{Tn} \quad V_{dc}], \quad (7)$$

$$Z = \begin{bmatrix} L_f & 0 & 0 & 0 \\ 0 & L_f & 0 & 0 \\ 0 & 0 & L_f & 0 \\ 0 & 0 & 0 & C_{dc} \end{bmatrix}, \quad (8)$$

$$B = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \quad (9)$$

$$A = \begin{bmatrix} -R_f & 0 & 0 & -\frac{d_1^*}{2} + \frac{1}{6}\sum_{k=1}^{3} d_k^* \\ 0 & -R_f & 0 & -\frac{d_2^*}{2} + \frac{1}{6}\sum_{k=1}^{3} d_k^* \\ 0 & 0 & -R_f & -\frac{d_3^*}{2} + \frac{1}{6}\sum_{k=1}^{3} d_k^* \\ d_1^* & d_2^* & d_3^* & -\frac{1}{R_L} \end{bmatrix} \quad (10)$$

This mathematical model is a general model, it provides an exact solution if the switching function d_k^* is defined. It is also valid in the computer simulation. However, it is time-variant, nonlinear, and includes switching functions, therefore, it is difficult to evaluate the closed-form solutions including stead-state and dynamic performance of the system [5].

However, if the system response in minor current loop is independent of the outer voltage loop, then the analysis can be simplified. In order to simplify the design procedure, especially for the engineers, we assume the minor loop has reached the steady state when proceeding with the output loop. Thus, a simplification in design procedure can be obtained.

3. Control System Design

3.1 Current Regulator

In this paper, the ramp comparison control is chosen as the switching strategy, thus the ON or OFF states of switches are determined by the pulse width modulators. If the modulating signals are smaller than the carrier of a triangular wave, then the corresponding switches SW1, SW2, SW3 are ON, otherwise OFF. Based on the state-space averaging technique and ignoring the high-frequency components, the average voltage in one switching period for phase R is obtained as:

$$(d_1^* \frac{V_{dc}}{2})_{av} = -\frac{i_{mR}}{2E_c} V_{dc}, \quad (11)$$

where E_c is the peak value of the triangular wave. Similarly, we have the same form equations for phase S and T. Here, three independent current loop regulators are used. If we consider the source voltage and v_{on} as disturbances, the control block diagram of the current loop including the current regulator G_{ACR} and a noise filter G_{fb} can be constructed as Fig. 2, where K_{PWM} is the gain of the pulse width modulator and is represented as:

$$K_{PWM} = \frac{V_{dc}}{2E_c}. \tag{12}$$

To improve the control performance of the current loop, the current regulator and the noise filter are chosen as

$$G_{ACR} = \frac{\tau_{z1}s+1}{(\tau_{p1}s+1)(\tau_{p2}s+1)}, \tag{13}$$

$$G_{fb} = \frac{k_{CT}}{\tau_{p3}s+1}. \tag{14}$$

3.2 Voltage Regulator

Here, we prepare to introduce a simple design concept, termed the power balance concept, instead of a complicated analysis of the voltage loop control. The dynamic equation of the dc bus voltage is shown as follows:

$$i_o = C_{dc}\frac{dV_{dc}}{dt} + i_{load}, \tag{15}$$

The averaged small signal model is based on the idea of power balance

$$3v_{rms}i_{rms} = V_{dc}i_o, \tag{16}$$

Since the current commands are obtained from the voltage regulator output through a multiplier where they are multiplied by the related voltage signal, so in a closed-form control block diagram, we have

$$i_{rms} = k_{rms}v_{rms}i_{ref}, \tag{17}$$

$$k_{rms} = k_{ACR}k_{pt}k_m, \tag{18}$$

where k_{ACR} is the closed loop gain of the current. By neglecting the higher order terms, and combining with the voltage regulator G_{ACR}, we obtain the small signal control block diagram of the system. It is shown as Fig. 3, where

$$G_k = \frac{3k_{rms}V^2{}_{rms}}{V_{dc}}, \tag{19}$$

$$Z_L(s) = \frac{1}{sC_{dc}}, \tag{20}$$

$$G_z = \frac{I_o}{V_{dc}}, \tag{21}$$

$$G_{vin} = \frac{6k_{rms}V_{rms}I_{ref}}{V_{dc}}. \tag{22}$$

Thus, we can deduce the expression of the dc output voltage as

$$\hat{v}_{dc} = T_{ref}\hat{v}_{ref} + T_v\hat{v}_{rms} - Z_o\hat{i}_{load}, \tag{23}$$

where T_{ref}, T_v, Z_o are denoted as the control function, the audio susceptibility, and the dc bus output impedance, respectively, and can be derived as follows:

$$T_{ref} = \frac{\hat{v}_{dc}}{\hat{v}_{ref}} = \frac{G_kZ_LG_{AVR}}{\Delta}, \tag{24}$$

$$T_v = \frac{\hat{v}_{dc}}{\hat{v}_{rms}} = \frac{Z_LG_{vin}}{\Delta}, \tag{25}$$

$$Z_o = -\frac{\hat{v}_{dc}}{\hat{i}_{load}} = \frac{Z_L}{\Delta}, \tag{26}$$

$$\Delta = 1 + Z_L(k_{fb}G_kG_{AVR} + G_z). \tag{27}$$

Above equations show the system bandwidth is affected by the voltage regulator G_{AVR}, the input voltage, and the dc bus voltage. It appears that a large input voltage leading to a wider system bandwidth, and a larger output voltage decreasing the system bandwidth.

3.3 Power Control Mode

When the proposed CPFU's inverter operates in the power control mode, it is used to transfer the test energy by feeding in-phase current to the utility. As it is simple to achieve, no further discussion presents here, a detailed information can be referred from Ref.[3].

3.4 Power Factor Correction Mode

When the CPFU's inverter operates in the power factor correction mode, it can be used to transfer the test energy

and reduce the reactive and harmonic current drawn from the utility by the tested equipment. Assume

$$V_s(t) = v_m \sin \omega t, \tag{28}$$

$$i_L(t) = \sum_{n=1}^{\infty} a_n \sin n\omega t + \sum_{n=0}^{\infty} b_n \cos n\omega t, \tag{29}$$

Obviously, the first term of the above equation is the only term which drawing real power from utility, and it would be best if the utility is intended to supply only this term. There are two strategies to achieve this function. The first one is to detect the harmonic content, then the proposed CPFU's inverter generates the detected harmonics plus the delivered test energy. Several harmonics detection schemes such as the integration method and synchronous detection method [5-6] can be used to separate this term from the others. The second method is present in [7]. This strategy is with no detection, but only regulates the utility to supply the in-phase sinusoidal current which is corresponding to the fundamental term, a_1. The declarative method is based on the idea that the active power filter forces the mains current to be a sinewave and in phase with the main voltage. It presents the same good performance with the first method in normal case, but with a superior response in the situation of the main voltage unbalance and/or harmonic.

In this paper, we adopt the second strategy with a little modification. The proposed CPFU's inverter plays the parallel active power filter role together with additional function of test energy transfer when it is operating in power factor correction mode.

4. Experimental Results

In this paper, a practical exam of AC motor driver is presented. Fig. 4 shows the experimental results of the proposed AC motor driver burn-in test which operating in power control mode. Fig. 4(a) shows the utility voltage and AC motor driver input current, Fig. 4(b) shows the utility voltage and the CPFU's inverter output current. It shows clearly that the CPFU's inverter output current is in-phase with the utility and is sinusoidal. This means that only real power passes through the proposed CPFU' inverter. Fig. 4(c) shows the utility voltage and the current which used to compensate the switching loss, including the tested AC motor driver and the proposed CPFU. A measured result is shown in Table 1, where the overall efficiency of the proposed CPFU is lower in small test level and is higher in large test level. The dissipation includes the switching loss in the main circuit and control circuit, and the cooling fan loss. The total efficiency presented in the utility is above 80 percent; that is, about 80 percent of the test energy through the AC motor driver can be fed back to the utility.

Fig. 5 shows the experimental results for the CPFU operating in the power correction mode. Fig. 5(a) shows the utility voltage and AC motor driver input current. Fig. 5(b) shows the proposed CPFU's inverter output current, it shows the proposed CPFU output current is switched to compensate for the harmonics generated by the AC motor driver and is rich of harmonics. Fig. 5(c) shows the net input current drawn from the utility.

Comparing the experimental results in Fig. 4(c) with the experimental results in Fig. 5(c), we see that the power factor correction mode draws little reactive power from the utility. This point can also be verified by the measured data shown in Table 2

Table 1: Power control mode.

CPFU's input	CPFU's output	Efficiency (%)	Utility input current(rms.)
620W	470W	75.8	3.4A
1270W	1020W	80.3	5.9A
1810W	1530W	84.5	7.4A
2480W	2130W	85.9	9.5A
3060W	2650W	86.6	11.1A

Table 2: Power factor correction mode.

CPFU's input	CPFU's output	Efficiency (%)	Utility input current(rms)
650W	490W	75.4	1.5A
1130W	900W	79.6	2.8A
1700W	1410W	82.9	4.5A
2380W	2030W	85.2	6.1A
2630W	2260W	85.9	6.8A

5. Conclusion

In this paper, a simple and effective control strategy for consumption power feedback of a AC power supply burn-in test has been described. A current-mode control CPFU

system has been used. It provides two benefits including energy saving and tested equipment power factor correction. Prototype experiments have proven the performance of the proposed method to be effective. Additional benefits have also been obtained beyond the basic function of CPFU operation. The proposed method is suitable for AC equipments, including synchronized (UPS) or non-synchronized (AC motor driver), and can reduce energy costs during product burn-in tests.

Acknowledgement

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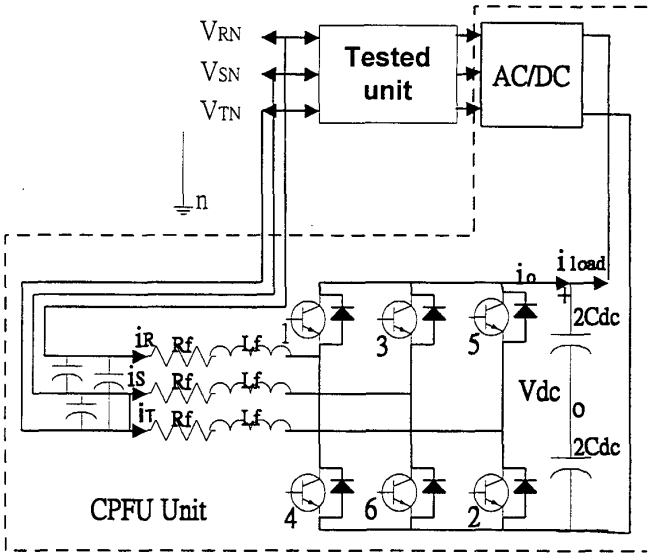

Fig. 1. The main circuit of the proposed CPFU system.

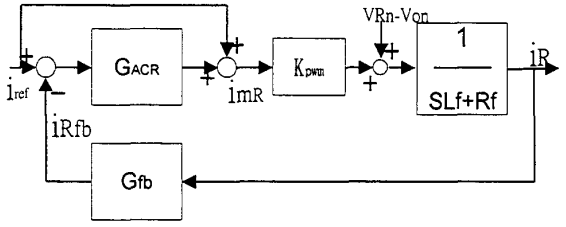

Fig. 2. The control block diagram of the current loop.

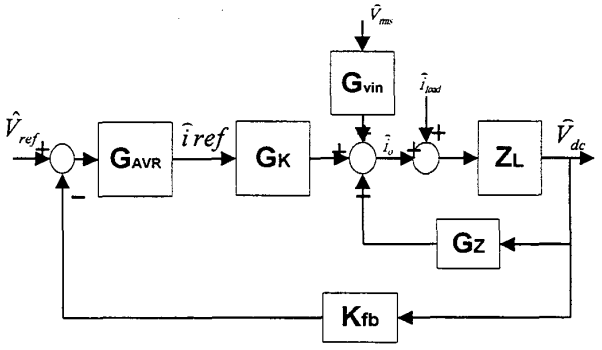

Fig. 3 Control block diagram of the voltage loop control

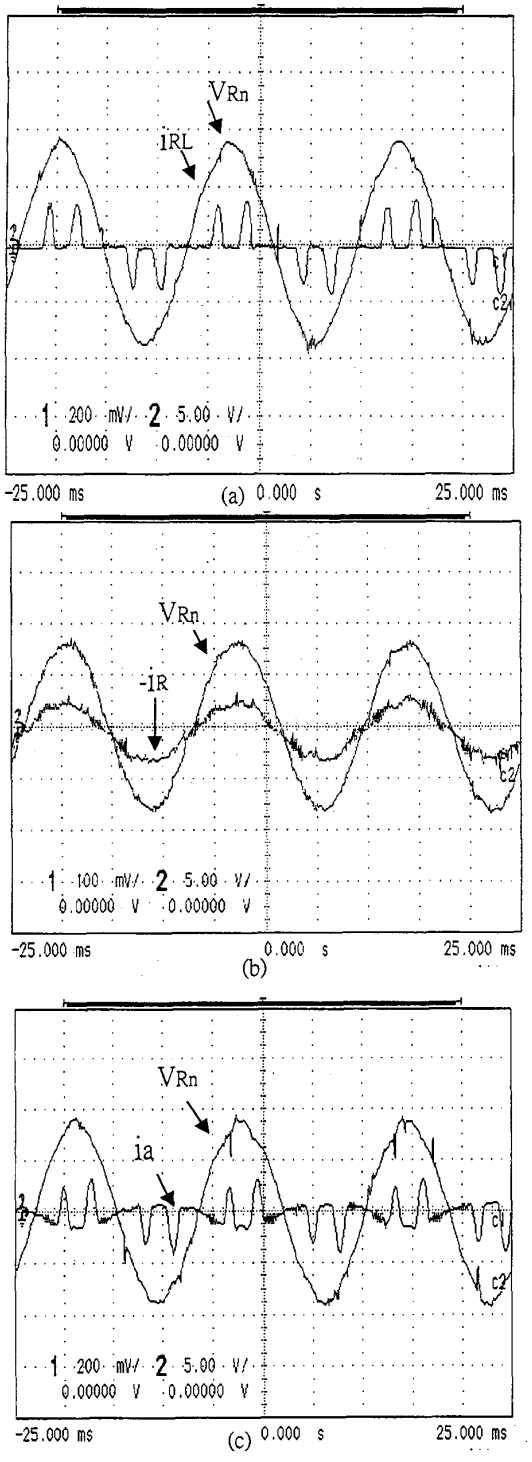

Fig. 4 The experimental results for the power control mode. (PT: 220/6, CT:200/1)

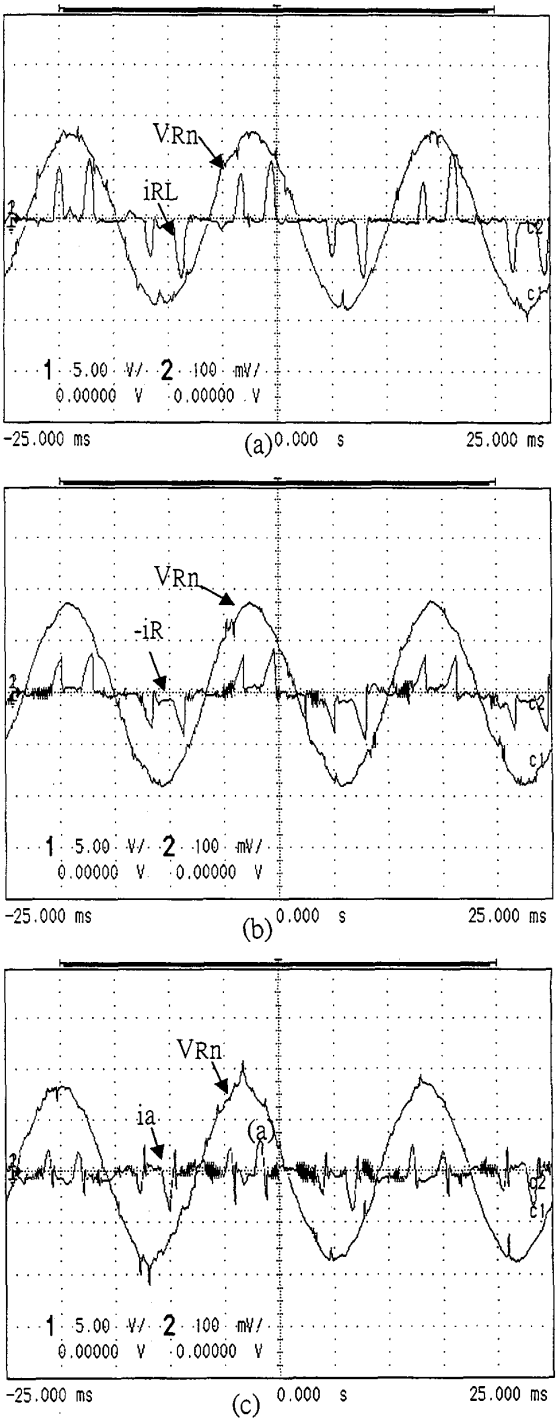

Fig. 5 The experimental results for power factor correction mode .(PT: 220/6, CT:200/1)