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# How to handle a IGBT

Information

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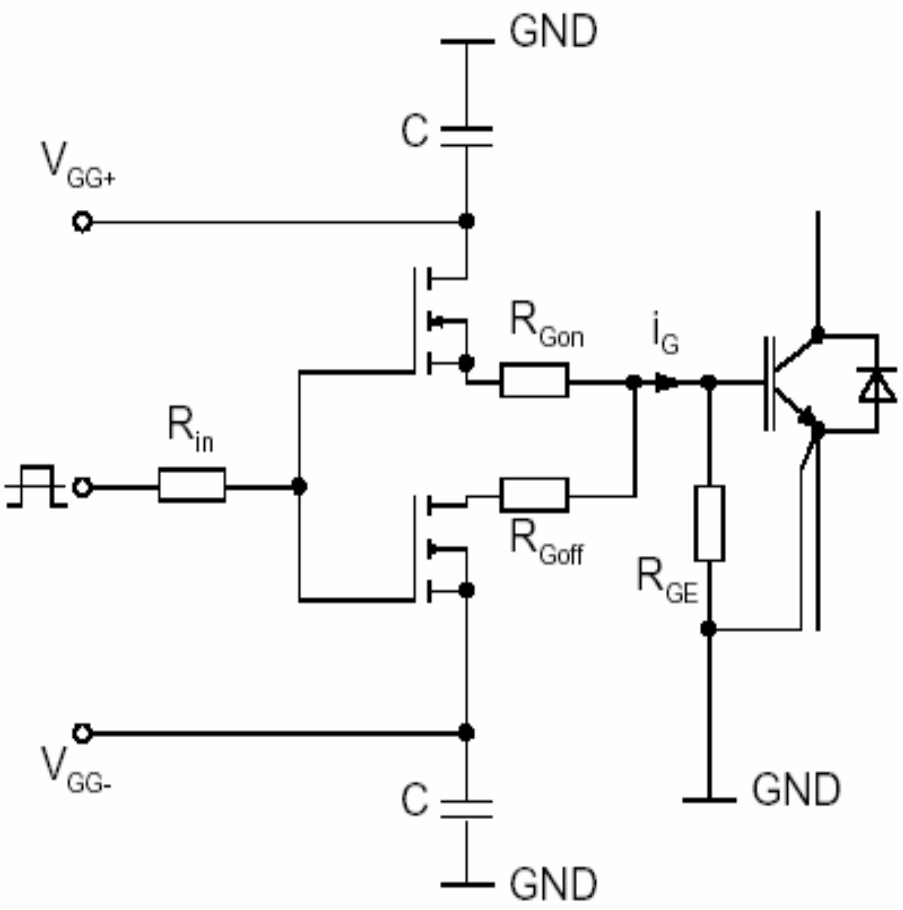
# How can we protect the gate?

Information

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# Gate Emitter Resistor

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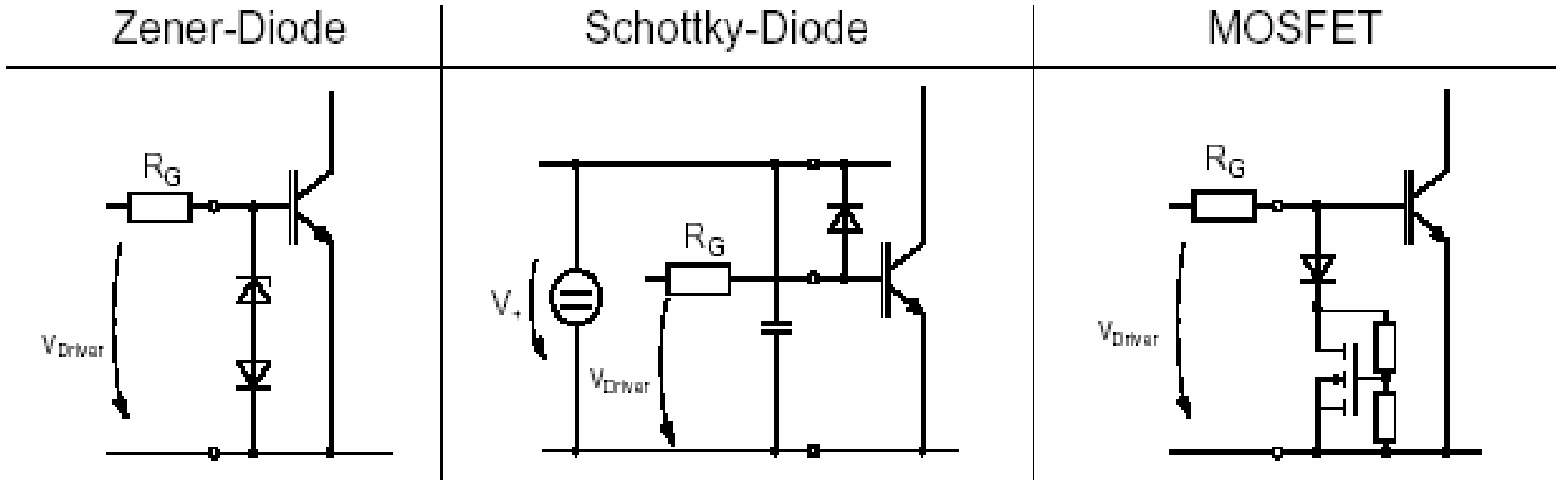




# Gate clamping

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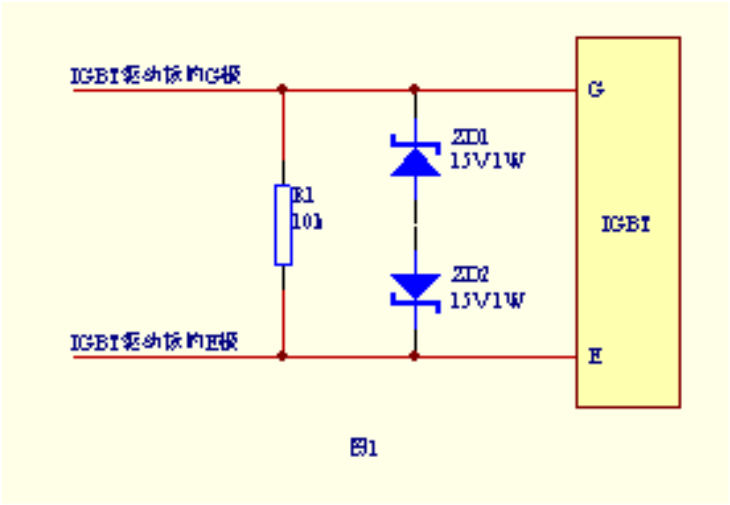


图1



# IGBT Gate protection

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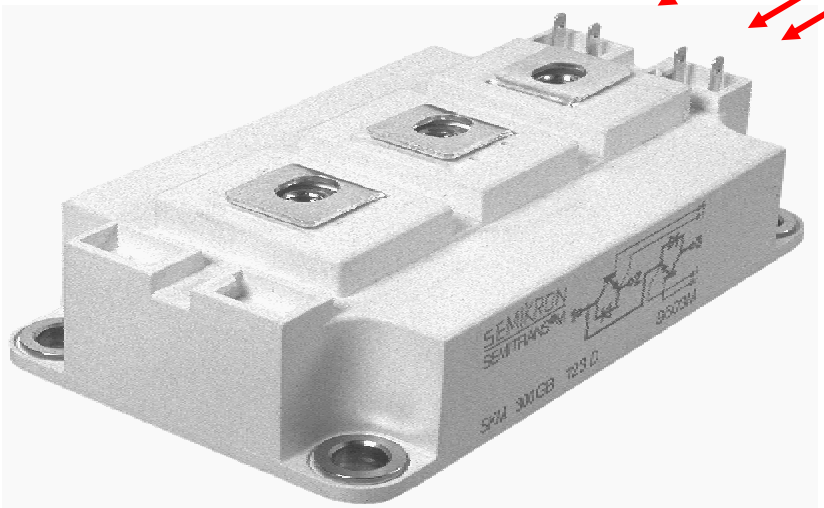
- **q** IGBT modules are ESD sensitive devices.
  - **u** Thus they will delivered with a short circuit connection between gate terminal and auxiliary emitter terminal



- **è** Remove this connection and handle the modules only when it is assured, that the environment is ESD proof



# Table of Contents

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# How should we calculate the driver?

- Which gate driver is suitable for the module SKM 200 GB 128D ?

SKM 200 GB 128 D

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**Absolute Maximum Ratings** $T_{case}$ = 25 °C, unless otherwise specified

| Symbol | Conditions | Values | Units |
|---|---|---|---|
| **IGBT** | | | |
| $V_{CES}$ | | 1200 | V |
| $I_C$ | $T_{case}$ = 25 (80) °C | 286 (205) | A |
| $I_{CRM}$ | $T_{case}$ = 25 (80) °C, $t_p$ = 1 ms | 850 (470) | A |
| $V_{GES}$ | | ± 20 | V |
| $T_{vj}$ ($T_{stg}$) | $T_{operation}$ < $T_{stg}$ | −40 ... +150 (125) | °C |
| $V_{isol}$ | AC, 1 min. | 4000 | V |
| **Inverse Diode** | | | |
| $I_{FAV}$ = − $I_C$ | $T_{case}$ = 25 (80) °C | 190 (130) | A |
| $I_{FRM}$ | $T_{case}$ = 25 (80) °C, $t_p$ < 1 ms | 850 (470) | A |
| $I_{FSM}$ | $t_p$ = 10 ms; sin.; $T_j$ = 150 °C | 1450 | A |
| **Freewheeling Diode** | | | |
| $I_{FAV}$ = − $I_C$ | $T_{case}$ = 25 (80) °C | | A |
| $I_{FRM}$ | $T_{case}$ = 25 (80) °C, $t_p$ < 1 ms | | A |
| $I_{FSM}$ | $t_p$ = 10 ms; sin.; $T_j$ = 150 °C | | A |

**Characteristics** $T_{case}$ = 25 °C, unless otherwise specified

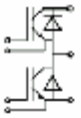
| Symbol | Conditions | min. | typ. | max. | Units |
|---|---|---|---|---|---|
| **IGBT** | | | | | |
| $V_{GE(TO)}$ | $V_{GE}$ = $V_{CE}$, $I_C$ = 6 mA | 4,5 | 5,5 | 6,45 | V |
| $I_{CES}$ | $V_{GE}$ = 0, $V_{CE}$ = $V_{CES}$, $T_j$ = 25 (125) °C | | | 1bd | mA |
| $V_{CE(TO)}$ | $T_j$ = 25 (125) °C | | 1,0 (0,9) | 1,15 | V |
| $r_{CE}$ | $V_{GE}$ = 15 V; $T_j$ = 25 (125) °C | | 6,7 (9,3) | 9,3(1bd) | mΩ |
| $V_{CE(sat)}$ | $I_C$ = 150 A, $V_{GE}$ = 15 V, chip level | | 2,0 (2,3) | 2,4 | V |
| $C_{ies}$ | | | 13 | | nF |
| $C_{oes}$ | $V_{CE}$ = 0, $V_{CE}$ = 25 V, f = 1 MHz | | 2 | | nF |
| $C_{res}$ | | | 2 | | nF |
| $L_{CE}$ | | | | | |

SEMITRANS™ M
SPT IGBT Module

SKM 200 GB 128 D

Preliminary Data

SEMITRANS 3



GB

Features

Design parameters:

**$f_{sw}$ = 10 kHz**

**Rg = 7** Ω

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# Example for design parameters

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- The suitable gate driver must provide the required
  - Gate charge ($Q_G$)
  - Average current ($I_{outAV}$)
  - Gate pulse current ($I_{g.pulse}$)

at the applied switching frequency ($f_{sw}$)



# Demands for the gate driver

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- Gate charge ($Q_G$) can be determined from fig. 6 of the SEMITRANS data sheet

The typical turn-on and turn-off voltage of the gate driver is

$V_{GG+}$ = +15V

$V_{GG-}$ = -8V

Þ $Q_G$ = 1390nC

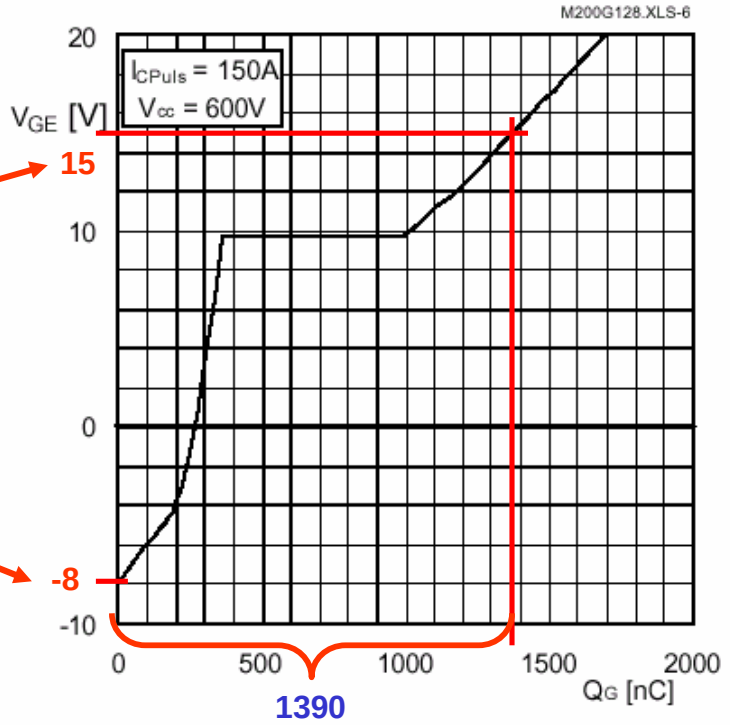


Fig. 6 Typ. gate charge characteristic



# Determination of Gate Charge

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- Calculation of average current:

$I_{outAV} = P / \Delta U \qquad \Delta U = +Ug - (-Ug)$

with $P = E * f_{sw} = Q_G * \Delta U * f_{sw}$

$\Rightarrow I_{outAV} = Q_G * f_{sw}$

$= 1390nC * 10kHz = 13.9mA$



# Calculation of the average current

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- Examination of the peak gate current with minimum gate resistance
  - E.g. $R_{G.on} = R_{G.off} = 7\Omega$
  - $I_{g.puls} \approx \Delta U / R_G = 23V / 7\Omega = 2.3A$



# Calculation of the peak gate current

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## q P tot – Gate resistor

- **u $P_{tot\ Gate\ resistor} = I_{out\ AV} \times \Delta U$**

- **u More information:**

The problem occurs when the user forgets about the peak power rating of the gate resistor.
The peak power rating of many "ordinary" SMD resistors is quite small. There are SMD resistors available with higher peak power ratings. For example, if you take an SKD driver apart, you will see that the gate resistors are in a different SMD package to all the other resistors (except one or two other places that also need high peak power). The problem was less obvious with through hole components simply because the resistors were physically bigger.

The Philips resistor data book has a good section on peak power ratings.



# Power explication of the Gate Resistor

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- The absolute maximum ratings of the suitable gate driver must be equal or higher than the applied and calculated values
  - Gate charge $Q_G$ = 1390nC
  - Average current $I_{outAV}$ = 13,9mA
  - Peak gate current $I_{g.pulse}$ = 2.3A
  - Switching frequency $f_{sw}$ = 10kHz
  - Collector Emitter voltage $V_{CE}$ = 1200V
- Number of driver channels: 2 (GB module)
  - dual driver



# Choice of the suitable gate driver

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- According to the applied and calculated values, the driver e. g. SKHI 22A is able to drive SKM200GB128D

**Absolute Maximum Ratings**

| Symbol | Term | | Values | Units |
|---|---|---|---|---|
| $V_S$ | Supply voltage prim. | | 18 | V |
| $V_{iH}$ | Input signal volt. (High) | SKHIxxA | $V_S$ + 0,3 | V |
| | | SKHI22B | 5 + 0,3 | V |
| $Iout_{PEAK}$ | Output peak current | | 8 | A |
| $Iout_{AVmax}$ | Output average current | | 40 | mA |
| $f_{max}$ | max. switching frequency | | 50 | kHz |
| $V_{CE}$ | Collector emitter voltage sense across the IGBT | | 1700 | V |
| dv/dt | Rate of rise and fall of voltage secondary to primary side | | 50 | kV/µs |
| $V_{isolIO}$ | Isolation test voltage input-output (1 min.AC) | Standard | 2500 | Vac |
| | | Version „H4" | 4000 | Vac |
| $V_{isol12}$ | Isolation test voltage ouput 1 - output 2 (1 min.AC) | | 1500 | V |
| $R_{Gonmin}$ | Minimum rating for $R_{Gon}$ | | 3 | Ω |
| $R_{Goffmin}$ | Minimum rating for $R_{Goff}$ | | 3 | Ω |
| $Q_{out/pulse}$ | Max. rating for output charge per pulse | | 4 [1)] | µC |
| $T_{op}$ | Operating temperature | | - 40... + 85 | °C |
| $T_{stg}$ | Storage temperature | | - 40... + 85 | °C |

Calculated and applied values:

- $I_{g.pulse}$ = 2.3A @ $R_g$ = 7Ω
- $I_{outAV}$ = 13.9mA
- $f_{sw}$ = 10kHz
- $V_{CE}$ = 1200V
- $Q_G$ = 1390nC

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# Comparison with the parameters in the driver data sheet

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# Influence of dead time

consideration

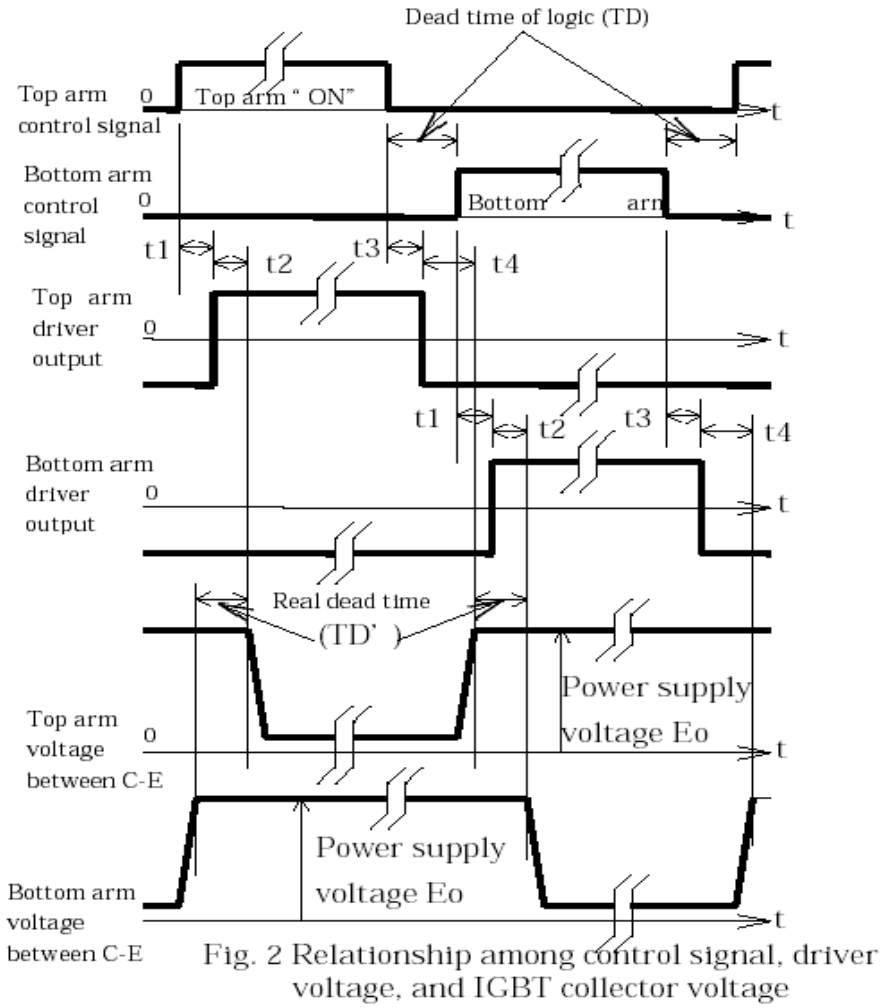


Fig. 2 Relationship among control signal, driver voltage, and IGBT collector voltage

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# Dead time of logic and IGBTs terminals

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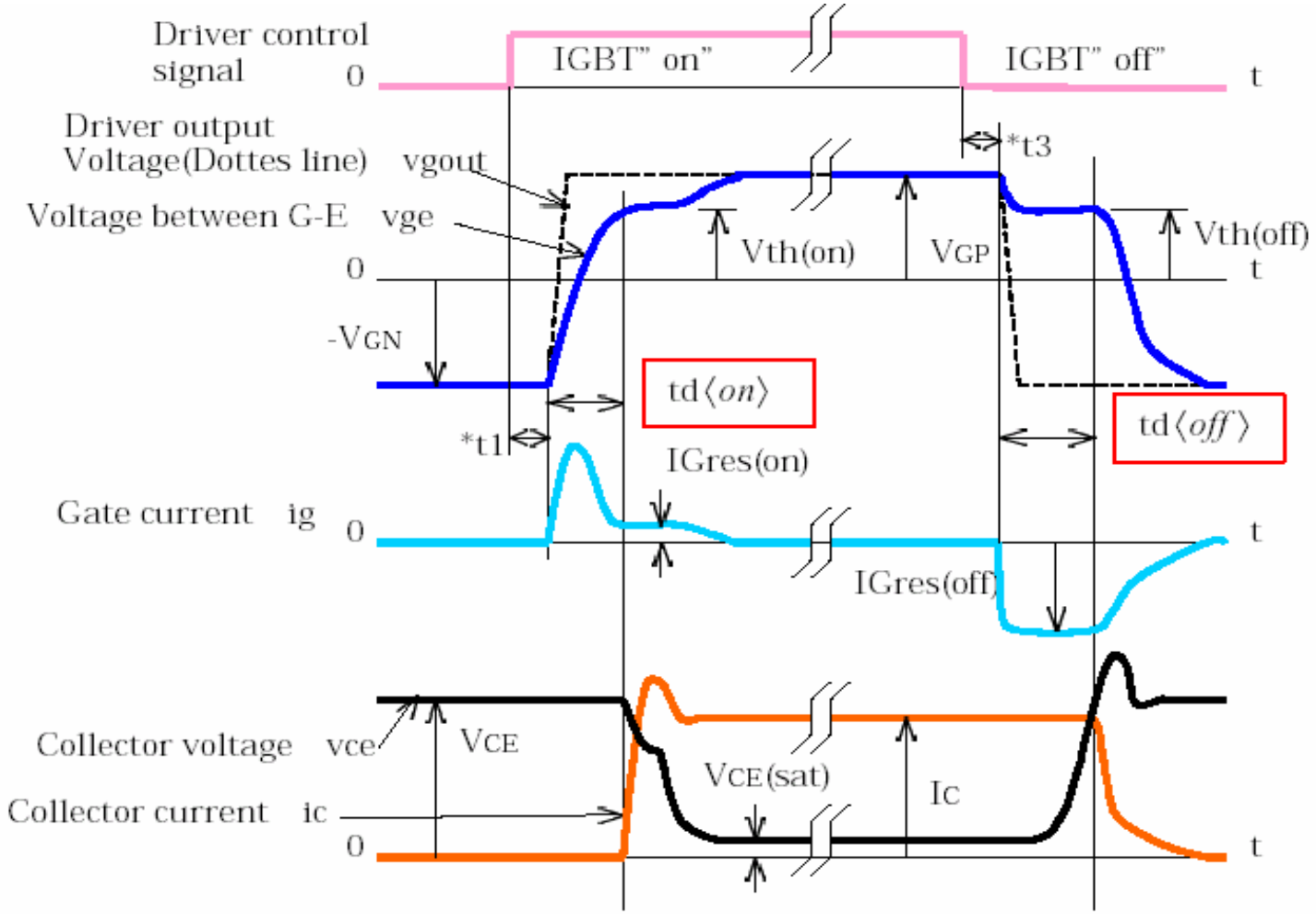


# Dead time

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- Example:
  - Dead time = 3 us logic level
    - Turn on delay 1 us
    - Turn off delay 2.5 us
      - Real dead time:  3us – (2.5us-1us) = 1.5 us



# Dead time explanation

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# Influence of the stray inductance

Explanation

- **q** Why low inductive DC-link design?
  - **u** Due to stray inductances in the DC link, voltage overshoots occur during switch off of the IGBT:

$$v_{overshoot} = L_{stray} \cdot \frac{di}{dt}$$

  - **u** These voltage overshoots may destroy the IGBT module because they are added to the DC-link voltage and may leed to $V_{CE} > V_{CEmax}$

$$v_{CE} = v_{overshoot} + v_{DC\ link}$$

- **è** With low inductive DC-Link design (small $L_{stray}$) these voltage overshoots can be reduced significantly.



# Motivation

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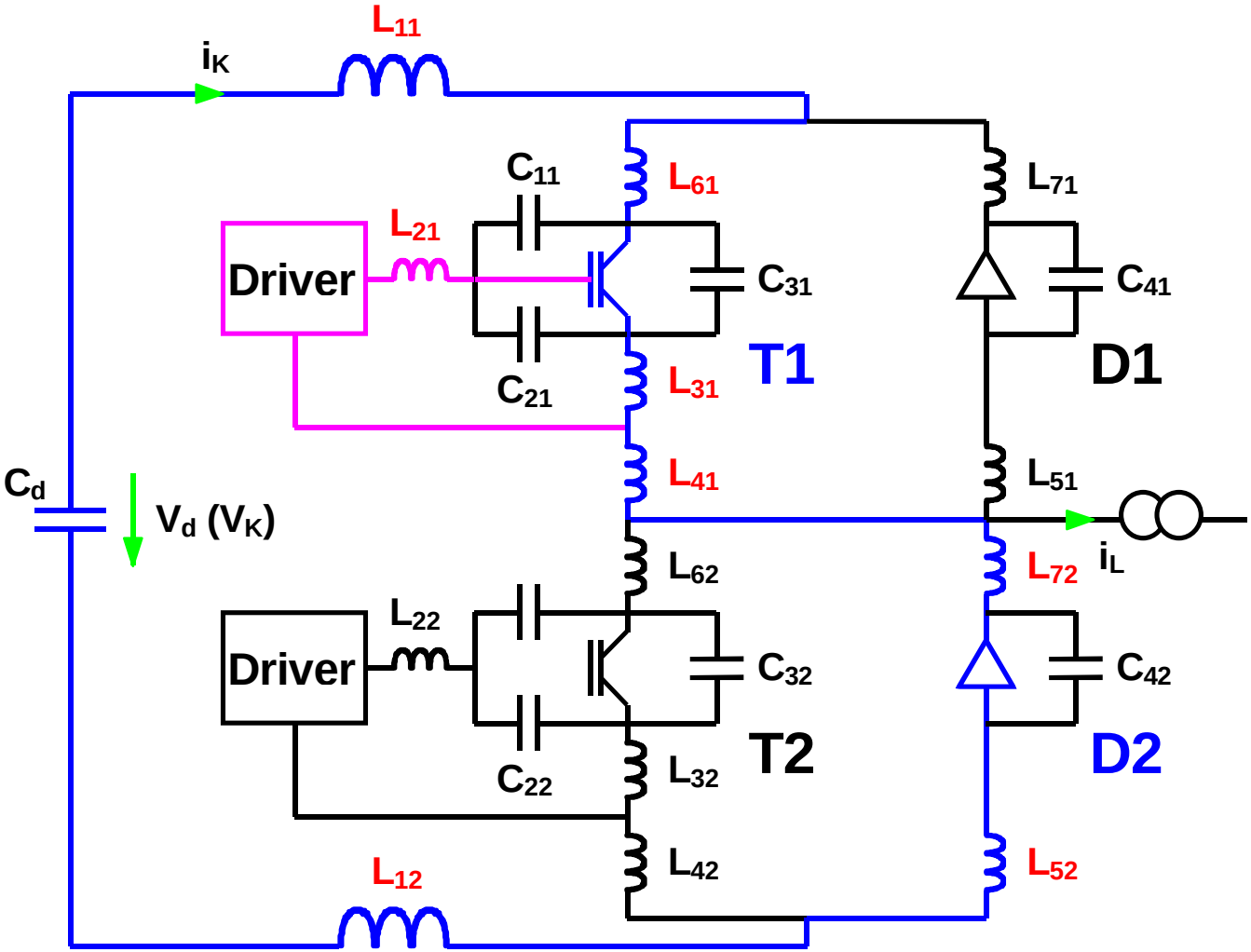




# Parasitic Elements in a Commutation Circuit

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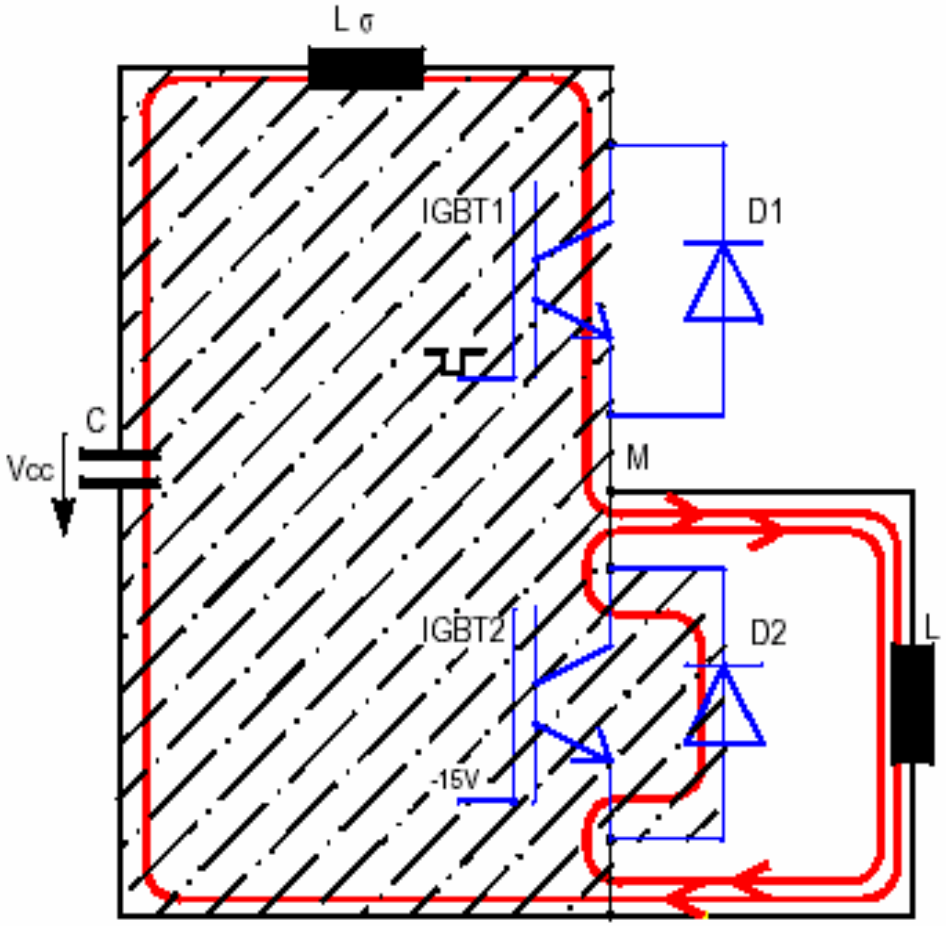


# What means: stray inductance?

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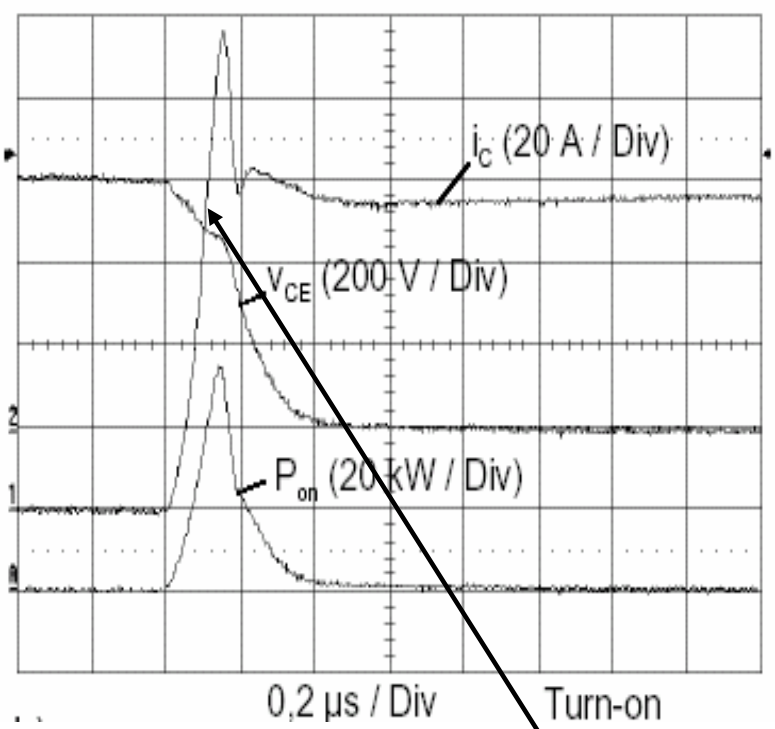
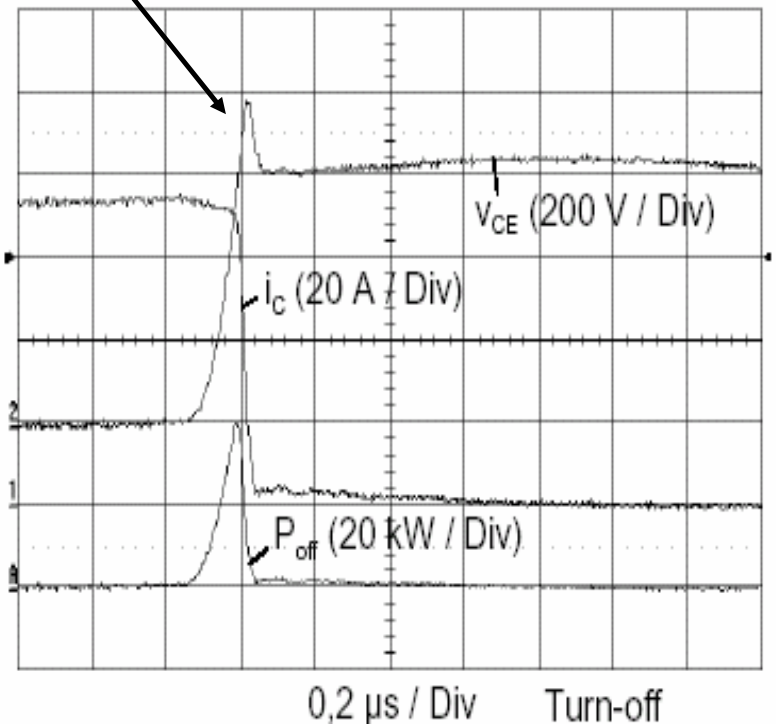
Over voltage by a IGBT modules on the terminals




Voltage drop because of the stray inductance

# Turn on and turn off

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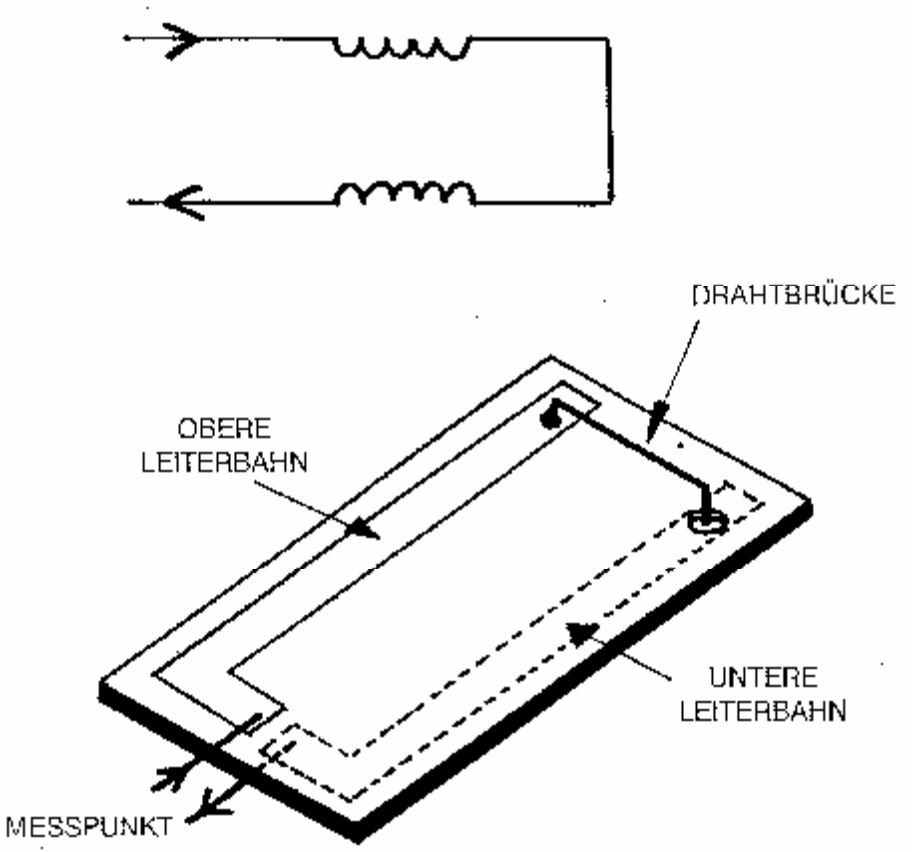




# decrease the Inductance

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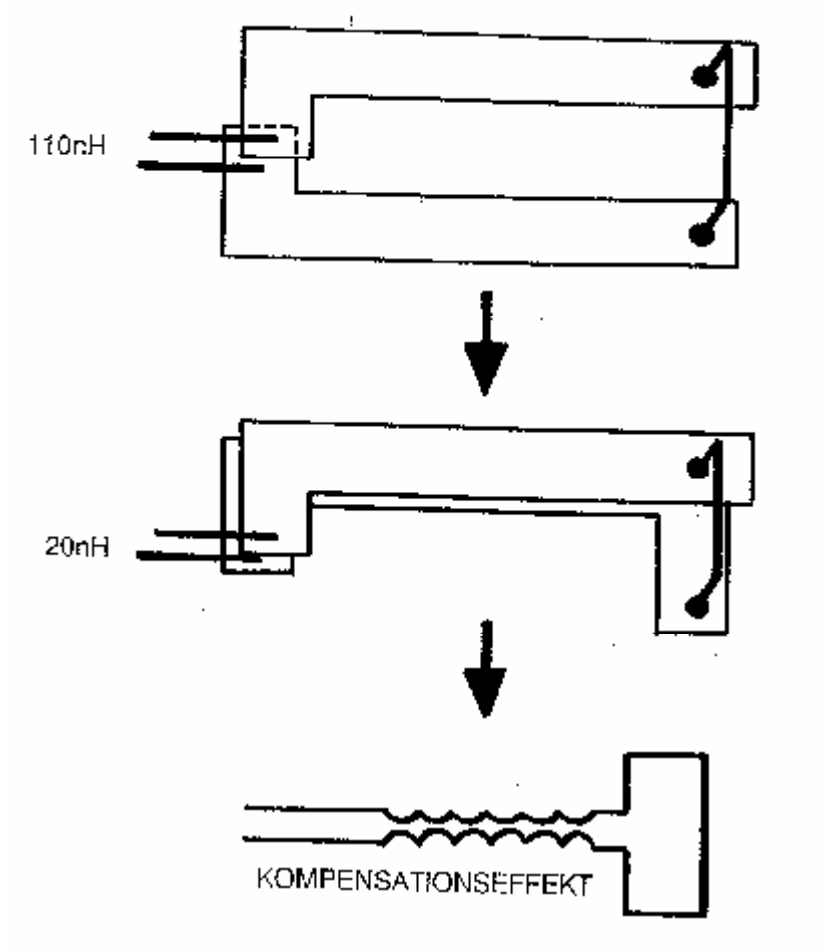




# Decrease the Inductance

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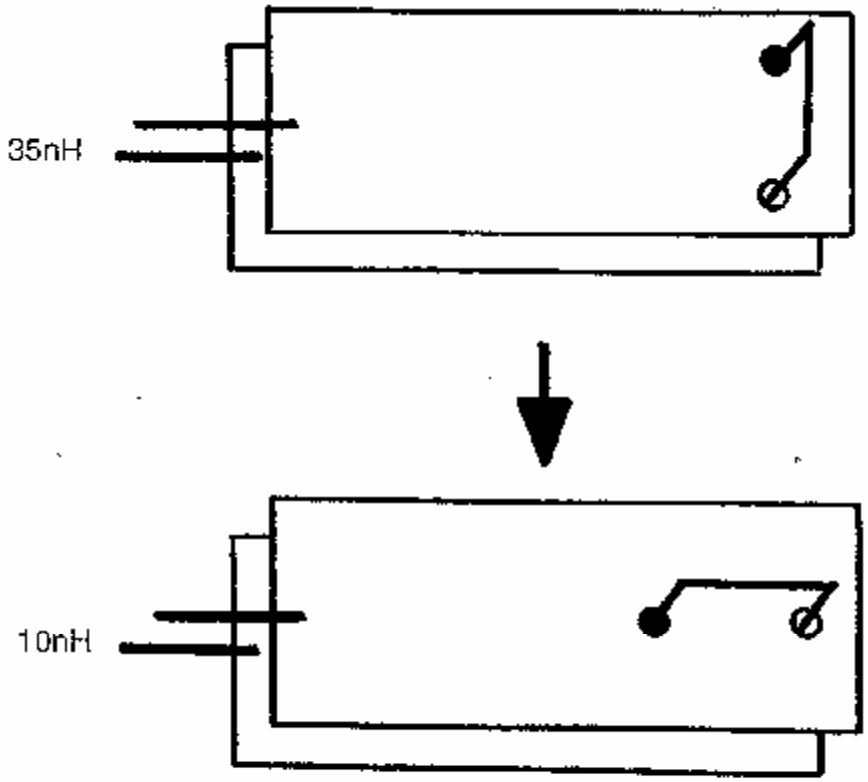


WARUM IST DIES BESSER?



# Decrease the Inductance

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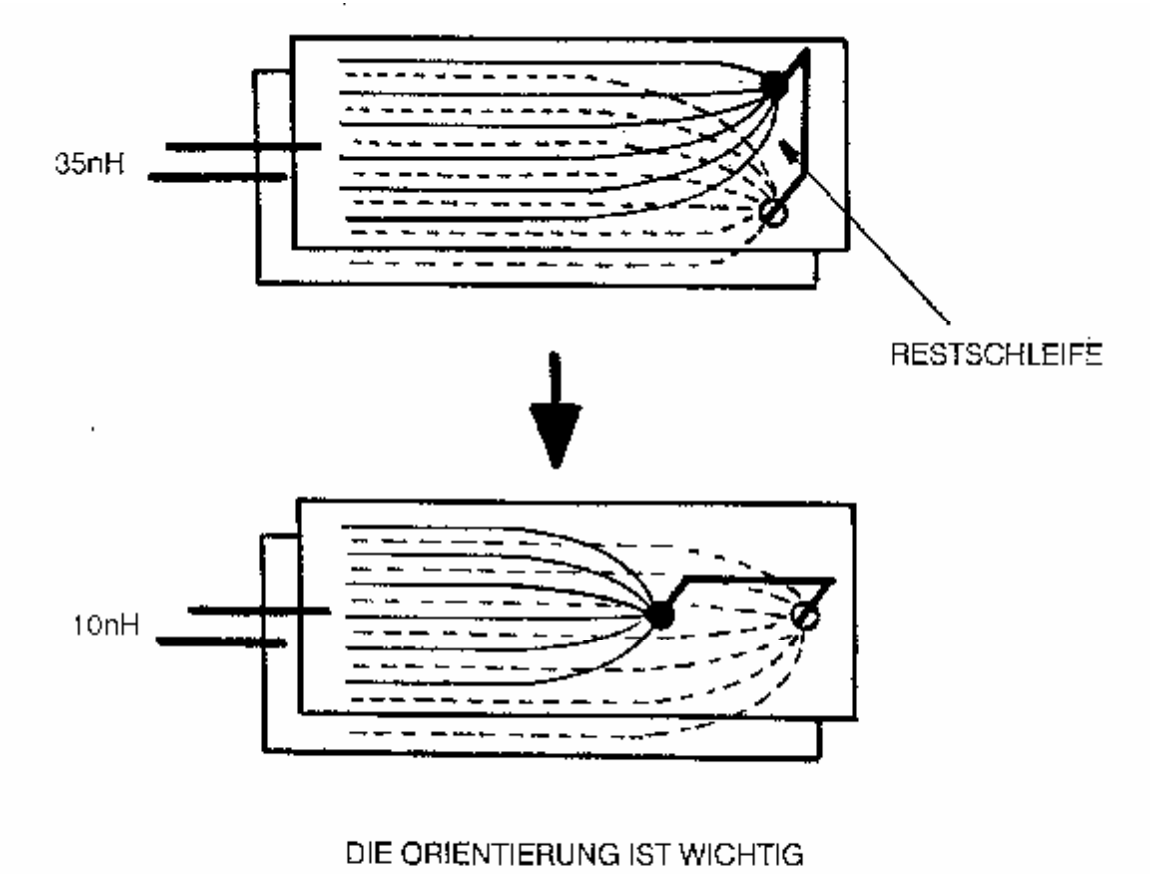


# Decrease the Inductance

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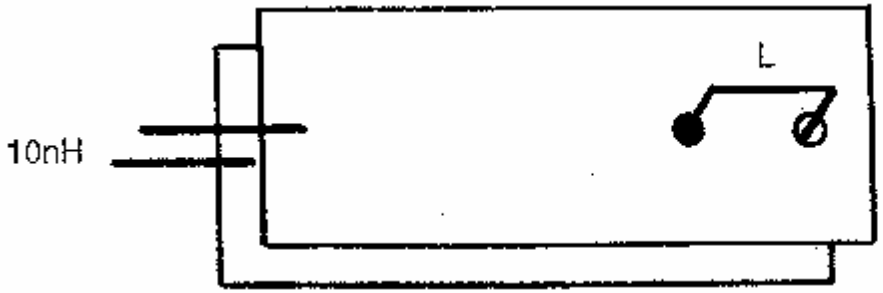
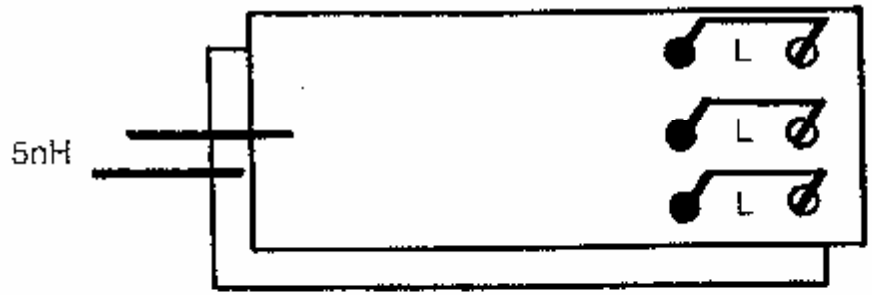



$\Delta V = L \cdot \frac{dI}{dt}$

. . . . . DAS NOCH VERBESSERT WERDEN KANN




$\Delta V = \frac{1}{3} L \cdot \frac{dI}{dt}$

DURCH PARALLELE KOMPONENTEN



# Decrease the Inductance

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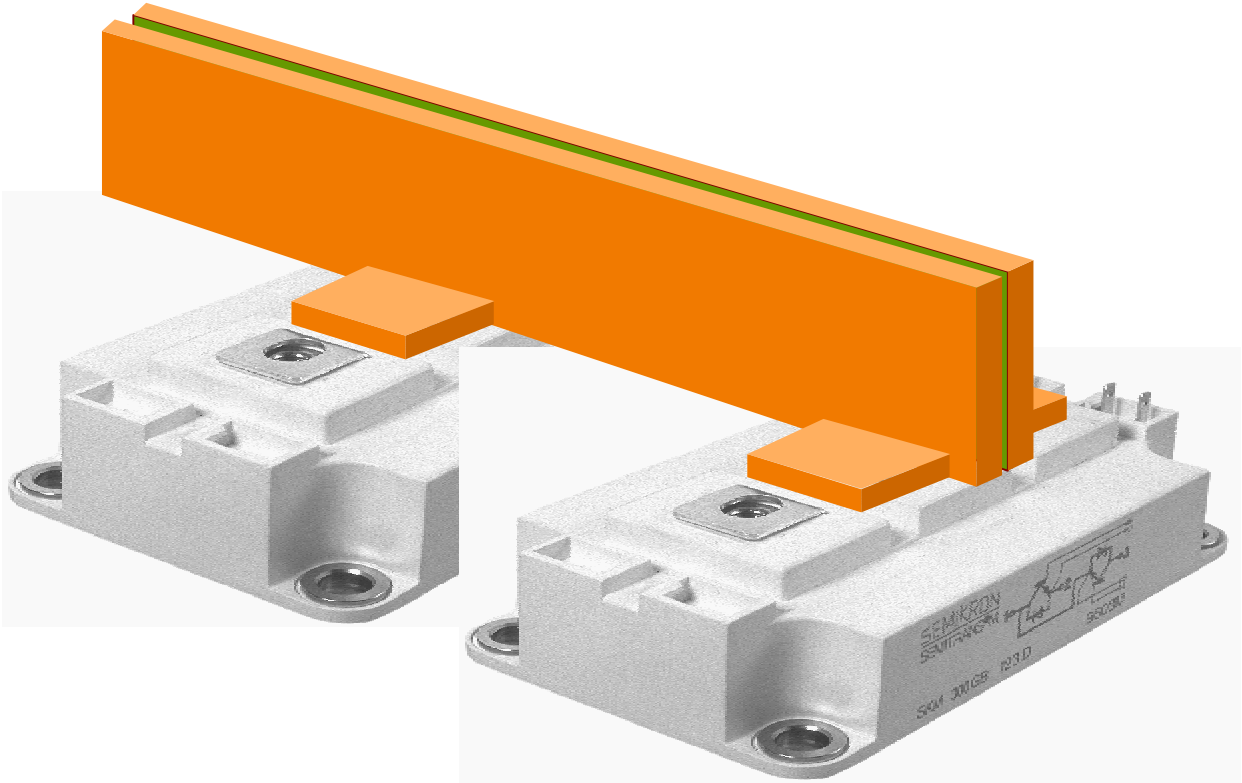
- For paralleling standard modules a minimum requirement is DC-link design with two paralleled bars





# Low Inductance DC-link Design

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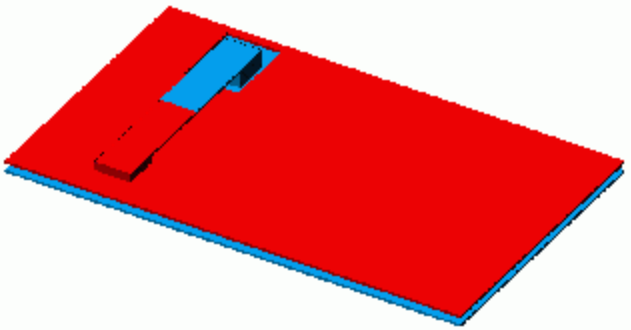
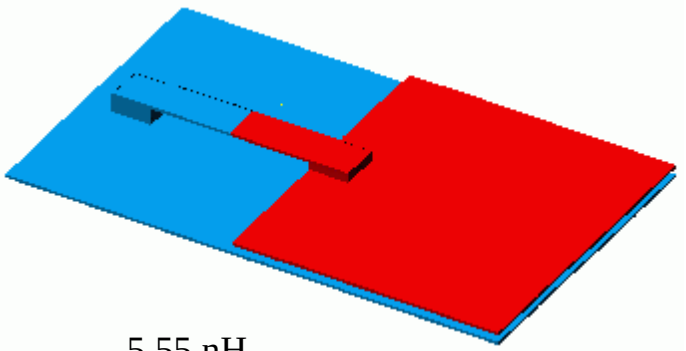
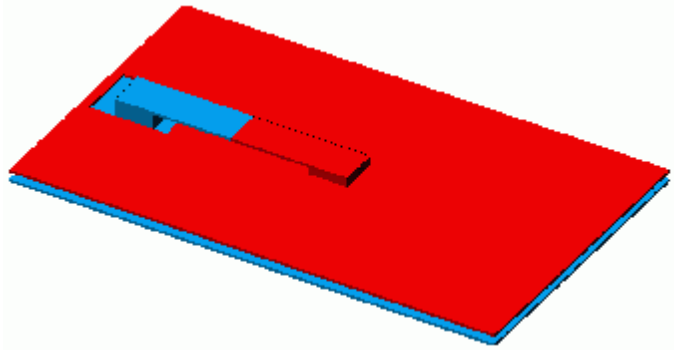


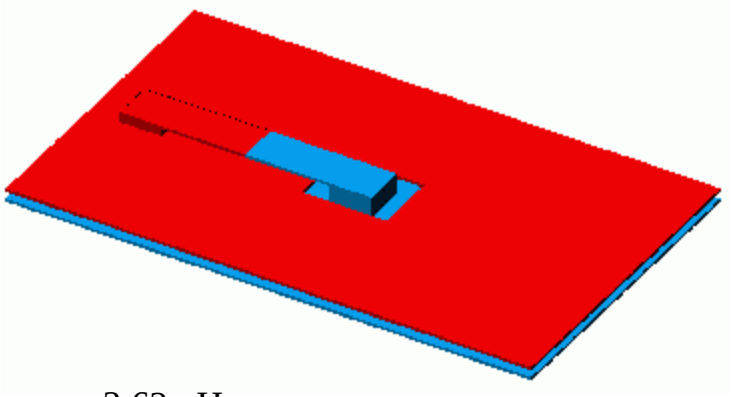
4,56 nH



5,55 nH



4,42 nH



3,62 nH



# Influence of +/- terminal structure

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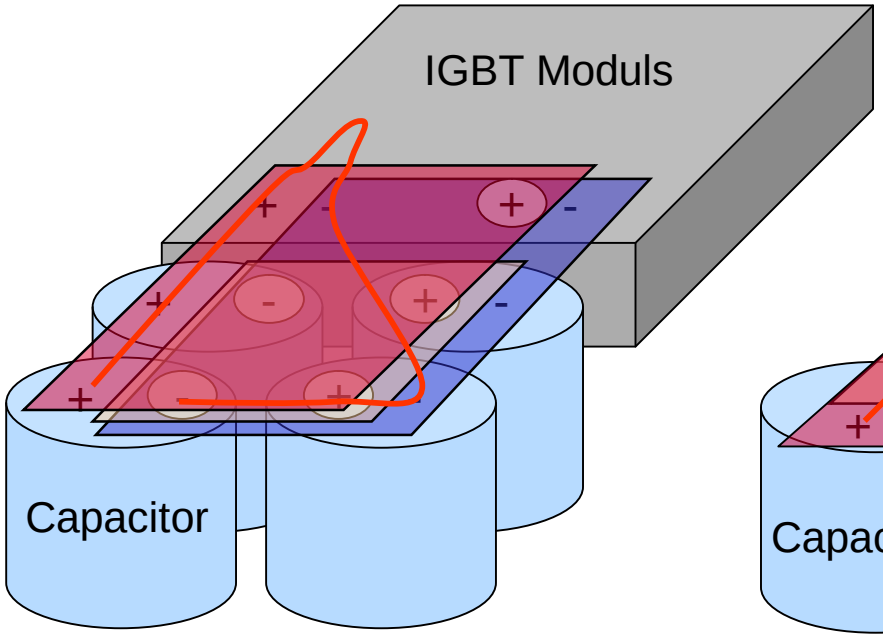
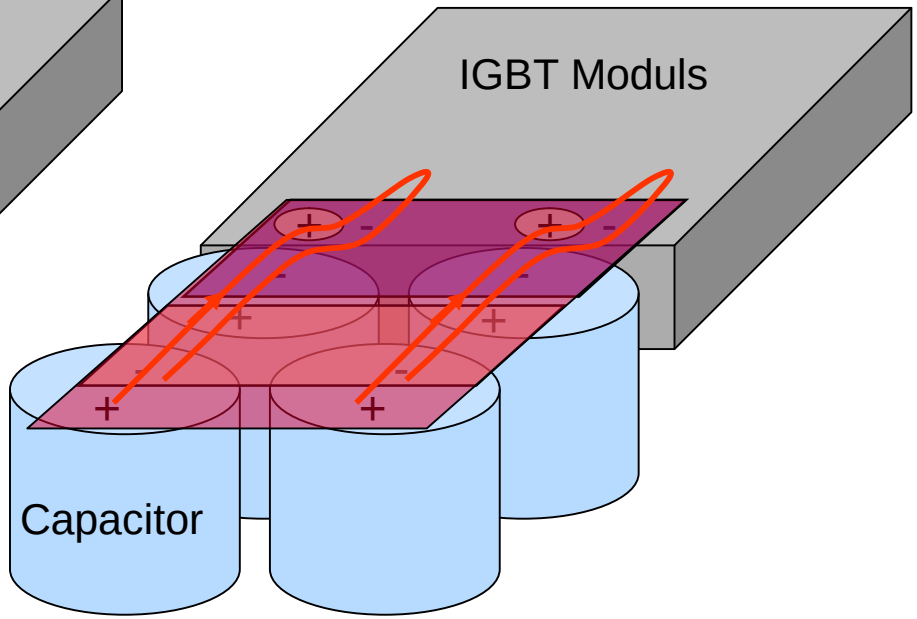
- Comparison of different designs
  - Two capacitors in series
  - Two serial capacitors in parallel

Typical solution




**Low inductive solution**






# Low inductance DC-link design

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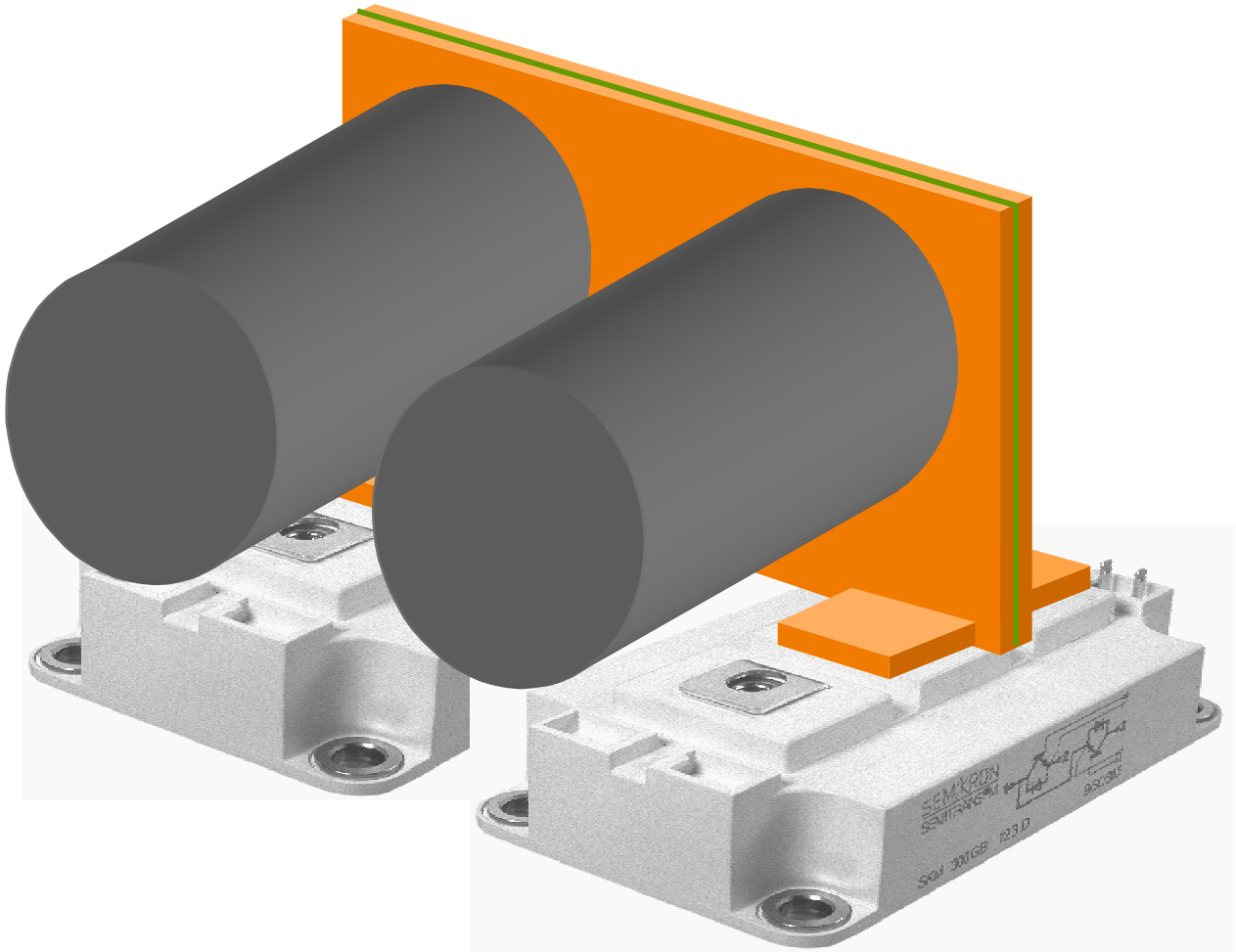

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# Low Inductance DC-link Design

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- Also the capacitors have to be decided
  - Capacitors with different internal stray inductance are available
  - Choose a capacitor with very low stray inductance!

$L_{stray}$ = ?

Ask your supplier!



# Low inductance DC-link capacitors

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# Snubbers

Explanation

- **q** Why use a snubber capacitor?
  - **u** Due to stray inductances in the DC link, voltage overshoots occur during switch off of the IGBT:

$$v_{overshoot} = L_{stray} \cdot \frac{di}{dt}$$

  - **u** These voltage overshoots may destroy the IGBT module because they are added to the DC-link voltage and may leed to $V_{CE} > V_{CEmax}$

$$v_{CE} = v_{overshoot} + v_{DC\ link}$$

- **è** The snubber capacitor works as a low pass filter and “takes over” the voltage overshoot



# Motivation

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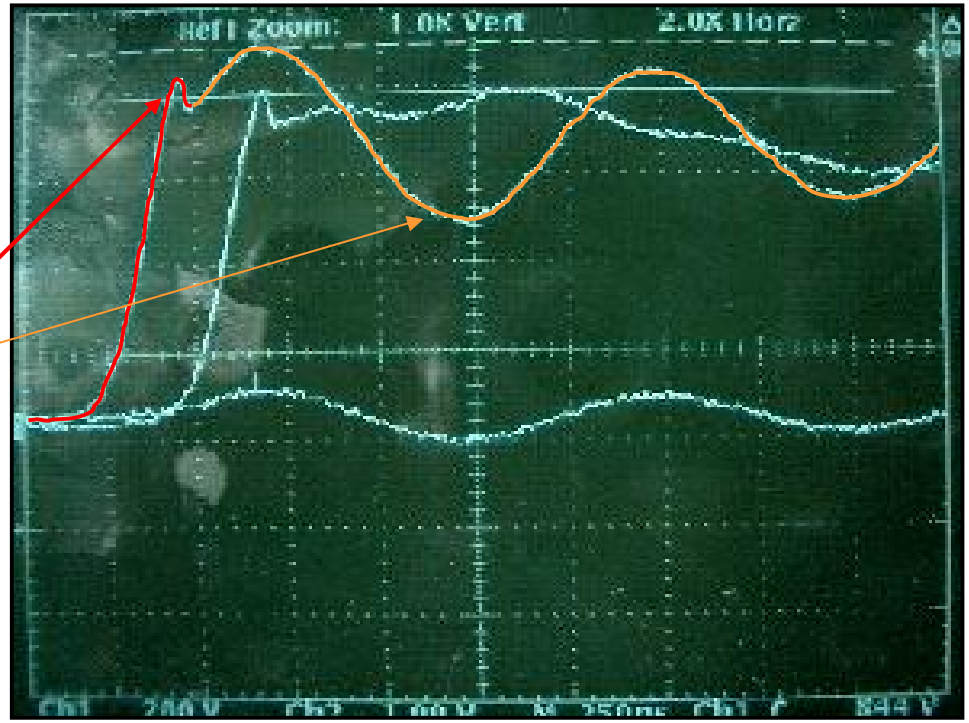
- But still: the snubber capacitor needs to be optimised
  - The wrong snubber does not reduce the voltage overshoots
  - Together with the stray inductance of the DC-link oscillations can occur

IGBT switch off
(raise of $V_{CE}$)

before optimisation

Voltage overshoot

Oscillation






# Not sufficient snubber capacitors

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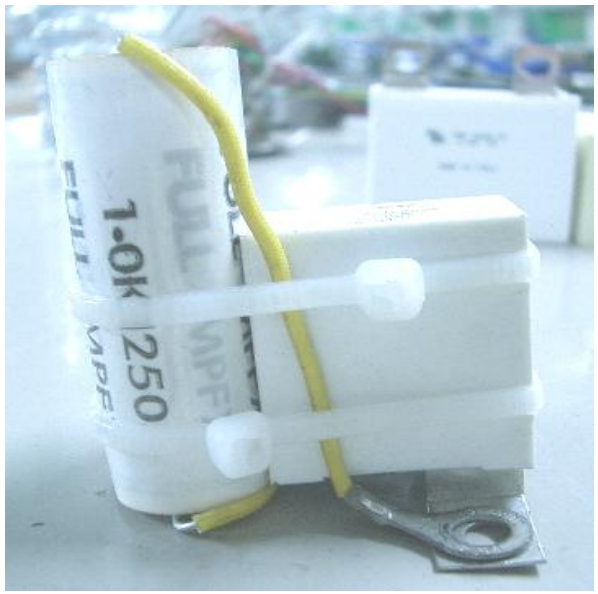
- These capacitors did not work satisfactory as snubber:






# Not sufficient snubber capacitors

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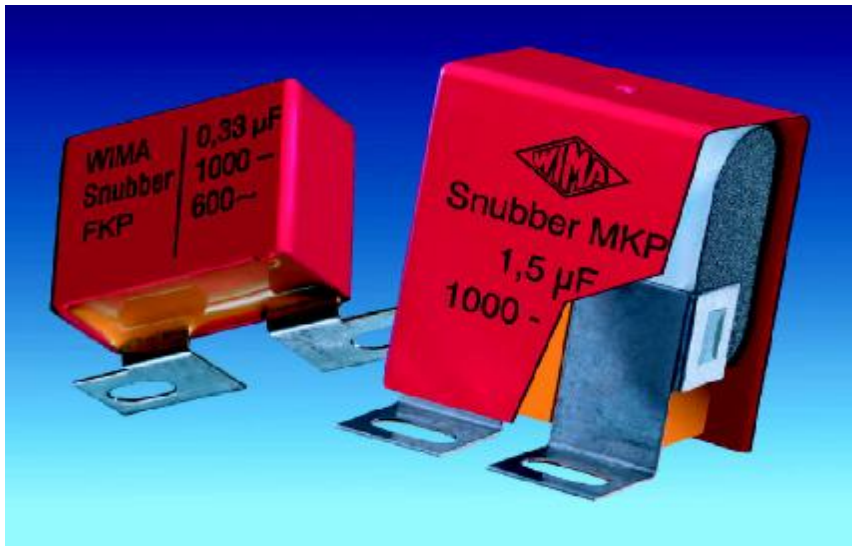
- From different suppliers different snubber capacitors are available.
- In a “trial and error” process the optimum can be find, based on measurements.




# Available snubber capacitors

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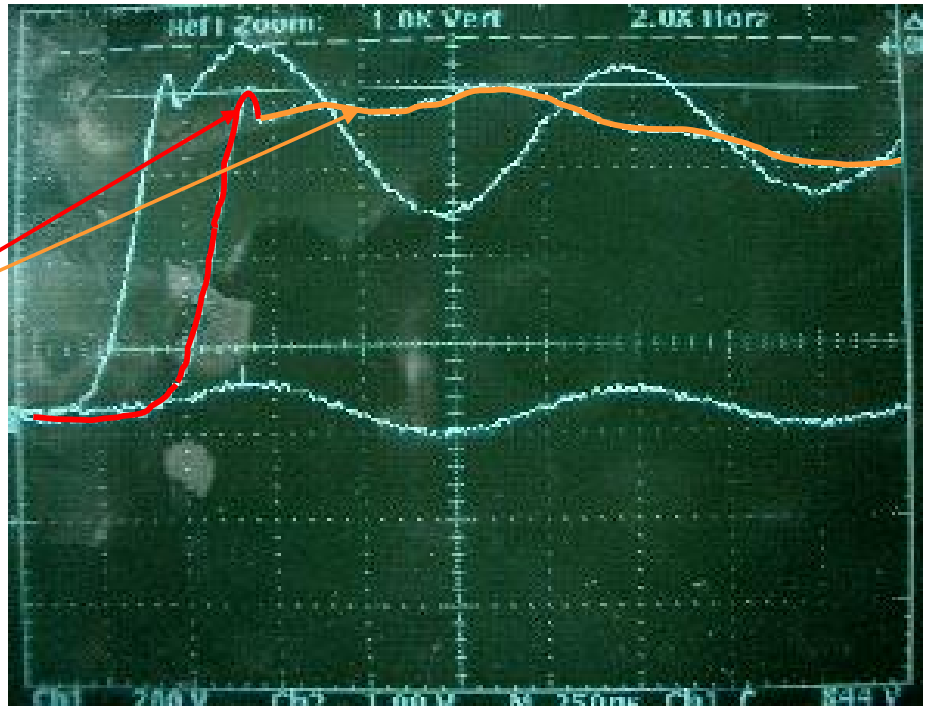
- After optimisation:
  - Significantly reduced voltage overshoots
  - No oscillations

IGBT switch off
(raise of $V_{CE}$)

after optimisation

Voltage overshoot

No oscillation






# Optimal snubber capacitor

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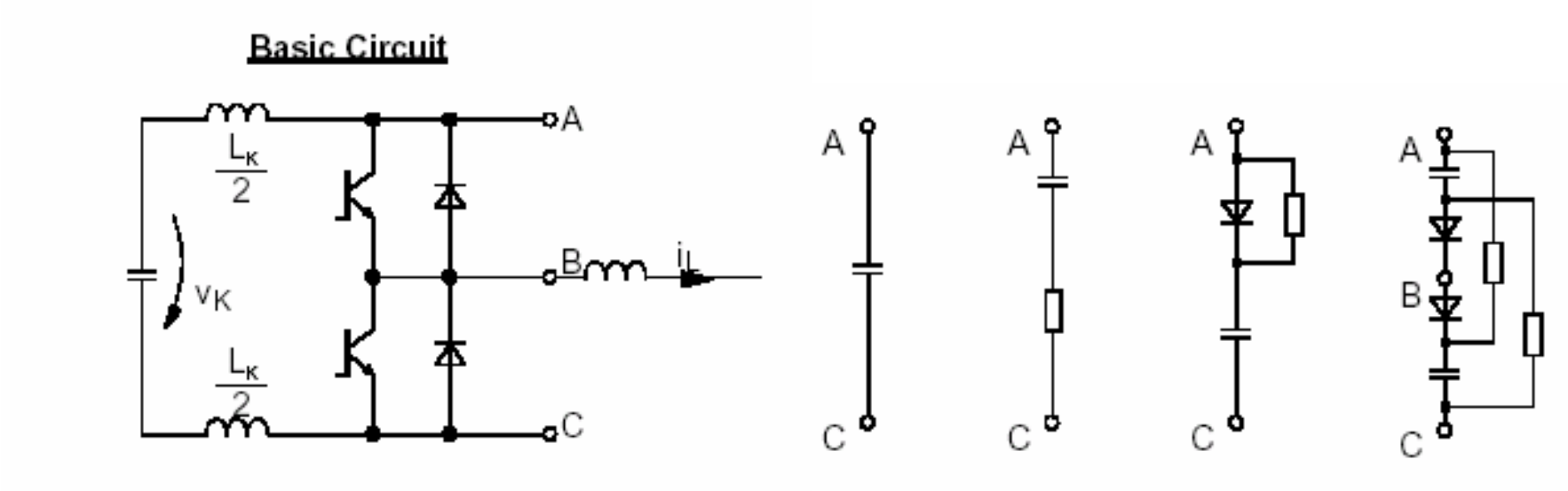


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# Snubber networks to reduce over voltage

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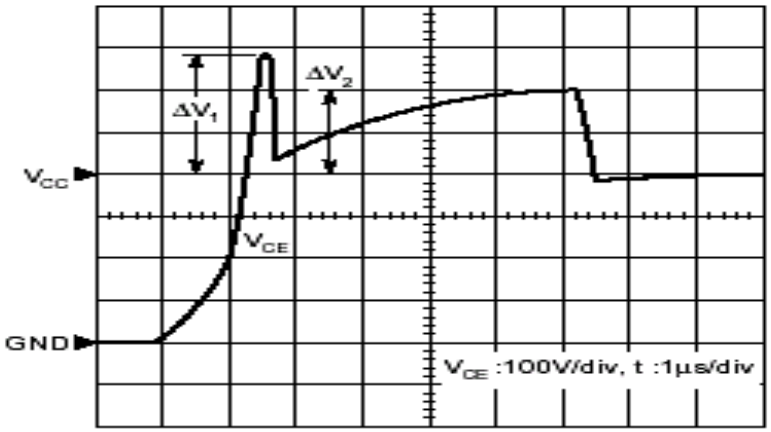


$\Delta V_1 = L_S \times di/dt$

Where:

$L_S$ = Parasitic Snubber Inductance
di/dt = Turn-off or diode recovery di/dt

$1/2\ L_B i^2 = 1/2\ C\Delta V_2^2$

Where:

$L_B$ = Parasitic Bus Inductance
i = Operating Current
C = Value of Snubber Capacitor
$\Delta V_2$ = Peak Snubber Voltage

$$C = L_B i^2 \div \Delta V_2^2$$

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# Calculation of a snubber capacitor

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